# STR73xF

ARM7TDMI™ 32-bit MCU with Flash, 3x CAN, 4 UARTs, 20 timers, ADC, 12 comm. interfaces

- ■ **Core**
  - ARM7TDMI 32-bit RISC CPU
  - 32 MIPS @ 36 MHz
- ■ **Temperature range -40 to 105 °C**
- ■ **Memories**
  - Up to 256 Kbytes FLASH program memory (10,000 cycles endurance, data retention 20 years at 55°C)
  - 16 Kbytes RAM
- ■ **Clock, reset and supply management**
  - 4.5 - 5.5V application supply and I/Os
  - Embedded 1.8V regulator for core supply
  - Embedded oscillator running from external 4-8MHz crystal or ceramic resonator
  - Up to 36 MHz CPU freq. with internal PLL
  - Internal RC oscillator 32kHz or 2MHz software configurable for fast startup and backup clock
  - Realtime Clock for clock-calendar function
  - Wakeup Timer driven by internal RC for wakeup from STOP mode
  - 5 power saving modes: SLOW, WFI, LPWFI, STOP and HALT modes
- ■ **Nested interrupt controller**
  - Fast interrupt handling with multiple vectors
  - 64 maskable IRQs with 64 vectors and 16 priority levels
  - 2 maskable FIQ sources
  - 16 ext. interrupts, up to 32 wake-up lines
- ■ **Up to 112 I/O ports**

TQFP100 14 x 14

TQFP144 20 x 20

LFBGA144 10 x 10 x 1.7

- 72/112 multifunctional bidirectional I/Os
- ■ **DMA**
  - 4 DMA controllers with 4 channels each
- ■ **Timers**
  - 16-bit watchdog timer (WDG)
  - 6/10 16-bit timers (TIM) each with: 2 input captures, 2 output compares, PWM and pulse counter modes
  - 6 16-bit PWM modules (PWM)
  - 3 16-bit timebase timers with 8-bit prescalers
- ■ **12 communications interfaces**
  - 2 I²C interfaces
  - 4 UART asynchronous serial interfaces
  - 3 BSPI synchronous serial interfaces
  - Up to 3 CAN interfaces (2.0B Active)
- ■ **10-bit A/D converter**
  - 12/16 channels
  - Conversion time: min 3µs, range: 0 to 5V
- ■ **Development tools support**
  - JTAG interface

Table 1. Device summary

Features	STR730FZx		STR735FZx		STR731FVx			STR736FVx		
FLASH memory - bytes	128K	256K	128K	256K	64K	128K	256K	64K	128K	256K
RAM - bytes	16K				16K					
Peripheral Functions	10 TIM Timers, 112 I/Os, 32 Wake-Up lines, 16 ADC channels				6 TIM Timers, 72 I/Os, 18 Wake-Up lines, 12 ADC channels					
CAN Peripherals	3		0		3			0		
Operating Voltage	4.5 to 5.5V									
Operating Temperature	-40 to +105°C									
Packages	**T**=TQFP144 20 x 20 **H**=LFBGA144 10 x10				**T**=TQFP100 14x14					

Contents

1   Introduction

This datasheet provides the STR73x Ordering Information, Mechanical and Electrical Device Characteristics.

For complete information on the STR73xF Microcontroller memory, registers and peripherals. please refer to the STR73x Reference Manual.

For information on programming, erasing and protection of the internal Flash memory please refer to the STR7 Flash Programming Reference Manual

For information on the ARM7TDMI core please refer to the ARM7TDMI Technical Reference Manual.

1.1   Overview

ARM core with embedded Flash & RAM

STR73xF family combines the high performance ARM7TDMI™ CPU with an extensive range of peripheral functions and enhanced I/O capabilities. All devices have on-chip high-speed single voltage FLASH memory and high-speed RAM. The STR73xF family has an embedded ARM core and is therefore compatible with all ARM tools and software.

Extensive tools support

STMicroelectronics' 32-bit, ARM core-based microcontrollers are supported by a complete range of high-end and low-cost development tools to meet the needs of application developers. This extensive line of hardware/software tools includes starter kits and complete development packages all tailored for ST's ARM core-based MCUs.

The range of development packages includes third-party solutions that come complete with a graphical development environment and an in-circuit emulator/programmer featuring a JTAG application interface. These support a range of embedded operating systems (OS), while several royalty-free OSs are also available.

For more information, please refer to ST MCU site http://www.st.com/mcu

Figure 1 shows the general block diagram of the device family.

Package Choice: Reduced Pin-Count TQFP100 or Feature-Rich 144-pin TQFP or LFBGA

The STR73xF family is available in 3 packages. The TQFP144 and LFBGA144 versions have the full set of all features. The 100-pin version has fewer timers, I/Os and ADC channels. Refer to the Device Summary on Page 1 for a comparison of the I/Os available on each package.

The family includes versions with and without CAN.

High Speed Flash Memory

The Flash program memory is organized in 32-bit wide memory cells which can be used for storing both code and data constants. It is accessed by CPU with zero wait states @ 36 MHz.

The STR7 embedded Flash memory can be programmed using In-Circuit Programming or In-Application programming.

The Flash memory endurance is 10K write/erase cycles and the data retention is 20 years at 55°C.

IAP (In-Application Programming): The IAP is the ability to re-program the Flash memory of a microcontroller while the user program is running.

ICP (In-Circuit Programming): The ICP is the ability to program the Flash memory of a microcontroller using JTAG protocol while the device is mounted on the user application board.

The Flash memory can be protected against different types of unwanted access (read/write/erase). There are two types of protection:

● Sector Write Protection
● Flash Debug Protection (locks JTAG access)

Flexible Power Management

To minimize power consumption, you can program the STR73xF to switch to SLOW, WFI LPWFI, STOP or HALT modes depending on the current system activity in the application.

Flexible Clock Control

Two clock sources are used to drive the microcontroller, a main clock driven by an external crystal or ceramic resonator and an internal backup RC oscillator that operates at 2MHz or 32 kHz. The embedded PLL can be configured to generate an internal system clock of up to 36 MHz. The PLL output frequency can be programmed using a wide selection of multipliers and dividers.

Voltage Regulators

The STR73xF requires an external 4.5 to 5.5V power supply. There are two internal Voltage Regulators for generating the 1.8V power supply needed by the core and peripherals. The main VR is switched off and the Low Power VR switched on when the application puts the STR73xF in Low Power Wait for Interrupt (LPWFI) mode.

Low Voltage Detectors

The voltage regulator and Flash modules each have an embedded LVD that monitors the internal 1.8V supply. If the voltage drops below a certain threshold, the LVD will reset the STR73xF.

Note: An external power-on reset must be provided ensure the microcontroller starts-up correctly.

1.2   On-Chip Peripherals

CAN Interfaces

The three CAN modules are compliant with the CAN specification V2.0 part B (active). The bit rate can be programmed up to 1 MBaud. These are not available in the STR735 and STR736.

DMA

4 DMA controllers, each with 4 data streams manage memory to memory, peripheral to memory and memory to peripheral transfers. The DMA requests are connected to TIM timers, BSPI0, BSPI1, BSPI2 and ADC. One of the streams can be configured to be triggered by a software request, independently from any peripheral activity.

16-bit Timers (TIM)

Each of the ten timers (six in 100-pin devices) have a 16-bit free-running counter with 7-bit prescaler, up to two input capture/output compare functions, a pulse counter function, and a PWM channel with selectable frequency. This provides a total of 16 independent PWMs (12 in 100-pin devices) when added with the PWM modules (see next paragraph).

PWM Modules (PWM)

The six 16-bit PWM modules have independently programmable periods and duty-cycles, with 5+3 bit prescaler factor.

Timebase Timers (TB)

The three 16-bit Timebase Timers with 8-bit prescaler for general purpose time triggering operations.

Realtime Clock (RTC)

The RTC provides a set of continuously running counters driven by separate clock signal derived from the main oscillator. The RTC can be used as a general timebase or clock/calendar/alarm function. When the STR73xF is in LPWFI mode the RTC keeps running, powered by the low power voltage regulator.

UARTs

The 4 UARTs allow full duplex, asynchronous, communications with external devices with independently programmable TX and RX baud rates up to 625K baud.

Buffered Serial Peripheral Interfaces (BSPI)

Each of the three BSPIs allow full duplex, synchronous communications with external devices, master or slave communication at up 6 Mb/s (@36 MHz System Clock).

I^2C Interfaces

The two I^2C Interfaces provide multi-master and slave functions, support normal and fast I^2C mode (400 kHz) and 7 or 10-bit addressing modes.

A/D Converter

The 10-bit Analog to Digital Converter, converts up to 16 channels in single-shot or continuous conversion modes (12 channels in 100-pin devices). The minimum conversion time is 3us.

Watchdog

The 16-bit Watchdog Timer protects the application against hardware or software failures and ensures recovery by generating a reset.

I/O Ports

Up to 112 I/O ports (72 in 100-pin devices) are programmable as general purpose input/output or Alternate Function.

External Interrupts and Wake-Up Lines

16 external interrupts lines are available for application use. In addition, up to 32 external Wakeup lines (18 in 100-pin devices) can be used as general purpose interrupts or to wake-up the application from STOP mode.

2 Block Diagram

Figure 1. STR730F/STR735F block diagram

*CAN peripherals not available on STR735F.

AF: alternate function on I/O port pin
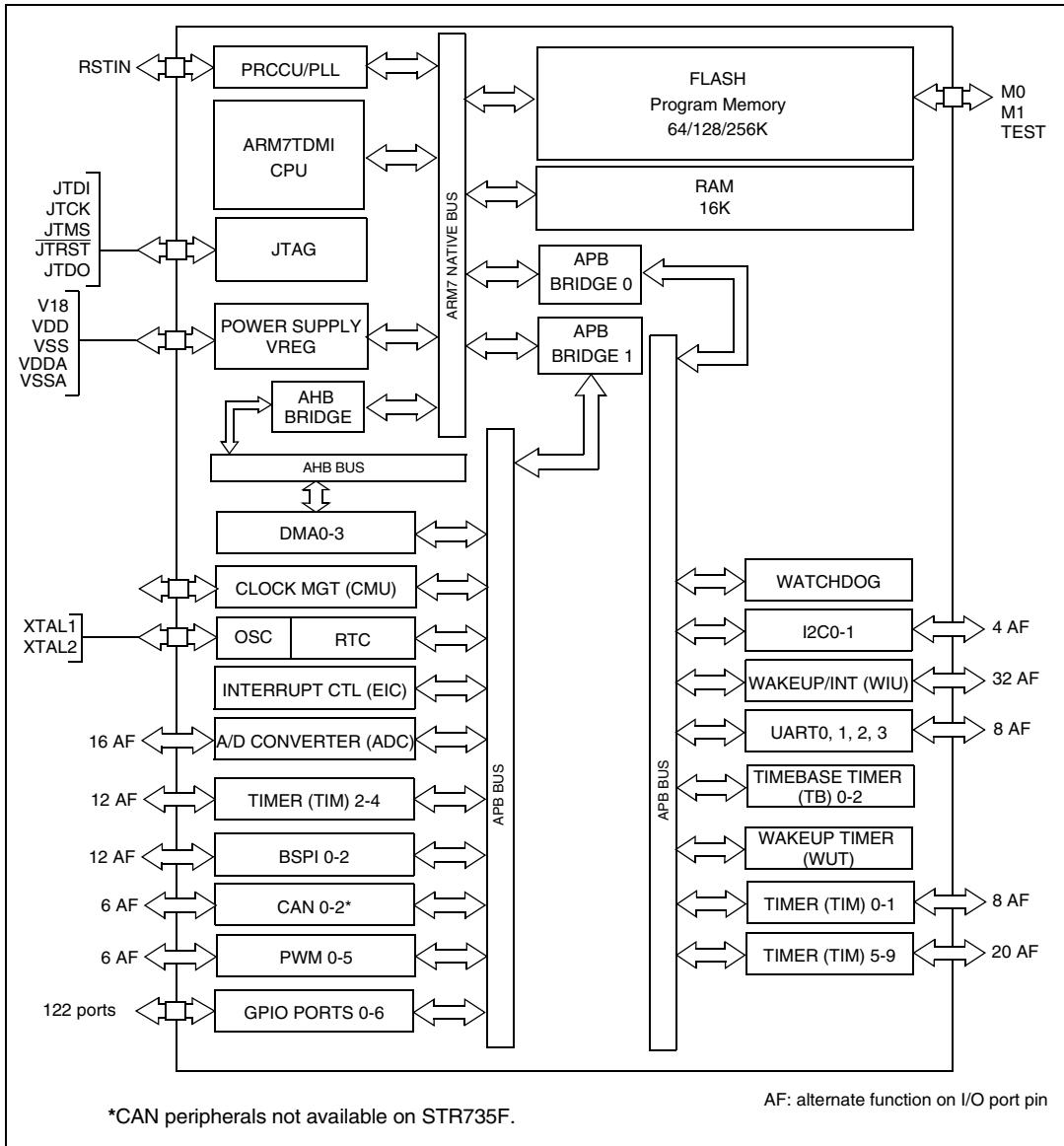
Figure 2.   STR731F/STR736 block diagram

*CAN peripherals not available on STR736F.

AF: alternate function on I/O port pin
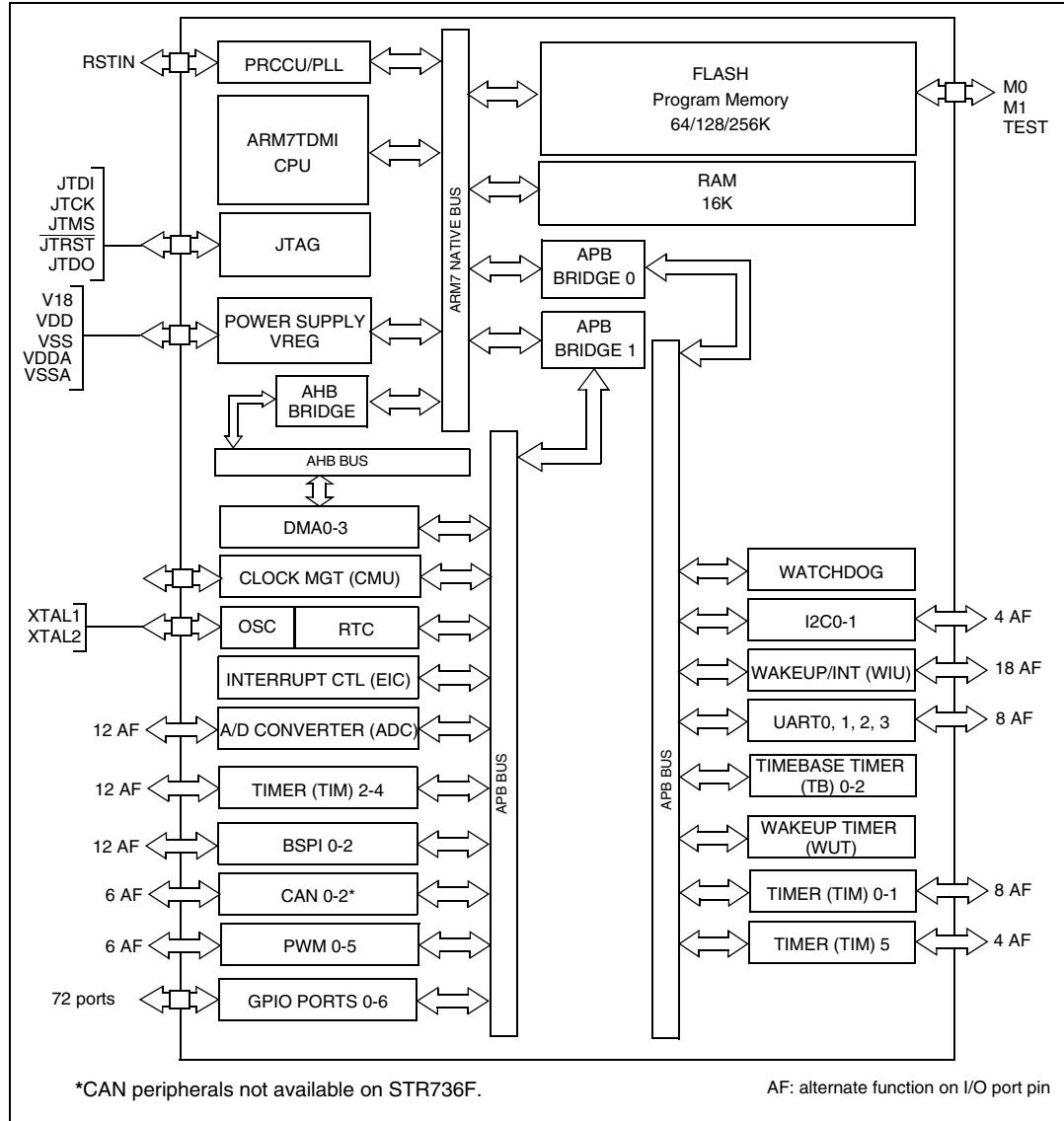
2.1 Related Documentation

Available from www.arm.com:

ARM7TDMI Technical Reference Manual

Available from http://www.st.com:

STR73x Reference Manual

STR7 Flash Programming Reference Manual

STR73x Software Library User Manual

For a list of related application notes refer to http://www.st.com.

2.2 Pin description

2.2.1 STR730F/STR735F (TQFP144)

Figure 3. STR730F/STR735F pin configuration (top view)

Note 1: CAN alternate functions not available on STR735F.
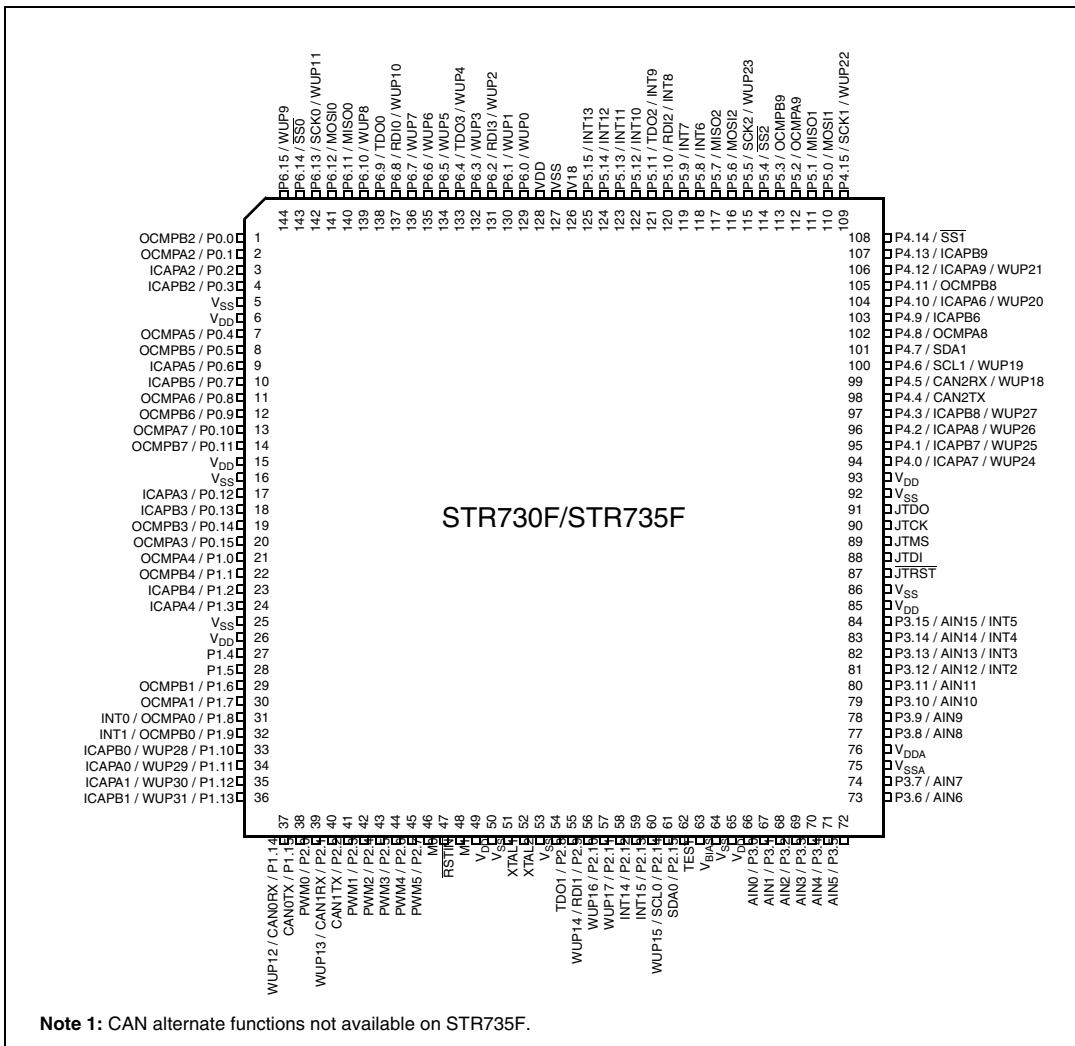
2.2.2   STR730F/STR735F (LFBGA144)

Table 2.   STR730F/STR735F LFBGA ball connections

Ball	Name	Ball	Name	Ball	Name	Ball	Name
A1	P0.0 / OCMPB2	B1	P0.4 / OCMPA5	C1	P0.5 / OCMPB5	D1	V_{SS}
A2	P6.10 / WUP8	B2	P0.1 / OCMPA2	C2	P0.2 / ICAPA2	D2	V_{DD}
A3	P6.9 / TDO0	B3	P6.15 / WUP9	C3	P0.3 / ICAPB2	D3	P0.6 / ICAPA5
A4	P6.12 / MOSI0	B4	P6.13 / SCKO / WUP11	C4	P6.14 / SSO	D4	P0.7 /ICAPB5
A5	P6.6 / WUP6	B5	P6.7 / WUP7	C5	P6.8 / RDI0 / WUP10	D5	P6.11 / MISO0
A6	V_{18}	B6	P6.2 / WUP2 / RDI3	C6	P6.3 / WUP3	D6	P6.4 / WUP4 /TDO3
A7	P5.15 / INT13	B7	P5.14 / INT12	C7	V_{SS}	D7	VDD
A8	P5.8 / INT6	B8	P5.9 / INT7	C8	P5.10 / INT8 / RDI2	D8	P5.12 / INT10
A9	P5.2 / OCMPA9	B9	P5.3 / OCMPB9	C9	P5.4 / SS2	D9	P5.5 / SCK2 / WUP23
A10	P5.7 / MISO2	B10	P5.0 / MOSI1	C10	P5.1 / MISO1	D10	P4.13 / ICAPB9
A11	P5.6 / MOSI2	B11	P4.15 / SCK1 / WUP22	C11	P4.14 / SS1	D11	P4.12 / ICAPA9 / WUP21
A12	P5.11 / TDO2 / INT9	B12	P4.8 / OCMPA8	C12	P4.7 / SDA1	D12	P4.11 / OCMPB8
E1	P0.8 / OCMPA6	F1	V_{DD}	G1	V_{SS}	H1	V_{DD}
E2	P0.9 / OCMPB6	F2	P0.13 / ICAPB3	G2	P1.2 / ICAPB4	H2	P1.8 / OCMPA0 / INT0
E3	P0.10 / OCMPA7	F3	P0.14 / OCMPB3	G3	P1.3 / ICAPA4	H3	P1.9 / OCMPB0 / INT1
E4	P0.11 / OCMPB7	F4	P0.15 / OCMPA3	G4	V_{SS}	H4	P1.10 / ICAPB0 / WUP28
E5	P0.12 / ICAPA3	F5	P1.0 / OCMPA4	G5	P1.5	H5	XTAL2
E6	P6.5 / WUP5	F6	P1.1 / OCMPB4	G6	P2.11 / WUP17	H6	P2.10 / WUP16
E7	P6.0 / WUP0	F7	P6.1 / WUP1	G7	P4.0 / ICAPA7 / WUP24	H7	P2.15 / SDA 0
E8	P5.13 / INT11	F8	P4.4 / CAN2TX[1]	G8	VDD	H8	JTMS
E9	P4.10 / ICAPA6 / WUP20	F9	P4.3 / ICAPB8 / WUP27	G9	VSS	H9	VSS
E10	P4.9 / ICAPB6	F10	P4.2 / ICAPA8 / WUP26	G10	JTDO	H10	VDD
E11	P4.6 / SCL1 / WUP19	F11	P4.1 / ICAPB7 / WUP25	G11	JTCK	H11	P3.15 / AIN15 / INT5
E12	P4.5 / WUP18 / CAN2RX[1]	F12	JTDI	G12	nJTRST	H12	P3.14 / AIN14 / INT4
J1	P1.4	K1	P1.6 / OCMPB1	L1	P1.7 / OCMPA1	M1	P1.14 / CAN0RX[1] / WUP12
J2	P1.11 / ICAPA0 / WUP29	K2	P1.13 / ICAPB1 / WUP31	L2	P1.15 / CAN0TX[1]	M2	P2.4 / PWM2
J3	P1.12 / ICAPA1 / WUP30	K3	P2.1 / CAN1RX[1] / WUP13	L3	P2.0 / PWM0	M3	P2.5 / PWM3
J4	P2.7 / PWM5	K4	P2.6 / PWM4	L4	P2.3 / PWM1	M4	P2.2 / CAN1TX[1]
J5	V_{DD}	K5	M1	L5	RSTIN	M5	M0
J6	P2.9 / RDI1 / WUP14	K6	P2.8 / TDO1	L6	V_{SS}	M6	V_{SS}
J7	P2.14 / SCL 0 / WUP15	K7	P2.13 / INT15	L7	P2.12 / INT14	M7	XTAL1
J8	P3.1 / AIN1	K8	P3.0 / AIN0	L8	VBIAS	M8	TST
J9	P3.13 / AIN13 / INT3	K9	P3.4 / AIN4	L9	P3.3 / AIN3	M9	P3.2 / AIN2
J10	P3.12 / AIN12 / INT2	K10	V_{DDA}	L10	P3.5 / AIN5	M10	V_{SS}
J11	P3.9 / AIN9	K11	V_{SSA}	L11	P3.7 / AIN7	M11	V_{DD}
J12	P3.8 / AIN8	K12	P3.11 / AIN11	L12	P3.10 / AIN10	M12	P3.6 / AIN6

Note 1: CAN alternate functions not available on STR735F.

2.2.3 STR731F/STR736F (TQFP100)

Figure 4.   STR731F/STR736F pin configuration (top view)

Note 1: CAN alternate functions not available on STR736F.
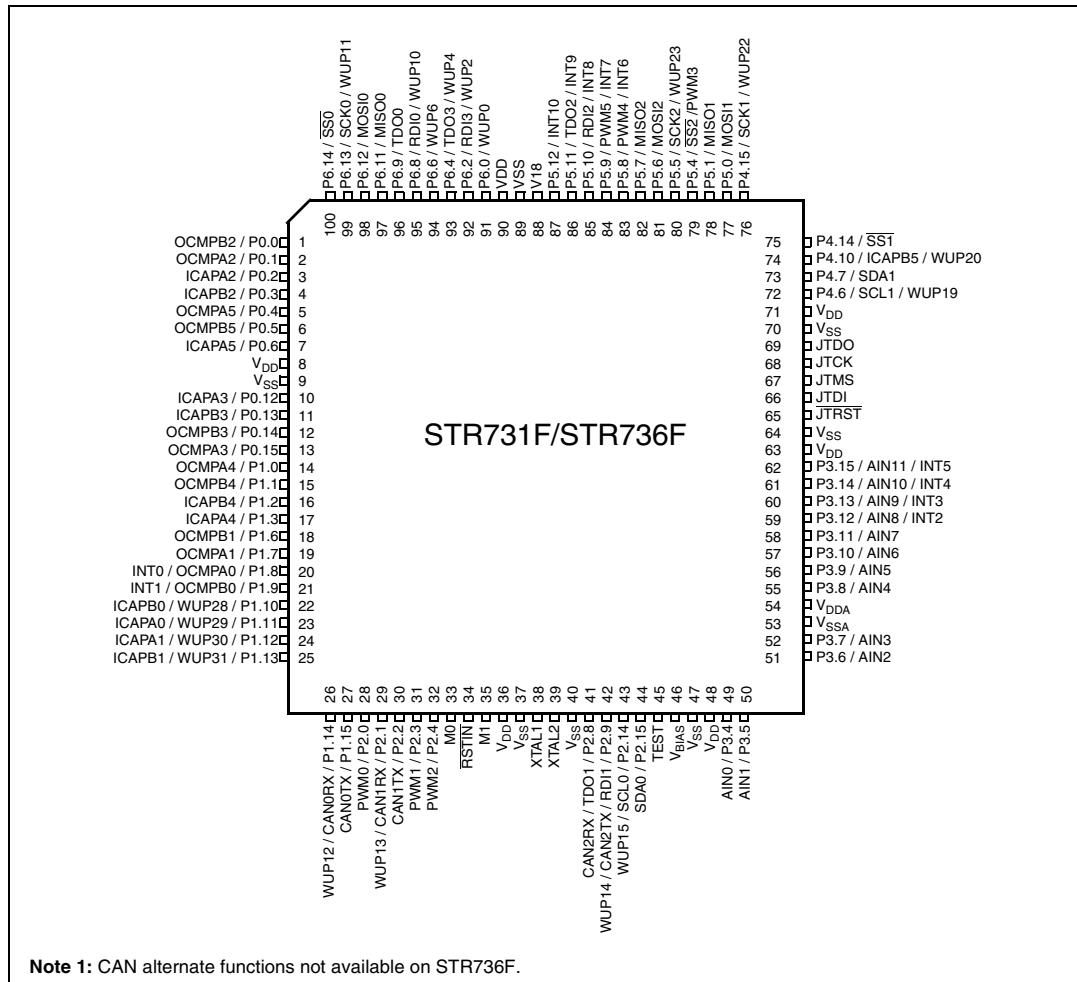
Legend / Abbreviations for *Table 3*:

Type: I = input, O = output, S = supply, HiZ= high impedance,

In/Output level: T_T= TTL 0.8V / 2V with input trigger
                      C_T= CMOS $0.3V_{DD}/0.7V_{DD}$ with input trigger

Port and control configuration:

Input: pu/pd = with internal 100kΩ weak pull-up or pull down

Output: OD = open drain (logic level)
                   PP = push-pull

Interrupts:

                   INTx =external interrupt line

                   WUPx =Wake-Up interrupt line

The reset state of the I/O ports is input floating. To avoid excess power consumption, unused I/O ports must be tied to ground.

Table 3. STR73xF pin description

Pin n°			Pin Name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
1	A1	1	P0.0/OCMPB2	I/O	T_T			2mA	X	X	Port 0.0	TIM2: Output Compare B output
2	B2	2	P0.1/OCMPA2	I/O	T_T			2mA	X	X	Port 0.1	TIM2: Output Compare A output
3	C2	3	P0.2/ICAPA2	I/O	T_T			2mA	X	X	Port 0.2	TIM2: Input Capture A input
4	C3	4	P0.3/ICAPB2	I/O	T_T			2mA	X	X	Port 0.3	TIM2: Input Capture B input
5	D1		V_{SS}	S							Ground	
6	D2		V_{DD}	S							Supply voltage (5V)	
7	B1	5	P0.4/OCMPA5	I/O	T_T			2mA	X	X	Port 0.4	TIM5: Output Compare A output
8	C1	6	P0.5/OCMPB5	I/O	T_T			2mA	X	X	Port 0.5	TIM5: Output Compare B output
9	D3	7	P0.6/ICAPA5	I/O	T_T			2mA	X	X	Port 0.6	TIM5: Input Capture A input
10	D4		P0.7/ICAPB5	I/O	T_T			2mA	X	X	Port 0.7	TIM5: Input Capture B input
11	E1		P0.8/OCMPA6	I/O	T_T			2mA	X	X	Port 0.8	TIM6: Output Compare A output
12	E2		P0.9/OCMPB6	I/O	T_T			2mA	X	X	Port 0.9	TIM6: Output Compare B output
13	E3		P0.10/OCMPA7	I/O	T_T			2mA	X	X	Port 0.10	TIM7: Output Compare A output
14	E4		P0.11/OCMPB7	I/O	T_T			2mA	X	X	Port 0.11	TIM7: Output Compare B output
15	F1	8	V_{DD}	S							Supply voltage (5V)	
16	G1	9	V_{SS}	S							Ground	
17	E5	10	P0.12/ICAPA3	I/O	T_T			2mA	X	X	Port 0.12	TIM3: Input Capture A input

Table 3.   STR73xF pin description

Pin n°			Pin Name	Type	Input			Output			Main function (after reset)	Alternate function
TQFP144	LFBGA144	TQFP100			Input Level	pu/pd	interrupt	Capability	OD	PP		
18	F2	11	P0.13/ICAPB3	I/O	T_T			2mA	X	X	Port 0.13	TIM3: Input Capture B input
19	F3	12	P0.14/OCMPB3	I/O	T_T			2mA	X	X	Port 0.14	TIM3: Output Compare B output
20	F4	13	P0.15/OCMPA3	I/O	T_T			2mA	X	X	Port 0.15	TIM3: Output Compare A output
21	F5	14	P1.0/OCMPA4	I/O	T_T			2mA	X	X	Port 1.0	TIM4: Output Compare A output
22	F6	15	P1.1/OCMPB4	I/O	T_T			2mA	X	X	Port 1.1	TIM4: Output Compare B output
23	G2	16	P1.2/ICAPB4	I/O	T_T			2mA	X	X	Port 1.2	TIM4: Input Capture B input
24	G3	17	P1.3/ICAPA4	I/O	T_T			2mA	X	X	Port 1.3	TIM4: Input Capture A input
25	G4		V_{SS}	S							Ground	
26	H1		V_{DD}	S							Supply voltage (5V)	
27	J1		P1.4	I/O	T_T			2mA	X	X	Port 1.4	
28	G5		P1.5	I/O	T_T			2mA	X	X	Port 1.5	
29	K1	18	P1.6/OCMPB1	I/O	T_T			2mA	X	X	Port 1.6	TIM1: Output Compare B output
30	L1	19	P1.7/OCMPA1	I/O	T_T			2mA	X	X	Port 1.7	TIM1: Output Compare A output
31	H2	20	P1.8/OCMPA0	I/O	T_T		INT0	2mA	X	X	Port 1.8	TIM0: Output Compare A output
32	H3	21	P1.9/OCMPB0	I/O	T_T		INT1	2mA	X	X	Port 1.9	TIM0: Output Compare B output
33	H4	22	P1.10/ICAPB0	I/O	T_T		WUP28	2mA	X	X	Port 1.10	TIM0: Input Capture B input
34	J2	23	P1.11/ICAPA0	I/O	T_T		WUP29	2mA	X	X	Port 1.11	TIM0: Input Capture A input
35	J3	24	P1.12/ICAPA1	I/O	T_T		WUP30	2mA	X	X	Port 1.12	TIM1: Input Capture A input
36	K2	25	P1.13/ICAPB1	I/O	T_T		WUP31	2mA	X	X	Port 1.13	TIM1: Input Capture B input
37	M1	26	P1.14/CAN0RX	I/O	T_T		WUP12	2mA	X	X	Port 1.14	CAN0: Receive Data input
38	L2	27	P1.15/CAN0TX	I/O	T_T			2mA	X	X	Port 1.15	CAN0: Transmit Data output
39	L3	28	P2.0/PWM0	I/O	T_T			2mA	X	X	Port 2.0	PWM0: PWM output
40	K3	29	P2.1/CAN1RX	I/O	T_T		WUP13	2mA	X	X	Port 2.1	CAN1: Receive Data input
41	M4	30	P2.2/CAN1TX	I/O	T_T			2mA	X	X	Port 2.2	CAN1: Transmit Data output
42	L4	31	P2.3/PWM1	I/O	T_T			2mA	X	X	Port 2.3	PWM1: PWM output
43	M2	32	P2.4/PWM2	I/O	T_T			2mA	X	X	Port 2.4	PWM2: PWM output

Table 3.   STR73xF pin description

TQFP144	LFBGA144	TQFP100	Pin Name	Type	Input Level	pu/pd	interrupt	Capability	OD	PP	Main function (after reset)	Alternate function	
44	M3		P2.5/PWM3	I/O	T_T			2mA	X	X	Port 2.5	PWM3: PWM output	
45	K4		P2.6/PWM4	I/O	T_T			2mA	X	X	Port 2.6	PWM4: PWM output	
46	J4		P2.7/PWM5	I/O	T_T			2mA	X	X	Port 2.7	PWM5: PWM output	
47	M5	33	M0	I	T_T	pd					BOOT: Mode selection 0 input		
48	L5	34	RSTIN	I	C_T	pu					Reset input		
49	K5	35	M1	I	T_T	pd					BOOT: Mode selection 1 input		
50	J5	36	V_{DD}	S							Supply voltage (5V)		
51	M6	37	V_{SS}	S							Ground		
52	M7	38	XTAL1	I							Oscillator amplifier circuit input and internal clock generator input.		
53	H5	39	XTAL2	O							Oscillator amplifier circuit output.		
54	L6	40	V_{SS}	S							Ground		
55	K6	41	P2.8/TDO1/CAN2RX	I/O	T_T			2mA	X	X	Port 2.8	UART1: Transmit Data output	CAN2: Receive Data input (TQFP100 only)
56	J6	42	P2.9/RDI1/CAN2TX	I/O	T_T		WUP14	2mA	X	X	Port 2.9	UART1: Receive Data input	CAN2: Transmit Data output (TQFP100 only)
57	H6		P2.10	I/O	T_T		WUP16	2mA	X	X	Port 2.10		
58	G6		P2.11	I/O	T_T		WUP17	2mA	X	X	Port 2.11		
59	L7		P2.12	I/O	T_T		INT14	2mA	X	X	Port 2.12		
60	K7		P2.13	I/O	T_T		INT15	2mA	X	X	Port 2.13		
61	J7	43	P2.14/SCL0	I/O	T_T		WUP15	2mA	X	X	Port 2.14	I2C0:Serial Clock	
62	H7	44	P2.15/SDA0	I/O	T_T			2mA	X	X	Port 2.15	I2C0:Serial Data	
63	M8	45	Test	I		pd					Reserved pin. Must be tied to ground		

Table 3.   STR73xF pin description

TQFP144	LFBGA144	TQFP100	Pin Name	Type	Input Level	pu/pd	interrupt	Capability	OD	PP	Main function (after reset)	Alternate function
64	L8	46	V_{BIAS}	S							Internal RC Oscillator bias. A 1.3MΩ external resistor has to be connected to this pin when a 32kHZ RC oscillator frequency is used.	
65	M10	47	V_{SS}	S							Ground	
66	M11	48	V_{DD}	S							Supply voltage (5V)	
67	K8		P3.0/AIN0	I/O	T_T			2mA	X	X	Port 3.0	ADC: Analog input 0
68	J8		P3.1/AIN1	I/O	T_T			2mA	X	X	Port 3.1	ADC: Analog input 1
69	M9		P3.2/AIN2	I/O	T_T			2mA	X	X	Port 3.2	ADC: Analog input 2
70	L9		P3.3/AIN3	I/O	T_T			2mA	X	X	Port 3.3	ADC: Analog input 3
71	K9	49	P3.4/AIN4	I/O	T_T			2mA	X	X	Port 3.4	ADC: Analog input 4 (AIN0 in TQFP100)
72	L10	50	P3.5/AIN5	I/O	T_T			2mA	X	X	Port 3.5	ADC: Analog input 5 (AIN1 in TQFP100)
73	M12	51	P3.6/AIN6	I/O	T_T			2mA	X	X	Port 3.6	ADC: Analog input 6 (AIN2 in TQFP100)
74	L11	52	P3.7/AIN7	I/O	T_T			2mA	X	X	Port 3.7	ADC: Analog input 7 (AIN3 in TQFP100)
75	K11	53	V_{SSA}	S							Reference ground for A/D converter	
76	K10	54	V_{DDA}	S							Reference voltage for A/D converter	
77	J12	55	P3.8/AIN8	I/O	T_T			2mA	X	X	Port 3.8	ADC: Analog input 8 (AIN4 in TQFP100)
78	J11	56	P3.9/AIN9	I/O	T_T			2mA	X	X	Port 3.9	ADC: Analog input 9 (AIN5 in TQFP100)
79	L12	57	P3.10/AIN10	I/O	T_T			2mA	X	X	Port 3.10	ADC: Analog input 10 (AIN6 in TQFP100)
80	K12	58	P3.11/AIN11	I/O	T_T			2mA	X	X	Port 3.11	ADC: Analog input 11 (AIN7 in TQFP100)
81	J10	59	P3.12/AIN12	I/O	T_T		INT2	2mA	X	X	Port 3.12	ADC: Analog input 12 (AIN8 in TQFP100)
82	J9	60	P3.13/AIN13	I/O	T_T		INT3	2mA	X	X	Port 3.13	ADC: Analog input 13 (AIN9 in TQFP100)
83	H12	61	P3.14/AIN14	I/O	T_T		INT4	2mA	X	X	Port 3.14	ADC: Analog input 14 (AIN10 in TQFP100)
84	H11	62	P3.15/AIN15	I/O	T_T		INT5	2mA	X	X	Port 3.15	ADC: Analog input 15 (AIN11 in TQFP100)
85	H10	63	V_{DD}	S							Supply voltage (5V)	

Table 3.   STR73xF pin description

Pin n°												
							Input		**Output**		**Main function (after reset)**	**Alternate function**
TQFP144	**LFBGA144**	**TQFP100**	**Pin Name**	**Type**	**Input Level**	**pu/pd**	**interrupt**	**Capability**	**OD**	**PP**		
86	H9	64	V$_{SS}$	S							Ground	
87	G12	65	JTRST	I	T$_T$	pu						JTAG Reset Input
88	F12	66	JTDI	I	T$_T$	pu						JTAG Data input
89	H8	67	JTMS	I	T$_T$	pu						JTAG Mode Selection Input
90	G11	68	JTCK	I	T$_T$	pd						JTAG Clock Input
91	G10	69	JTDO	O				4mA				JTAG data output. **Note:** Reset state = HiZ
92	G9	70	V$_{SS}$	S							Ground	
93	G8	71	V$_{DD}$	S							Supply voltage (5V)	
94	G7		P4.0/ICAPA7	I/O	T$_T$		WUP24	2mA	X	X	Port 4.0	TIM7: Input Capture A input
95	F11		P4.1/ICAPB7	I/O	T$_T$		WUP25	2mA	X	X	Port 4.1	TIM7: Input Capture B input
96	F10		P4.2/ICAPA8	I/O	T$_T$		WUP26	2mA	X	X	Port 4.2	TIM8: Input Capture A input
97	F9		P4.3/ICAPB8	I/O	T$_T$		WUP27	2mA	X	X	Port 4.3	TIM8: Input Capture B input
98	F8		P4.4/CAN2TX	I/O	T$_T$			2mA	X	X	Port 4.4	CAN2: Transmit Data output
99	E12		P4.5/CAN2RX	I/O	T$_T$		WUP18	2mA	X	X	Port 4.5	CAN2: Receive Data input
100	E11	72	P4.6/SCL1	I/O	T$_T$		WUP19	2mA	X	X	Port 4.6	I2C1:Serial Clock
101	C12	73	P4.7/SDA1	I/O	T$_T$			2mA	X	X	Port 4.7	I2C1:Serial Data
102	B12		P4.8/OCMPA8	I/O	T$_T$			2mA	X	X	Port 4.8	TIM8: Output Compare A output
103	E10		P4.9/ICAPB6	I/O	T$_T$			2mA	X	X	Port 4.9	TIM6: Input Capture B input
104	E9	74	P4.10/ICAPA6/ICAPB5	I/O	T$_T$		WUP20	2mA	X	X	Port 4.10	TIM6: Input Capture A input (144-pin pkg only) / TIM5: Input Capture B input (TQFP100 only)
105	D12		P4.11/OCMPB8	I/O	T$_T$			2mA	X	X	Port 4.11	TIM8: Output Compare B output
106	D11		P4.12/ICAPA9	I/O	T$_T$		WUP21	2mA	X	X	Port 4.12	TIM9: Input Capture A input
107	D10		P4.13/ICAPB9	I/O	T$_T$			2mA	X	X	Port 4.13	TIM9: Input Capture B input
108	C11	75	P4.14/$\overline{SS}$1	I/O	T$_T$			2mA	X	X	Port 4.14	BSPI1: Slave Select
109	B11	76	P4.15/SCK1	I/O	T$_T$		WUP22	2mA	X	X	Port 4.15	BSPI1: Serial Clock

Table 3. STR73xF pin description

TQFP144	LFBGA144	TQFP100	Pin Name	Type	Input Level	pu/pd	interrupt	Capability	OD	PP	Main function (after reset)	Alternate function	
	Pin n°				Input			Output					
110	B10	77	P5.0/MOSI1	I/O	T_T			2mA	X	X	Port 5.0	BSPI1: Master Output/Slave input	
111	C10	78	P5.1/MISO1	I/O	T_T			2mA	X	X	Port 5.1	BSPI1: Master input/Slave output	
112	A9		P5.2/OCMPA9	I/O	T_T			2mA	X	X	Port 5.2	TIM9: Output Compare A output	
113	B9		P5.3/OCMPB9	I/O	T_T			2mA	X	X	Port 5.3	TIM9: Output Compare B output	
114	C9	79	P5.4/$\overline{SS}$2/PWM3	I/O	T_T			2mA	X	X	Port 5.4	BSPI2: Slave Select	PWM3: PWM output (TQFP100 only)
115	D9	80	P5.5/SCK2	I/O	T_T		WUP23	2mA	X	X	Port 5.5	BSPI2: Serial Clock	
116	A11	81	P5.6/MOSI2	I/O	T_T			2mA	X	X	Port 5.6	BSPI2: Master Output/Slave input	
117	A10	82	P5.7/MISO2	I/O	T_T			2mA	X	X	Port 5.7	BSPI2: Master input/Slave output	
118	A8	83	P5.8/PWM4	I/O	T_T		INT6	2mA	X	X	Port 5.8	PWM4: PWM output (TQFP100 only)	
119	B8	84	P5.9/PWM5	I/O	T_T		INT7	2mA	X	X	Port 5.9	PWM5: PWM output (TQFP100 only)	
120	C8	85	P5.10/RDI2	I/O	T_T		INT8	2mA	X	X	Port 5.10	UART2: Receive Data input	
121	A12	86	P5.11/TDO2	I/O	T_T		INT9	2mA	X	X	Port 5.11	UART2: Transmit Data output	
122	D8	87	P5.12	I/O	T_T		INT10	2mA	X	X	Port 5.12		
123	E8		P5.13	I/O	T_T		INT11	2mA	X	X	Port 5.13		
124	B7		P5.14	I/O	T_T		INT12	2mA	X	X	Port 5.14		
125	A7		P5.15	I/O	T_T		INT13	2mA	X	X	Port 5.15		
126	A6	88	V_{18}	S							Supply voltage for core provided by internal voltage regulator		
127	C7	89	V_{SS}	S							Ground		
128	D7	90	V_{DD}	S							Supply voltage (5V)		
129	E7	91	P6.0	I/O	T_T		WUP0	8mA	X	X	Port 6.0		
130	F7		P6.1	I/O	T_T		WUP1	2mA	X	X	Port 6.1		

Table 3.   **STR73xF pin description**

TQFP144	LFBGA144	TQFP100	Pin Name	Type	Input Level	pu/pd	interrupt	Capability	OD	PP	Main function (after reset)	Alternate function
					Input			**Output**				
131	B6	92	P6.2/RDI3	I/O	T_T		WUP2	2mA	X	X	Port 6.2	UART3: Receive Data input
132	C6		P6.3	I/O	T_T		WUP3	2mA	X	X	Port 6.3	
133	D6	93	P6.4/TDO3	I/O	T_T		WUP4	2mA	X	X	Port 6.4	UART3: Transmit Data output
134	E6		P6.5	I/O	T_T		WUP5	2mA	X	X	Port 6.5	
135	A5	94	P6.6	I/O	T_T		WUP6	2mA	X	X	Port 6.6	
136	B5		P6.7	I/O	T_T		WUP7	2mA	X	X	Port 6.7	
137	C5	95	P6.8/RDI0	I/O	T_T		WUP10	2mA	X	X	Port 6.8	UART0: Receive Data input
138	A3	96	P6.9/TDO0	I/O	T_T			2mA	X	X	Port 6.9	UART0: Transmit Data output
139	A2		P6.10	I/O	T_T		WUP8	2mA	X	X	Port 6.10	
140	D5	97	P6.11/MISO0	I/O	T_T			2mA	X	X	Port 6.11	BSPI0: Master input/Slave output
141	A4	98	P6.12/MOSI0	I/O	T_T			2mA	X	X	Port 6.12	BSPI0: Master Output/Slave input
142	B4	99	P6.13/SCK0	I/O	T_T		WUP11	2mA	X	X	Port 6.13	BSPI0: Serial Clock
143	C4	100	P6.14/$\overline{SS0}$	I/O	T_T			2mA	X	X	Port 6.14	BSPI0: Slave Select
144	B3		P6.15	I/O	T_T		WUP9	2mA	X	X	Port 6.15	

2.3 Memory Mapping

Figure 5 shows the various memory configurations of the STR73xF system. The system memory map (from 0x0000_0000 to 0xFFFF_FFFF) is shown on the left part of the figure, the right part shows maps of the Flash and APB areas. For flexibility the Flash or RAM addresses can be aliased to Block 0 addresses using the remapping feature

Most reserved memory spaces (gray shaded areas in *Figure 5*) are protected from access by the user code. When an access this memory space is attempted, an ABORT signal is generated. Depending on the type of access, the ARM processor will enter "prefetch abort" state (Exception vector 0x0000_000C) or "data abort" state (Exception vector 0x0000_0010). It is up to the application software to manage these abort exceptions.

Figure 5. Memory map
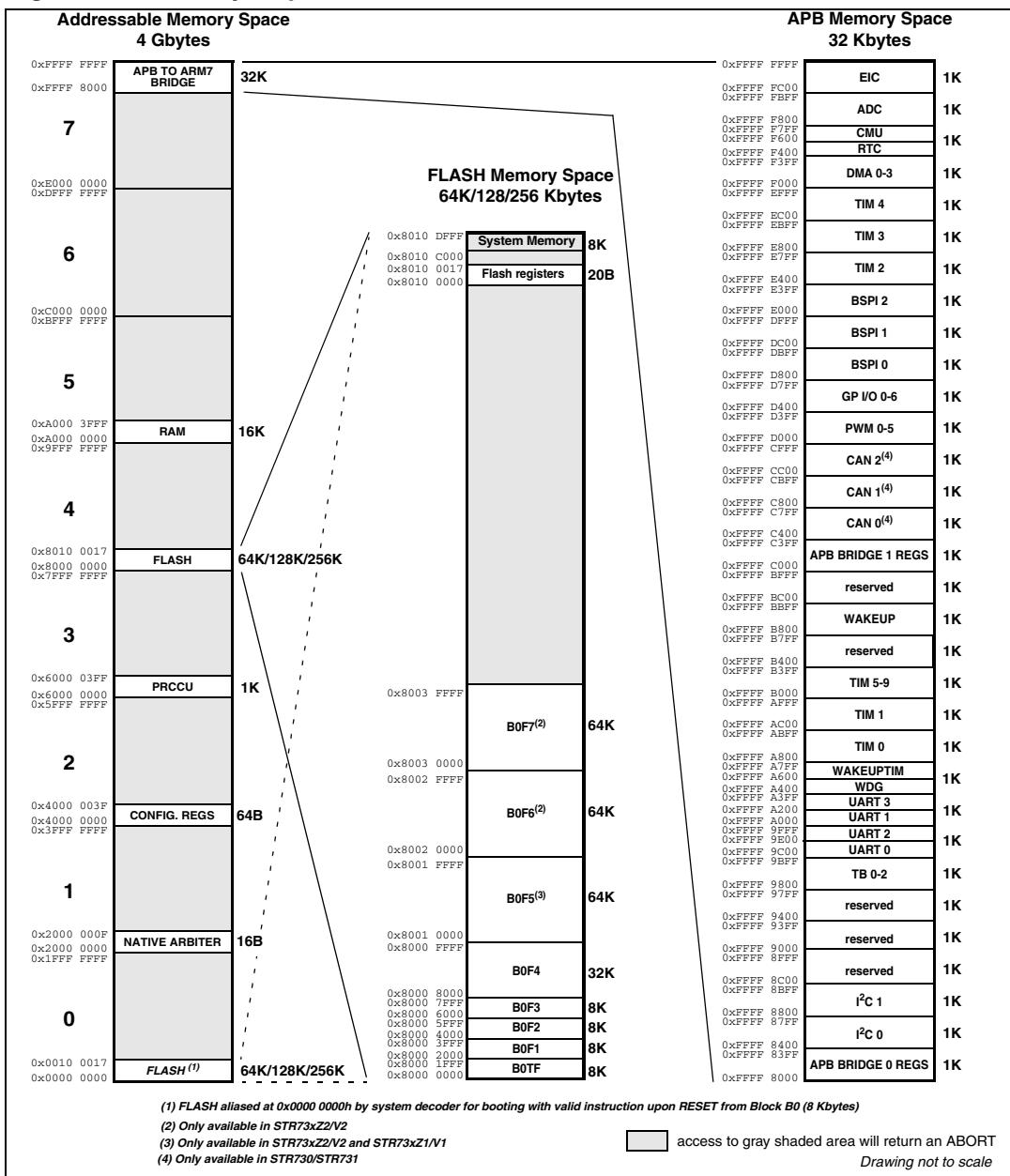
3 Electrical characteristics

This product contains devices to protect the inputs against damage due to high static voltages, however it is advisable to take normal precautions to avoid application of any voltage higher than the specified maximum rated voltages.

For proper operation it is recommended that V_{IN} be higher than V_{SS} and lower than V_{DD}. Reliability is enhanced if unused inputs are connected to an appropriate logic voltage level (V_{DD} or V_{SS}).

Caution: All values indicated in this section are preliminary and to be confirmed by product characterization.

3.1 Absolute maximum ratings

Stresses exceeding the recommended "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. During overload conditions ($V_{IN} > V_{DD}$ or $V_{IN} < V_{SS}$) the voltage on pins with respect to ground (V_{SS}) must not exceed the recommended values.

Table 4.   Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
V_{DD}	Voltage on V_{DD} pins with respect to ground (V_{SS})	−0.3 to +6.0	V
V_{SSA}	Voltage on V_{SSA} pin with respect to ground (V_{SS})	V_{SS}	V
V_{DDA}	Voltage on V_{DDA} pin with respect to ground (V_{SS})	−0.3 to V_{DD} + 0.3	V
V_{IN}	Voltage on any pin with respect to ground (V_{SS})	−0.3 to V_{DD} + 0.3	V
I_{INJ}	Input current on any pin during overload condition	±10[1]	mA
	Absolute sum of all input currents during overload condition	±75	mA
T_{ST}	Storage temperature	−55 to +150	°C
ESD	ESD Susceptibility (Human Body Model)	2000	V

1. In 144-pin devices, only +10mA on P0.3, P1.13, P3.6 and P4.13 pins (negative injection not allowed).

3.2 Recommended operating conditions

Table 5. **Operating Conditions**

Symbol	Parameter	Value		Unit
		Min	**Max**	
V_{DD}	Operating Supply Voltage with respect to ground (V_{SS})	4.5	5.5	V
V_{SSA}	Voltage on V_{SSA} pin with respect to ground (V_{SS})	V_{SS}	V_{SS}	V
V_{DDA}	Operating Analog Reference Voltage with respect to ground (V_{SS})	4.5	V_{DD} + 0.1	V
T_A	Ambient temperature under bias	−40	+105	°C
T_J	Junction temperature under bias	−40	+125	°C

Note: *RAM data retention is not guaranteed when V_{DD} is below 3.5 Volt.*

3.3 Voltage regulator characteristics

V_{DD} = 5V ± 10%, T_A = -40 / +105°C, unless otherwise specified.

Table 6. **Voltage Regulator Characteristics**

Symbol	Parameter	Conditions	Value			Unit
			Min	**Typ**	**Max**	
V_{OUT}	Main Regulator Output Voltage			1.8		
C_{V18}	External decoupling capacitor to be connected between V18 pin and nearest VSS pin.			100		nF

3.4 Preliminary power consumption data

Table 7 to *Table 8* give expected typical values based on bench measurements on a small number of parts.

Table 7.   STR73xF consumption in Run mode at 25°C and 85°C

Conditions		f_{MCLK} (MHz)	f_{ADC} (MHz)	Typical I_{DD} (mA)
V_{DD}= 5.5V, RC Oscillator off, PLL on, RTC enabled, 1 Timer (TIM) running, and ADC running in scan mode.	Code executing in RAM	10	10	20
		20		29
		36	9	42
	Code executing in Flash	10	10	22
		20		32
		36	9	48

Table 8.   STR73xF consumption in Run and low power modes at 25°C

Mode	Conditions	f_{MCLK}	Typical I_{DD}
RUN	All peripherals on	36MHz	76mA
		24MHz	56mA
WFI	Main Voltage Regulator on, Flash on, EIC on, WIU on, GPIOs on.	36MHz	33mA
		24MHz	31mA
SLOW	PLL off, Main Voltage Regulator on	4MHz	11mA
	CLOCK2/16, Main Voltage Regulator on,	250kHz	8mA
	CLOCK2/16, Main Voltage Regulator off,	250kHz	3mA
	RC oscillator running in Low Frequency, Main Quartz oscillator off, Main Voltage Regulator off	29kHz	2.5mA
LPWFI	CLOCK2/16, Main Voltage Regulator off, LP Voltage Regulator = 2mA, Flash in power down mode..	250kHz	528µA
STOP	Main Voltage Regulator off, RTC on, RC oscillator off	-	378µA
	Main Voltage Regulator off, RTC off, RC oscillator off, LP Voltage Regulator = 6mA	-	83µA
	Main Voltage Regulator off, RTC off, RC oscillator off, LP Voltage Regulator = 4mA	-	64µA
	Main Voltage Regulator off, RTC off, RC oscillator off, LP Voltage Regulator = 2mA	-	44µA
HALT	RTC off, LP Voltage Regulator = 2mA	-	44µA

3.5 DC electrical characteristics

V_{DD} = 5V ± 10%, T_A = -40 / +105°C, unless otherwise specified.

Table 9. DC electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
V_{IH}	Input High Level TTL Schmitt Trigger M0, M1 144-pin: P0(15:0), P1(15:0), P2(15:0), P3(15:0), P4(15:0), P5(15:0), P6(15:0), 100-pin: P0(15:0), P1(15:0), P2(15:0), P3(15:0), P4(7:0)		2.0	-	V_{DD}+0.3	V
	Input High Level TTL Schmitt Trigger JTDI, JTCK, $\overline{JTRST}$, JTMS		2.0	-	V_{DD}+0.3	V
	Input High Level CMOS Schmitt Trigger $\overline{RSTIN}$		0.7V_{DD}	-	V_{DD}+0.3	V
V_{IL}	Input Low Level TTL Schmitt Trigger M0, M1 144-pin: P0(15:0), P1(15:0), P2(15:0), P3(15:0), P4(15:0), P5(15:0), P6(15:0), 100-pin: P0(15:0), P1(15:0), P2(15:0), P3(15:0), P4(7:0)		-0.3	-	0.8	V
	Input Low Level TTL Schmitt Trigger JTDI, JTCK, $\overline{JTRST}$, JTMS		-0.3	-	0.8	V
	Input Low Level CMOS Schmitt Trigger $\overline{RSTIN}$		-0.3	-	0.3V_{DD}	V

Table 9. DC electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	**Typ**	**Max**	
V$_{HYS}$	Input Hysteresis TTL Schmitt Trigger M0, M1 144-pin: P0(15:0), P1(15:0), P2(15:0), P3(15:0), P4(15:0), P5(15:0), P6(15:0), 100-pin: P0(15:0), P1(15:0), P2(15:0), P3(15:0), P4(7:0)		450	-	-	mV
	Input Hysteresis TTL Schmitt Trigger JTDI, JTCK, JTRST, JTMS		450	-	-	mV
	Input Hysteresis CMOS Schmitt Trigger RSTIN	Output Low Level standard 144-pin: P0(15:0), P1(15:0), P2(15:0), P3(15:0), P4(15:0), P5(15:0), P6(15:1) 100-pin:P0(15:0), P1(15:0), P2(15:0), P3(15), P3(13:0), P4(7:0)	800	-	-	mV
V$_{OH}$[1]	Output high level standard 144-pin: P0(15:0), P1(15:0), P2(15:0), P3(15:0), P4(15:0), P5(15:0), P6(15:1) 100-pin: P0(15:0), P1(15:0), P2(15:0), P3(15), P3(13:0), P4(7:0)	Push Pull, I$_{OH}$ = 2mA	V$_{DD}$ - 0.8	-	-	V
	Output high level standard 144-pin: P6(0) 100-pin: P3(14)	Push Pull, I$_{OH}$ = 8mA	V$_{DD}$ - 0.8	-	-	V
	Output high level (JTAG) JTDO	Push Pull, I$_{OH}$ = 4mA	V$_{DD}$ - 0.8	-	-	V

Table 9. DC electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	**Typ**	**Max**	
V_{OL}	Output Low Level standard 144-pin: P0(15:0), P1(15:0), P2(15:0), P3(15:0), P4(15:0), P5(15:0), P6(15:1) 100-pin: P0(15:0), P1(15:0), P2(15:0), P3(15), P3(13:0), P4(7:0)	Push Pull, I_{OL} = 2mA	-	-	0.4	V
	Output low level standard 144-pin: P6(0) 100-pin: P3(14)	Push Pull, I_{OL} = 8mA	-	-	0.4	V
	Output low level (JTAG) JTDO	Push Pull, I_{OL} = 4mA	-	-	0.4	V
t_{tr}	Output transition time standard (10%-90% and 90%-10%) 144-pin: P0(15:0), P1(15:0), P2(15:0), P3(15:0), P4(15:0), P5(15:0), P6(15:1) 100-pin: P0(15:0), P1(15:0), P2(15:0), P3(15), P3(13:0), P4(7:0)	C_L = 20pF C_L = 50pF	3 6	5 10	10 20	ns
	Output transition time standard (10%-90% and 90%-10%) 144-pin: P6(0) 100-pin: P3(14)	C_L = 50pF C_L = 100pF	1 3	3 5	7 10	ns
	Output transition time (10%-90% and 90%-10%) JTDO	C_L = 20pF C_L = 50pF	2 3	3 6	7 12	ns
R_{WPU}	Weak Pull-Up Resistor		80	120	200	kΩ
R_{WPD}	Weak Pull-Down Resistor		80	120	200	kΩ

Table 9. DC electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	**Typ**	**Max**	
I_{lkg}	Input Leakage Current Standard M0, M1, JTDI, JTCK, JTRST, JTMS, RSTIN 144-pin: P0(15:0), P1(15:0), P2(15:0), P4(15:0), P5(15:0), P6(15:0) 100-pin: P0(15:0), P1(15:0), P2(15:14), P2(1:0), P3(15:0), P4(7:0)		-	-	1	µA
	Input Leakage Current Analog Input		-	-	1	µA

1. This specification is not valid for outputs which are switched to open drain mode. In this case, the respective output will float and the voltage is imposed by external circuitry.

3.6 $\overline{\text{RSTIN}}$ input filter characteristics

V_{DD} = 5V ± 10%, T_A = -40 / +105°C, unless otherwise specified.

Table 10. $\overline{\text{RSTIN}}$ **input filter characteristics**

Symbol	Parameter	Conditions	Value			Unit
			Min	**Typ**	**Max**	
t_{FRST}	$\overline{\text{RSTIN}}$ Input Filtered Pulse		-	-	50	ns
t_{NFRST}	$\overline{\text{RSTIN}}$ Input Not Filtered Pulse		2000	-		ns
t_{START}	$\overline{\text{RSTIN}}$ removal after Power-up		100	-		µs

3.7 Main oscillator electrical characteristics

The STR73xF can operate with a crystal oscillator or resonator clock source. *Figure 6* describes a simple model of the internal oscillator driver as well as example of connection for a crystal oscillator or a resonator.

Figure 6.   Crystal oscillator and resonator
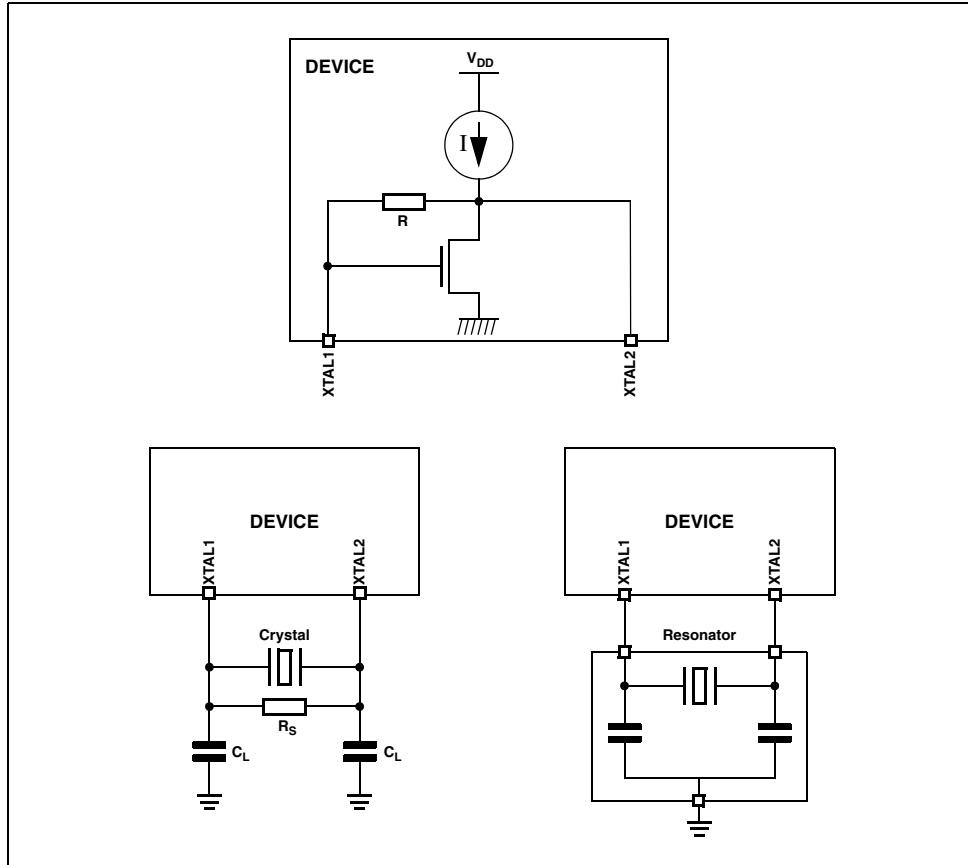
V_{DD} = 5V ± 10%, T_A = -40 / +105°C, unless otherwise specified.

Table 11.   Main oscillator electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{OSC}	Oscillator frequency		4		8	MHz
g_m	Oscillator Transconductance		1.5	2.3	4.2	mA/V
V_{OSC}	Oscillation amplitude	f_{OSC} = 4 MHz, T_A= 25°C	-	2.3	-	V
		f_{OSC} = 8 MHz, T_A= 25°C		1.5		
V_{AV}	Oscillator operating point	Sine wave middle, T_A= 25°C	-	0.85	-	V
t_{STUP}	Oscillator Start-up Time	External crystal, V_{DD} = 5.5V, f_{OSC} = 4 MHz, T_A=-40°C	-	-	12	ms
		External crystal, V_{DD} = 5.0V, f_{OSC} = 4 MHz, T_A=25°C	-	5.5	-	ms
		External crystal, V_{DD} = 5.5V, f_{OSC} = 6 MHz, T_A=-40°C	-	-	8	ms
		External crystal, V_{DD} = 5.0V, f_{OSC} = 6 MHz, T_A=25°C	-	3.3	-	ms
		External crystal, V_{DD} = 5.5V, f_{OSC} = 8 MHz, T_A=-40°C	-	-	7	ms
		External crystal, V_{DD} = 5.0V, f_{OSC} = 8 MHz, T_A= 25°C	-	2.7	-	ms

Table 11.   Main oscillator electrical characteristics

Symbol	Parameter	Conditions		Value			Unit
				Min	Typ	Max	
R$_{-ESR}$	Module of oscillator Negative Resistance	f$_{OSC}$ = 4 MHz Cp[1] = 10pF	C$_1$[2] = C$_2$ [3]= 10pF	150	555	-	Ω
			C$_1$ = C$_2$ = 20pF	490	1035	-	
			C$_1$ = C$_2$ = 30pF	490	1030	-	
			C$_1$ = C$_2$ = 40pF	380	850	-	
		f$_{OSC}$ = 5 MHz Cp = 10pF	C$_1$ = C$_2$ = 10pF	160	470	-	
			C$_1$ = C$_2$ = 20pF	415	800	-	
			C$_1$ = C$_2$ = 30pF	340	735	-	
			C$_1$ = C$_2$ = 40pF	260	580	-	
		f$_{OSC}$ = 6 MHz Cp = 10pF	C$_1$ = C$_2$ = 10pF	160	415	-	
			C$_1$ = C$_2$ = 20pF	325	640	-	
			C$_1$ = C$_2$ = 30pF	250	550	-	
			C$_1$ = C$_2$ = 40pF	180	420	-	
		f$_{OSC}$ = 7 MHz Cp = 10pF	C$_1$ = C$_2$ = 10pF	160	375	-	
			C$_1$ = C$_2$ = 20pF	260	525	-	
			C$_1$ = C$_2$ = 30pF	185	420	-	
			C$_1$ = C$_2$ = 40pF	135	315	-	
		f$_{OSC}$ = 8MHz Cp = 10pF	C$_1$ = C$_2$ = 10pF	155	340	-	
			C$_1$ = C$_2$ = 20pF	210	435	-	
			C$_1$ = C$_2$ = 30pF	145	335	-	
			C$_1$ = C$_2$ = 40pF	100	245	-	

1. C$_P$ represents the total capacitance between XTAL1 and XTAL2, including the shunt capacitance of the external quartz crystal as well as the total board parasitic cross-capacitance between XTAL1 track and XTAL2 track.

2. C$_1$ represents the total capacitance between XTAL1 and ground, including the external capacitance tied to XTAL1 pin (C$_L$) as well as the total parasitic capacitance between XTAL1 track and ground (this includes application board track capacitance to ground and device pin capacitance).

3. C$_2$ represents the total capacitance between XTAL2 and ground, including the external capacitance tied to XTAL1 pin (C$_L$) as well as the total parasitic capacitance between XTAL2 track and ground (this includes application board track capacitance to ground and device pin capacitance):

3.8   PLL electrical characteristics

V_{DD} = 5V ± 10%, T_A = -40 / +105°C, unless otherwise specified.

Table 12.   PLL Electrical Characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{PLLIN}[1]	PLL reference clock	FREF_RANGE = '0' FREF_RANGE = '1'	1.5 3.0		3.0 5.0	MHz
f_{PLLOUT}	PLL output clock	MX = "00" MX = "01" MX = "10" MX = "11"	20 x f_{PLLIN} 12 x f_{PLLIN} 28 x f_{PLLIN} 16 x f_{PLLIN}			MHz
f_{MCLK}	System clock	DX = 1..7	f_{PLLOUT}/DX		36	MHz
f_{FREE}	PLL free running frequency	FREF_RANGE = '0', MX0 = '1' FREF_RANGE = '0', MX0 = '0' FREF_RANGE = '1', MX0 = '1' FREF_RANGE = '1', MX0 = '0'		120 240 240 480		kHz
t_{LOCK}	PLL lock time	stable oscillator (f_{PLLIN} = 4 MHz), stable V_{DD}			300	µs
Δt_{PKJIT}	PLL jitter (pk to pk)	f_{PLLIN} = 4 MHz (pulse generator) f_{PLLIN} = 4 MHz (resonator)			1000 500	ps
Δt_{LTJIT}	PLL Long term jitter	f_{PLLIN} = 4 MHz (pulse generator)			10	ns

1. f_{PLLIN} is obtained from f_{OSC} directly or through an optional divider by 2.

3.9   RC oscillator electrical characteristics

V_{DD} = 5V ± 10%, T_A = -40 / +105°C, unless otherwise specified.

Table 13.   RC oscillator electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
f_{RC}	RC High Frequency			2.34		MHz
	RC Low Frequency			29		kHz
$I_{DD(RC)}$	RC High Frequency Current	T_A = 25°C, CMU_RCCTL=0x8		90		µA
	RC Low Frequency Current			10		µA

3.10 Flash electrical characteristics

V_{DD} = 5V ± 10%, T_A = -40 / +105°C, unless otherwise specified.

Table 14. Flash electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Typ	**Max**		
			T_A = 25 °C	T_A = 105 °C		
			0k[1] cycles	0k[1] cycles	10k cycles	
t_{WP}	Word Program (32-bit)		35	80	120	μs
t_{DWP}	Double Word Program (64-bit)		60	150	190	μs
t_{BP64}	Bank 0 Program (64K) (Double Word Program)		0.5	1.25	1.5	s
t_{BP128}	Bank 0 Program (128K) (Double Word Program)		1	2.5	3.1	s
t_{BP256}	Bank 0 Program (256K) (Double Word Program)		2	4.9	6.2	s
t_{SE8}	Sector Erase (8K)	Not preprogrammed	0.6	0.9	1.3	s
		Preprogrammed (all bits programmed to 0)	0.5	0.8	1.1	
t_{SE32}	Sector Erase (32K)	not preprogrammed	1.1	2.0	3.0	s
		Preprogrammed (all bits programmed to 0)	0.8	1.8	2.3	
t_{SE64}	Sector Erase (64K)	Not preprogrammed	1.7	3.7	5.3	s
		Preprogrammed (all bits programmed to 0)	1.3	3.3	3.8	
t_{RPD}	Recovery from Power-Down			20	20	μs
t_{PSL}	Program Suspend Latency			10	10	μs
t_{ESL}	Erase Suspend Latency			30	30	μs
t_{ESRR}	Erase Suspend Request Rate	Min delay between 2 requests	20	20	20	ms
t_{SP}	Set Protection		40	170	170	μs

1. 0k cycle data applies to new parts, not yet cycled by the customer but after approx. 100 test cycles during manufacture.

3.11 ADC electrical characteristics

V_{DD} = 5V ± 10%, T_A = -40 / +105°C, unless otherwise specified.

Table 15. ADC electrical characteristics

Symbol	Parameter	Conditions	Value			Unit
			Min	**Typ**	**Max**	
V_{SSA}	Analog Reference Ground		V_{SS}		V_{SS}	V
V_{DDA}	Analog Reference Voltage		4.5[1]		V_{DD}+0.1	V
V_{AINX}[2]	Analog Input voltage		V_{SSA}		V_{DDA}	V
f_{ADC}					10	MHz
C_{AIN}	ADC Input Capacitance	Not sampling Sampling		3 6		pF
t_S[3]	Sample time	10 MHz f_{ADC}	1			µs
t_C[4]	Conversion time	10 MHz f_{ADC}	3			µs
R_{ASRC}	Internal resistance of analog source			1		kΩ
I_{INJ}	Input current Injection	Current injection on one ADC input, different from the converted one	-10		10	mA
$|E_T|$	Total Unadjusted Error	No current injection	-2		+2	LSB
		Current injection on adjacent channel	-7		+7	LSB

1. V_{DDA} can be tied to ground when A/D converter is not in use: however extra consumption (around 200 uA) on main V_{DD} will occur due to internal analog circuitry not being completely turned off: so, it is recommended to keep V_{DDA} at V_{DD} level even when not in use.

2. V_{AINx} may exceed V_{SSA} and V_{DDA} limits, remaining within absolute maximum ratings, but the results of the conversion will be clamped respectively to 0x000 or 0x3FF.

3. During the sample time the input capacitance C_{AIN} can be charged/discharged by the external source. The internal resistance of the analog source must allow the capacitance to reach its final voltage level within t_S. After the end of the sample time t_S, changes to the analog input voltage have no effect on the conversion result. Values for the sample clock t_S depend on programming.

4. This parameter includes the sample time t_S, the time for determining the digital result and the time for loading the result register with the conversion result.

4 Package characteristics

4.1 Package mechanical data

Figure 7.   100-pin thin quad flat package

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.09		0.20	0.004		0.008
D		16.00			0.630	
D1		14.00			0.551	
E		16.00			0.630	
E1		14.00			0.551	
e		0.50			0.020	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
Number of Pins						
N	100					
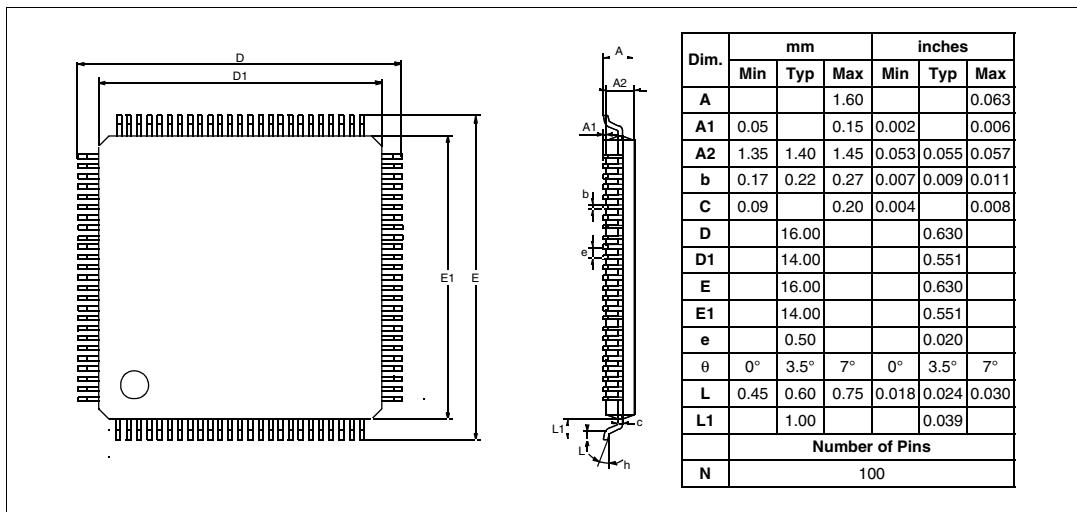
Figure 8.   144-pin thin quad flat package

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.063
A1	0.05		0.15	0.002		0.006
A2	1.35	1.40	1.45	0.053		0.057
b	0.17	0.22	0.27	0.007		0.011
c	0.09		0.20	0.004		0.008
D	21.80	22.00	22.20	0.858	0.867	0.874
D1	19.80	20.00	20.20	0.780	0.787	0.795
D3		17.50			0.699	
E	21.80	22.00	22.20	0.858	0.867	0.874
E1	19.80	20.00	20.20	0.780	0.787	0.795
E3		17.50			0.699	
e		0.50			0.020	
K	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.018	0.024	0.030
L1		1.00			0.039	
Number of Pins						
N	144					
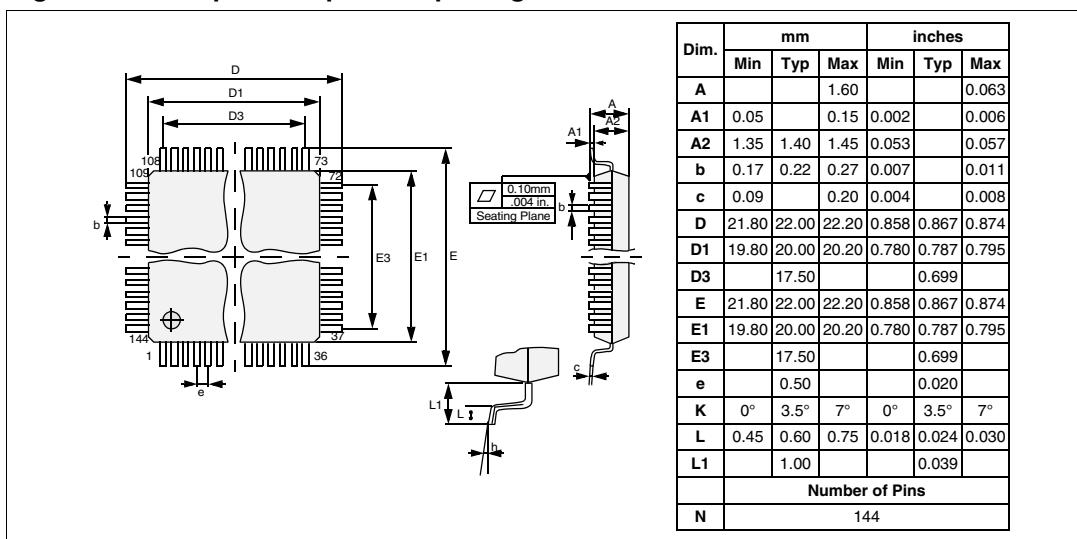
Figure 9.   144-ball low profile fine pitch ball grid array package

Dim.	mm			inches		
	Min	Typ	Max	Min	Typ	Max
A	1.21		1.70	0.048		0.067
A1	0.21			0.008		
A2		1.12			0.044	
b	0.35	0.40	0.45	0.014	0.016	0.018
D	9.85	10.00	10.15	0.388	0.394	0.400
D1		8.80			0.346	
E	9.85	10.00	10.15	0.388	0.394	0.400
E1		8.80			0.346	
e		0.80			0.031	
F		0.60			0.024	
ddd			0.10			0.004
eee			0.15			0.006
fff			0.08			0.003
	Number of Pins					
N	144					
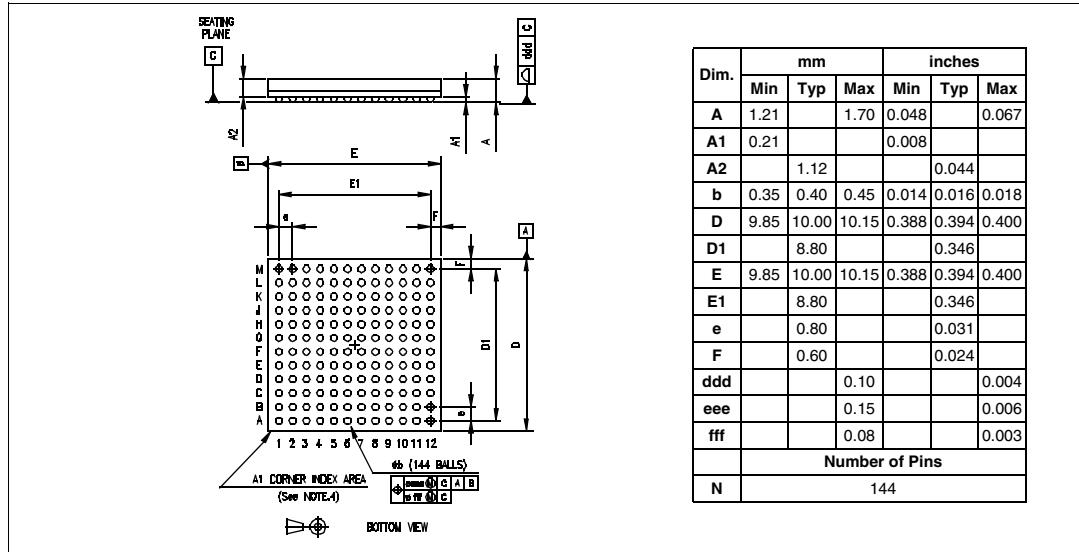
4.1.1 Power considerations

The average chip-junction temperature, T_J, in degrees Celsius, may be calculated using the following equation:

$$T_J = T_A + (P_D \times \Theta_{JA}) \qquad (1)$$

Where:

- T_A is the Ambient Temperature in °C,
- Θ_{JA} is the Package Junction-to-Ambient Thermal Resistance, in °C/W,
- P_D is the sum of P_{INT} and $P_{I/O}$ ($P_D = P_{INT} + P_{I/O}$),
- P_{INT} is the product of I_{DD} and V_{DD}, expressed in Watt. This is the Chip Internal Power,
- $P_{I/O}$ represents the Power Dissipation on Input and Output Pins; User Determined.

Most of the time for the applications $P_{I/O} < P_{INT}$ and may be neglected. On the other hand, $P_{I/O}$ may be significant if the device is configured to drive continuously external modules and/or memories.

An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is given by:

$$P_D = K / (T_J + 273°C) \qquad (2)$$

Therefore (solving equations 1 and 2):

$$K = P_D \times (T_A + 273°C) + \Theta_{JA} \times P_D^2 \qquad (3)$$

Where:

- K is a constant for the particular part, which may be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J may be obtained by solving equations (1) and (2) iteratively for any value of T_A

Table 16. Thermal Characteristics

Symbol	Description	Package	Value (typical)	Unit
Θ_{JA}	Thermal Resistance Junction-Ambient	LFBGA144	TBD	°C/W
		TQFP144	40	
		TQFP100	55	

5   Order codes

Table 17.   Order Codes

Partnumber	FLASH Kbytes	Package	RAM Kbytes	TIM Timers	6x PWM Module	CAN Periph	A/D Chan.	Wake-up Lines	I/O Ports	Temp. Range
STR730FZ1T7	128	TQFP144 20x20	16	10	1	3	16	32	112	-40 to +105°C
STR730FZ2T7	256	TQFP144 20x20								
STR730FZ1H7	128	LFBGA144 10x10								
STR730FZ2H7	256	LFBGA144 10x10								
STR735FZ1T7	128	TQFP144 20x20				0				
STR735FZ2T7	256	TQFP144 20x20								
STR735FZ1H7	128	LFBGA144 10x10								
STR735FZ2H7	256	LFBGA144 10x10								
STR731FV0T7	64	TQFP100 14x14		6		3	12	18	72	
STR731FV1T7	128	TQFP100 14x14								
STR731FV2T7	256	TQFP100 14x14								
STR736FV0T7	64	TQFP100 14x14				0				
STR736FV1T7	128	TQFP100 14x14								
STR736FV2T7	256	TQFP100 14x14								

6 Known limitations

6.1 Low Power Wait For Interrupt mode

When the STR73x device is put in Low Power Wait For Interrupt mode (LPWFI), the Flash goes into Low Power mode or Power Down mode, depending on the setting of the PWD bit in the Flash Control Register 0 (default is '0', Low Power mode). This default mode can create excessive voltage conditions on the transistor gates and may affect the long term behavior of the Low Power mode circuitry.

Workaround

There is no workaround. If Low Power Wait For Interrupt mode is used, it is strongly suggested to configure the Flash to enter Power Down mode (bit PWD = '1').

7 Revision history

Table 18. Revision history

Date	Revision	Description of Changes
19-Sep-2005	1	First release
2-Nov-2005	2	Removed Table 8 power consumption in LP modes Updated PLL frequency in *Section 1.1* and *Table 12*
8-Mar-2006	3	*Section 3.4: Preliminary power consumption data* updated *Section 3.5: DC electrical characteristics* updated *Section 6: Known limitations* added.

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