16 Mbit Dual-Bank Flash + 2/4 Mbit SRAM ComboMemory

SST34HF162G / SST34HF164G

Preliminary Specifications

FEATURES:

- **Flash Organization: 1M x16**
  - 16 Mbit: 12 Mbit + 4 Mbit
- **Concurrent Operation**
  - Read from or Write to SRAM while Erase/Program Flash
- **SRAM Organization:**
  - 2 Mbit:128K x16
  - 4 Mbit: 256K x16
- **Single 2.7-3.3V Read and Write Operations**
- **Superior Reliability**
  - Endurance: 100,000 Cycles (typical)
  - Greater than 100 years Data Retention
- **Low Power Consumption: (typical values @ 5 MHz)**
  - Active Current: Flash 10 mA (typical)
    SRAM 6 mA (typical)
  - Standby Current: 10 µA (typical)
- **Hardware Sector Protection (WP#)**
  - Protects 4 outer most sectors (4 KWord) in the larger bank by holding WP# low and unprotects by holding WP# high
- **Hardware Reset Pin (RST#)**
  - Resets the internal state machine to reading data array
- **Sector-Erase Capability**
  - Uniform 2 KWord sectors
- **Block-Erase Capability**
  - Uniform 32 KWord blocks
- **Read Access Time**
  - Flash: 70 ns
  - SRAM: 70 ns
- **Erase-Suspend / Erase-Resume Capabilities**
- **Latched Address and Data**
- **Fast Erase and Word-Program (typical):**
  - Sector-Erase Time: 18 ms
  - Block-Erase Time: 18 ms
  - Chip-Erase Time: 35 ms
  - Program Time: 7 µs
- **Automatic Write Timing**
  - Internal V_{PP} Generation
- **End-of-Write Detection**
  - Toggle Bit
  - Data# Polling
- **CMOS I/O Compatibility**
- **JEDEC Standard Command Set**
- **Packages Available**
  - 48-ball LFBGA (6mm x 8mm)
  - 48-ball LBGA (10mm x 12mm)
  - Non-Pb (lead-free) packages available

PRODUCT DESCRIPTION

The SST34HF16xG ComboMemory devices integrate a 1M x16 CMOS flash memory bank with either 128K x16 or 256K x16 CMOS SRAM memory bank in a multi-chip package (MCP). These devices are fabricated using SST's proprietary, high-performance CMOS SuperFlash technology incorporating the split-gate cell design and thick-oxide tunneling injector to attain better reliability and manufacturability compared with alternate approaches. The SST34HF16xG devices are ideal for applications such as cellular phones, GPS devices, PDAs, and other portable electronic devices in a low power and small form factor system.

The SuperFlash technology provides fixed Erase and Program times, independent of the number of Erase/Program cycles that have occurred. Therefore, the system software or hardware does not have to be modified or de-rated as is necessary with alternative flash technologies, whose Erase and Program times increase with accumulated Erase/Program cycles. The SST34HF16xG devices offer a guaranteed endurance of 10,000 cycles. Data retention is rated at greater than 100 years. With high-performance Program operations, the flash memory banks provide a typical Program time of 7 µsec. The entire flash memory bank can be erased and programmed word-by-word in 4 seconds (typically) for the SST34HF16xG, when using interface features such as Toggle Bit or Data# Polling to indicate the completion of Program operation. To protect against inadvertent flash write, the SST34HF16xG devices contain on-chip hardware and software data protection schemes.

The flash and SRAM operate as two independent memory banks with respective bank enable signals. The memory bank selection is done by two bank enable signals. The SRAM bank enable signal, BES#, selects the SRAM bank. The flash memory bank enable signal, BEF#, has to be used with Software Data Protection (SDP) command sequence when controlling the Erase and Program operations in the flash memory bank. The memory banks are superimposed in the same memory address space where they share common address lines, data lines, WE# and OE# which minimize power consumption and area. See Figure 1 for memory organization.

Designed, manufactured, and tested for applications requiring low power and small form factor, the SST34HF16xG are offered in both commercial and extended temperatures and a small footprint package to meet board space constraint requirements. See Figure 2 for pin assignments.

Device Operation

The SST34HF16xG use BES# and BEF# to control operation of either the flash or the SRAM memory bank. When BEF# is low, the flash bank is activated for Read, Program or Erase operation. When BES# is low the SRAM is activated for Read and Write operation. BEF# and BES# cannot be at low level at the same time. **If all bank enable signals are asserted, bus contention will result and the device may suffer permanent damage.** All address, data, and control lines are shared by flash and SRAM memory banks which minimizes power consumption and loading. The device goes into standby when BEF# and BES# bank enables are raised to V_{IHC} (Logic High) or when BEF# is high.

Concurrent Read/Write Operation

The SST34HF16xG provide the unique benefit of being able to read from or write to SRAM, while simultaneously erasing or programming the flash. This allows data alteration code to be executed from SRAM, while altering the data in flash. The following table lists all valid states.

CONCURRENT READ/WRITE STATE TABLE

Flash	SRAM
Program/Erase	Read
Program/Erase	Write

The device will ignore all SDP commands when an Erase or Program operation is in progress. Note that Product Identification commands use SDP; therefore, these commands will also be ignored while an Erase or Program operation is in progress.

Flash Read Operation

The Read operation of the SST34HF16xG is controlled by BEF# and OE#, both have to be low for the system to obtain data from the outputs. BEF# is used for device selection. When BEF# is high, the chip is deselected and only standby power is consumed. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when either BEF# or OE# is high. Refer to the Read cycle timing diagram for further details (Figure 7).

Flash Program Operation

These devices are programmed on a word-by-word basis. Before programming, one must ensure that the sector which is being programmed is fully erased.

The Program operation is accomplished in three steps:

1. Software Data Protection is initiated using the three-byte load sequence.
2. Address and data are loaded.

   During the Program operation, the addresses are latched on the falling edge of either BEF# or WE#, whichever occurs last. The data is latched on the rising edge of either BEF# or WE#, whichever occurs first.
3. The internal Program operation is initiated after the rising edge of the fourth WE# or BEF#, whichever occurs first. The Program operation, once initiated, will be completed typically within 7 µs.

See Figures 8 and 9 for WE# and BEF# controlled Program operation timing diagrams and Figure 21 for flowcharts. During the Program operation, the only valid reads are Data# Polling and Toggle Bit. During the internal Program operation, the host is free to perform additional tasks. Any commands issued during an internal Program operation are ignored.

Flash Sector- /Block-Erase Operation

These devices offer both Sector-Erase and Block-Erase operations. These operations allow the system to erase the devices on a sector-by-sector (or block-by-block) basis. The sector architecture is based on a uniform sector size of 2 KWord. The Block-Erase mode is based on a uniform block size of 32 KWord. The Sector-Erase operation is initiated by executing a six-byte command sequence with a Sector-Erase command (30H) and sector address (SA) in the last bus cycle. The Block-Erase operation is initiated by executing a six-byte command sequence with Block-Erase command (50H) and block address (BA) in the last bus cycle. The sector or block address is latched on the falling edge of the sixth WE# pulse, while the command (30H or 50H) is latched on the rising edge of the sixth WE# pulse. The internal Erase operation begins after the sixth WE# pulse. Any commands issued during the Block- or Sector-Erase operation are ignored except Erase-Suspend and Erase-Resume. See Figures 13 and 14 for timing waveforms.

Flash Chip-Erase Operation

The SST34HF16xG provide a Chip-Erase operation, which allows the user to erase all sectors/blocks to the "1" state. This is useful when the device must be quickly erased.

The Chip-Erase operation is initiated by executing a six-byte command sequence with Chip-Erase command (10H) at address 555H in the last byte sequence. The Erase operation begins with the rising edge of the sixth WE# or BEF#, whichever occurs first. During the Erase operation, the only valid read is Toggle Bits or Data# Polling. See Table 5 for the command sequence, Figure 12 for timing diagram, and Figure 24 for the flowchart. Any commands issued during the Chip-Erase operation are ignored.

Flash Erase-Suspend/-Resume Operations

The Erase-Suspend operation temporarily suspends a Sector- or Block-Erase operation thus allowing data to be read from any memory location, or program data into any sector/block that is not suspended for an Erase operation. The operation is executed by issuing a one-byte command sequence with Erase-Suspend command (B0H). The device automatically enters read mode within 20 µs after the Erase-Suspend command had been issued. Valid data can be read from any sector or block that is not suspended from an Erase operation. Reading at address location within erase-suspended sectors/blocks will output DQ_2 toggling and DQ_6 at "1". While in Erase-Suspend mode, a Program operation is allowed except for the sector or block selected for Erase-Suspend. To resume Sector-Erase or Block-Erase operation which has been suspended, the system must issue an Erase-Resume command. The operation is executed by issuing a one-byte command sequence with Erase Resume command (30H) at any address in the one-byte sequence.

Flash Write Operation Status Detection

The SST34HF16xG provides two software means to detect the completion of a Write (Program or Erase) cycle, in order to optimize the system Write cycle time. The software detection includes two status bits: Data# Polling (DQ_7) and Toggle Bit (DQ_6). The End-of-Write detection mode is enabled after the rising edge of WE#, which initiates the internal Program or Erase operation.

The actual completion of the nonvolatile write is asynchronous with the system; therefore, either a Data# Polling (DQ_7) or Toggle Bit (DQ_6) read may be simultaneous with the completion of the Write cycle. If this occurs, the system may possibly get an erroneous result, i.e., valid data may appear to conflict with either DQ_7 or DQ_6. In order to prevent spurious rejection, if an erroneous result occurs, the software routine should include a loop to read the accessed location an additional two (2) times. If both reads are valid, then the device has completed the Write cycle, otherwise the rejection is valid.

Flash Data# Polling (DQ_7)

When the device is in an internal Program operation, any attempt to read DQ_7 will produce the complement of the true data. Once the Program operation is completed, DQ_7 will produce true data. During internal Erase operation, any attempt to read DQ_7 will produce a '0'. Once the internal Erase operation is completed, DQ_7 will produce a '1'. The Data# Polling is valid after the rising edge of fourth WE# (or BEF#) pulse for Program operation. For Sector-, Block-, or Chip-Erase, the Data# Polling is valid after the rising edge of sixth WE# (or BEF#) pulse. See Figure 10 for Data# Polling (DQ_7) timing diagram and Figure 22 for a flowchart.

Toggle Bits (DQ_6 and DQ_2)

During the internal Program or Erase operation, any consecutive attempts to read DQ_6 will produce alternating "1"s and "0"s, i.e., toggling between 1 and 0. When the internal Program or Erase operation is completed, the DQ_6 bit will stop toggling. The device is then ready for the next operation. The toggle bit is valid after the rising edge of the fourth WE# (or BEF#) pulse for Program operations. For Sector-, Block-, or Chip-Erase, the toggle bit (DQ_6) is valid after the rising edge of sixth WE# (or BEF#) pulse. DQ_6 will be set to "1" if a Read operation is attempted on an Erase-suspended Sector/Block. If Program operation is initiated in a sector/block not selected in Erase-Suspend mode, DQ_6 will toggle.

An additional Toggle Bit is available on DQ_2, which can be used in conjunction with DQ_6 to check whether a particular sector is being actively erased or erase-suspended. Table 1 shows detailed status bit information. The Toggle Bit (DQ_2) is valid after the rising edge of the last WE# (or BEF#) pulse of a Write operation. See Figure 11 for Toggle Bit timing diagram and Figure 22 for a flowchart.

TABLE 1: WRITE OPERATION STATUS

Status		DQ_7	DQ_6	DQ_2
Normal Operation	Standard Program	DQ7#	Toggle	No Toggle
	Standard Erase	0	Toggle	Toggle
Erase-Suspend Mode	Read From Erase Suspended Sector/ Block	1	1	Toggle
	Read From Non-Erase Suspended Sector/ Block	Data	Data	Data
	Program	DQ7#	Toggle	No Toggle

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Note: DQ_7, DQ_6, and DQ_2 require a valid address when reading status information.

Data Protection

The SST34HF16xG provide both hardware and software features to protect nonvolatile data from inadvertent writes.

Hardware Data Protection

Noise/Glitch Protection: A WE# or BEF# pulse of less than 5 ns will not initiate a Write cycle.

V_{DD} Power Up/Down Detection: The Write operation is inhibited when V_{DD} is less than 1.5V.

Write Inhibit Mode: Forcing OE# low, BEF# high, or WE# high will inhibit the Write operation. This prevents inadvertent writes during power-up or power-down.

Hardware Block Protection

The SST34HF16xG provide a hardware block protection which protects the outermost 8 KWord in Bank 1. The block is protected when WP# is held low. See Figure 1 for Block-Protection location.

A user can disable block protection by driving WP# high thus allowing erase or program of data into the protected sectors. WP# must be held high prior to issuing the write command and remain stable until after the entire Write operation has completed.

Hardware Reset (RST#) - L3K only

The RST# pin provides a hardware method of resetting the device to read array data. When the RST# pin is held low for at least T_{RP}, any in-progress operation will terminate and return to Read mode (see Figure 18). When no internal Program/Erase operation is in progress, a minimum period of T_{RHR} is required after RST# is driven high before a valid Read can take place (see Figure 17).

The Erase operation that has been interrupted needs to be reinitiated after the device resumes normal operation mode to ensure data integrity. See Figures 17 and 18 for timing diagrams.

Software Data Protection (SDP)

The SST34HF16xG provide the JEDEC standard Software Data Protection scheme for all data alteration operations, i.e., Program and Erase. Any Program operation requires the inclusion of the three-byte sequence. The three-byte load sequence is used to initiate the Program operation, providing optimal protection from inadvertent Write operations, e.g., during the system power-up or power-down. Any Erase operation requires the inclusion of six-byte sequence. The SST34HF16xG are shipped with the Software Data Protection permanently enabled. See Table 5 for the specific software command codes. During SDP command sequence, invalid commands will abort the device to Read mode within T_{RC}. The contents of DQ_{15}-DQ_8 are "Don't Care" during any SDP command sequence.

Product Identification

The Product Identification mode identifies the device as SST34HF162G or SST34HF164G and the manufacturer as SST. This mode may be accessed by software operations only. The hardware device ID Read operation, which is typically used by programmers cannot be used on this device because of the shared lines between flash and SRAM in the multi-chip package. Therefore, application of high voltage to pin A_9 may damage this device. Users may use the software Product Identification operation to identify the part (i.e., using the device ID) when using multiple manufacturers in the same socket. For details, see Tables 4 and 5 for software operation, Figure 15 for the Software ID Entry and Read timing diagram and Figure 23 for the ID Entry command sequence flowchart.

TABLE 2: PRODUCT IDENTIFICATION

	ADDRESS	DATA
Manufacturer's ID	BK0000H	00BFH
Device ID		
SST34HF16xG	BK0001H	734BH

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Note: BK = Bank Address (A_{19}-A_{18})

Product Identification Mode Exit

In order to return to the standard Read mode, the Software Product Identification mode must be exited. Exit is accomplished by issuing the Software ID Exit command sequence, which returns the device to the Read mode. This command may also be used to reset the device to the Read mode after any inadvertent transient condition that apparently causes the device to behave abnormally, e.g., not read correctly. Please note that the Software ID Exit command is ignored during an internal Program or Erase operation. See Table 5 for software command codes, Figure 16 for timing waveform and Figure 23 for a flowchart.

SRAM Operation

With BES# low and BEF# high, the SST34HF162G/164G operate as either 128K x16 or 256K x16 CMOS SRAM, with fully static operation requiring no external clocks or timing strobes. The SST34HF162G/164G SRAM is mapped into the first 128 KWord address space. When BES# and BEF# are high, all memory banks are deselected and the device enters standby. Read and Write cycle times are equal. The control signals UBS# and LBS# provide access to the upper data byte and lower data byte. See Table 4 for SRAM Read and Write data byte control modes of operation.

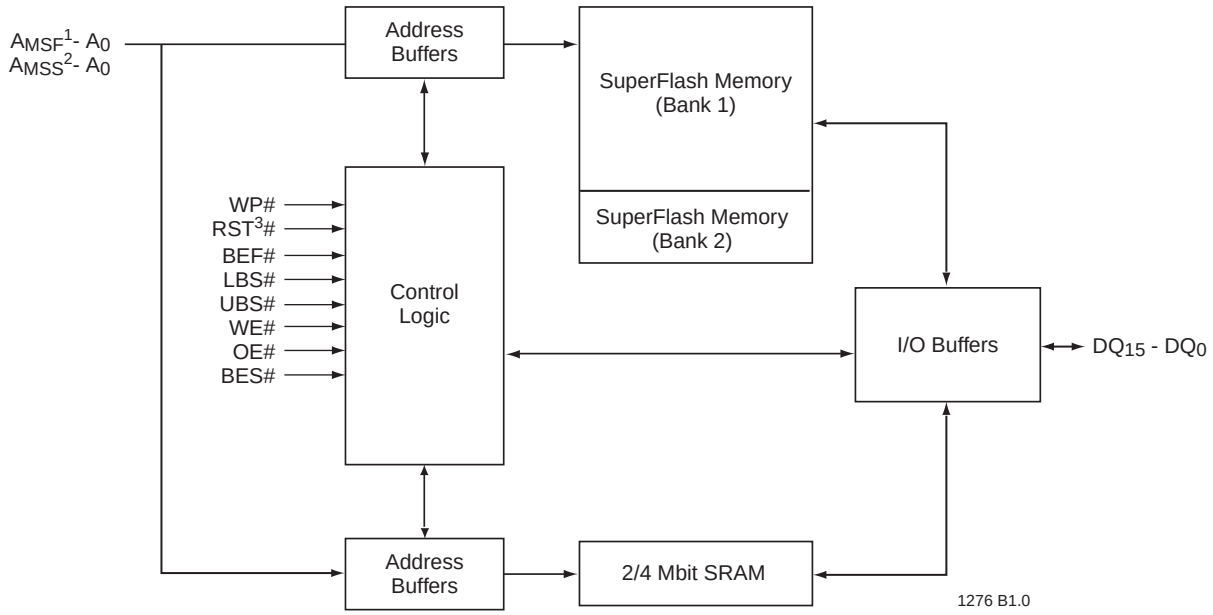
SRAM Read

The SRAM Read operation of the SST34HF162G/164G is controlled by OE# and BES#, both have to be low with WE# high for the system to obtain data from the outputs. BES# is used for SRAM bank selection. OE# is the output control and is used to gate data from the output pins. The data bus is in high impedance state when OE# is high. Refer to the Read cycle timing diagram, Figure 4, for further details.

SRAM Write

The SRAM Write operation of the SST34HF162G/164G is controlled by WE# and BES#, both have to be low for the system to write to the SRAM. During the Word-Write operation, the addresses and data are referenced to the rising edge of either BES# or WE# whichever occurs first. The write time is measured from the last falling edge of BES# or WE# to the first rising edge of BES# or WE#. Refer to the Write cycle timing diagrams, Figures 5 and 6, for further details.

FUNCTIONAL BLOCK DIAGRAM



Notes: 1. A_{MSF} = Most significant flash address
A_{MSF} = A_{19} for SST34HF162G/164G
2. A_{MSS} = Most significant SRAM address
A_{MSS} = A_{16} for SST34HF162G and A_{17} for SST34HF164G
3. RST# is only available on L3K package.

Sector Protection; 32 KWord Blocks; 2 KWord Sectors

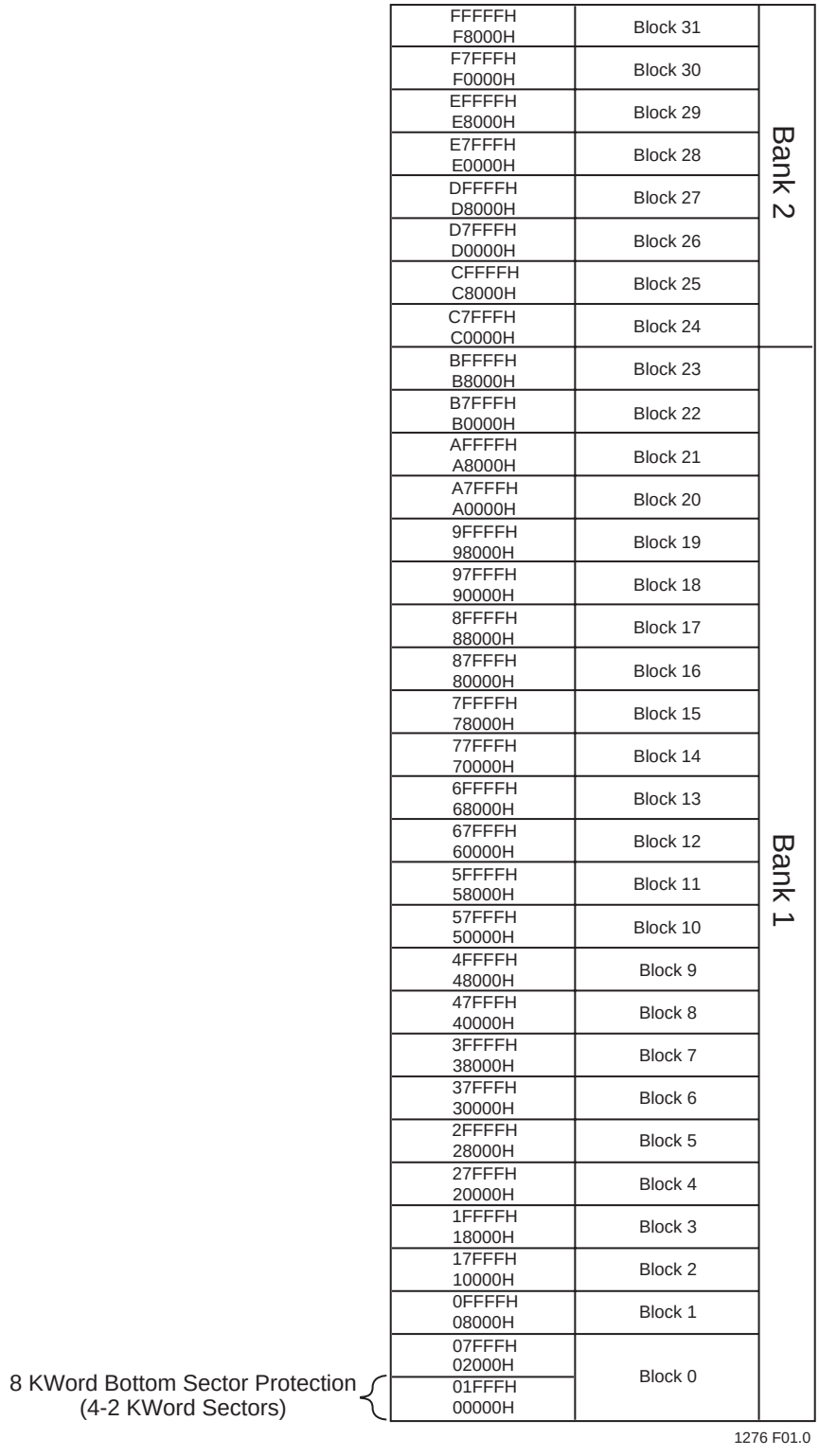


FIGURE 1: DUAL-BANK MEMORY ORGANIZATION

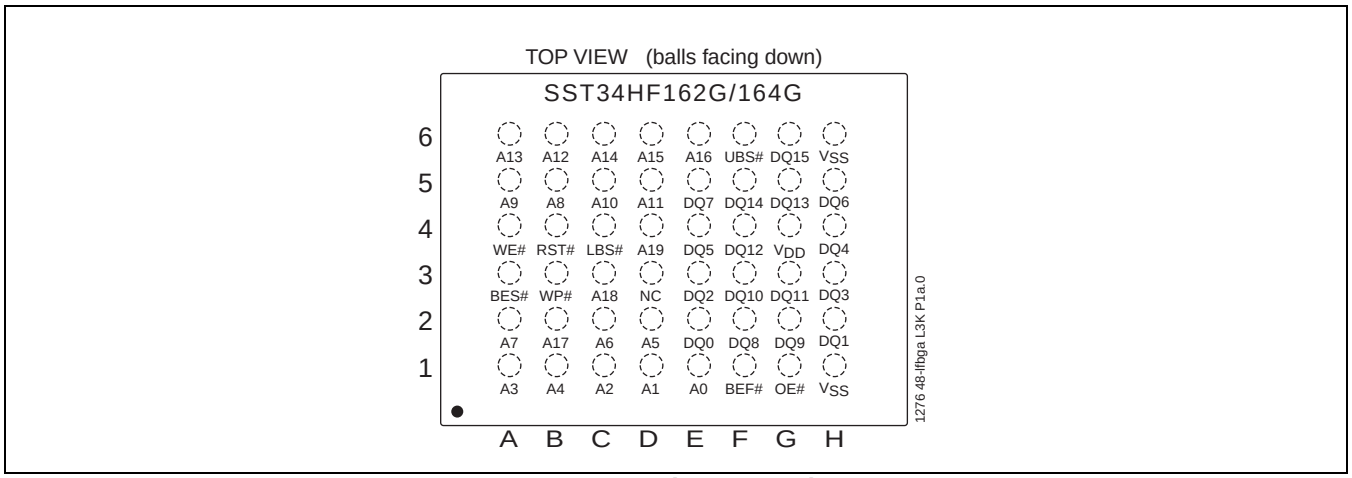


FIGURE 2: PIN ASSIGNMENTS FOR 48-BALL LFBGA (6MM X 8MM)

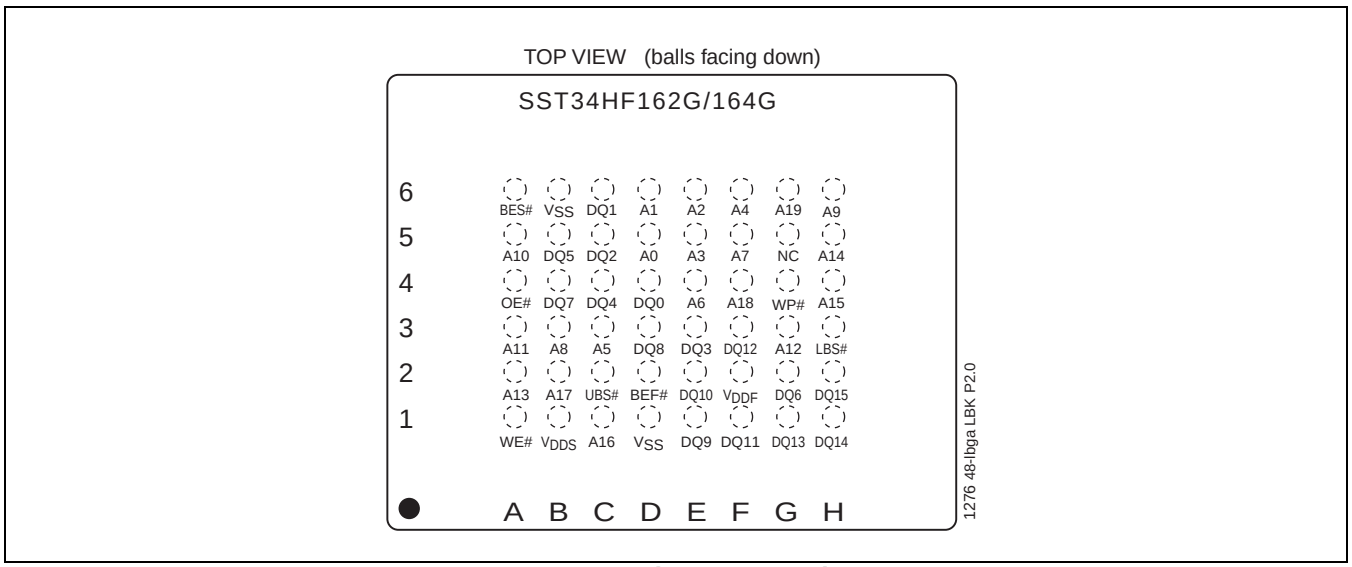


FIGURE 3: PIN ASSIGNMENTS FOR 48-BALL LBGA (10MM X 12MM)

TABLE 3: PIN DESCRIPTION

Symbol	Pin Name	Functions
A_{MSS}[1] to A_0	Address Inputs	To provide flash address, A_{19}-A_0. To provide SRAM address, A_{MSS}-A_0
DQ_{15}-DQ_0	Data Inputs/Outputs	To output data during Read cycles and receive input data during Write cycles. Data is internally latched during a flash Erase/Program cycle. The outputs are in tri-state when OE#, BES#, and BEF# are high.
BEF#	Flash Memory Bank Enable	To activate the Flash memory bank when BEF# is low
BES#	SRAM Memory Bank Enable	To activate the SRAM memory bank when BES# is low
OE#	Output Enable	To gate the data output buffers
WE#	Write Enable	To control the Write operations
UBS#	Upper Byte Control (SRAM)	To enable DQ_{15}-DQ_8
LBS#	Lower Byte Control (SRAM)	To enable DQ_7-DQ_0
WP#	Write Protect	To protect and unprotect the bottom 8 KWord (4 sectors) from Erase or Program operation
RST#	Reset	To Reset and return the device to Read mode
V_{SS}	Ground	
V_{DD}	Power Supply[2]	2.7-3.3V Power Supply
V_{DDF}	Power Supply (Flash)	2.7-3.3V Power Supply to Flash only
V_{DDS}	Power Supply (SRAM)	2.7-3.3V Power Supply to SRAM only
NC	No Connection	Unconnected pins

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1. A_{MSS} = Most Significant Address
   A_{MSS} = A_{16} for SST34HF162G and A_{17} for SST34HF164G
2. L3K package only

TABLE 4: OPERATIONAL MODES SELECTION FOR SRAM

Mode	BEF#[1]	BES#[1,2]	OE#[2]	WE#[2]	LBS#[2]	UBS#[2]	DQ_{15-0}	DQ_{15-8}	
Full Standby	V_{IH}	V_{IH}	X	X	X	X	HIGH-Z	HIGH-Z	HIGH-Z
		X	X	X	X	X			
Output Disable	V_{IH}	V_{IL}	V_{IH}	V_{IH}	X	X	HIGH-Z	HIGH-Z	HIGH-Z
		V_{IL}	X	X	V_{IH}	V_{IH}			
	V_{IL}	V_{IH}	V_{IH}	V_{IH}	X	X	HIGH-Z	HIGH-Z	HIGH-Z
		X							
Flash Read	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	D_{OUT}	D_{OUT}	DQ_{15-8}=HIGH-Z
		X							
Flash Write	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	X	D_{IN}	D_{IN}	DQ_{15-8}=HIGH-Z
		X							
Flash Erase	V_{IL}	V_{IH}	V_{IH}	V_{IL}	X	X	X	X	X
		X							
SRAM Read	V_{IH}	V_{IL}	V_{IL}	V_{IH}	V_{IL}	V_{IL}	D_{OUT}	D_{OUT}	D_{OUT}
					V_{IH}	V_{IL}	HIGH-Z	D_{OUT}	D_{OUT}
					V_{IL}	V_{IH}	D_{OUT}	HIGH-Z	HIGH-Z
SRAM Write	V_{IH}	V_{IL}	X	V_{IL}	V_{IL}	V_{IL}	D_{IN}	D_{IN}	D_{IN}
					V_{IH}	V_{IL}	HIGH-Z	D_{IN}	D_{IN}
					V_{IL}	V_{IH}	D_{IN}	HIGH-Z	HIGH-Z
Product Identification[3]	V_{IL}	V_{IH}	V_{IL}	V_{IH}	X	X	Manufacturer's ID[4] Device ID[4]		

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1. Do not apply BEF# = V_{IL} and BES# = V_{IL} at the same time
2. X can be V_{IL} or $V_{IH,}$ but no other value.
3. Software mode only
4. With A_{19}-A_{18} = $V_{IL;}$SST Manufacturer's ID = BFH, is read with A_0=0,
   SST34HF16xG Device ID = 734BH, is read with A_0=1

TABLE 5: SOFTWARE COMMAND SEQUENCE

Command Sequence	1st Bus Write Cycle		2nd Bus Write Cycle		3rd Bus Write Cycle		4th Bus Write Cycle		5th Bus Write Cycle		6th Bus Write Cycle	
	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]	Addr[1]	Data[2]
Program	555H	AAH	2AAH	55H	555H	A0H	WA[3]	Data				
Sector-Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	SA_X[4]	30H
Block-Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	BA_X[4]	50H
Chip-Erase	555H	AAH	2AAH	55H	555H	80H	555H	AAH	2AAH	55H	555H	10H
Erase-Suspend	XXXXH	B0H										
Erase-Resume	XXXXH	30H										
Software ID Entry[5]	555H	AAH	2AAH	55H	BK_X[6] 555H	90H						
Software ID Exit	555H	AAH	2AAH	55H	555H	F0H						
Software ID Exit	XXH	F0H										

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1. Address format A_{10}-A_0 (Hex), Addresses A_{19}-A_{11} can be V_{IL} or V_{IH}, but no other value, for the command sequence.
2. DQ_{15}-DQ_8 can be V_{IL} or V_{IH}, but no other value, for the command sequence
3. WA = Program word address
4. SA_X for Sector-Erase; uses A_{19}-A_{10} address lines
   BA_X for Block-Erase; uses A_{19}-A_{15} address lines
5. The device does not remain in Software Product Identification mode if powered down.
6. A_{19} and A_{18} = V_{IL}

Absolute Maximum Stress Ratings (Applied conditions greater than those listed under "Absolute Maximum Stress Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these conditions or conditions greater than those defined in the operational sections of this data sheet is not implied. Exposure to absolute maximum stress rating conditions may affect device reliability.)

Operating Temperature . . . . . -20°C to +85°C
Storage Temperature . . . . . -65°C to +125°C
D. C. Voltage on Any Pin to Ground Potential . . . . . -0.5V to V_{DD}[1]+0.3V
Transient Voltage (<20 ns) on Any Pin to Ground Potential . . . . . -1.0V to V_{DD}[1]+1.0V
Package Power Dissipation Capability (Ta = 25°C) 1.0W
Surface Mount Solder Reflow Temperature: . . . . . "with-Pb" units[2]: 240°C for 3 seconds
. . . . . "non-Pb" units: 260°C for 3 seconds
Output Short Circuit Current[3] . . . . . 50 mA

1. V_{DD} = V_{DDF} and V_{DDS}
2. Certain "with-Pb" package types are capable of 260°C for 3 seconds; please consult the factory for the latest information.
3. Outputs shorted for no more than one second. No more than one output shorted at a time.

OPERATING RANGE

Range	Ambient Temp	V_{DD}
Commercial	0°C to +70°C	2.7-3.3V
Extended	-20°C to +85°C	2.7-3.3V

AC CONDITIONS OF TEST

Input Rise/Fall Time	5 ns
Output Load	C_L = 30 pF
See Figures 19 and 20	

TABLE 6: DC OPERATING CHARACTERISTICS (V_{DD} = V_{DDF} AND V_{DDS} = 2.7-3.3V)

Symbol	Parameter	Limits			Test Conditions
		Min	Max	Units	
I_{DD}[1]	Active V_{DD} Current				Address input = V_{ILT}/V_{IHT}, at f=5 MHz, $V_{DD}=V_{DD}$ Max, all DQs open
	Read				OE#=V_{IL}, WE#=V_{IH}
	Flash		15	mA	BEF#=V_{IL}, BES#=V_{IH}
	SRAM		10	mA	BEF#=V_{IH}, BES#=V_{IL}
	Concurrent Operation		45	mA	BEF#=V_{IH}, BES#=V_{IL}
	Write[2]				WE#=V_{IL}
	Flash		40	mA	BEF#=V_{IL}, BES#=V_{IH}, OE#=V_{IH}
	SRAM		30	mA	BEF#=V_{IH}, BES#=V_{IL}
I_{SB}	Standby V_{DD} Current		30	µA	V_{DD} = V_{DD} Max, BEF#=BES#=V_{IHC}
I_{RT}	Reset V_{DD} Current[3]		30	µA	RST#=GND
I_{LI}	Input Leakage Current		1	µA	V_{IN}=GND to V_{DD}, $V_{DD}=V_{DD}$ Max
I_{LO}	Output Leakage Current		10	µA	V_{OUT}=GND to V_{DD}, $V_{DD}=V_{DD}$ Max
V_{IL}	Input Low Voltage		0.8	V	$V_{DD}=V_{DD}$ Min
V_{ILC}	Input Low Voltage (CMOS)		0.3	V	$V_{DD}=V_{DD}$ Max
V_{IH}	Input High Voltage	0.7 V_{DD}		V	$V_{DD}=V_{DD}$ Max
V_{IHC}	Input High Voltage (CMOS)	V_{DD}-0.3		V	$V_{DD}=V_{DD}$ Max
V_{OLF}	Flash Output Low Voltage		0.2	V	I_{OL}=100 µA, $V_{DD}=V_{DD}$ Min
V_{OHF}	Flash Output High Voltage	V_{DD}-0.2		V	I_{OH}=-100 µA, $V_{DD}=V_{DD}$ Min
V_{OLS}	SRAM Output Low Voltage		0.4	V	IOL =1 mA, $V_{DD}=V_{DD}$ Min
V_{OHS}	SRAM Output High Voltage	2.2		V	IOH =-500 µA, $V_{DD}=V_{DD}$ Min

T6.0 1276

1. See Figure 19
2. I_{DD} active while Erase or Program is in progress.
3. L3K package only

TABLE 7: RECOMMENDED SYSTEM POWER-UP TIMINGS

Symbol	Parameter	Minimum	Units
$T_{PU-READ}$[1]	Power-up to Read Operation	100	µs
$T_{PU-WRITE}$[1]	Power-up to Write Operation	100	µs

T7.0 1276

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 8: CAPACITANCE (Ta = 25°C, f=1 Mhz, other pins open)

Parameter	Description	Test Condition	Maximum
$C_{I/O}$[1]	I/O Pin Capacitance	$V_{I/O}$ = 0V	20 pF
C_{IN}[1]	Input Capacitance	V_{IN} = 0V	16 pF

T8.0 1276

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 9: FLASH RELIABILITY CHARACTERISTICS

Symbol	Parameter	Minimum Specification	Units	Test Method
N_{END}[1]	Endurance	10,000	Cycles	JEDEC Standard A117
T_{DR}[1]	Data Retention	100	Years	JEDEC Standard A103
I_{LTH}[1]	Latch Up	100 + I_{DD}	mA	JEDEC Standard 78

T9.0 1276

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

AC CHARACTERISTICS

TABLE 10: SRAM READ CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T_{RCS}	Read Cycle Time	70		ns
T_{AAS}	Address Access Time		70	ns
T_{BES}	Bank Enable Access Time		70	ns
T_{OES}	Output Enable Access Time		35	ns
T_{BYES}	UBS#, LBS# Access Time		70	ns
T_{BLZS}[1]	BES# to Active Output	0		ns
T_{OLZS}[1]	Output Enable to Active Output	0		ns
T_{BYLZS}[1]	UBS#, LBS# to Active Output	0		ns
T_{BHZS}[1]	BES# to High-Z Output		25	ns
T_{OHZS}[1]	Output Disable to High-Z Output		25	ns
T_{BYHZS}[1]	UBS#, LBS# to High-Z Output		35	ns
T_{OHS}	Output Hold from Address Change	10		ns

T10.0 1276

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.

TABLE 11: SRAM WRITE CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T_{WCS}	Write Cycle Time	70		ns
T_{BWS}	Bank Enable to End-of-Write	60		ns
T_{AWS}	Address Valid to End-of-Write	60		ns
T_{ASTS}	Address Set-up Time	0		ns
T_{WPS}	Write Pulse Width	60		ns
T_{WRS}	Write Recovery Time	0		ns
T_{BYWS}	UBS#, LBS# to End-of-Write	60		ns
T_{ODWS}	Output Disable from WE# Low		30	ns
T_{OEWS}	Output Enable from WE# High	0		ns
T_{DSS}	Data Set-up Time	30		ns
T_{DHS}	Data Hold from Write Time	0		ns

T11.0 1276

TABLE 12: FLASH READ CYCLE TIMING PARAMETERS V_{DD} = 2.7-3.3V

Symbol	Parameter	Min	Max	Units
T_{RC}	Read Cycle Time	70		ns
T_{CE}	Chip Enable Access Time		70	ns
T_{AA}	Address Access Time		70	ns
T_{OE}	Output Enable Access Time		35	ns
T_{CLZ}[1]	BEF# Low to Active Output	0		ns
T_{OLZ}[1]	OE# Low to Active Output	0		ns
T_{CHZ}[1]	BEF# High to High-Z Output		20	ns
T_{OHZ}[1]	OE# High to High-Z Output		20	ns
T_{OH}[1]	Output Hold from Address Change	0		ns
T_{RP}[1,2]	RST# Pulse Width	500		ns
T_{RHR}[1,2]	RST# High Before Read	50		ns
T_{RY}[1,2,3]	RST# Pin Low to Read		20	µs

T12.0 1276

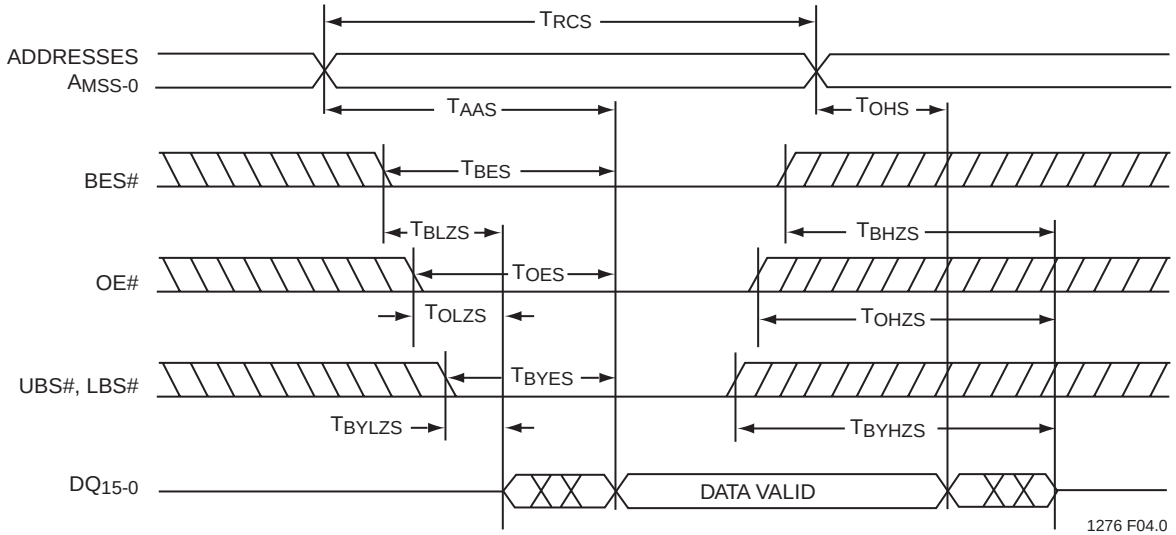
1. This parameter is measured only for initial qualification and after the design or process change that could affect this parameter.
2. L3K package only
3. This parameter applies to Sector-Erase, Block-Erase and Program operations. This parameter does not apply to Chip-Erase.

TABLE 13: FLASH PROGRAM/ERASE CYCLE TIMING PARAMETERS

Symbol	Parameter	Min	Max	Units
T_{BP}	Program Time		12	µs
T_{AS}	Address Setup Time	0		ns
T_{AH}	Address Hold Time	40		ns
T_{CS}	WE# and BEF# Setup Time	0		ns
T_{CH}	WE# and BEF# Hold Time	0		ns
T_{OES}	OE# High Setup Time	0		ns
T_{OEH}	OE# High Hold Time	10		ns
T_{CP}	BEF# Pulse Width	40		ns
T_{WP}	WE# Pulse Width	40		ns
T_{WPH}[1]	WE# Pulse Width High	30		ns
T_{CPH}[1]	BEF# Pulse Width High	30		ns
T_{DS}	Data Setup Time	30		ns
T_{DH}[1]	Data Hold Time	0		ns
T_{IDA}[1]	Software ID Access and Exit Time		150	ns
T_{ES}	Erase-Suspend Latency		20	µs
T_{BR}[1]	Bus# Recovery Time		1	µs
T_{SE}	Sector-Erase		25	ms
T_{BE}	Block-Erase		25	ms
T_{SCE}	Chip-Erase		50	ms

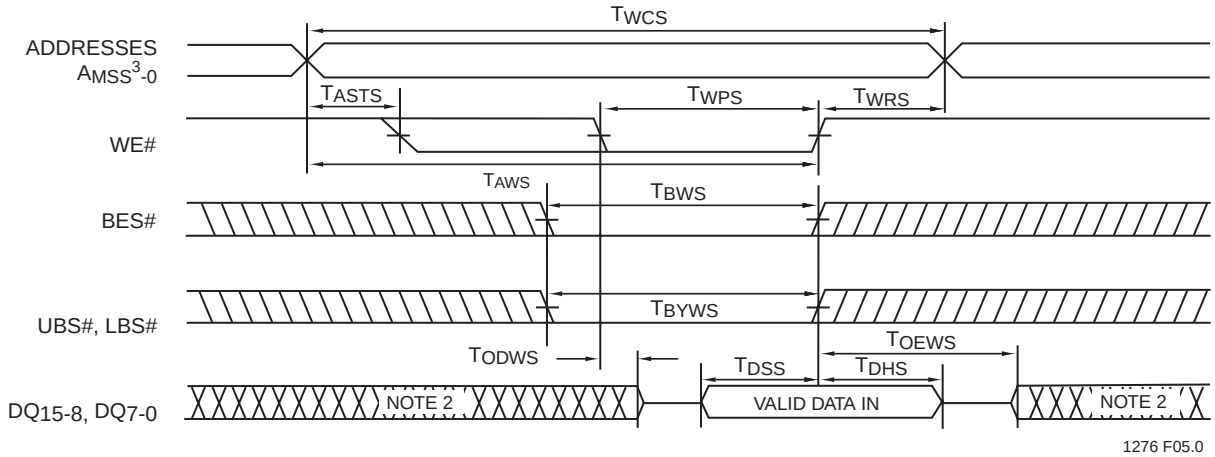
T13.1 1276

1. This parameter is measured only for initial qualification and after a design or process change that could affect this parameter.



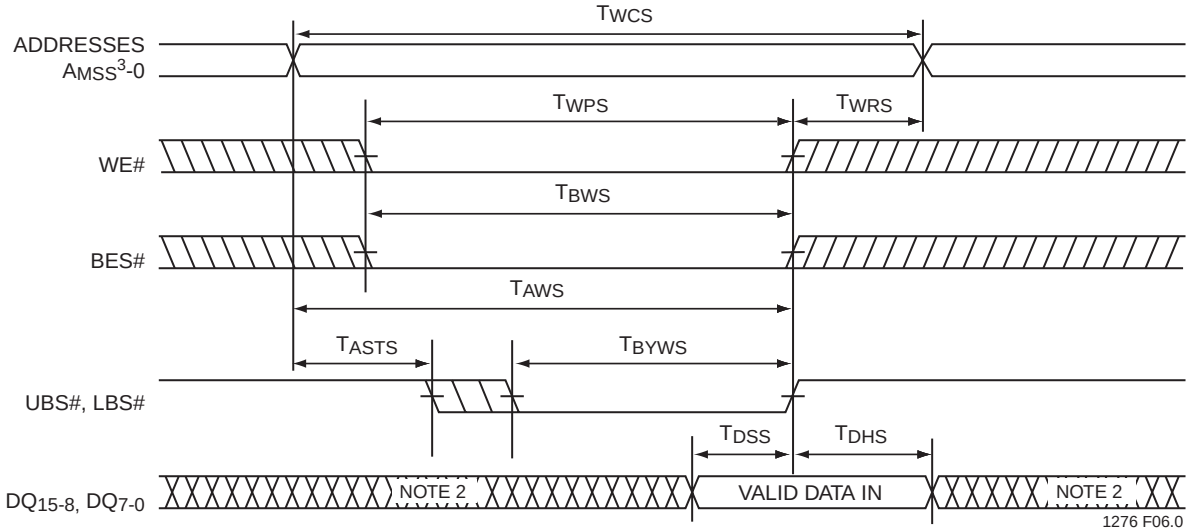
Note: A_{MSS} = Most Significant Address
A_{MSS} = A_{16} for SST34HF162G and A_{17} SST34HF164G

FIGURE 4: SRAM READ CYCLE TIMING DIAGRAM



Note: 1. If OE# is High during the Write cycle, the outputs will remain at high impedance.
2. If BES# goes low coincident with or after WE# goes low, the output will remain at high impedance.
If BES# goes high coincident with or before WE# goes high, the output will remain at high impedance.
Because D_{IN} signals may be in the output state at this time, input signals of reverse polarity must not be applied.
3. A_{MSS} = Most Significant SRAM Address
A_{MSS} = A_{16} for SST34HF162G and A_{17} for SST34HF164G

FIGURE 5: SRAM WRITE CYCLE TIMING DIAGRAM (WE# CONTROLLED)[1]



Note: 1. If OE# is High during the Write cycle, the outputs will remain at high impedance.
2. Because D_{IN} signals may be in the output state at this time, input signals of reverse polarity must not be applied.
3. A_{MSS} = Most Significant SRAM Address
A_{MSS} = A_{16} for SST34HF162G and A_{17} for SST34HF164G

FIGURE 6: SRAM WRITE CYCLE TIMING DIAGRAM (UBS#, LBS# CONTROLLED)[1]

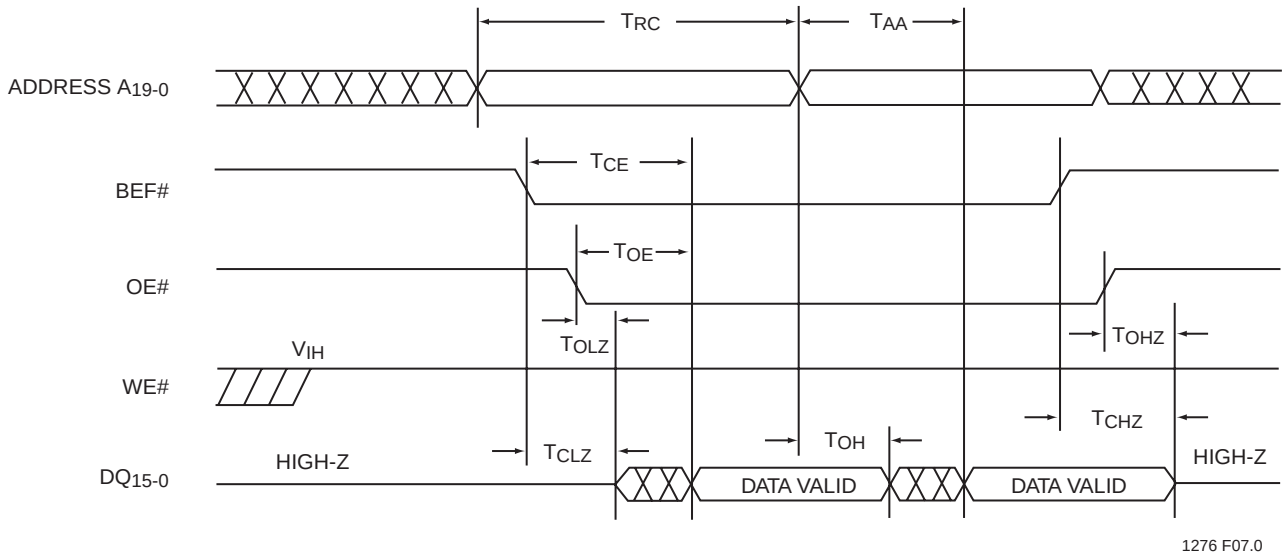
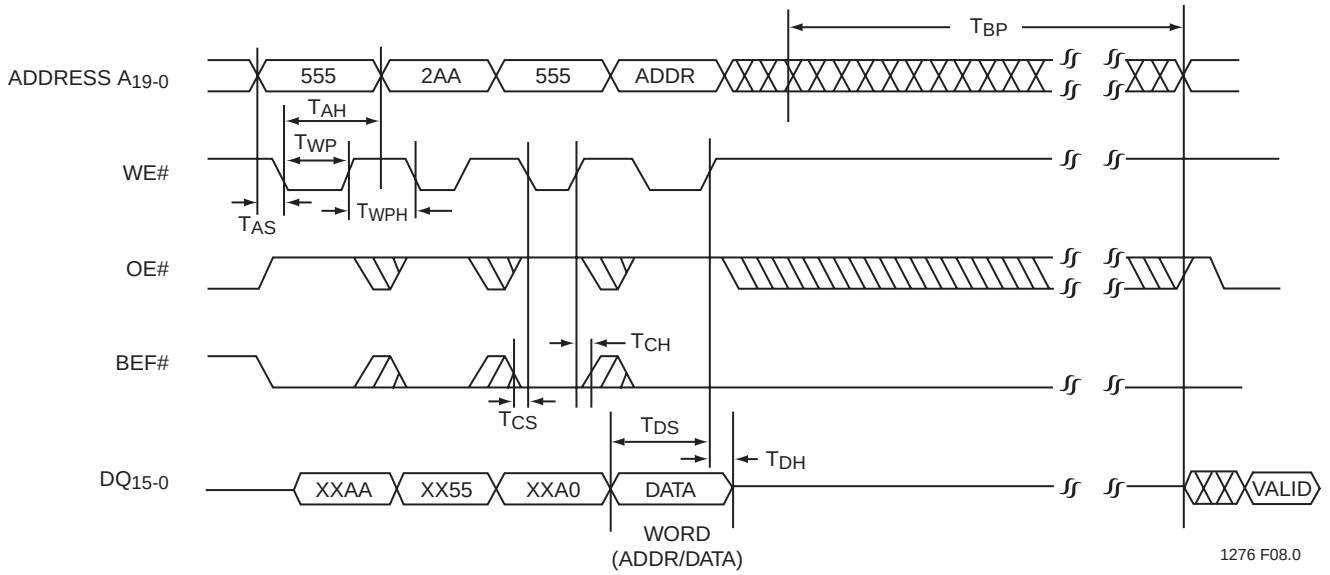
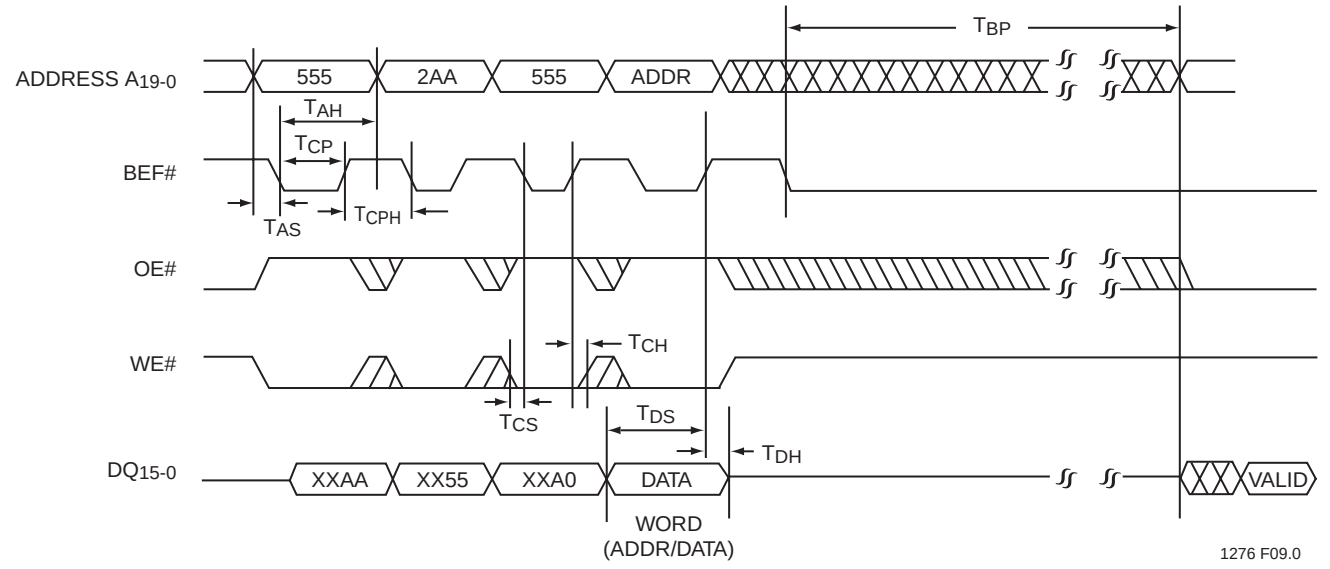


FIGURE 7: FLASH READ CYCLE TIMING DIAGRAM



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 8: FLASH WE# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 9: FLASH BEF# CONTROLLED PROGRAM CYCLE TIMING DIAGRAM

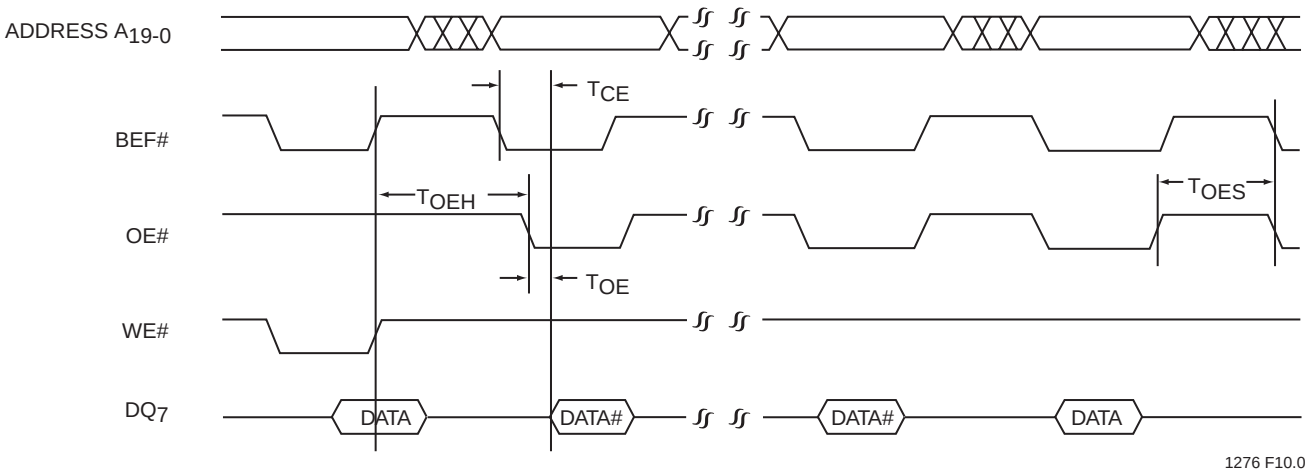


FIGURE 10: FLASH DATA# POLLING TIMING DIAGRAM

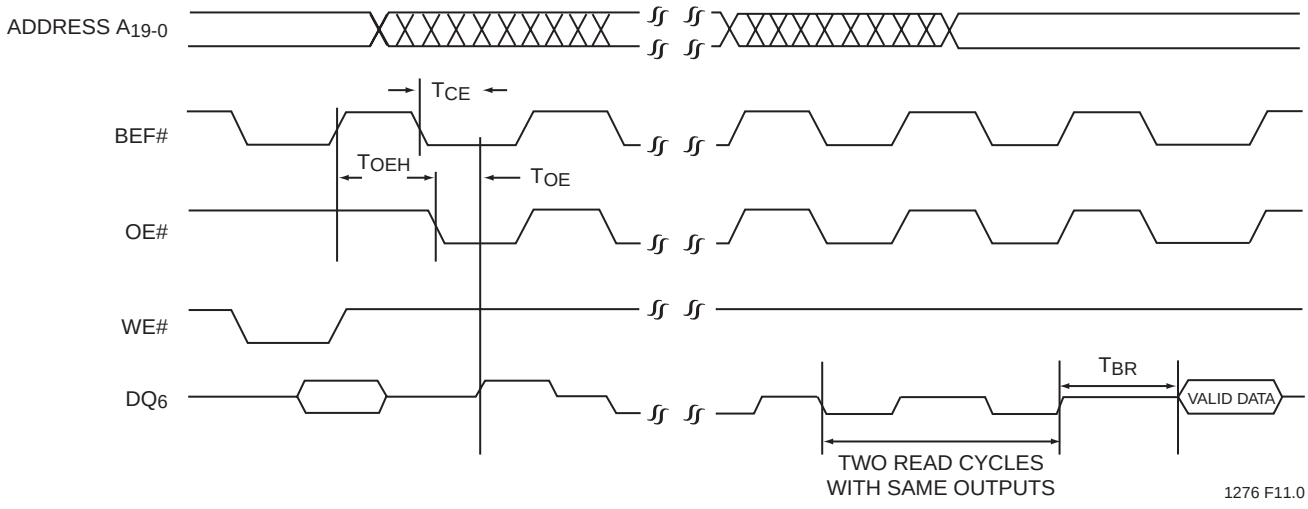
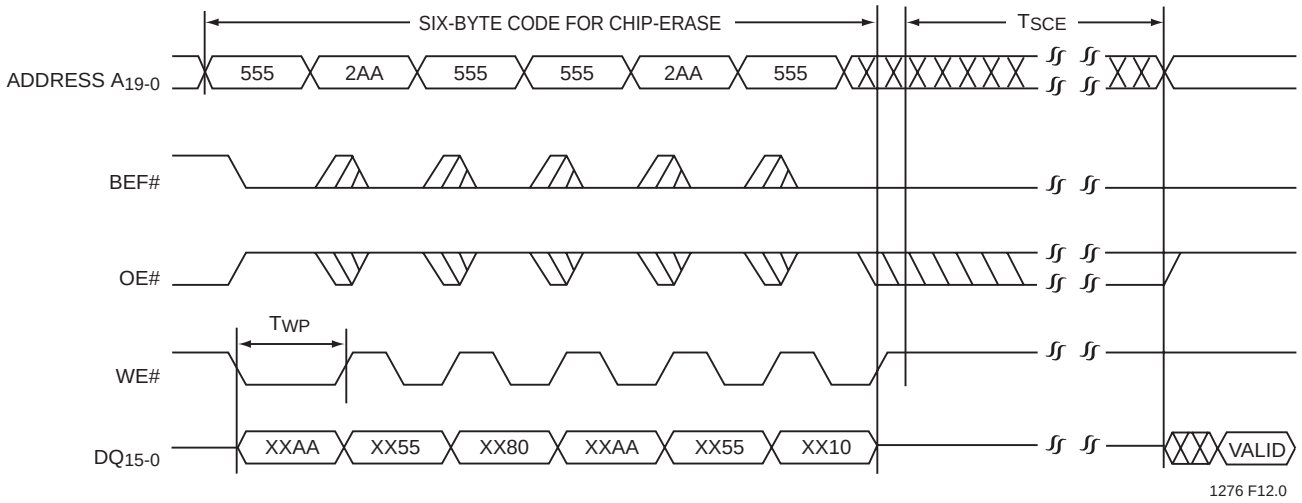
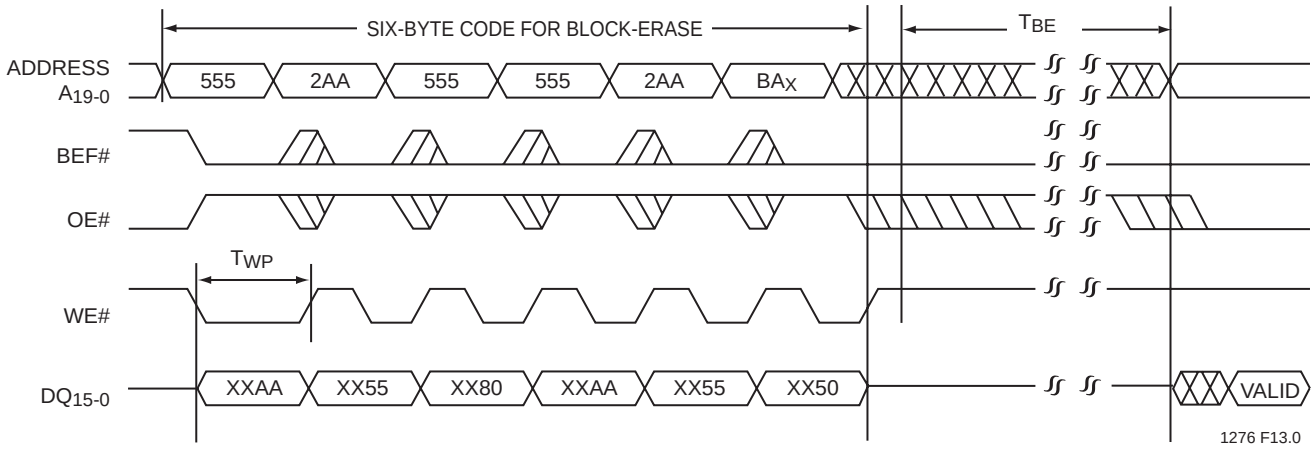


FIGURE 11: FLASH TOGGLE BIT TIMING DIAGRAM



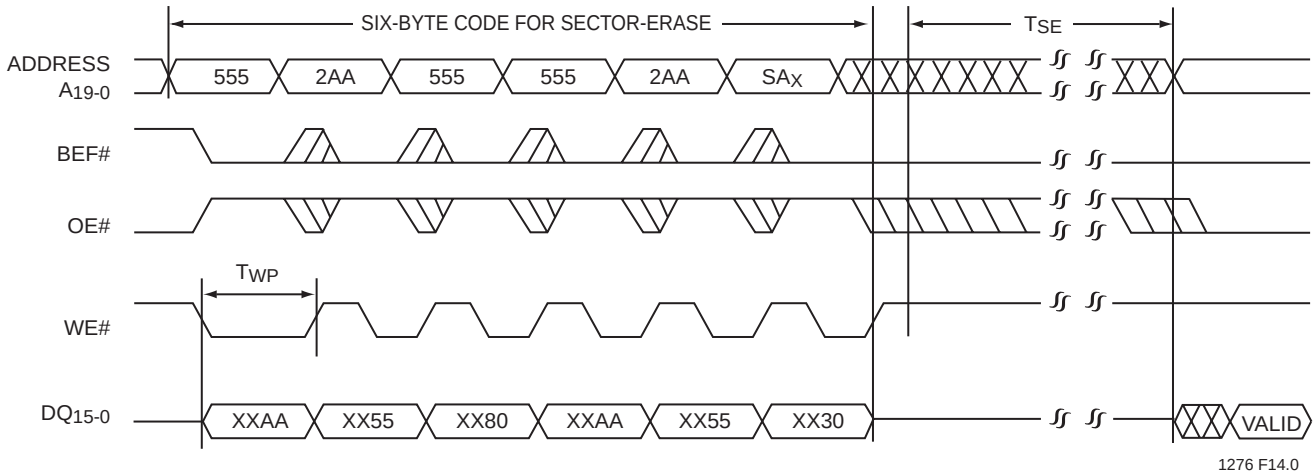
Note: This device also supports BEF# controlled Chip-Erase operation.
The WE# and BEF# signals are interchangeable as long as minimum timings are met. (See Table 13.)
X can be V_{IL} or $V_{IH,}$ but no other value.

FIGURE 12: FLASH WE# CONTROLLED CHIP-ERASE TIMING DIAGRAM



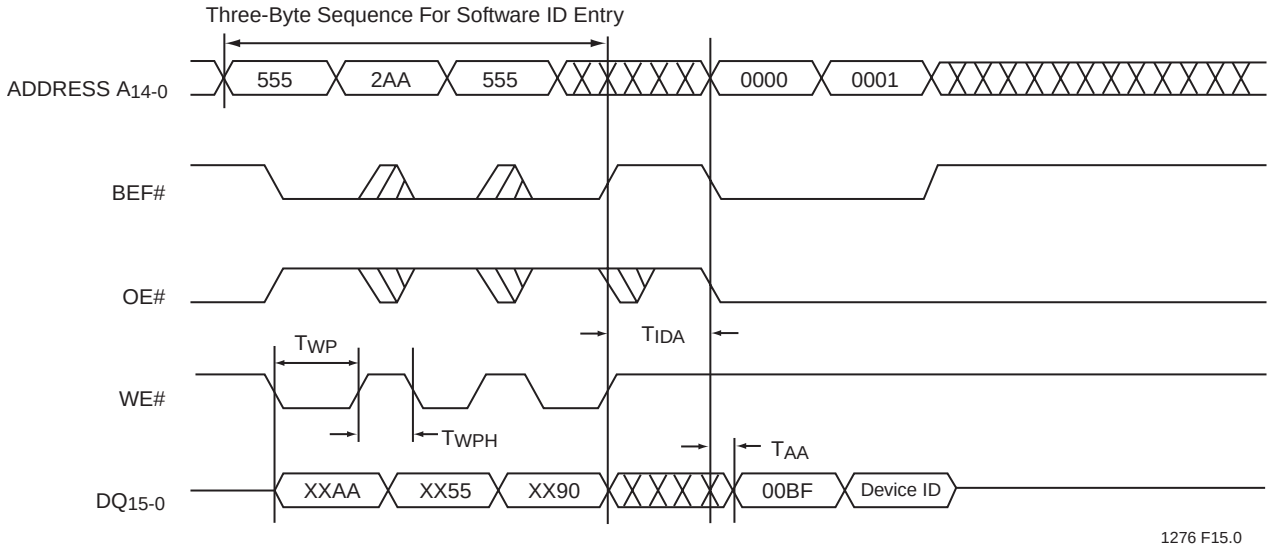
Note: This device also supports BEF# controlled Block-Erase operation.
The WE# and BEF# signals are interchangeable as long as minimum timings are met. (See Table 13.)
BA_X = Block Address
X can be V_{IL} or $V_{IH,}$ but no other value.

FIGURE 13: FLASH WE# CONTROLLED BLOCK-ERASE TIMING DIAGRAM



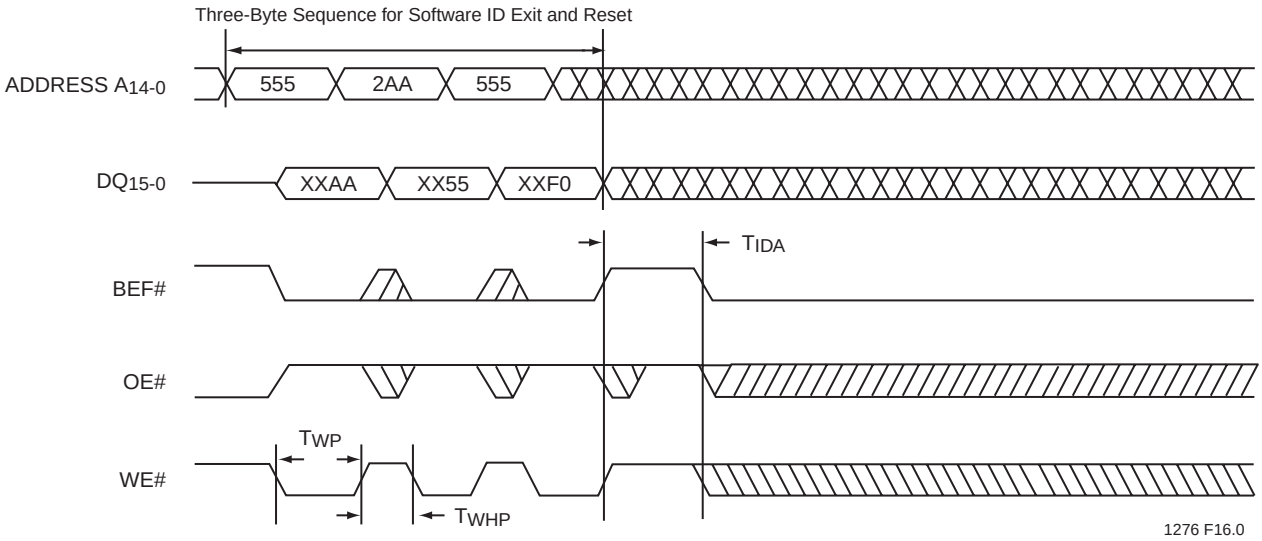
Note: This device also supports BEF# controlled Sector-Erase operation.
The WE# and BEF# signals are interchangeable as long as minimum timings are met. (See Table 13.)
SA_X = Sector Address
X can be V_{IL} or $V_{IH,}$ but no other value.

FIGURE 14: FLASH WE# CONTROLLED SECTOR-ERASE TIMING DIAGRAM



Note: X can be V_{IL} or $V_{IH,}$ but no other value.
Device ID - 734BH for SST34HF16xG

FIGURE 15: FLASH SOFTWARE ID ENTRY AND READ



Note: X can be V_{IL} or V_{IH}, but no other value

FIGURE 16: FLASH SOFTWARE ID EXIT

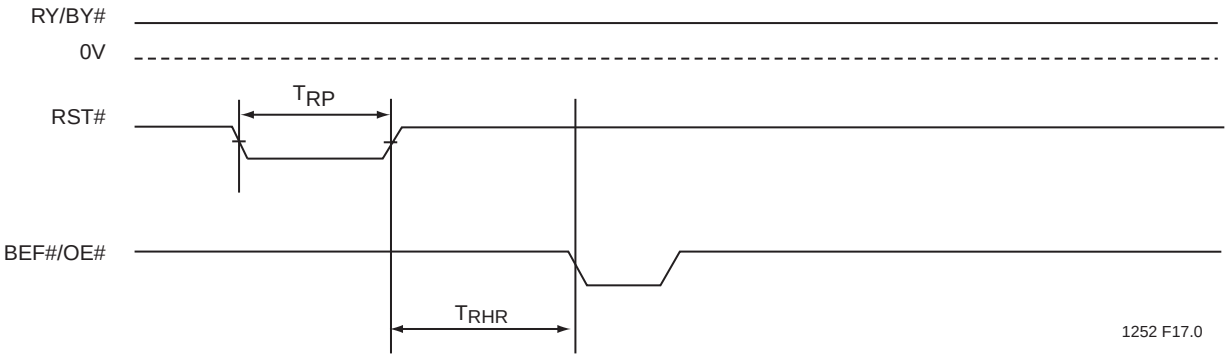


FIGURE 17: RST# TIMING (WHEN NO INTERNAL OPERATION IS IN PROGRESS) L3K PACKAGE ONLY

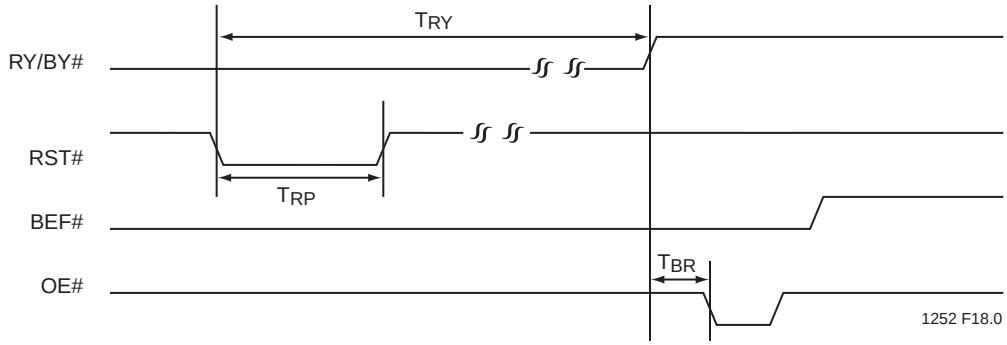
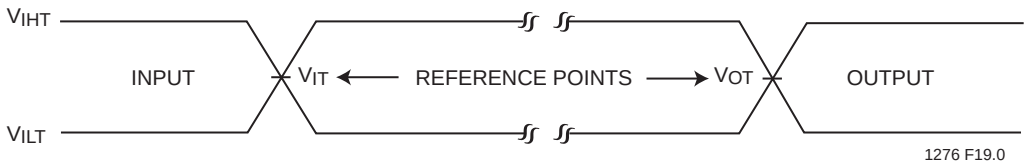


FIGURE 18: RST# TIMING (DURING SECTOR- OR BLOCK-ERASE OPERATION) L3K PACKAGE ONLY



AC test inputs are driven at V_{IHT} (0.9 V_{DD}) for a logic "1" and V_{ILT} (0.1 V_{DD}) for a logic "0". Measurement reference points for inputs and outputs are V_{IT} (0.5 V_{DD}) and V_{OT} (0.5 V_{DD}). Input rise and fall times (10% ↔ 90%) are <5 ns.

Note: V_{IT} - V_{INPUT} Test
V_{OT} - V_{OUTPUT} Test
V_{IHT} - V_{INPUT} HIGH Test
V_{ILT} - V_{INPUT} LOW Test

FIGURE 19: AC INPUT/OUTPUT REFERENCE WAVEFORMS

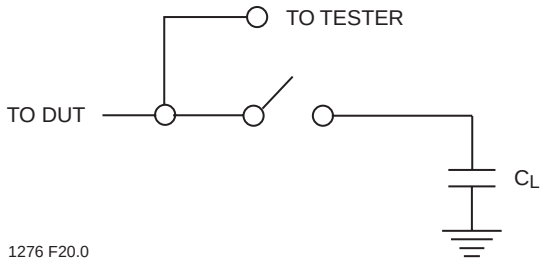
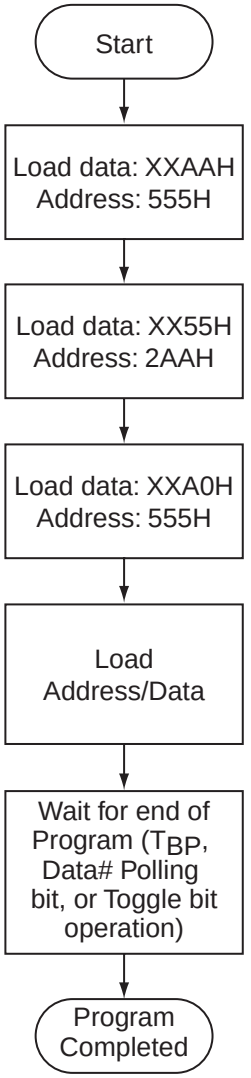


FIGURE 20: A TEST LOAD EXAMPLE



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 21: PROGRAM ALGORITHM

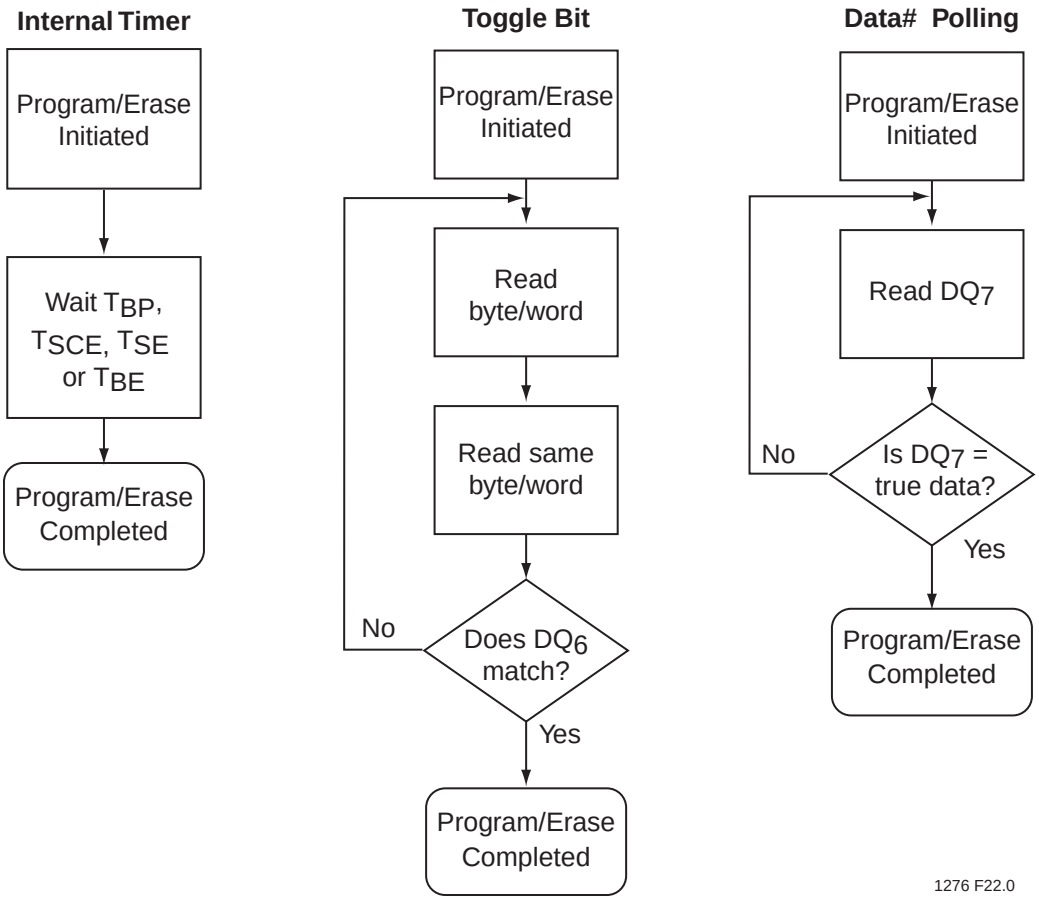
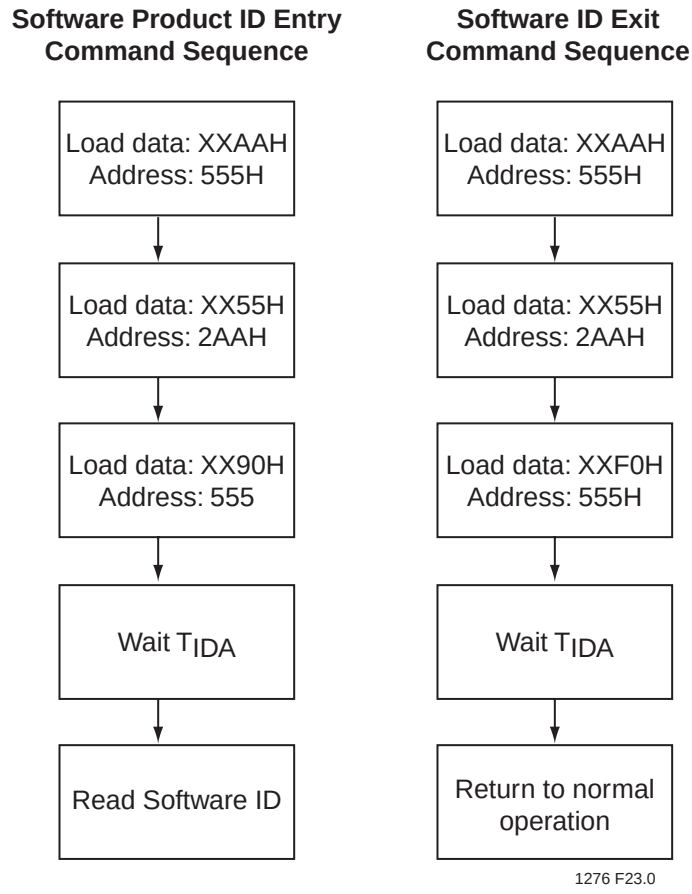
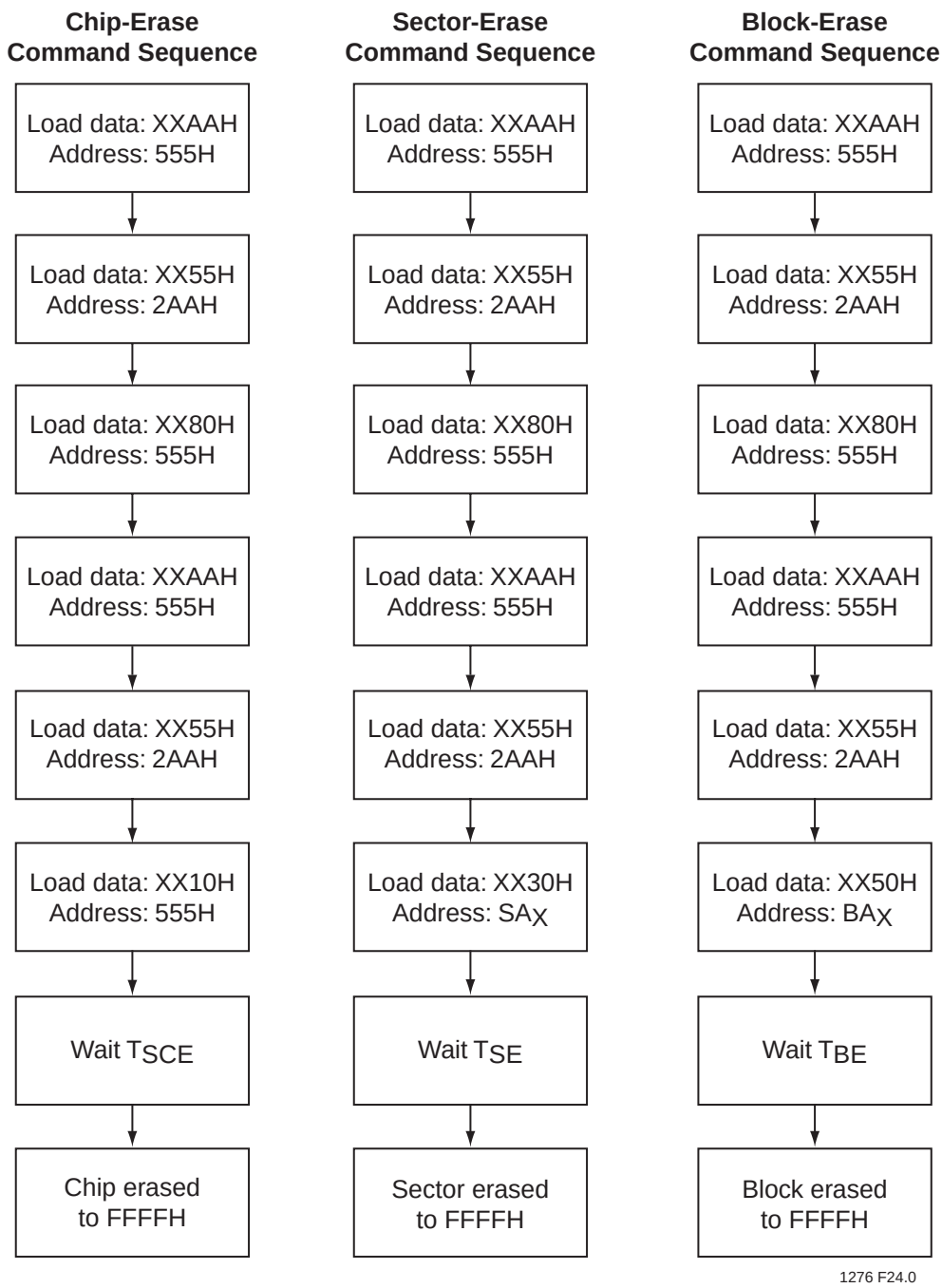


FIGURE 22: WAIT OPTIONS



Note: X can be V_{IL} or V_{IH}, but no other value.

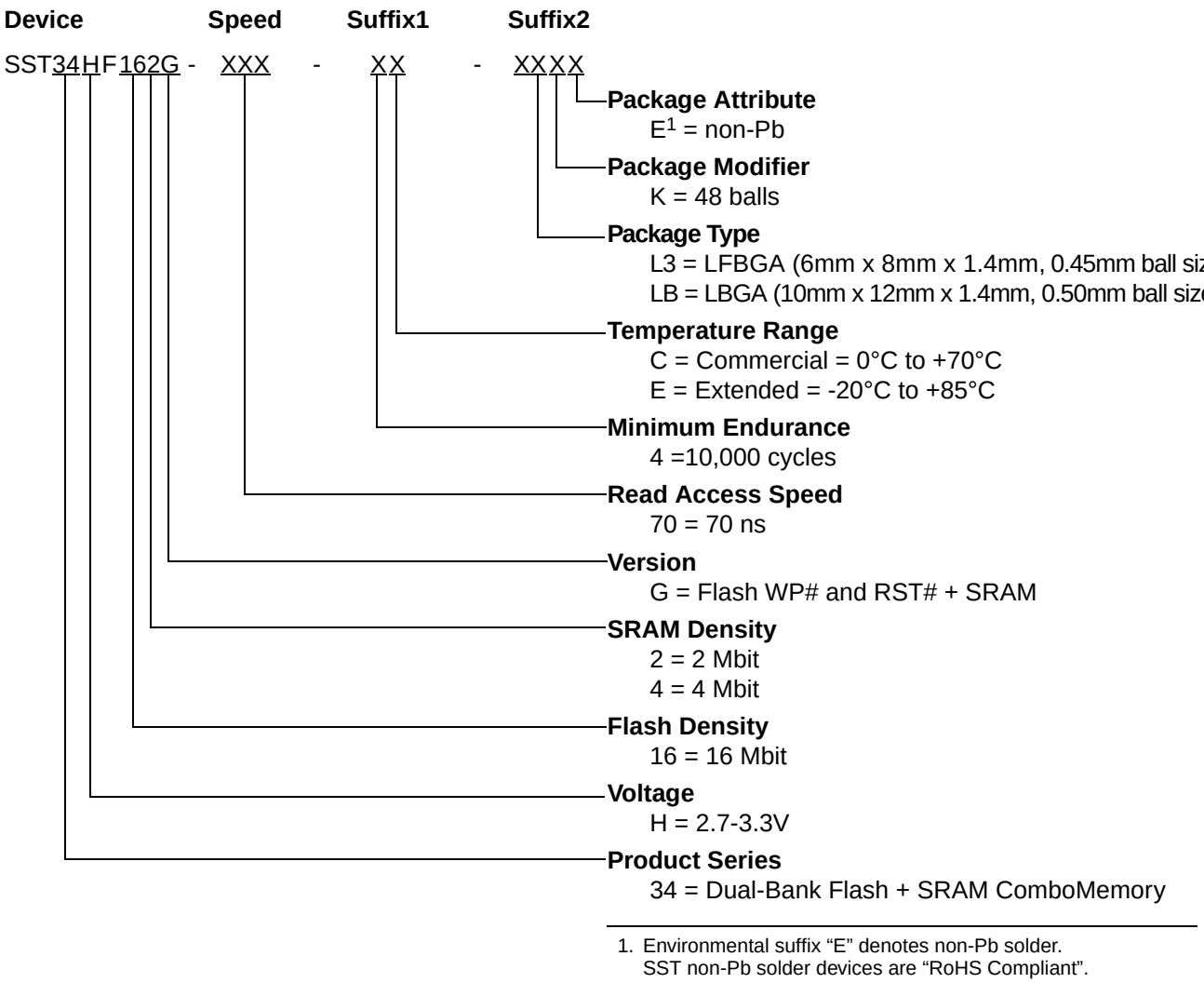
FIGURE 23: SOFTWARE PRODUCT ID COMMAND FLOWCHARTS



Note: X can be V_{IL} or V_{IH}, but no other value.

FIGURE 24: ERASE COMMAND SEQUENCE

PRODUCT ORDERING INFORMATION



1. Environmental suffix “E” denotes non-Pb solder.
SST non-Pb solder devices are “RoHS Compliant”.

Valid combinations for SST34HF162G

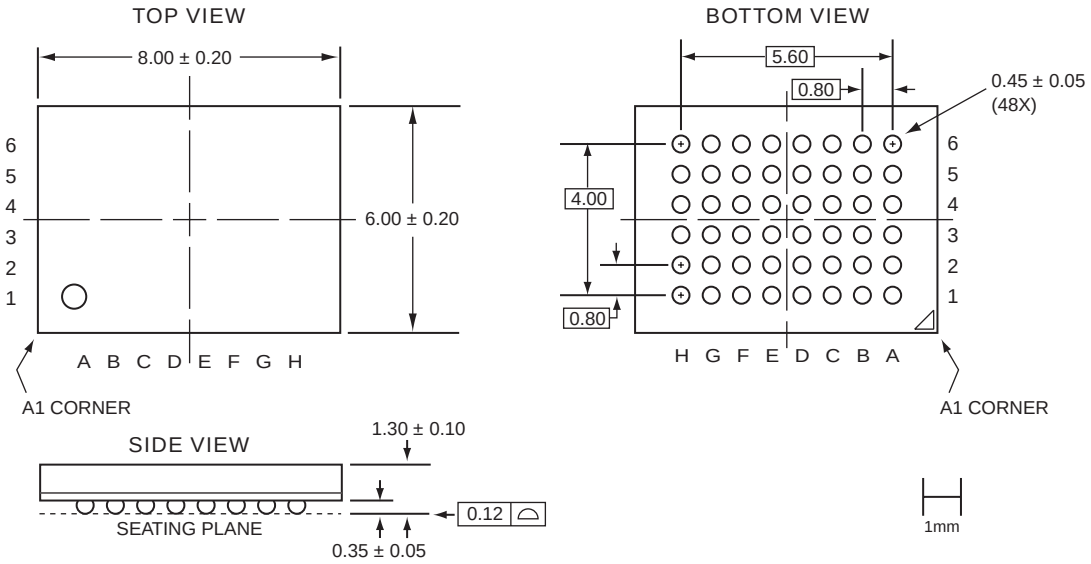
SST34HF162G-70-4C-LBK	SST34HF162G-70-4C-L3KE
SST34HF162G-70-4E-LBK	SST34HF162G-70-4E-L3KE

Valid combinations for SST34HF164G

SST34HF164G-70-4C-LBK	SST34HF164G-70-4C-L3KE
SST34HF164G-70-4E-LBK	SST34HF164G-70-4E-L3KE

Note: Valid combinations are those products in mass production or will be in mass production. Consult your SST sales representative to confirm availability of valid combinations and to determine availability of new combinations.

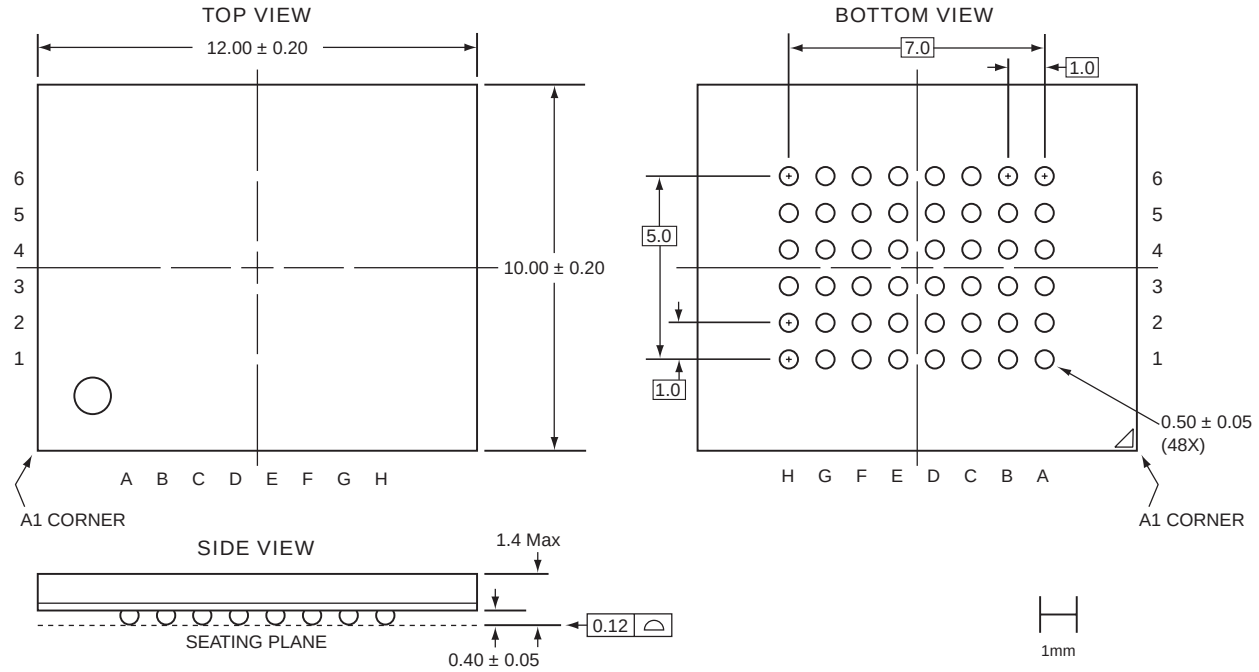
PACKAGING DIAGRAMS



Note: 1. Except for total height dimension, complies with JEDEC Publication 95, MO-210, variant 'AB-1', although some dimensions may be more stringent.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.12 mm
4. Ball opening size is 0.38 mm (± 0.05 mm)

48-lfbga-L3K-6x8-450mic-5

48-BALL LOW-PROFILE, FINE-PITCH BALL GRID ARRAY (LFBGA) 6MM X 8MM
SST PACKAGE CODE: L3K



Note: 1. Although many dimensions are similar to those of JEDEC Publication 95, MO-210, this specific package is not registered.
2. All linear dimensions are in millimeters.
3. Coplanarity: 0.12 mm
4. Ball opening size is 0.4 mm (± 0.05 mm)

48-lbga-LBK-10x12-500mic-2

48-BALL LOW-PROFILE BALL GRID ARRAY (LBGA) 10MM X 12MM
SST PACKAGE CODE: LBK

TABLE 14: REVISION HISTORY

Number	Description	Date
00	• Initial Release	Nov 2004