FAIRCHILD SEMICONDUCTOR®

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RMPA0966 *i-Lo*™ WCDMA Band V Power Amplifier Module

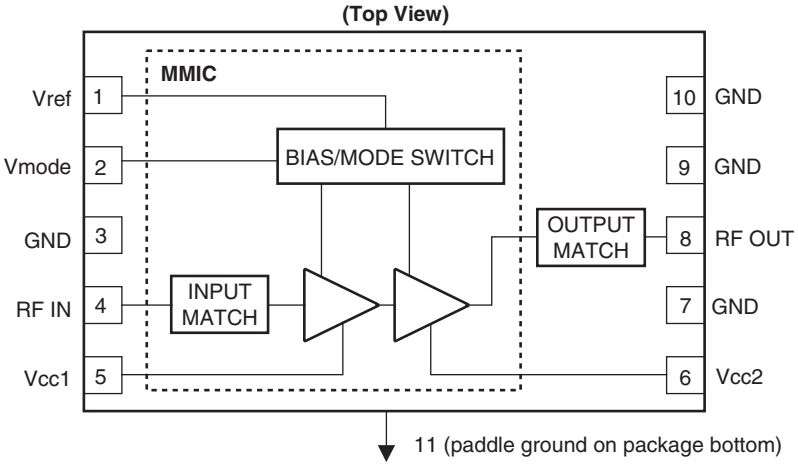
Features

- 42% CDMA/WCDMA efficiency at +28dBm Pout
- 21% CDMA/WCDMA efficiency (56mA total current) at +16dBm Pout
- Meets HSDPA performance requirements
- 50% AMPS mode efficiency at +31dBm Pout
- Low quiescent current (Iccq): 15mA in low-power mode
- Single positive-supply operation with low power and shutdown modes
  - 3.4V typical Vcc operation
  - Low Vref (2.85V) compatible with advanced handset chipsets
- Compact Lead-free compliant LCC package – (4.0 X 4.0 x 1.0 mm nominal)
- Industry standard pinout
- Internally matched to 50 Ohms and DC blocked RF input/output

General Description

The RMPA0966 Power Amplifier Module (PAM) is Fairchild's latest innovation in 50Ω matched, surface mount modules targeting Cellular CDMA/WCDMA/HSDPA, AMPS and Wireless Local Loop (WLL) applications. Answering the call for ultra-low DC power consumption and extended battery life in portable electronics, the RMPA0966 uses novel proprietary circuitry to dramatically reduce amplifier current at low to medium RF output power levels (<+16 dBm), where the handset most often operates. A simple two-state Vmode control is all that is needed to reduce operating current by more than 60% at 16 dBm output power, and quiescent current (Iccq) by as much as 70% compared to traditional power-saving methods. No additional circuitry, such as DC-to-DC converters, are required to achieve this remarkable improvement in amplifier efficiency. Further, the 4x4x1.0mm LCC package is pin-compatible and a drop-in replacement for last generation 4x4mm PAMs widely used today, minimizing the design time to apply this performance-enhancing technology. The multi-stage GaAs Microwave Monolithic Integrated Circuit (MMIC) is manufactured using Fairchild RF's InGaP Heterojunction Bipolar Transistor (HBT) process.

Functional Block Diagram



Absolute Maximum Ratings(1)

Symbol	Parameter	Value	Units
Vcc1, Vcc2	Supply Voltages	5.0	V
Vref	Reference Voltage	2.6 to 3.5	V
Vmode	Power Control Voltage	3.5	V
Pin	RF Input Power	+10	dBm
Tstg	Storage Temperature	-55 to +150	°C

Note:
1. No permanent damage with one parameter set at extreme limit. Other parameters set to typical values.

Electrical Characteristics(2)

Symbol	Parameter	Comments	Min.	Typ.	Max.	Units
f	Operating Frequency		824		849	MHz
CDMA/WCDMA OPERATION						
Gp	Power Gain	Po=+28 dBm; Vmode=0V Po=+16 dBm; Vmode≥2.0V		30 20		dB dB
Po	Linear Output Power	Vmode=0V Vmode≥2.0V	28 16			dBm dBm
PAEd	PAEd (digital) @ +28dBm	Vmode=0V		42		%
	PAEd (digital) @ +16dBm	Vmode≥2.0V		21		%
Itot	High Power Total Current	Po=+28 dBm, Vmode=0V		440		mA
	Low Power Total Current	Po=+16 dBm, Vmode≥2.0V		56		mA
CDMA	Adjacent Channel Power Ratio	IS-95 A/B Modulation				
ACPR1	±885KHz Offset	Po=+28 dBm; Vmode=0V Po=+16 dBm; Vmode≥2.0V		-50 -55		dBc dBc
ACPR2	±1.98MHz Offset	Po=+28 dBm; Vmode=0V Po=+16 dBm; Vmode≥2.0V		-60 -65		dBc dBc
WCDMA	Adjacent Channel Leakage Ratio	WCDMA Modulation 3GPP 3.2 03-00 DPCCH +1 DCDCH				
ACLR1	±5MHz Offset	Po=+28 dBm; Vmode=0V Po=+16 dBm; Vmode≥2.0V		-40 -45		dBc dBc
ACLR2	±10MHz Offset	Po=+28 dBm; Vmode=0V Po=+16 dBm; Vmode≥2.0V		-53 -60		dBc dBc
AMPS OPERATION						
Gp	Power Gain	Po=+31 dBm		29		dB
PAEa	Power-Added Efficiency (analog)	Po=+31 dBm		50		%
GENERAL CHARACTERISTICS						
VSWR	Input Impedance			2.0:1	2.5:1	
NF	Noise Figure			4		dB
Rx No	Receive Band Noise Power	Po≤+28 dBm; 869 to 894MHz		-134		dBm/Hz
2fo-5fo	Harmonic Suppression(4)	Po≤+28 dBm			-30	dBc
S	Spurious Outputs(3)(4)	Load VSWR≤5.0:1			-60	dBc
	Ruggedness w/ Load Mismatch(4)	No permanent damage.			10:1	
Tc	Case Operating Temperature		-30		85	°C
DC CHARACTERISTICS						
Iccq	Quiescent Current	Vmode≥2.0V		15		mA
Iref	Reference Current	Po≤+28 dBm		2		mA
Icc(off)	Shutdown Leakage Current	No applied RF signal		1	5	µA

Notes:
2. All parameters met at Tc = +25°C, Vcc = +3.4V, Vref = 2.85V and load VSWR ≤ 1.2:1, unless otherwise noted.
3. All phase angles.
4. Guaranteed by design.

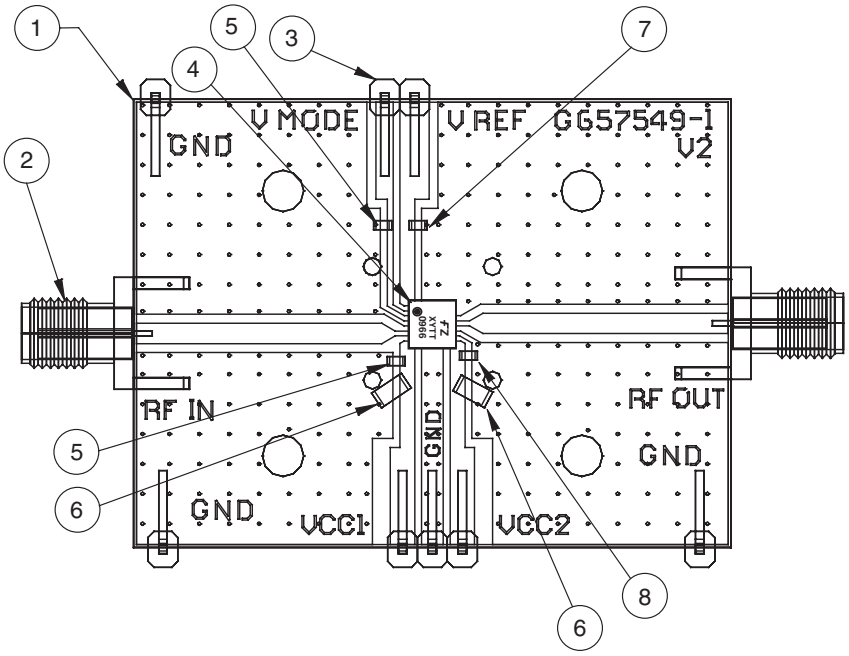
Recommended Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
f	Operating Frequency	824		849	MHz
Vcc1, Vcc2	Supply Voltage	3.0	3.4	4.2	V
Vref	Reference Voltage (Operating) (Shutdown)	 2.7 0	 2.85	 3.1 0.5	 V V
Vmode	Bias Control Voltage (Low-Power) (High-Power)	 1.8 0	 2.0	 3.0 0.5	 V V
Pout	Linear Output Power (High-Power) (Low-Power)		 +16	 +28	 dBm dBm
Tc	Case Operating Temperature	-30		+85	°C

DC Turn-On Sequence

1) Vcc1 = Vcc2 = 3.4V (typical)
2) Vref = 2.85V (typical)
3) High-Power: Vmode = 0V (Pout > 16 dBm)
   Low-Power: Vmode = 2V (Pout < 16 dBm)

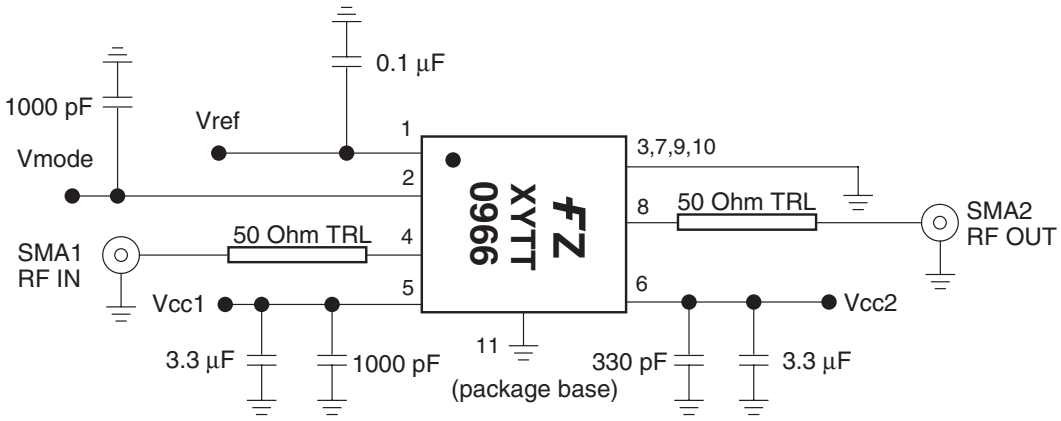
Evaluation Board Layout



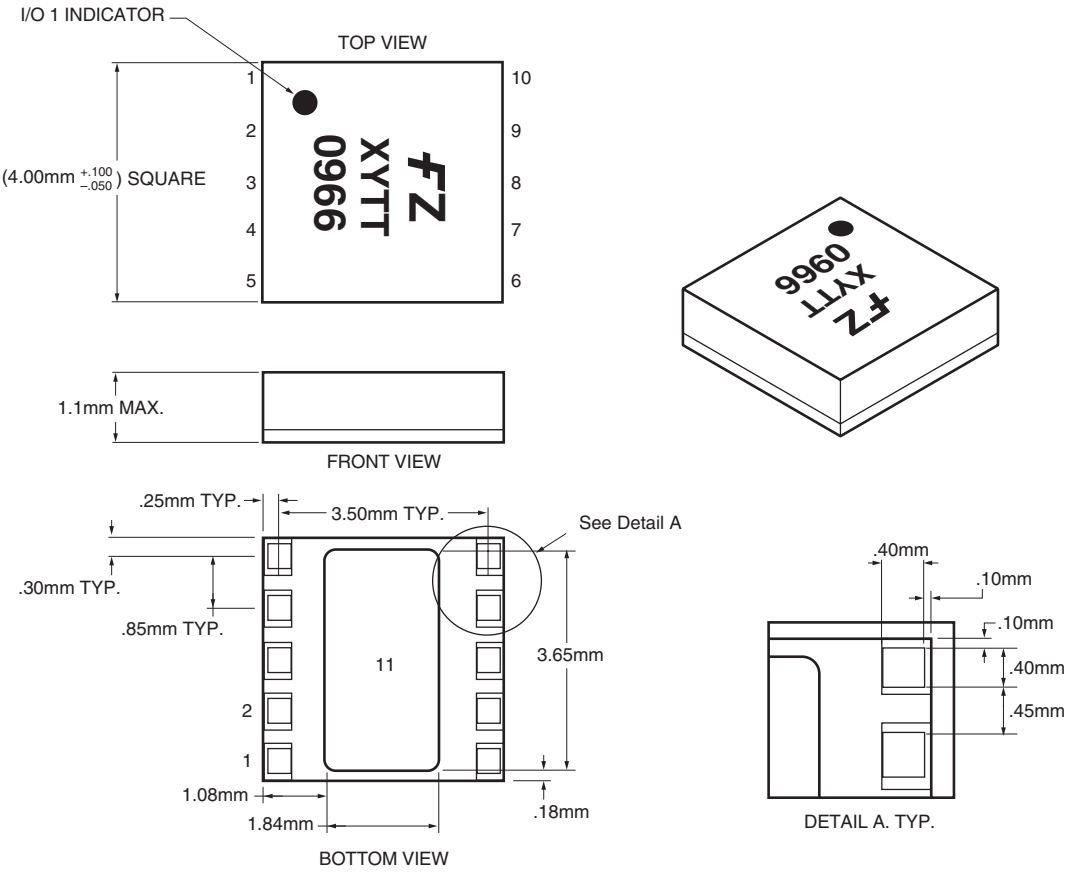
Materials List

Qty	Item No.	Part Number	Description	Vendor
1	1	G657549-1 V2	PC Board	Fairchild
2	2	#142-0701-841	SMA Connector	Johnson
8	3	#2340-5211TN	Terminals	3M
Ref	4		Assembly, RMPA0966	Fairchild
2	5	GRM39X7R102K50V	1000pF Capacitor (0603)	Murata
2	5 (Alt)	ECJ-1VB1H102K	1000pF Capacitor (0603)	Panasonic
2	6	C3216X5R1A335M	3.3µF Capacitor (1206)	TDK
1	7	GRM39Y5V104Z16V	0.1µF Capacitor (0603)	Murata
1	7 (Alt)	ECJ-1VB1C104K	0.1µF Capacitor (0603)	Panasonic
1	8	GRM39X7R331K50V	330pF Capacitor (0603)	Murata
A/R	9	SN63	Solder Paste	Indium Corp.
A/R	10	SN96	Solder Paste	Indium Corp.

Evaluation Board Schematic



Package Outline



Signal Descriptions

Pin #	Signal Name	Description
1	Vref	Reference Voltage
2	Vmode	High Power/Low Power Mode Control
3	GND	Ground
4	RF In	RF Input Signal
5	Vcc1	Supply Voltage to Input Stage
6	Vcc2	Supply Voltage to Output Stage
7	GND	Ground
8	RF Out	RF Output Signal
9	GND	Ground
10	GND	Ground
11	GND	Paddle Ground

Applications Information

CAUTION: THIS IS AN ESD SENSITIVE DEVICE.

Precautions to Avoid Permanent Device Damage:

- Cleanliness: Observe proper handling procedures to ensure clean devices and PCBs. Devices should remain in their original packaging until component placement to ensure no contamination or damage to RF, DC and ground contact areas.
- Device Cleaning: Standard board cleaning techniques should not present device problems provided that the boards are properly dried to remove solvents or water residues.
- Static Sensitivity: Follow ESD precautions to protect against ESD damage:
  - A properly grounded static-dissipative surface on which to place devices.
  - Static-dissipative floor or mat.
  - A properly grounded conductive wrist strap for each person to wear while handling devices.
- General Handling: Handle the package on the top with a vacuum collet or along the edges with a sharp pair of bent tweezers. Avoiding damaging the RF, DC, and ground contacts on the package bottom. Do not apply excessive pressure to the top of the lid.
- Device Storage: Devices are supplied in heat-sealed, moisture-barrier bags. In this condition, devices are protected and require no special storage conditions. Once the sealed bag has been opened, devices should be stored in a dry nitrogen environment.

Device Usage:
Fairchild recommends the following procedures prior to assembly.

- Assemble the devices within 7 days of removal from the dry pack.
- During the 7-day period, the devices must be stored in an environment of less than 60% relative humidity and a maximum temperature of 30°C
- If the 7-day period or the environmental conditions have been exceeded, then the dry-bake procedure per JEDEC J-STD-020 must be performed.

Solder Materials & Temperature Profile:
Reflow soldering is the preferred method of SMT attachment. Hand soldering is not recommended.

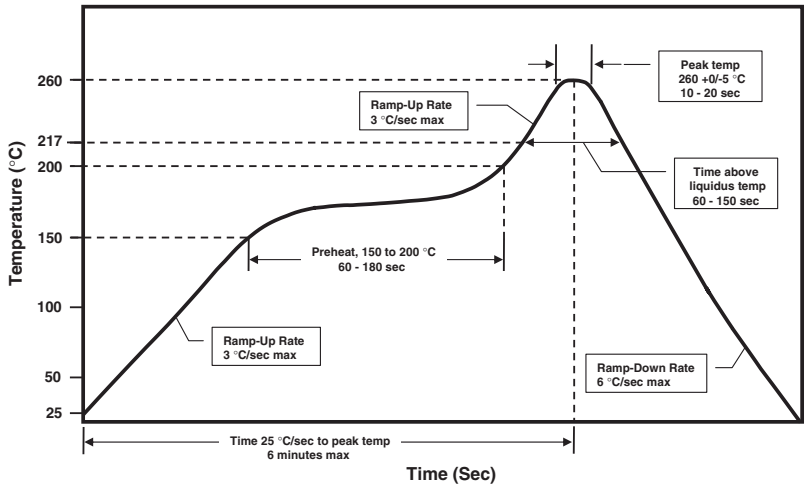
Reflow Profile

- Ramp-up: During this stage the solvents are evaporated from the solder paste. Care should be taken to prevent rapid oxidation (or paste slump) and solder bursts caused by violent solvent out-gassing. A maximum heating rate is 3°C/sec.
- Pre-heat/soak: The soak temperature stage serves two purposes; the flux is activated and the board and devices achieve a uniform temperature. The recommended soak condition is: 60-180 seconds at 150-200°C.
- Reflow Zone: If the temperature is too high, then devices may be damaged by mechanical stress due to thermal mismatch or there may be problems due to excessive solder oxidation. Excessive time at temperature can enhance the formation of inter-metallic compounds at the lead/board interface and may lead to early mechanical failure of the joint. Reflow must occur prior to the flux being completely driven off. The duration of peak reflow temperature should not exceed 20 seconds. Soldering temperatures should be in the range 255–260°C, with a maximum limit of 260°C.
- Cooling Zone: Steep thermal gradients may give rise to excessive thermal shock. However, rapid cooling promotes a finer grain structure and a more crack-resistant solder joint. The illustration below indicates the recommended soldering profile.

Solder Joint Characteristics:
Proper operation of this device depends on a reliable void-free attachment of the heat sink to the PWB. The solder joint should be 95% void-free and be a consistent thickness.

Rework Considerations:
Rework of a device attached to a board is limited to reflow of the solder with a heat gun. The device should be subjected to no more than 15°C above the solder melting temperature for no more than 5 seconds. No more than 2 rework operations should be performed.

Recommended Solder Reflow Profile



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