

PLL Clock Multiplier

Features

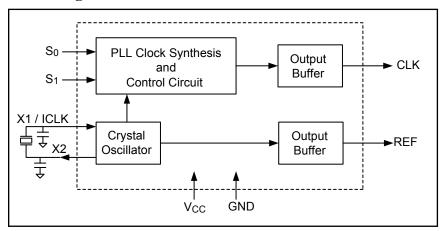
- Zero ppm multiplication error
- Input crystal frequency of 5 30MHz
- Input clock frequency of 4 50MHz
- Output clock frequencies up to 200MHz
- Low period jitter 80ps (100~200MHz)
- Duty cycle 45/55% of output clock
- 9 Selectable frequencies controlled by S₀ and S₁ pins
- Operating voltages of 3.0 to 5.5V
- · Packaging:
 - 8-pin SOIC (W)
 - Pb-Free and Green 8-pin SOIC (WE)

Description

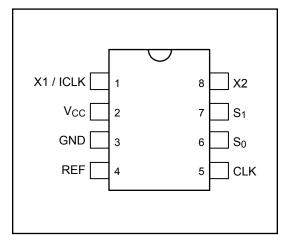
Pericom Semiconductor's PI6C4512 is a precision general-purpose clock synthesizer that reaches maximum 200MHz. This device uses an external low-cost crystal to generate very accurate rate and stable system clocks. This is the most cost effective way to reduce high-price, high frequency crystals. Using PLL techniques, the device uses a standard fundamental mode, inexpensive crystal to produce output clocks up to 200 MHz.

The internal Logic divider is to generate nine different popular multiplication factors, allowing one chip to output many common frequencies.

Block Diagram



Pin Configuration



Clock Output Table

S_1	S_0	CLK
0	0	x 4
0	M	x (16/3)
0	40,	x 5
M	0	x 2.5
M	M	x 2
M	1	x (10/3)
1	0	x 6
1	M	x 3
1	1	x 8

Notes:

1. M = leave unconnected (self-biases to V_{CC}/2).



Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested)

Storage temperature	65 to 150°C
Ambient Operating Temperature	
Supply Voltage to Ground Potential (V _{CC})	0.3 to +7.0V
Inputs (Referenced to GND)	0.5 to V _{CC} +0.5V
Clock Output (Referenced to GND)	0.5 to V _{CC} +0.5V
Soldering Temperature (Max of 10 seconds)	260°C (Max.10s)

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Pin Description

Name	Pin	Description	
X1/ICLK	1	Crystal connection or clock input.	
V_{CC}	2	Connect to +3.3V or +5V.	
GND	3	Ground	
REF	4	Buffered crystal oscillator output clock	
CLK	5	Clock output	
S_0	6	Multiplier select pin 0. Connect to GND or V _{CC} or float (no connection)	
S_1	7	Multiplier select pin 1. Connect to GND or V _{CC} or float (no connection)	
X2	8	Crystal connection. Leave unconnected for clock input.	

External Components

The PI6C4512 requires a minimum number of external components for proper operation. Decoupling capacitors of $0.01\mu F$ should be connected between each V_{DD} and GND as close to the chip as possible. A series termination resistor of 33Ω may be used for each clock output. The crystal should be a fundamental mode, parallel resonant. Crystal capacitors should be connected from X_1 to ground and X_2 to ground to optimize the inital accuracy. The value of these capacitors igiven by the following equation, where C_L is the crystal load capacitance: Crystal caps (pF) = (C_L -15) x2. So for a crystal with 18pF load capacitance, two 6pF caps should be used.

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Recommended Operation Conditions

Symbol	Description	Test Condition	Min.	Тур.	Max.	Units
V_{CC}	Supply Voltage		3		5.5	V
TA	Operating Temperature		0		70	°C

DC Electrical Characteristics ($V_{CC} = 3.3V \pm 0.3V$, $T_A = 0 \sim 70^{\circ}C$, unless otherwise noted)

Symbol	Description	Test Condition	Pin	Min.	Тур.	Max.	Units
V _{CC}	Supply voltage		V _{CC}	3		5.5	V
I_{CC}	Supply current	no load, 20MHz Crystal	V_{CC}	`	12	20	mA
V_{IH}	Input logic high		ICLK	$(V_{CC}/2) + 1$	V _{CC} /2		
V_{IL}	Input logic low		ICLK		V _{CC} /2	(V _{CC} /2)-1	
V_{IH}	Input logic high		S ₀ , S ₁	V _{CC} -0.5			
V_{IM}	Input mid-level		S_0, S_1		V _{CC} /2		V
$V_{\rm IL}$	Input logic low		S ₀ , S ₁			0.5	
V_{OH}	High-level output voltage	$I_{OH} = -12mA$	CLK, REF	2.4			
V_{OL}	Low-level output voltage	$I_{OL} = 12mA$	CLK, REF			0.4	
Is	Short circuit current		CLK		±70		mA

AC Electrical Characteristics ($V_{CC} = 3.3V \pm 0.3V$, $T_A = 0 \sim 70$ °C, unless noted)

Symbol	Parameter	Test Condition	Pin	Min.	Typ.	Max.	Unit
	Innert Francisco	Crystal	ICLK	5		30	
f_{IN}	Input Frequency	Clock	ICLK	4		50	MII-
	V _{CC} : 4.5 to 5.5V	CLK	20		200	MHz	
f_{OUT}	Output frequency ⁽²⁾	V _{CC} : 3.0 to 3.6V	CLK	20		180	
t _r	Output clock rise time	0.8 to 2.0V, with 15pF load	CLK		1		
t_{f}	Output clock fall time	2.0 to 0.8V, with 15pF load	CLK		1		ns
Duty	Output clock duty ycle	At V _{CC} /2	CLK	45	50	55	%
	PLL bandwidth ⁽¹⁾			10			kHz
	Period Jitter	100MHz~200MHz	CLK		80	100	ps

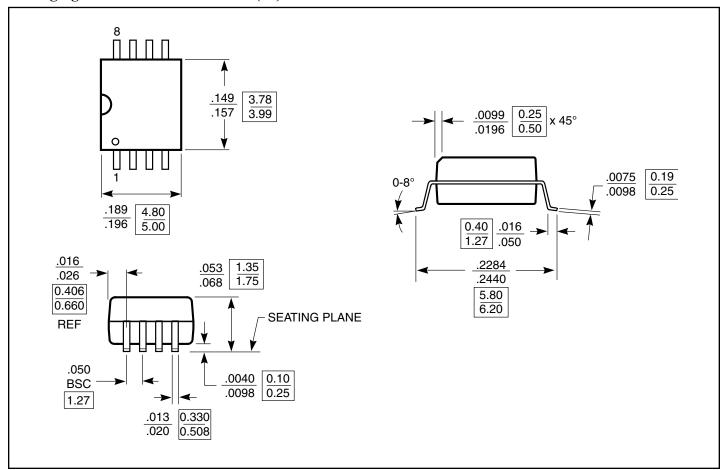
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Notes:

- 1. Only reference for design
- 2. The phase relationship between input and output clocks can change at power up.



Packaging Mechanical: 8-Pin SOIC (W)



Ordering Information

Ordering Code	Package Code	Package Description
PI6C4512W	W	8-pin SOIC
PI6C4512WE	WE	Pb-Free and Green 8-pin SOIC

Notes

1. Thermal characteristics can be found on the company web site at www.pericom.com/packaging/

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