

November 2004

Ultra Low Offset Voltage Operational Amplifier

Features

- This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.
- Low Offset Voltage **60 μ V (Max)**
10 μ V (Typ)
- Low Offset Voltage Drift **0.6 μ V/ $^{\circ}$ C (Max)**
0.1 μ V/ $^{\circ}$ C (Typ)
- High Voltage Gain **126dB (Min)**
150dB (Typ)
- High CMRR **110dB (Min)**
140dB (Typ)
- High PSRR **110dB (Min)**
135dB (Typ)
- Low Noise **11nV/ $\sqrt{\text{Hz}}$ (Max)**
9nV/ $\sqrt{\text{Hz}}$ (Typ)
- Low Power Consumption **51mW (Max)**
- Wide Gain Bandwidth Product **2MHz (Min)**
- Unity Gain Stable

Applications

- High Gain Instrumentation Amplifiers
- Precision Control Systems
- Precision Integrators
- High Resolution Data Converters
- Precision Threshold Detectors
- Low Level Transducer Amplifiers

Description

The HA-5177/883 is a monolithic, all bipolar, precision operational amplifier, utilizing Intersil Dielectric Isolation and advance processing techniques. This design features a combination of precision input characteristics, wide gain bandwidth (2MHz) and high speed (0.5V/ μ s min) and is an improved version of the HA-5135/883.

The HA-5177/883 uses advanced matching techniques and laser trimming to produce low offset voltage (10 μ V typ, 60 μ V max) and low offset voltage drift (0.1 μ V/ $^{\circ}$ C typ, 0.6 μ V/ $^{\circ}$ C max). This design also features low voltage noise (9nV/ $\sqrt{\text{Hz}}$ typ), Low current noise (0.32pA/ $\sqrt{\text{Hz}}$ typ), nanoamp input currents, and 126dB minimum gain.

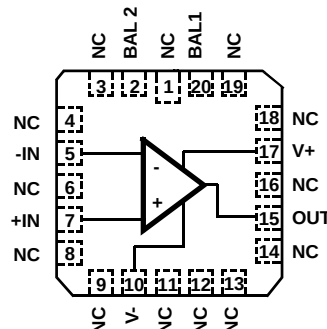
These outstanding features along with high CMRR (140dB typ, 110dB min) and high PSRR (135dB typ, 110dB min) make this unity gain stable amplifier ideal for high resolution data acquisition systems, precision integrators, and low level transducer amplifiers.

Part Number Information

PART NUMBER	TEMPERATURE RANGE	PACKAGE
HA4-5177/883	-55 $^{\circ}$ C to +125 $^{\circ}$ C	20 Lead Ceramic LCC

Pinout

HA-5177/883
(CLCC)
TOP VIEW



Absolute Maximum Ratings

Voltage Between V+ and V- Terminals 44V
 Differential Input Voltage (Note 1). 7V
 Voltage at Either Input Terminal V+ to V-
 Input Current. 25mA
 Output Current Full Short Circuit Protection
 Junction Temperature (T_J) +175°C
 Storage Temperature Range -65°C to +150°C
 ESD Rating. <2000V
 Lead Temperature (Soldering 10s). +300°C

Thermal Information

Thermal Resistance θ_{JA} θ_{JC}
 Ceramic LCC Package 80°C/W 28°C/W
 Package Power Dissipation Limit at +75°C for T_J ≤ +175°C
 Ceramic LCC Package 1.54W
 Package Power Dissipation Derating Factor Above +75°C
 Ceramic LCC Package 15.4mW/°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Operating Conditions

Operating Temperature Range -55°C to +125°C $V_{INCM} \leq 1/2 (V+ - V-)$
 Operating Supply Voltage ±15V $R_L \geq 600\Omega$

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: V_{SUPPLY} = ±15V, R_{SOURCE} = 50Ω, R_{LOAD} = 100kΩ, V_{OUT} = 0V, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Input Offset Voltage	V _{IO}	V _{CM} = 0V	1	+25°C	-60	60	μV
			2, 3	+125°C, -55°C	-100	100	μV
Input Bias Current	I _B	V _{CM} = 0V, R _S = 10kΩ, 50Ω $\left(\frac{ I_{B+} + I_{B-} }{2} \right)$	1	+25°C	-6	6	nA
			2, 3	+125°C, -55°C	-8	8	nA
Input Offset Current	I _{IO}	V _{CM} = 0V, +R _S = 10kΩ, -R _S = 10kΩ	1	+25°C	-6	6	nA
			2, 3	+125°C, -55°C	-8	8	nA
Common Mode Range	+CMR	V+ = +3V, V- = -27V	1	+25°C	12	-	V
			2, 3	+125°C, -55°C	12	-	V
	-CMR	V+ = +27V, V- = -3V	1	+25°C	-	-12	V
			2, 3	+125°C, -55°C	-	-12	V
Large Signal Voltage Gain	+A _{VOL}	V _{OUT} = 0V and +10V, R _L = 2kΩ	4	+25°C	126	-	dB
			5, 6	+125°C, -55°C	120	-	dB
	-A _{VOL}	V _{OUT} = 0V and -10V, R _L = 2kΩ	4	+25°C	126	-	dB
			5, 6	+125°C, -55°C	120	-	dB
Common Mode Rejection Ratio	+CMRR	ΔV _{CM} = 10V, V+ = +5V, V- = -25V, V _{OUT} = -10	1	+25°C	116	-	dB
			2, 3	+125°C, -55°C	110	-	dB
	-CMRR	ΔV _{CM} = 10V, V+ = +25V, V- = -5V, V _{OUT} = +10	1	+25°C	116	-	dB
			2, 3	+125°C, -55°C	110	-	dB
Output Voltage Swing	+V _{OUT1}	R _L = 2kΩ	4	+25°C	12	-	V
			5, 6	+125°C, -55°C	12	-	V
	-V _{OUT1}	R _L = 2kΩ	4	+25°C	-	-12	V
			5, 6	+125°C, -55°C	-	-12	V
	+V _{OUT2}	R _L = 600Ω	4	+25°C	10	-	V
			4	+25°C	-	-10	V

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)Device Tested at: $V_{SUPPLY} = \pm 15V$, $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 100k\Omega$, $V_{OUT} = 0V$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Output Current	+I _{OUT}	V _{OUT} = -10V	4	+25°C	15	-	mA
			5, 6	+125°C, -55°C	15	-	mA
	-I _{OUT}	V _{OUT} = +10V	4	+25°C	-	-15	mA
			5, 6	+125°C, -55°C	-	-15	mA
Quiescent Power Supply Current	+I _{CC}	V _{OUT} = 0V, I _{OUT} = 0mA	1	+25°C	-	1.7	mA
			2, 3	+125°C, -55°C	-	1.7	mA
	-I _{CC}	V _{OUT} = 0V, I _{OUT} = 0mA	1	+25°C	-1.7	-	mA
			2, 3	+125°C, -55°C	-1.7	-	mA
Power Supply Rejection Ratio	+PSRR	$\Delta V_{SUP} = 15V$, V+ = +5V, V- = -15V, V+ = +20V, V- = -15V	1	+25°C	110	-	dB
			2, 3	+125°C, -55°C	110	-	dB
	-PSRR	$\Delta V_{SUP} = 15V$, V+ = +15V, V- = -5V, V+ = +15V, V- = -20V	1	+25°C	110	-	dB
			2, 3	+125°C, -55°C	110	-	dB
Offset Voltage Adjustment	+V _{IOAdj}	Note 2	1	+25°C	0.3	-	mV
			2, 3	+125°C, -55°C	0.3	-	mV
	-V _{IOAdj}	Note 2	1	+25°C	-	-0.3	mV
			2, 3	+125°C, -55°C	-	-0.3	mV

NOTES:

1. The input stage has series 500Ω resistors along with back to back diodes. This provides large differential input voltage protection for a slight increase in noise voltage.
2. This test is for functionality only to assure adjustment through 0V.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICSDevice Tested at: $V_{SUPPLY} = \pm 15V$, $R_{SOURCE} = 50\Omega$, $R_{LOAD} = 2k\Omega$, $C_{LOAD} = 50pF$, $A_{VCL} = +1V/V$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Slew Rate	+SR	V _{OUT} = -3V to +3V, V _{IN} S.R. ≤ 25V/μs	7	+25°C	0.5	-	V/μs
	-SR	V _{OUT} = +3V to -3V, V _{IN} S.R. ≤ 25V/μs	7	+25°C	0.5	-	V/μs
Rise and Fall Time	t _R	V _{OUT} = 0 to +200mV 10% ≤ T _R ≤ 90%	7	+25°C	-	420	ns
	t _F	V _{OUT} = 0 to -200mV 10% ≤ T _F ≤ 90%	7	+25°C	-	420	ns
Overshoot	+OS	V _{OUT} = 0 to +200mV	7	+25°C	-	40	%
	-OS	V _{OUT} = 0 to -200mV	7	+25°C	-	40	%

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Characterized at: $V_{SUPPLY} = \pm 15V$, $R_{LOAD} = 2k\Omega$, $C_{LOAD} = 50pF$, $A_V = +1V/V$, Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	NOTES	TEMPERATURE	LIMITS		UNITS
					MIN	MAX	
Average Offset Voltage Drift	$V_{IO TC}$	$V_{CM} = 0V$	1	-55°C to +125°C	-	0.6	$\mu V/^{\circ}C$
Average Offset Current Drift	$I_{IO TC}$	Versus Temperature	1	-55°C to +125°C	-	40	$pA/^{\circ}C$
Average Bias Current Drift	$I_{R TC}$	Versus Temperature	1	-55°C to +125°C	-	40	$pA/^{\circ}C$
Differential Input Resistance	R_{IN}	$V_{CM} = 0V$	1	+25°C	20	-	$M\Omega$
Low Frequency Peak-to-Peak Noise Voltage	E_{NP-P}	0.1Hz to 10Hz	1	+25°C	-	0.6	μV_{P-P}
Low Frequency Peak-to-Peak Noise Current	I_{NP-P}	0.1Hz to 10Hz	1	+25°C	-	45	pA_{P-P}
Input Noise Voltage Density	E_N	$R_S = 20\Omega$, $f_O = 10Hz$	1	+25°C	-	18	$nV/\sqrt{Hz}$
		$R_S = 20\Omega$, $f_O = 100Hz$	1	+25°C	-	13	$nV/\sqrt{Hz}$
		$R_S = 20\Omega$, $f_O = 1kHz$	1	+25°C	-	11	$nV/\sqrt{Hz}$
Input Noise Current Density	I_N	$R_S = 2M\Omega$, $f_O = 10Hz$	1	+25°C	-	4	$pA/\sqrt{Hz}$
		$R_S = 2M\Omega$, $f_O = 100Hz$	1	+25°C	-	2.3	$pA/\sqrt{Hz}$
		$R_S = 2M\Omega$, $f_O = 1kHz$	1	+25°C	-	1	$pA/\sqrt{Hz}$
Gain Bandwidth Product	GBWP	$V_O = 100mV$, $1Hz \leq f_O \leq 100kHz$	1	+25°C	2	-	MHz
Full Power Bandwidth	FPBW	$V_{PEAK} = 10V$	1, 2	+25°C	8	-	kHz
Minimum Closed Loop Stable Gain	CLSG	$R_L = 2k\Omega$, $C_L = 50pF$	1	-55°C to +125°C	+1	-	V/V
Settling Time	t_S	To 0.1% for a 10V Step	1	+25°C	-	15	μs
Output Resistance	R_{OUT}	Open Loop	1	+25°C	-	70	Ω
Power Consumption	PC	$V_{OUT} = 0V$, $I_{OUT} = 0mA$	1, 3	-55°C to +125°C	-	51	mW

NOTES:

- Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.
- Full Power Bandwidth guarantee based on Slew Rate measurement using $FPBW = \text{Slew Rate}/(2\pi V_{PEAK})$.
- Power Consumption based upon Quiescent Supply Current test maximum. (No load on outputs.)

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3, 4, 5, 6, 7
Group A Test Requirements	1, 2, 3, 4, 5, 6, 7
Groups C and D Endpoints	1

NOTE:

- PDA applies to Subgroup 1 only.

Die Characteristics

DIE DIMENSIONS:

72 x 103 x 19 mils $\pm$ 1 mils
 1840 x 2620 x 483 μ m $\pm$ 25.4 μ m

METALLIZATION:

Type: Al, 1% Cu
 Thickness: 16k $\text{\AA}$ $\pm$ 2k $\text{\AA}$

GLASSIVATION:

Type: Nitride (Si₃N₄) over Silox (SiO₂, 5% Phos.)
 Silox Thickness: 12k $\text{\AA}$ $\pm$ 2k $\text{\AA}$
 Nitride Thickness: 3.5k $\text{\AA}$ $\pm$ 1.5k $\text{\AA}$

WORST CASE CURRENT DENSITY:

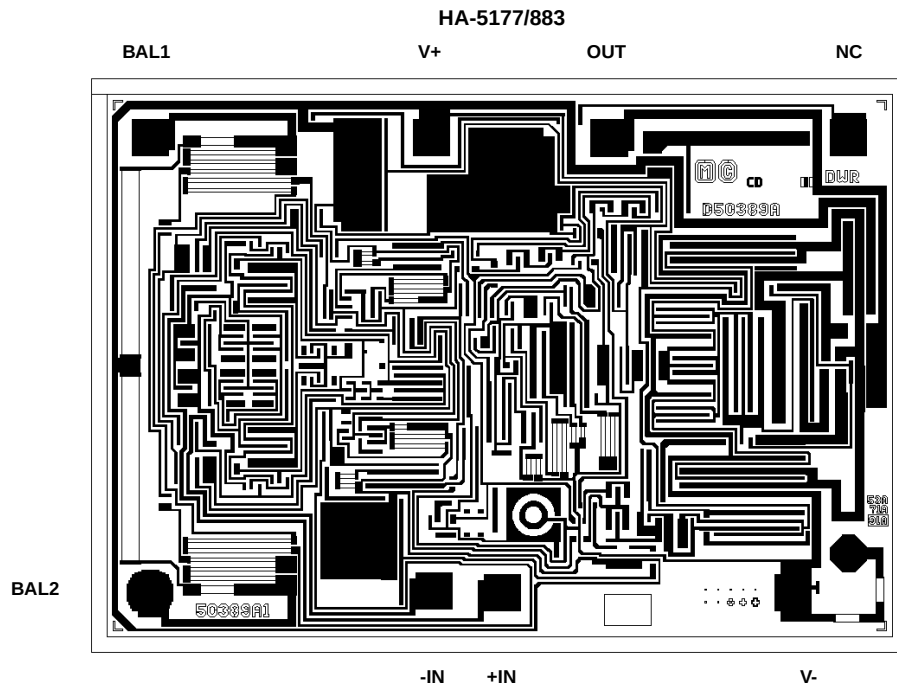
6.0 x 10⁴ A/cm²

SUBSTRATE POTENTIAL (Powered Up): V-

TRANSISTOR COUNT: 71

PROCESS: Bipolar Dielectric Isolation

Metallization Mask Layout



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