

**HIGH PERFORMANCE, LOW POWER  
256K X 4 BIT FAST PAGE MODE  
CMOS DYNAMIC RAM**

HIGH PERFORMANCE V53C104D	60	70	80
Max. $\overline{\text{RAS}}$ Access Time, ( $t_{\text{RAC}}$ )	60 ns	70 ns	80 ns
Max. Column Address Access Time, ( $t_{\text{CAA}}$ )	30 ns	35 ns	40 ns
Min. Fast Page Mode Cycle Time, ( $t_{\text{PC}}$ )	40 ns	45 ns	50 ns
Min. Read/Write Cycle Time, ( $t_{\text{RC}}$ )	120 ns	130 ns	150 ns

**Features**

- 256K x 4 Organization
- RAS access time: 60,70,80 ns
- Low power dissipation for V53C104D-80
  - Operating Current – 70 mA max.
  - TTL Standby Current – 2.0 mA max.
- Low CMOS Standby Current
  - V53C104D – 1.0 mA max.
- Read-Modify-Write, RAS-Only Refresh,  $\overline{\text{CAS}}$ -Before- $\overline{\text{RAS}}$  Refresh capability.
- Common I/O capability
- Refresh Interval
  - V53C104D – 512 cycles/8ms
- Fast Page Mode for a sustained data rate greater than 25 MHz
- Standard packages are 20 pin Plastic DIP and 26/20 pin SOJ

**Description**

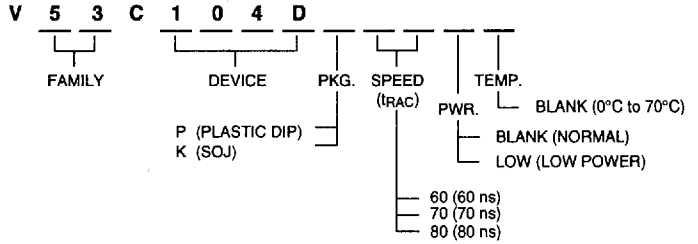
The V53C104D is a high speed 262,144 x 4 bit CMOS dynamic random access memory. The V53C104D offers a combination of features: Fast Page Mode for high data bandwidth, fast usable speed, CMOS standby current.

All inputs and outputs are TTL compatible. Input and output capacitances are significantly lowered to allow increased system performance. Fast Page Mode operation allows random access of up to 512 (x4) bits within a row with cycle times as short as 40 ns. Because of static circuitry, the  $\overline{\text{CAS}}$  clock is not in the critical timing path. The flow-through column address latches allow address pipelining while relaxing many critical system timing requirements for fast usable speed. These features make the V53C104D ideally suited for graphics, digital signal processing and high performance computing systems

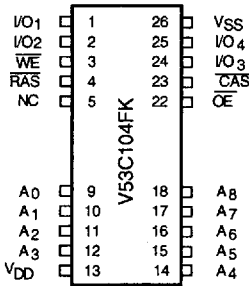
**Device Usage Chart**

Operating Temperature Range	Package Outline		Access Time (ns)			Power	Temperature Mark
	P	K	60	70	80	Std.	
0°C to 70 °C	•	•	•	•	•	•	Blank

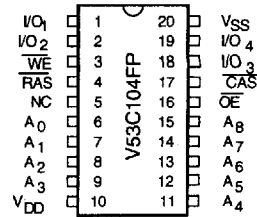
Description	Pkg.	Pin Count
Plastic DIP	P	20
SOJ	K	26/20



**26/20 Lead SOJ Package  
PIN CONFIGURATION  
Top View**



**20 Lead Plastic DIP  
PIN CONFIGURATION  
Top View**



**Pin Names**

A <sub>0</sub> -A <sub>8</sub>	Address Inputs
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{CAS}}$	Column Address Strobe
$\overline{\text{WE}}$	Write Enable
$\overline{\text{OE}}$	Output Enable
I/O <sub>1</sub> -I/O <sub>4</sub>	Data Input, Output
V <sub>DD</sub>	+5V Supply
V <sub>SS</sub>	0V Supply
NC	No Connect

**Absolute Maximum Ratings\***

Ambient Temperature  
 Under Bias ..... -10°C to +80°C  
 Storage Temperature (plastic) ..... -55°C to +125°C  
 Voltage Relative to V<sub>SS</sub> ..... -1.0 V to +7.0 V  
 Voltage on V<sub>DD</sub> relative to V<sub>SS</sub> ..... -1.0 V to +7.0 V  
 Data Output Current ..... 50 mA  
 Power Dissipation ..... 1.0 W

\*Note: Operation above Absolute Maximum Ratings can adversely affect device reliability.

V53C104D Rev. 1.0 January 1995

**Capacitance\***

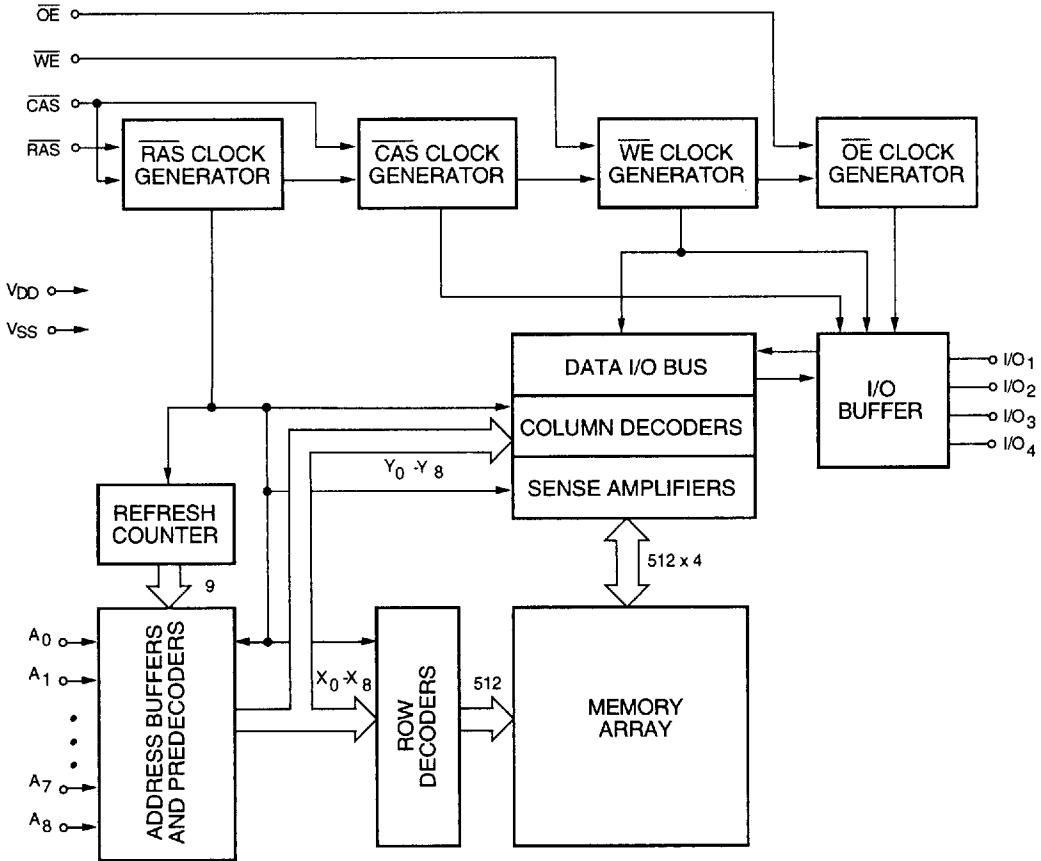
T<sub>A</sub> = 25°C, V<sub>DD</sub> = 5 V ± 10%, V<sub>SS</sub> = 0 V

Symbol	Parameter	Typ.	Max.	Unit
C <sub>IN1</sub>	Address Input	—	6	pF
C <sub>IN2</sub>	$\overline{\text{RAS}}$ , $\overline{\text{CAS}}$ , $\overline{\text{WE}}$ , $\overline{\text{OE}}$	—	7	pF
C <sub>OUT</sub>	Data Input/Output	—	6	pF

\* Note: Capacitance is sampled and not 100% tested

Block Diagram

256K x 4



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**DC and Operating Characteristics (1-2)**

$T_A = 0^\circ\text{C}$  to  $70^\circ\text{C}$ ,  $V_{DD} = 5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ , unless otherwise specified.

Symbol	Parameter	Access Time	V53C104D		Unit	Test Conditions	Notes
			Min.	Max.			
$I_{LI}$	Input Leakage Current (any input pin)		-10	10	$\mu\text{A}$	$V_{SS} \leq V_{IN} \leq V_{DD}$	
$I_{LO}$	Output Leakage Current (for High-Z State)		-10	10	$\mu\text{A}$	$V_{SS} \leq V_{OUT} \leq V_{DD}$ RAS, CAS at $V_{IH}$	
$I_{DD1}$	$V_{DD}$ Supply Current, Operating	60		90	mA	$t_{RC} = t_{RC}(\text{min.})$	1, 2
		70		80			
		80		75			
$I_{DD2}$	$V_{DD}$ Supply Current, TTL Standby			.5	mA	RAS, CAS at $V_{IH}$ other inputs $\geq V_{SS}$	
$I_{DD3}$	$V_{DD}$ Supply Current, RAS-Only Refresh	60		90	mA	$t_{RC} = t_{RC}(\text{min.})$	2
		70		80			
		80		75			
$I_{DD4}$	$V_{DD}$ Supply Current, Fast Page Mode Operation	60		80	mA	Minimum Cycle	1, 2
		70		70			
		80		65			
$I_{DD5}$	Standby, Output Enabled			3.0	mA	RAS= $V_{IH}$ , CAS= $V_{IL}$ other inputs $\geq V_{SS}$	1
$I_{DD6}$	$V_{DD}$ Supply Current CMOS Standby			50	$\mu\text{A}$	RAS $\geq V_{DD} - 0.2\text{ V}$ , CAS $\geq V_{DD} - 0.2\text{ V}$ other input $\geq V_{SS}$	
$V_{IL}$	Input Low Voltage		-1.0	0.8	V		3
$V_{IH}$	Input High Voltage		2.4	$V_{DD}+1$	V		3
$V_{OL}$	Output Low Voltage			0.4	V	$I_{OL} = 4.2\text{ mA}$	
$V_{OH}$	Output High Voltage		2.4		V	$I_{OH} = -5\text{ mA}$	

**AC Characteristics**

T<sub>A</sub> = 0°C to 70°C, V<sub>DD</sub> = 5 V ±10%, V<sub>SS</sub> = 0V unless otherwise noted

AC Test conditions, input pulse levels 0 to 3V

#	JEDEC Symbol	Symbol	Parameter	60		70		80		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
1	t <sub>RL1RH1</sub>	t <sub>RAS</sub>	$\overline{\text{RAS}}$ Pulse Width	60	16K	70	16K	80	16K	ns	
2	t <sub>RL2RL2</sub>	t <sub>RC</sub>	Read or Write Cycle Time	110		130		150		ns	
3	t <sub>RH2RL2</sub>	t <sub>RP</sub>	$\overline{\text{RAS}}$ Precharge Time	40		50		60		ns	
4	t <sub>RL1CH1</sub>	t <sub>CSH</sub>	$\overline{\text{CAS}}$ Hold Time	60		70		80		ns	
5	t <sub>CL1CH1</sub>	t <sub>CAS</sub>	$\overline{\text{CAS}}$ Pulse Width	15	100K	20	100K	20	100K	ns	
6	t <sub>RL1CL1</sub>	t <sub>RCD</sub>	$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay	20	40	20	50	20	60	ns	4
7	t <sub>WH2CL2</sub>	t <sub>RCS</sub>	Read Command Setup Time	0		0		0		ns	
8	t <sub>AVRL2</sub>	t <sub>ASR</sub>	Row Address Setup Time	0		0		0		ns	
9	t <sub>RL1AX</sub>	t <sub>RAH</sub>	Row Address Hold Time	10		10		12		ns	
10	t <sub>AVCL2</sub>	t <sub>ASC</sub>	Column Address Setup Time	0		0		0		ns	
11	t <sub>CL1AX</sub>	t <sub>CAH</sub>	Column Address Hold Time	12		15		15		ns	
12	t <sub>CL1RH1(R)</sub>	t <sub>RSH (R)</sub>	$\overline{\text{RAS}}$ Hold Time (Read Cycle)	20		20		20		ns	
13	t <sub>CH2RL2</sub>	t <sub>CRP</sub>	$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	10		10		10		ns	
14	t <sub>CH2WX</sub>	t <sub>RCH</sub>	Read Command Hold Time Referenced to $\overline{\text{CAS}}$	0		0		0		ns	5
15	t <sub>RH2WX</sub>	t <sub>RRH</sub>	Read Command Hold Time Referenced to $\overline{\text{RAS}}$	0		0		0		ns	5
16	t <sub>OEL1RH2</sub>	t <sub>ROH</sub>	$\overline{\text{RAS}}$ Hold Time Referenced to $\overline{\text{OE}}$	15		15		20		ns	
17	t <sub>GL1QV</sub>	t <sub>OAC</sub>	Access Time from $\overline{\text{OE}}$		15		15		20	ns	
18	t <sub>CL1QV</sub>	t <sub>CAC</sub>	Access Time from $\overline{\text{CAS}}$		20		20		20	ns	6,7
19	t <sub>RL1QV</sub>	t <sub>RAC</sub>	Access Time from $\overline{\text{RAS}}$		60		70		80	ns	6,8,9
20	t <sub>AVQV</sub>	t <sub>CAA</sub>	Access Time from Column Address		30		35		40	ns	6,7, 10

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**AC Characteristics (Cont'd.)**

#	JEDEC Symbol	Symbol	Parameter	60		70		80		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
21	t <sub>CL10X</sub>	t <sub>LZ</sub>	$\overline{OE}$ or $\overline{CAS}$ to Low-Z Output	0		0		0		ns	16
22	t <sub>CH20Z</sub>	t <sub>HZ</sub>	$\overline{OE}$ or $\overline{CAS}$ to High-Z Output	0	15	0	15	0	20	ns	16
23	t <sub>RL1AX</sub>	t <sub>AR</sub>	Column Address Hold Time from $\overline{RAS}$	50		55		60		ns	
24	t <sub>RL1AV</sub>	t <sub>RAD</sub>	$\overline{RAS}$ to Column Address Delay Time	15	30	15	35	17	40	ns	11
25	t <sub>CL1RH1(W)</sub>	t <sub>RSH(W)</sub>	$\overline{RAS}$ or $\overline{CAS}$ Hold Time in Write Cycle	20		20		20		ns	
26	t <sub>WL1CH1</sub>	t <sub>CWL</sub>	Write Command to $\overline{CAS}$ Lead Time	15		20		20		ns	
27	t <sub>WL1CL2</sub>	t <sub>WCS</sub>	Write Command Setup Time	0		0		0		ns	12,13
28	t <sub>CL1WH1</sub>	t <sub>WCH</sub>	Write Command Hold Time	12		15		15		ns	
29	t <sub>WL1WH1</sub>	t <sub>WP</sub>	Write Pulse Width	10		15		15		ns	
30	t <sub>RL1WH1</sub>	t <sub>WCR</sub>	Write Command Hold Time from $\overline{RAS}$	50		55		60		ns	
31	t <sub>WL1RH1</sub>	t <sub>RWL</sub>	Write Command to $\overline{RAS}$ Lead Time	15		20		20		ns	
32	t <sub>DVWL2</sub>	t <sub>DS</sub>	Data in Setup Time	0		0		0		ns	14
33	t <sub>WL1DX</sub>	t <sub>DH</sub>	Data in Hold Time	12		15		15		ns	14
34	t <sub>WL1GL2</sub>	t <sub>WOH</sub>	Write to $\overline{OE}$ Hold Time	15		20		20		ns	14
35	t <sub>GH2DX</sub>	t <sub>OED</sub>	$\overline{OE}$ to Data Delay Time	15		15		20		ns	14
36	t <sub>RL2RL2 (RMW)</sub>	t <sub>RWC</sub>	Read-Modify-Write Cycle Time	160		185		205		ns	
37	t <sub>RL1RH1</sub>	t <sub>RASP</sub>	$\overline{RAS}$ Pulse Width (Fast Page Mode)	60	100K	70	100K	80	100K	ns	
38	t <sub>CL1WL2</sub>	t <sub>CWD</sub>	$\overline{CAS}$ to $\overline{WE}$ Delay	45		45		50		ns	12

**AC Characteristics** (Cont'd.)

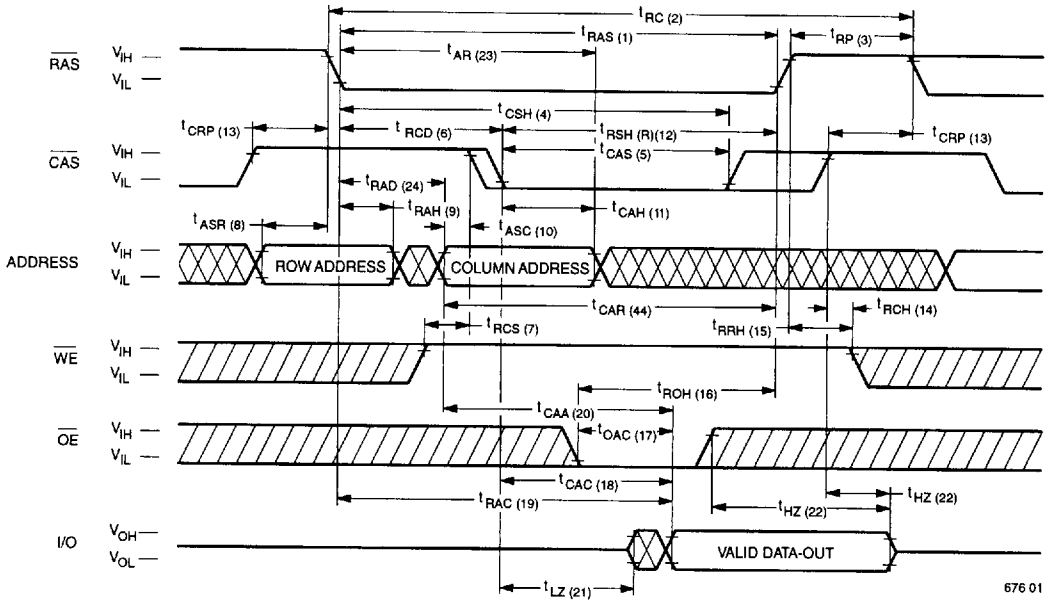
#	JEDEC Symbol	Symbol	Parameter	60		70		80		Unit	Notes
				Min.	Max.	Min.	Max.	Min.	Max.		
39	t <sub>RL1WL2</sub>	t <sub>RWD</sub>	RAS to WE Delay in Read-Modify-Write Cycle	90		100		110		ns	12
40	t <sub>CL1CH1</sub>	t <sub>CRW</sub>	CAS Pulse Width (RMW)	60		65		70		ns	
41	t <sub>AVWL2</sub>	t <sub>AWD</sub>	Col. Address to WE Delay	60		65		70		ns	12
42	t <sub>CL2CL2</sub>	t <sub>PC</sub>	Fast Page Mode Read or Write Cycle Time	35		40		45		ns	
43	t <sub>CH2CL2</sub>	t <sub>CP</sub>	CAS Precharge Time	10		10		10		ns	
44	t <sub>AVRH1</sub>	t <sub>CAR</sub>	Column Address to RAS Setup Time	30		35		40		ns	
45	t <sub>CH2QV</sub>	t <sub>CAP</sub>	Access Time from Column Precharge		35		40		45	ns	7
46	t <sub>RL1DX</sub>	t <sub>DHR</sub>	Data in Hold Time Referenced to RAS	50		55		60		ns	
47	t <sub>CL1RL2</sub>	t <sub>CSR</sub>	CAS Setup Time CAS-before-RAS Refresh	10		10		10		ns	
48	t <sub>RH2CL2</sub>	t <sub>RPC</sub>	RAS to CAS Precharge Time	5		5		5		ns	
49	t <sub>RL1CH1</sub>	t <sub>CHR</sub>	CAS Hold Time CAS-before-RAS Refresh	15		15		25		ns	
50	t <sub>CL2CL2 (RMW)</sub>	t <sub>PCM</sub>	Fast Page Mode Read-Modify-Write Cycle Time	90		100		105		ns	
	t <sub>T</sub>	t <sub>T</sub>	Transition Time (Rise and Fall)	3	50	3	50	3	50	ns	15
		t <sub>REF</sub>	Refresh Interval (512 Cycles)		8		8		8	ms	17

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1.  $I_{DD}$  is dependent on output loading when the device output is selected. Specified  $I_{DD}$  (max.) is measured with the output open.
2.  $I_{DD}$  is dependent upon the number of address transitions. Specified  $I_{DD}$  (max.) is measured with a maximum of two transitions per address cycle in Fast Page Mode.
3. Specified  $V_{IL}$  (min.) is steady state operating. During transitions,  $V_{IL}$  (min.) may undershoot to  $-1.0$  V for a period not to exceed 20 ns. All AC parameters are measured with  $V_{IL}$  (min.)  $\geq V_{SS}$  and  $V_{IH}$  (max.)  $\leq V_{DD}$ .
4.  $t_{RCD}$  (max.) is specified for reference only. Operation within  $t_{RCD}$  (max.) limits insures that  $t_{RAC}$  (max.) and  $t_{CAA}$  (max.) can be met. If  $t_{RCD}$  is greater than the specified  $t_{RCD}$  (max.), the access time is controlled by  $t_{CAA}$  and  $t_{CAC}$ .
5. Either  $t_{RRH}$  or  $t_{RCH}$  must be satisfied for a Read Cycle to occur.
6. Measured with a load equivalent to two TTL inputs and 100 pF.
7. Access time is determined by the longest of  $t_{CAA}$ ,  $t_{CAC}$  and  $t_{CAP}$ .
8. Assumes that  $t_{RAD} \leq t_{RAD}$  (max.). If  $t_{RAD}$  is greater than  $t_{RAD}$  (max.),  $t_{RAC}$  will increase by the amount that  $t_{RAD}$  exceeds  $t_{RAD}$  (max.).
9. Assumes that  $t_{RCD} \leq t_{RCD}$  (max.). If  $t_{RCD}$  is greater than  $t_{RCD}$  (max.),  $t_{RAC}$  will increase by the amount that  $t_{RCD}$  exceeds  $t_{RCD}$  (max.).
10. Assumes that  $t_{RAD} \geq t_{RAD}$  (max.).
11. Operation within the  $t_{RAD}$  (max.) limit ensures that  $t_{RAC}$  (max.) can be met.  $t_{RAD}$  (max.) is specified as a reference point only. If  $t_{RAD}$  is greater than the specified  $t_{RAD}$  (max.) limit, the access time is controlled by  $t_{CAA}$  and  $t_{CAC}$ .
12.  $t_{WCS}$ ,  $t_{RWD}$ ,  $t_{AWD}$  and  $t_{CWD}$  are not restrictive operating parameters.
13.  $t_{WCS}$  (min.) must be satisfied in an Early Write Cycle.
14.  $t_{DS}$  and  $t_{DH}$  are referenced to the latter occurrence of  $\overline{CAS}$  or  $\overline{WE}$ .
15.  $t_r$  is measured between  $V_{IH}$  (min.) and  $V_{IL}$  (max.). AC-measurements assume  $t_r = 5$  ns.
16. Assumes a three-state test load (5 pF and a 380 Ohm Thevenin equivalent).
17. An initial 200  $\mu$ s pause and 8  $\overline{RAS}$ -containing cycles are required when exiting an extended period of bias without clocks. An extended period of time without clocks is defined as one that exceeds the specified Refresh Interval.

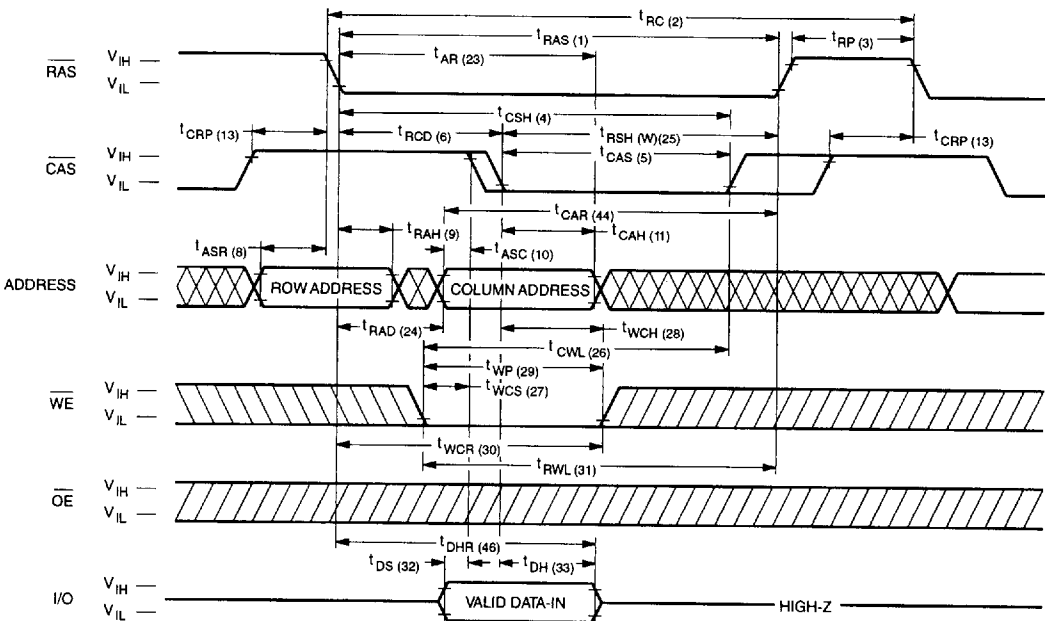


Waveforms of Read Cycle

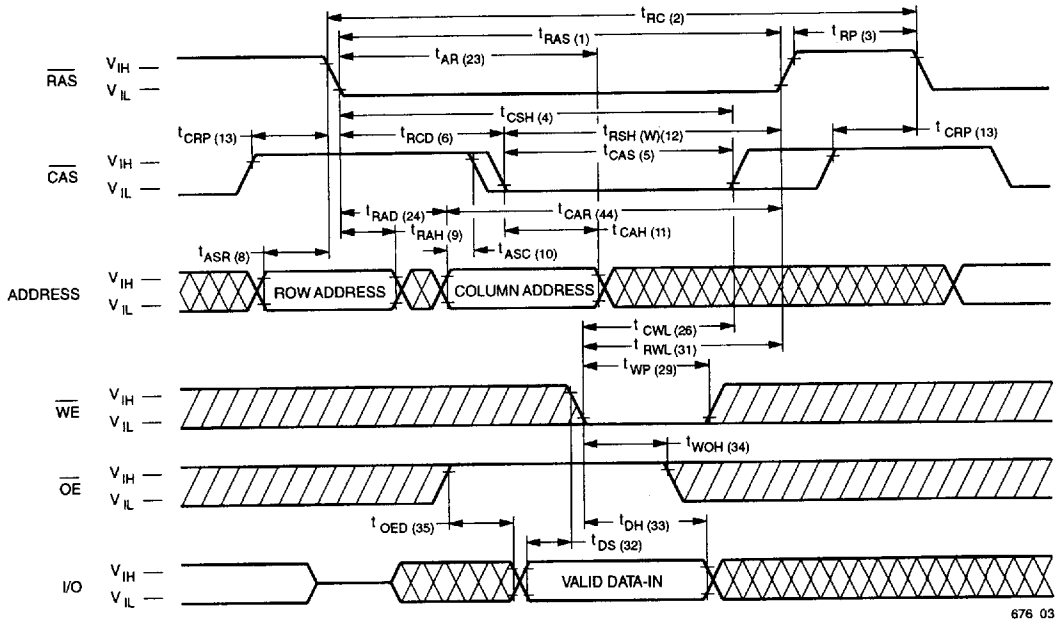


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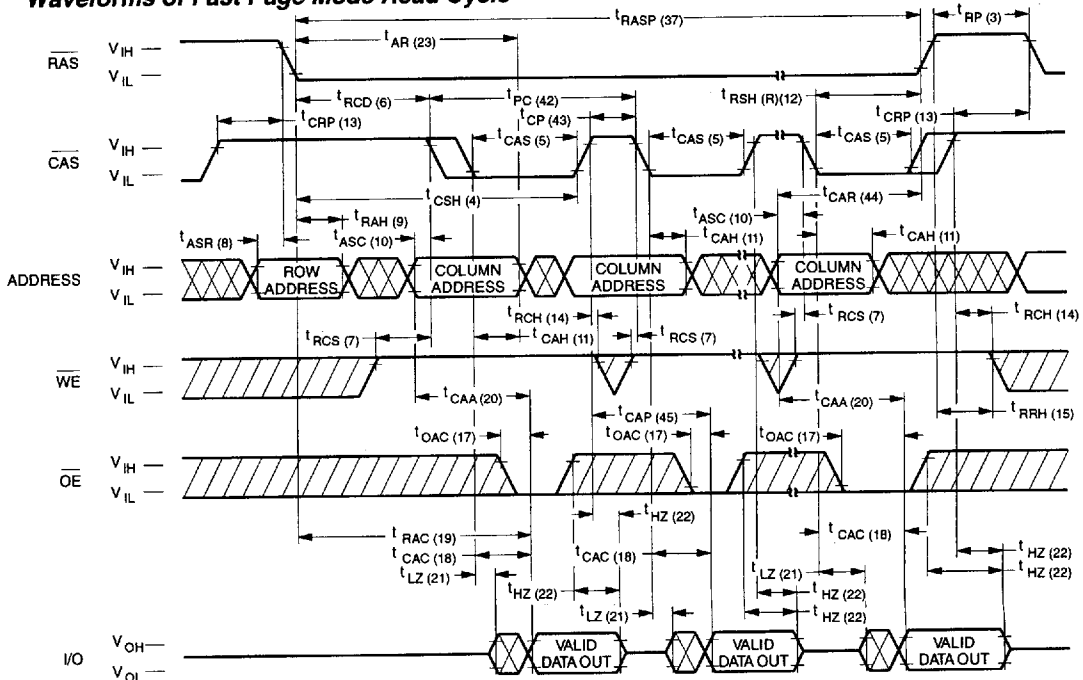
Waveforms of Early Write Cycle



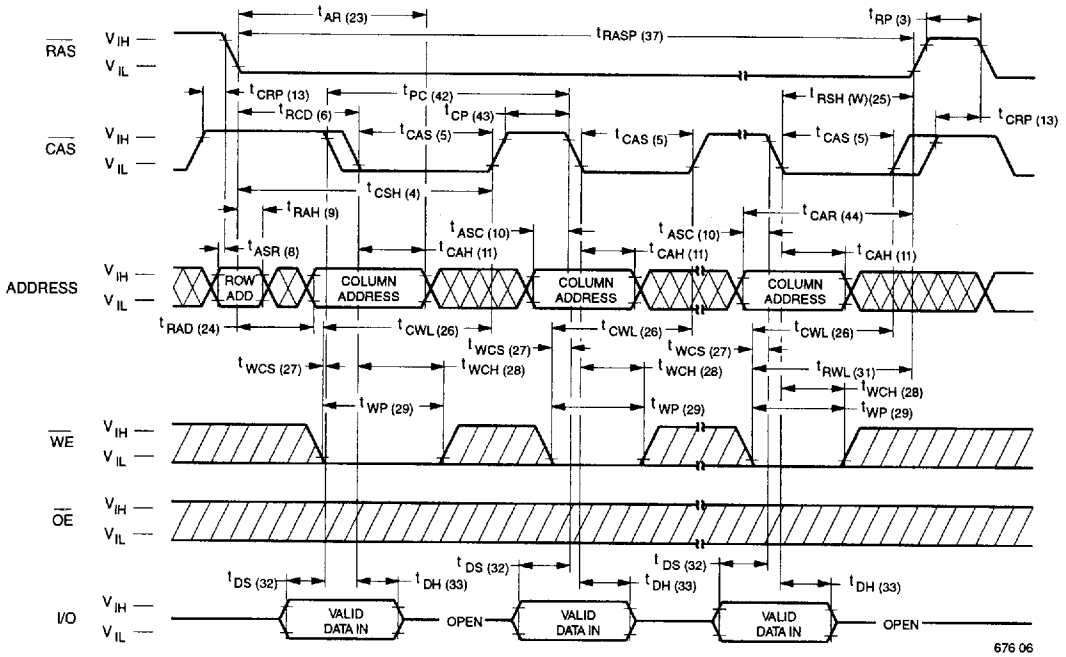
**Waveforms of OE-Controlled Write Cycle**



**Waveforms of Fast Page Mode Read Cycle**

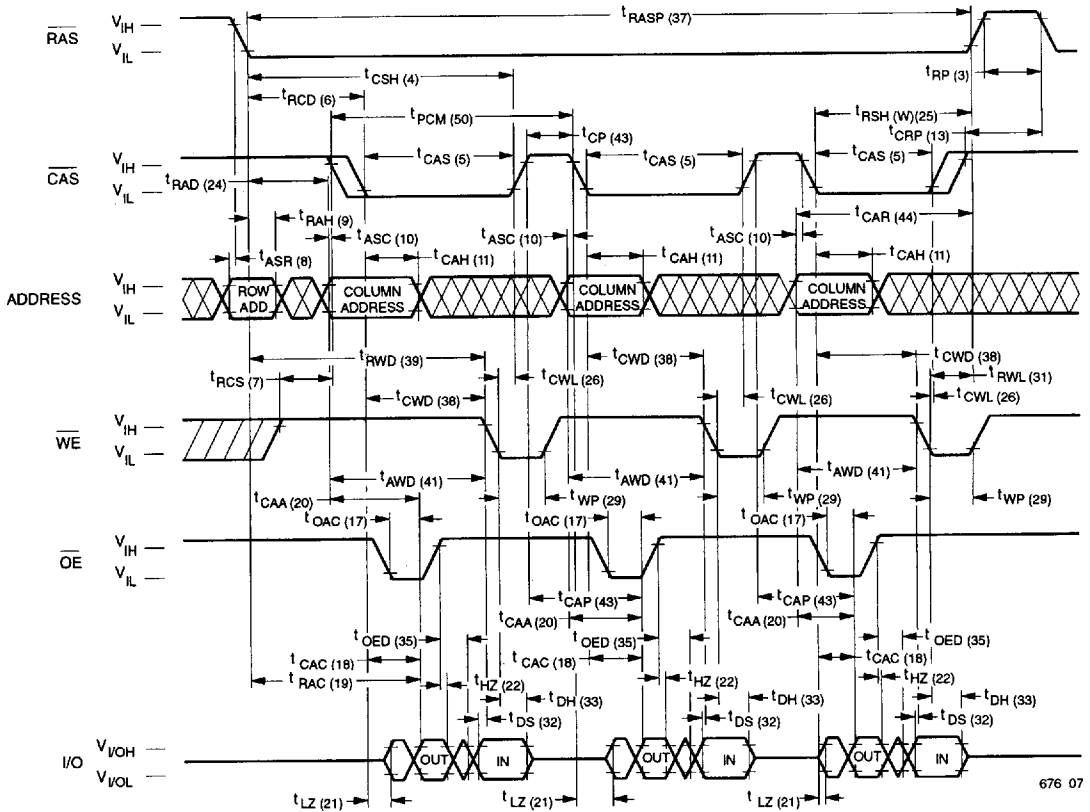


Waveforms of Fast Page Mode Write Cycle



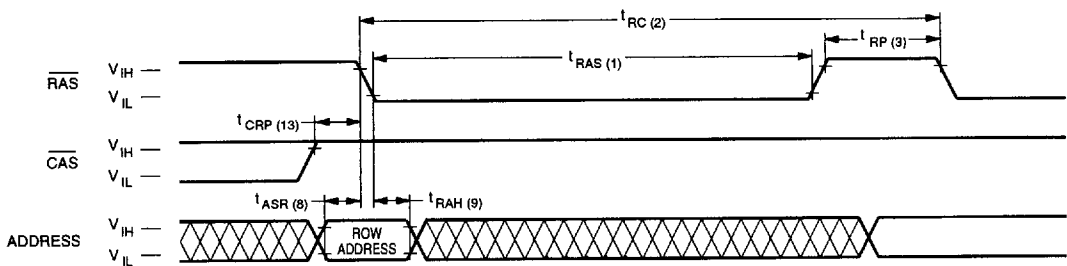
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Waveforms of Fast Page Mode Read-Write Cycle



676 07

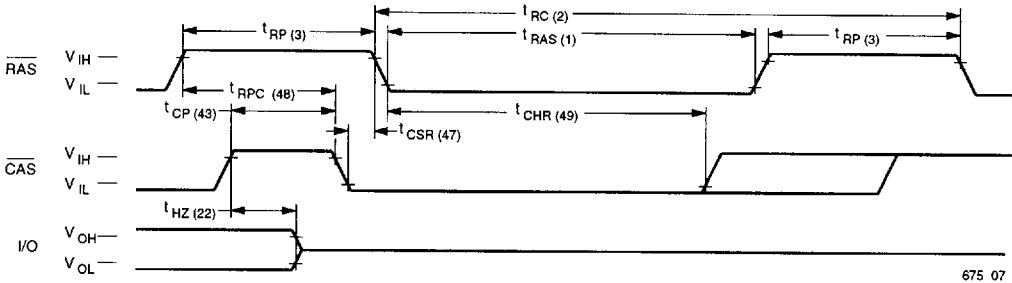
Waveforms of  $\overline{\text{RAS}}$ -Only Refresh Cycle



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NOTE:  $\overline{\text{WE}}$ ,  $\overline{\text{OE}}$  = Don't care

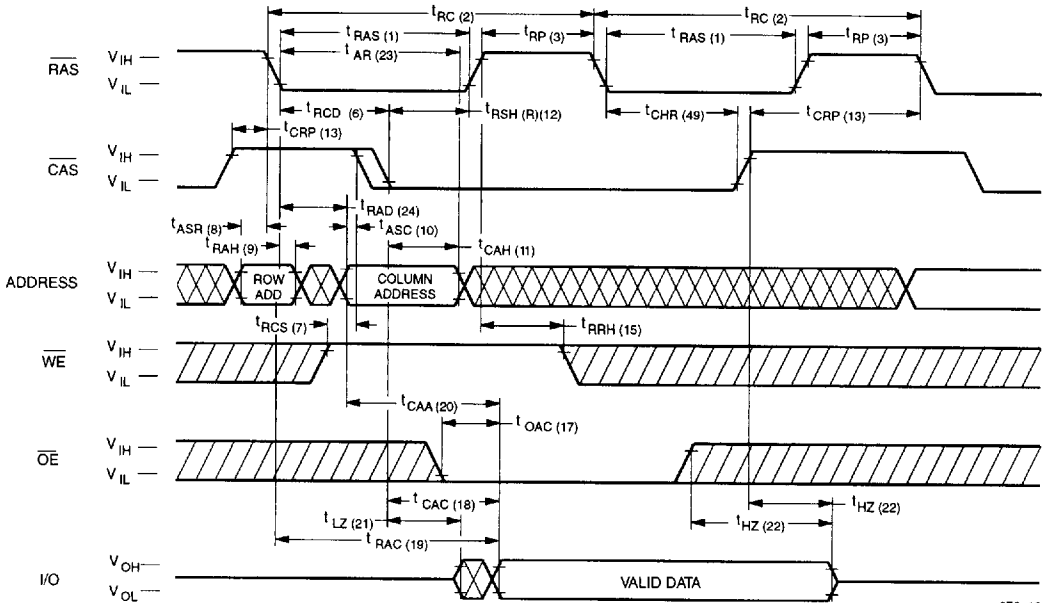
Waveforms of CAS-before-RAS Refresh Cycle



675 07

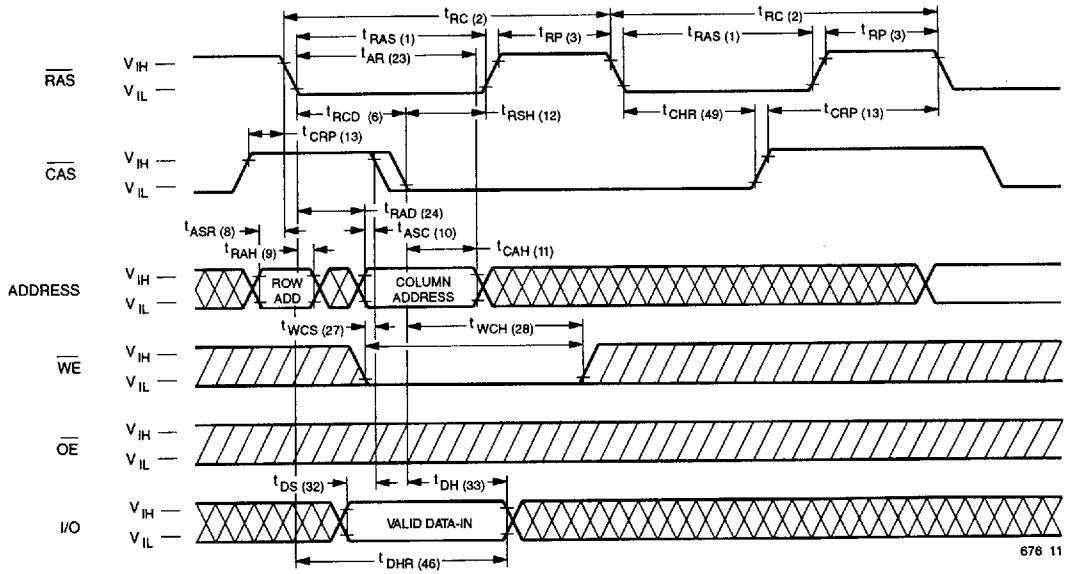
NOTE:  $\overline{WE}$ ,  $\overline{OE}$ ,  $A_0-A_7$  = Don't care

Waveforms of Hidden Refresh Cycle (Read)



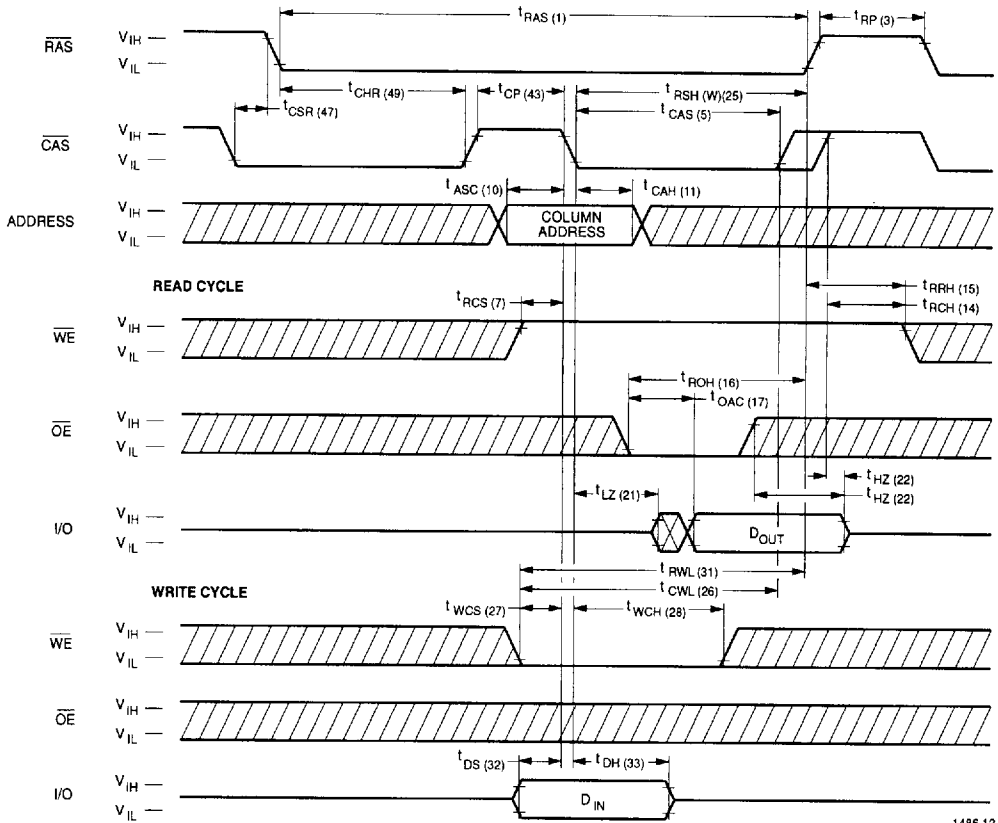
676 10

Waveforms of Hidden Refresh Cycle (Write)



676 11

Waveforms of  $\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$  Refresh Counter Test Cycle



1486 12

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### Functional Description

The V53C104D is a CMOS dynamic RAM optimized for high data bandwidth, low power applications. It is functionally similar to a traditional dynamic RAM. The V53C104D reads and writes data by multiplexing an 18-bit address into a 9-bit row and a 9-bit column address. The row address is latched by the Row Address Strobe ( $\overline{RAS}$ ). The column address "flows through" an internal address buffer and is latched by the Column Address Strobe ( $\overline{CAS}$ ). Because access time is primarily dependent on a valid column address rather than the precise time that the  $\overline{CAS}$  edge occurs, the delay time from  $\overline{RAS}$  to  $\overline{CAS}$  has little effect on the access time.

### Memory Cycle

A memory cycle is initiated by bringing  $\overline{RAS}$  low. Any memory cycle, once initiated, must not be ended or aborted before the minimum  $t_{RAS}$  time has expired. This ensures proper device operation and data integrity. A new cycle must not be initiated until the minimum precharge time  $t_{RP}/t_{CP}$  has elapsed.

### Read Cycle

A Read cycle is performed by holding the Write Enable ( $\overline{WE}$ ) signal High during a  $\overline{RAS}/\overline{CAS}$  operation. The column address must be held for a minimum specified by  $t_{AR}$ . Data Out becomes valid only when  $t_{OAC}$ ,  $t_{RAC}$ ,  $t_{CAA}$  and  $t_{CAC}$  are all satisfied. As a result, the access time is dependent on the timing relationships between these parameters. For example, the access time is limited by  $t_{CAA}$  when  $t_{RAC}$ ,  $t_{CAC}$  and  $t_{OAC}$  are all satisfied.

### Write Cycle

A Write Cycle is performed by taking  $\overline{WE}$  and  $\overline{CAS}$  low during a  $\overline{RAS}$  operation. The column address is latched by  $\overline{CAS}$ . The Write Cycle can be  $\overline{WE}$  controlled or  $\overline{CAS}$  controlled depending on whether  $\overline{WE}$  or  $\overline{CAS}$  falls later. Consequently, the input data must be valid at or before the falling edge of  $\overline{WE}$  or  $\overline{CAS}$ , whichever occurs last. In the  $\overline{CAS}$ -controlled Write Cycle, when the leading edge of  $\overline{WE}$  occurs prior to the  $\overline{CAS}$  low transition, the I/O data pins will be in the High-Z state at the beginning of the Write function.

Ending the Write with  $\overline{RAS}$  or  $\overline{CAS}$  will maintain the output in the High-Z state.

In the  $\overline{WE}$  controlled Write Cycle,  $\overline{OE}$  must be in the high state and  $t_{OED}$  must be satisfied.

### Refresh Cycle

To retain data, 512 Refresh Cycles are required in each 8 ms period. There are two ways to refresh the memory:

1. By clocking each of the 512 row addresses ( $A_0$  through  $A_8$ ) with  $\overline{RAS}$  at least once every 8 ms. Any Read, Write, Read-Modify-Write or  $\overline{RAS}$ -only cycle refreshes the addressed row.
2. Using a  $\overline{CAS}$ -before- $\overline{RAS}$  Refresh Cycle. If  $\overline{CAS}$  makes a transition from low to high to low after the previous cycle and before  $\overline{RAS}$  falls,  $\overline{CAS}$ -before- $\overline{RAS}$  refresh is activated. The V53C104D uses the output of an internal 9-bit counter as the source of row addresses and ignore external address inputs.

$\overline{CAS}$ -before- $\overline{RAS}$  is a "refresh-only" mode and no data access or device selection is allowed. Thus, the output remains in the High-Z state during the cycle. A  $\overline{CAS}$ -before- $\overline{RAS}$  counter test mode is provided to ensure reliable operation of the internal refresh counter.

### Data Retention Mode

The V53C104D offers a CMOS standby mode that is entered by causing the  $\overline{RAS}$  clock to swing between a valid  $V_{LL}$  and an "extra high"  $V_{IH}$  within 0.2 V of  $V_{DD}$ . While the  $\overline{RAS}$  clock is at the "extra high" level, the V53C104D power consumption is reduced to the low  $I_{DD6}$  level. Overall  $I_{DD}$  consumption when operating in this mode can be calculated as follows:

$$I = \frac{(t_{RC}) \times (I_{DD1}) + (t_{RX} - t_{RC}) \times (I_{DD6})}{t_{RX}}$$

Where:  $t_{RC}$  = Refresh Cycle Time  
 $t_{RX}$  = Refresh Interval / 512



**Fast Page Mode Operation**

Fast Page Mode operation permits all 512 columns within a selected row of the device to be randomly accessed at a high data rate. Maintaining  $\overline{\text{RAS}}$  low while performing successive  $\overline{\text{CAS}}$  cycles retains the row address internally and eliminates the need to reapply it for each cycle. The column address buffer acts as a transparent or flow-through latch while  $\overline{\text{CAS}}$  is high. Thus, access begins from the occurrence of a valid column address rather than from the falling edge of  $\overline{\text{CAS}}$ , eliminating  $t_{\text{ASC}}$  and  $t_r$  from the critical timing path.  $\overline{\text{CAS}}$  latches the address into the column address buffer and acts as an output enable. During Fast Page Mode operation, Read, Write, Read-Modify-Write or Read-Write-Read cycles are possible at random addresses within a row. Following the initial entry cycle into Fast Page Mode, access is  $t_{\text{CAA}}$  or  $t_{\text{CAP}}$  controlled. If the column address is valid prior to the rising edge of  $\overline{\text{CAS}}$ , the access time is referenced to the  $\overline{\text{CAS}}$  rising edge and is specified by  $t_{\text{CAP}}$ . If the column address is valid after the rising  $\overline{\text{CAS}}$  edge, access is timed from the occurrence of a valid address and is specified by  $t_{\text{CAA}}$ . In both cases, the falling edge of  $\overline{\text{CAS}}$  latches the address and enables the output.

Fast Page Mode provides a sustained data rate of 25 MHz for applications that require high data rates such as bit-mapped graphics or high-speed signal processing. The following equation can be used to calculate the maximum data rate:

$$\text{Data Rate} = \frac{512}{t_{\text{RC}} + 511 \times t_{\text{PC}}}$$

**Data Output Operation**

The V53C104D Input/Output is controlled by  $\overline{\text{OE}}$ ,  $\overline{\text{CAS}}$ ,  $\overline{\text{WE}}$  and  $\overline{\text{RAS}}$ . A  $\overline{\text{RAS}}$  low transition enables the transfer of data to and from the selected row address in the Memory Array. A  $\overline{\text{RAS}}$  high transition disables data transfer and latches the output data if the output is enabled. After a memory cycle is initiated with a  $\overline{\text{RAS}}$  low transition, a  $\overline{\text{CAS}}$  low transition or  $\overline{\text{CAS}}$  low level enables the internal I/O path. A  $\overline{\text{CAS}}$  high transition or a  $\overline{\text{CAS}}$  high level disables the I/O path and the output driver if it is enabled. A  $\overline{\text{CAS}}$  low transition while  $\overline{\text{RAS}}$  is high has no effect on the I/O data path or on the output drivers. The output drivers, when otherwise enabled, can be disabled by holding

$\overline{\text{OE}}$  high. The  $\overline{\text{OE}}$  signal has no effect on any data stored in the output latches. A  $\overline{\text{WE}}$  low level can also disable the output drivers when  $\overline{\text{CAS}}$  is low. During a Write cycle, if  $\overline{\text{WE}}$  goes low at a time in relationship to  $\overline{\text{CAS}}$  that would normally cause the outputs to be active, it is necessary to use  $\overline{\text{OE}}$  to disable the output drivers prior to the  $\overline{\text{WE}}$  low transition to allow Data In Setup Time ( $t_{\text{DS}}$ ) to be satisfied.

**Power-On**

After application of the  $V_{\text{DD}}$  supply, an initial pause of 200  $\mu\text{s}$  is required followed by a minimum of 8 initialization cycles (any combination of cycles containing a  $\overline{\text{RAS}}$  clock). Eight initialization cycles are required after extended periods of bias without clocks (greater than the Refresh Interval).

During Power-On, the  $V_{\text{DD}}$  current requirement of the V53C104D is dependent on the input levels of  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$ . If  $\overline{\text{RAS}}$  is low during Power-On, the device will go into an active cycle and  $I_{\text{DD}}$  will exhibit current transients. It is recommended that  $\overline{\text{RAS}}$  and  $\overline{\text{CAS}}$  track with  $V_{\text{DD}}$  or be held at a valid  $V_{\text{IH}}$  during Power-On to avoid current surges.

**Table 1. V53C104D Data Output Operation for Various Cycle Types**

Cycle Type	I/O State
Read Cycles	Data from Addressed Memory Cell
$\overline{\text{CAS}}$ -Controlled Write Cycle (Early Write)	High-Z
$\overline{\text{WE}}$ -Controlled Write Cycle (Late Write)	$\overline{\text{OE}}$ Controlled. High $\overline{\text{OE}}$ = High-Z I/Os
Read-Modify-Write Cycles	Data from Addressed Memory Cell
Fast Page Mode Read	Data from Addressed Memory Cell
Fast Page Mode Write Cycle (Early Write)	High-Z
Fast Page Mode Read-Modify-Write Cycle	Data from Addressed Memory Cell
$\overline{\text{RAS}}$ -only Refresh	High-Z
$\overline{\text{CAS}}$ -before- $\overline{\text{RAS}}$ Refresh Cycle	Data remains as in previous cycle
$\overline{\text{CAS}}$ -only Cycles	High-Z

**2**