Data Sheet | July 11, 2006 | FN6295.1

## 100V, 3A/4A Peak, High Frequency Half-Bridge Drivers

The ISL2110, ISL2111 are 100V, high frequency, half-bridge N-channel power MOSFET driver ICs. They are based on the popular HIP2100, HIP2101 half-bridge drivers, but offer several performance improvements. Peak output pull-up/pull-down current has been increased to 3A/4A, which significantly reduces switching power losses and eliminates the need for external totem-pole buffers in many applications. Also, the low end of the $V_{DD}$ operational supply range has been extended to 8VDC. The ISL2110 has additional input hysteresis for superior operation in noisy environments and the inputs of the ISL2111, like those of the ISL2110, can now safely swing to the $V_{DD}$ supply rail.

## Ordering Information

| PART NUMBER (Notes 1, 2) | PART MARKING | TEMP. RANGE (°C) | PACKAGE (Pb-Free) | PKG. DWG. # |
|---|---|---|---|---|
| ISL2110ABZ | 2110ABZ | -40 to 125 | 8 Ld SOIC | M8.15 |
| ISL2110AR4Z | 2110AR4Z | -40 to 125 | 12 Ld 4x4 DFN | L12.4x4A |
| ISL2111ABZ | 2111ABZ | -40 to 125 | 8 Ld SOIC | M8.15 |
| ISL2111AR4Z | 2111AR4Z | -40 to 125 | 12 Ld 4x4 DFN | L12.4x4A |

NOTES:

1. Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
2. Add “-T” suffix for Tape and Reel packing option.

## Features

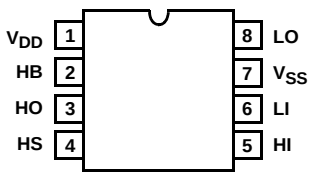
- Drives N-Channel MOSFET Half-Bridge
- SOIC and DFN Package Options
- SOIC and DFN Packages Compliant with 100V Conductor Spacing Guidelines per IPC-2221
- Pb-Free Plus Anneal Available (RoHS Compliant)
- Bootstrap Supply Max Voltage to 114VDC
- On-Chip 1Ω Bootstrap Diode
- Fast Propagation Times for Multi-MHz Circuits
- Drives 1nF Load with Typical Rise/Fall Times of 9ns/7.5ns
- CMOS Compatible Input Thresholds (ISL2110)
- 3.3V/TTL Compatible Input Thresholds (ISL2111)
- Independent Inputs Provide Flexibility
- No Start-Up Problems
- Outputs Unaffected by Supply Glitches, HS Ringing Below Ground or HS Slewing at High dv/dt
- Low Power Consumption
- Wide Supply Voltage Range (8V to 14V)
- Supply Undervoltage Protection
- 1.6Ω/1Ω Typical Output Pull-Up/Pull-Down Resistance

## Applications

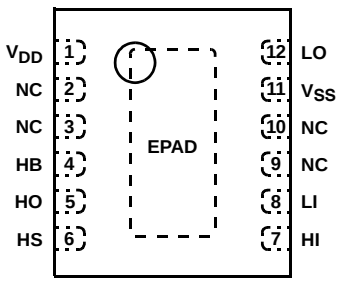
- Telecom Half-Bridge DC/DC Converters
- Telecom Full-Bridge DC/DC Converters
- Two-Switch Forward Converters
- Active-Clamp Forward Converters
- Class-D Audio Amplifiers

## Pinouts

**ISL2110, ISL2111 (SOIC)**
TOP VIEW

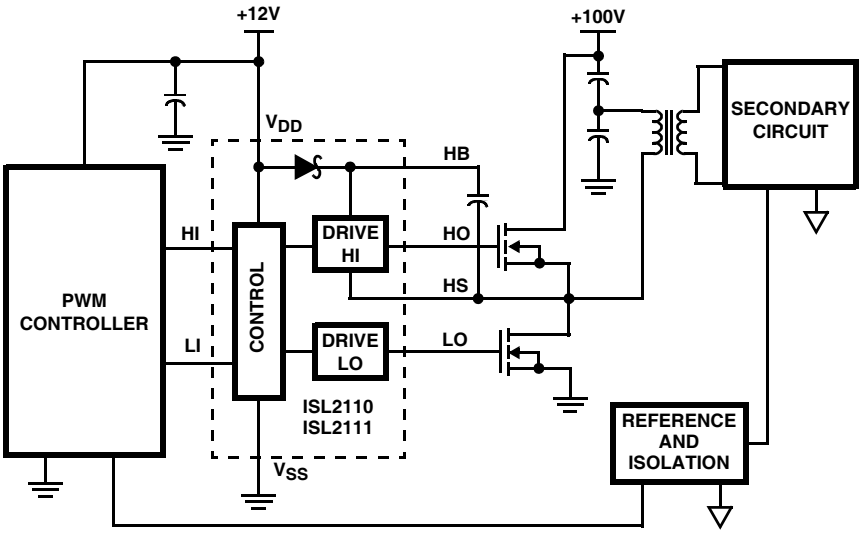



**ISL2110, ISL2111 (DFN)**
TOP VIEW

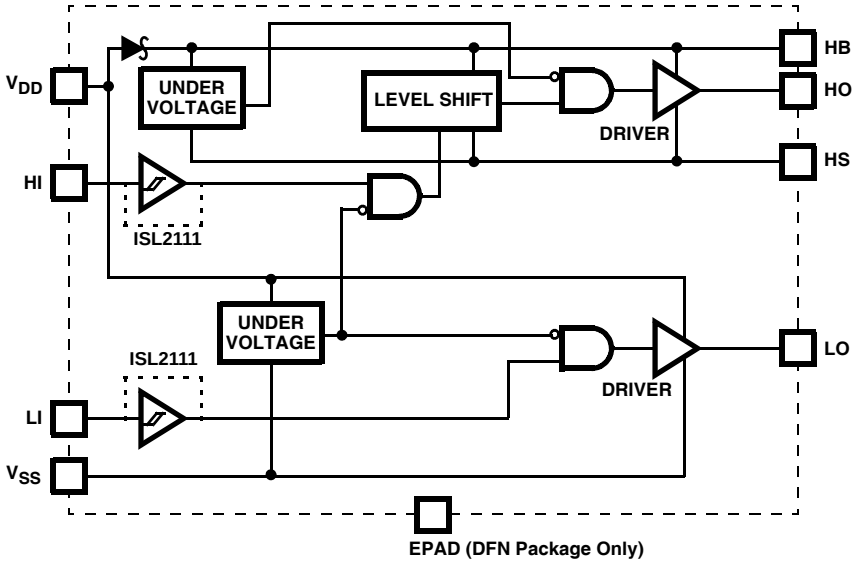



NOTE: EPAD = Exposed PAD.

## Application Block Diagram




## Functional Block Diagram




*EPAD = Exposed Pad. The EPAD is electrically isolated from all other pins. For best thermal performance connect the EPAD to the PCB power ground plane.

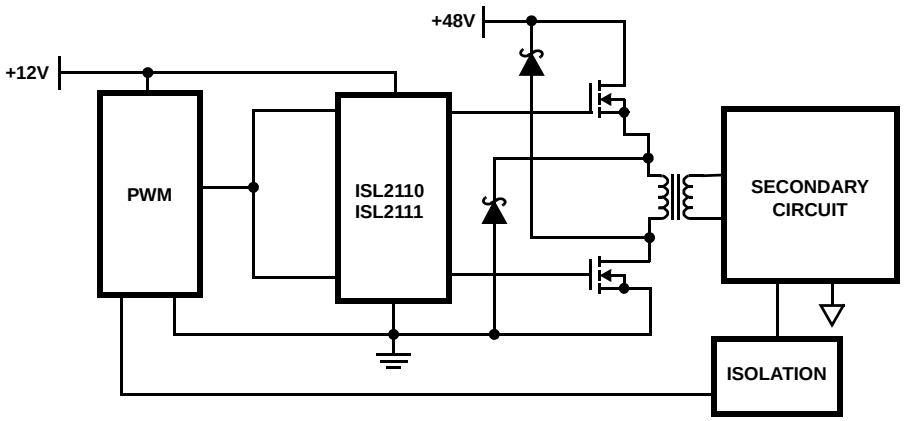



FIGURE 1. TWO-SWITCH FORWARD CONVERTER

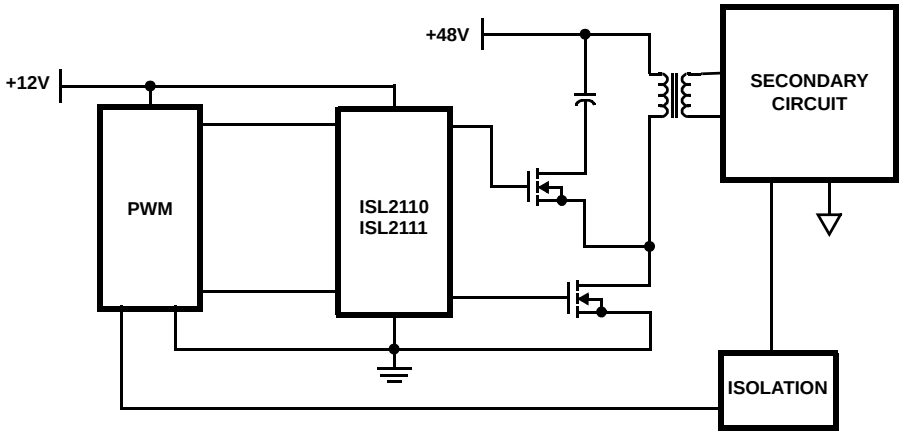



FIGURE 2. FORWARD CONVERTER WITH AN ACTIVE-CLAMP

## Absolute Maximum Ratings

Supply Voltage, $V_{DD}$, $V_{HB}$ - $V_{HS}$ (Notes 3, 4) . . . . . -0.3V to 18V
LI and HI Voltages (Note 4) . . . . . -0.3V to $V_{DD}$ + 0.3V
Voltage on LO (Note 4) . . . . . -0.3V to $V_{DD}$ + 0.3V
Voltage on HO (Note 4) . . . . . $V_{HS}$ - 0.3V to $V_{HB}$ + 0.3V
Voltage on HS (Continuous) (Note 4) . . . . . -1V to 110V
Voltage on HB (Note 4) . . . . . 118V
Average Current in $V_{DD}$ to HB Diode . . . . . 100mA

## Maximum Recommended Operating Conditions

Supply Voltage, $V_{DD}$ . . . . . 8V to 14V
Voltage on HS . . . . . -1V to 100V
Voltage on HS . . . . . (Repetitive Transient) -5V to 105V
Voltage on HB . . $V_{HS}$ + 7V to $V_{HS}$ + 14V and $V_{DD}$ - 1V to $V_{DD}$ + 100V
HS Slew Rate. . . . . <50V/ns

## Thermal Information

| Thermal Resistance (Typical) | $\theta_{JA}$ (°C/W) | $\theta_{JC}$ (°C/W) |
|---|---|---|
| SOIC (Note 5) . . . . . | 95 | N/A |
| DFN (Note 6) . . . . . | 40 | 3 |

Max Power Dissipation at 25°C in Free Air (SOIC, Note 5) . . . . 1.3W
Max Power Dissipation at 25°C in Free Air (DFN, Note 6) . . . . . 3.1W
Storage Temperature Range . . . . . -65°C to 150°C
Junction Temperature Range. . . . . -55°C to 150°C
Lead Temperature (Soldering 10s - SOIC Lead Tips Only) . . . 300°C
For recommended soldering conditions see Tech Brief TB389.

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the recommended operating conditions of this specification is not implied.*

NOTES:

3. The ISL2110 and ISL2111 are capable of derated operation at supply voltages exceeding 14V. Figure 22 shows the high-side voltage derating curve for this mode of operation.
4. All voltages referenced to $V_{SS}$ unless otherwise specified.
5. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board. See Tech Brief TB379 for details.
6. $\theta_{JA}$ is measured in free air with the component mounted on a high effective thermal conductivity test board with "direct attach" features. For $\theta_{JC}$, the "case temp" is measured at the center of the exposed metal pad on the package underside. See Tech Brief TB379 for details.

## Electrical Specifications

$V_{DD}$ = $V_{HB}$ = 12V, $V_{SS}$ = $V_{HS}$ = 0V, No Load on LO or HO, Unless Otherwise Specified

| PARAMETERS | SYMBOL | TEST CONDITIONS | $T_J$ = 25°C | | | $T_J$ = -40°C to 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| **SUPPLY CURRENTS** | | | | | | | | |
| $V_{DD}$ Quiescent Current | $I_{DD}$ | ISL2110; LI = HI = 0V | - | 0.1 | 0.25 | - | 0.3 | mA |
| $V_{DD}$ Quiescent Current | $I_{DD}$ | ISL2111; LI = HI = 0V | - | 0.3 | 0.45 | - | 0.55 | mA |
| $V_{DD}$ Operating Current | $I_{DDO}$ | ISL2110; f = 500kHz | - | 3.4 | 5.0 | - | 5.5 | mA |
| $V_{DD}$ Operating Current | $I_{DDO}$ | ISL2111; f = 500kHz | - | 3.5 | 5.0 | - | 5.5 | mA |
| Total HB Quiescent Current | $I_{HB}$ | LI = HI = 0V | - | 0.1 | 0.15 | - | 0.2 | mA |
| Total HB Operating Current | $I_{HBO}$ | f = 500kHz | - | 3.4 | 5.0 | - | 5.5 | mA |
| HB to $V_{SS}$ Current, Quiescent | $I_{HBS}$ | LI = HI = 0V; $V_{HB}$ = $V_{HS}$ = 114V | - | 0.05 | 1.5 | - | 10 | µA |
| HB to $V_{SS}$ Current, Operating | $I_{HBSO}$ | f = 500kHz; $V_{HB}$ = $V_{HS}$ = 114V | - | 1.2 | - | - | - | mA |
| **INPUT PINS** | | | | | | | | |
| Low Level Input Voltage Threshold | $V_{IL}$ | ISL2110 | 3.7 | 4.4 | - | 3.5 | - | V |
| Low Level Input Voltage Threshold | $V_{IL}$ | ISL2111 | 1.4 | 1.8 | - | 1.2 | - | V |
| High Level Input Voltage Threshold | $V_{IH}$ | ISL2110 | - | 6.6 | 7.4 | - | 7.6 | V |
| High Level Input Voltage Threshold | $V_{IH}$ | ISL2111 | - | 1.8 | 2.2 | - | 2.4 | V |
| Input Voltage Hysteresis | $V_{IHYS}$ | ISL2110 | - | 2.2 | - | - | - | V |
| Input Pull-down Resistance | $R_I$ | | - | 210 | - | 100 | 500 | kΩ |
| **UNDER VOLTAGE PROTECTION** | | | | | | | | |
| $V_{DD}$ Rising Threshold | $V_{DDR}$ | | 6.1 | 6.6 | 7.1 | 5.8 | 7.4 | V |
| $V_{DD}$ Threshold Hysteresis | $V_{DDH}$ | | - | 0.6 | - | - | - | V |

**Electrical Specifications** $V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, Unless Otherwise Specified **(Continued)**

| PARAMETERS | SYMBOL | TEST CONDITIONS | $T_J$ = 25°C | | | $T_J$ = -40°C to 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| HB Rising Threshold | $V_{HBR}$ | | 5.5 | 6.1 | 6.8 | 5.0 | 7.1 | V |
| HB Threshold Hysteresis | $V_{HBH}$ | | - | 0.6 | - | - | - | V |
| **BOOT STRAP DIODE** | | | | | | | | |
| Low Current Forward Voltage | $V_{DL}$ | $I_{VDD-HB}$ = 100µA | - | 0.5 | 0.6 | - | 0.7 | V |
| High Current Forward Voltage | $V_{DH}$ | $I_{VDD-HB}$ = 100mA | - | 0.7 | 0.9 | - | 1 | V |
| Dynamic Resistance | $R_D$ | $I_{VDD-HB}$ = 100mA | - | 0.7 | 1 | - | 1.5 | Ω |
| **LO GATE DRIVER** | | | | | | | | |
| Low Level Output Voltage | $V_{OLL}$ | $I_{LO}$ = 100mA | - | 0.1 | 0.18 | - | 0.25 | V |
| High Level Output Voltage | $V_{OHL}$ | $I_{LO}$ = -100mA, $V_{OHL} = V_{DD} - V_{LO}$ | - | 0.16 | 0.23 | - | 0.3 | V |
| Peak Pull-Up Current | $I_{OHL}$ | $V_{LO}$ = 0V | - | 3 | - | - | - | A |
| Peak Pull-Down Current | $I_{OLL}$ | $V_{LO}$ = 12V | - | 4 | - | - | - | A |
| **HO GATE DRIVER** | | | | | | | | |
| Low Level Output Voltage | $V_{OLH}$ | $I_{HO}$ = 100mA | - | 0.1 | 0.18 | - | 0.25 | V |
| High Level Output Voltage | $V_{OHH}$ | $I_{HO}$ = -100mA, $V_{OHH} = V_{HB} - V_{HO}$ | - | 0.16 | 0.23 | - | 0.3 | V |
| Peak Pull-Up Current | $I_{OHH}$ | $V_{HO}$ = 0V | - | 3 | - | - | - | A |
| Peak Pull-Down Current | $I_{OLH}$ | $V_{HO}$ = 12V | - | 4 | - | - | - | A |

**Switching Specifications** $V_{DD} = V_{HB} = 12V$, $V_{SS} = V_{HS} = 0V$, No Load on LO or HO, Unless Otherwise Specified

| PARAMETERS | SYMBOL | TEST CONDITIONS | $T_J$ = 25°C | | | $T_J$ = -40°C to 125°C | | UNITS |
|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | |
| Lower Turn-Off Propagation Delay (LI Falling to LO Falling) | $t_{LPHL}$ | | - | 32 | 50 | - | 60 | ns |
| Upper Turn-Off Propagation Delay (HI Falling to HO Falling) | $t_{HPHL}$ | | - | 32 | 50 | - | 60 | ns |
| Lower Turn-On Propagation Delay (LI Rising to LO Rising) | $t_{LPLH}$ | | - | 39 | 50 | - | 60 | ns |
| Upper Turn-On Propagation Delay (HI Rising to HO Rising) | $t_{HPLH}$ | | - | 38 | 50 | - | 60 | ns |
| Delay Matching: Upper Turn-Off to Lower Turn-On | $t_{MON}$ | | 1 | 8 | - | - | 16 | ns |
| Delay Matching: Lower Turn-Off to Upper Turn-On | $t_{MOFF}$ | | 1 | 6 | - | - | 16 | ns |
| Either Output Rise Time (10% to 90%) | $t_{RC}$ | $C_L$ = 1nF | - | 9 | - | - | - | ns |
| Either Output Fall Time (90% to 10%) | $t_{FC}$ | $C_L$ = 1nF | - | 7.5 | - | - | - | ns |
| Either Output Rise Time (3V to 9V) | $t_R$ | $C_L$ = 0.1µF | - | 0.3 | 0.4 | - | 0.5 | µs |
| Either Output Fall Time (9V to 3V) | $t_F$ | $C_L$ = 0.1µF | - | 0.19 | 0.3 | - | 0.4 | µs |
| Minimum Input Pulse Width that Changes the Output | $t_{PW}$ | | - | - | - | - | 50 | ns |
| Bootstrap Diode Turn-On or Turn-Off Time | $t_{BS}$ | | - | 10 | - | - | - | ns |

## Pin Descriptions

| SYMBOL | DESCRIPTION |
|---|---|
| $V_{DD}$ | Positive supply to lower gate driver. Bypass this pin to $V_{SS}$. |
| HB | High-side bootstrap supply. External bootstrap capacitor is required. Connect positive side of bootstrap capacitor to this pin. Bootstrap diode is on-chip. |
| HO | High-side output. Connect to gate of high-side power MOSFET. |
| HS | High-side source connection. Connect to source of high-side power MOSFET. Connect negative side of bootstrap capacitor to this pin. |
| HI | High-side input. |
| LI | Low-side input. |
| $V_{SS}$ | Chip negative supply, which will generally be ground. |
| LO | Low-side output. Connect to gate of low-side power MOSFET. |
| EPAD | Exposed pad. Connect to ground or float. The EPAD is electrically isolated from all other pins. |

## Timing Diagrams

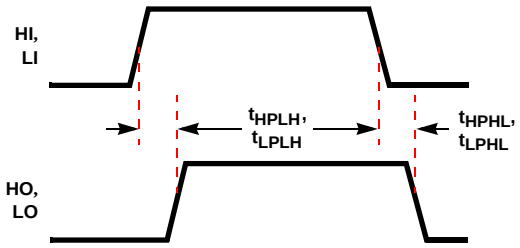



FIGURE 3. PROPAGATION DELAYS

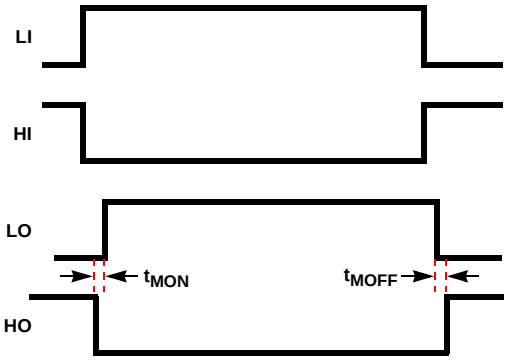



FIGURE 4. DELAY MATCHING

## Typical Performance Curves

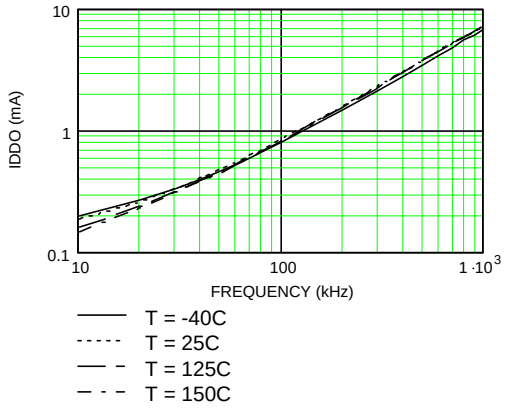



FIGURE 5. ISL2110 IDD OPERATING CURRENT vs FREQUENCY

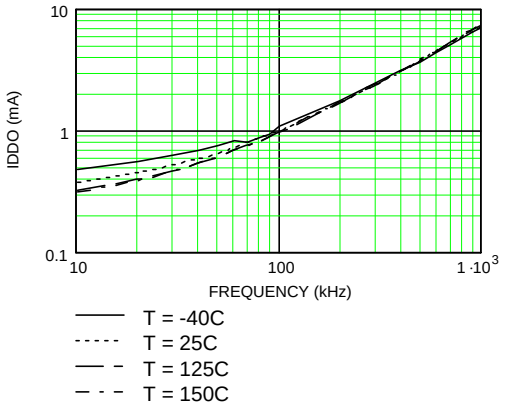



FIGURE 6. ISL2111 IDD OPERATING CURRENT vs FREQUENCY

## Typical Performance Curves (Continued)

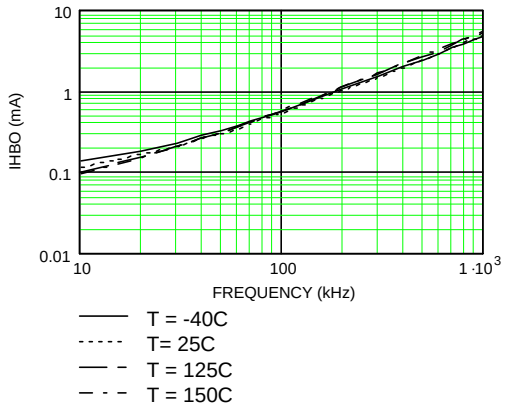



FIGURE 7. IHB OPERATING CURRENT vs FREQUENCY

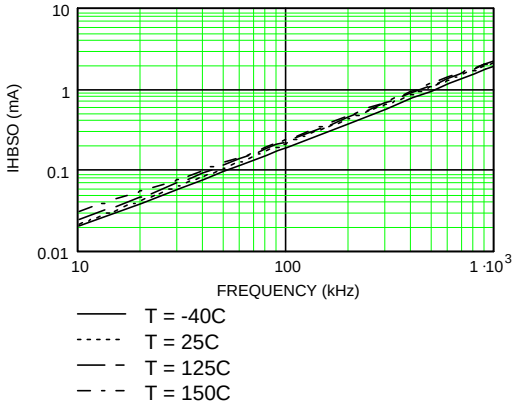



FIGURE 8. IHBS OPERATING CURRENT vs FREQUENCY

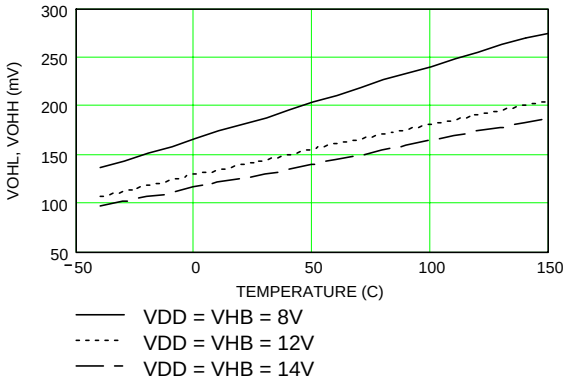



FIGURE 9. HIGH LEVEL OUTPUT VOLTAGE vs TEMPERATURE

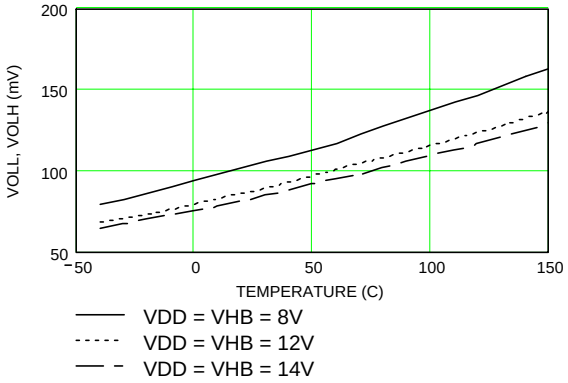



FIGURE 10. LOW LEVEL OUTPUT VOLTAGE vs TEMPERATURE

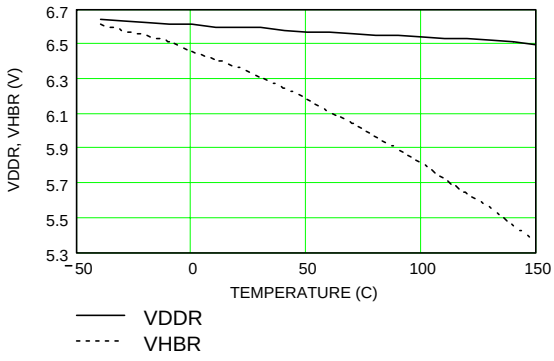



FIGURE 11. UNDERVOLTAGE LOCKOUT THRESHOLD vs TEMPERATURE

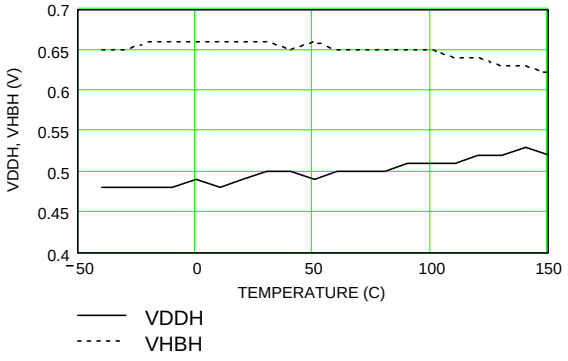



FIGURE 12. UNDERVOLTAGE LOCKOUT HYSTERESIS vs TEMPERATURE

## Typical Performance Curves (Continued)

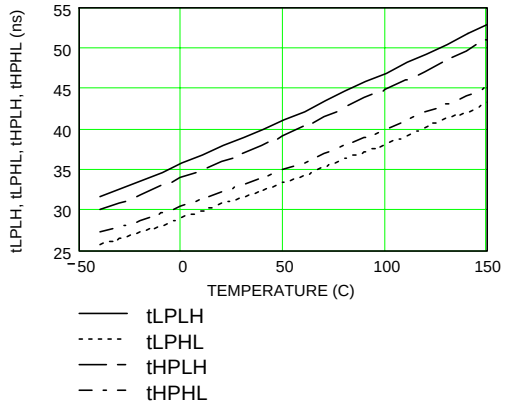



FIGURE 13. ISL2110 PROPAGATION DELAYS vs TEMPERATURE

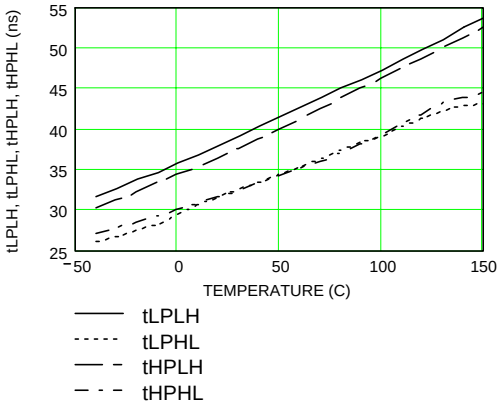



FIGURE 14. ISL2111 PROPAGATION DELAYS vs TEMPERATURE

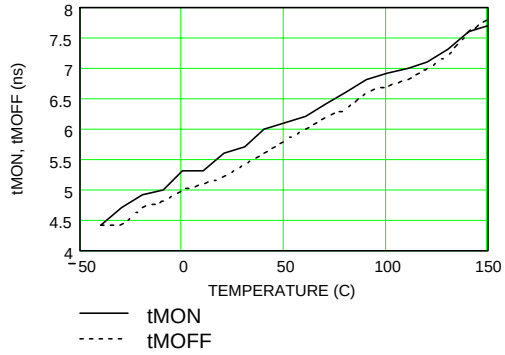



FIGURE 15. ISL2110 DELAY MATCHING vs TEMPERATURE

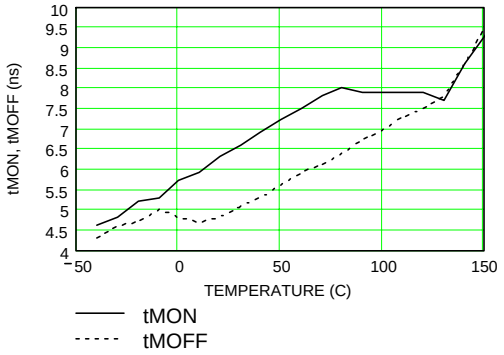



FIGURE 16. ISL2111 DELAY MATCHING vs TEMPERATURE

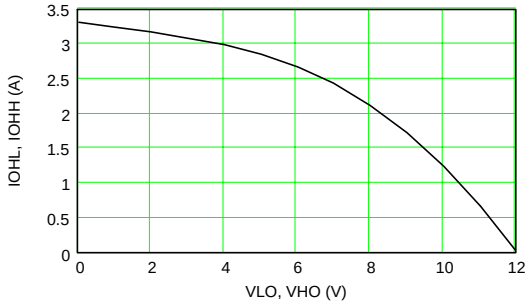



FIGURE 17. PEAK PULL-UP CURRENT vs OUTPUT VOLTAGE

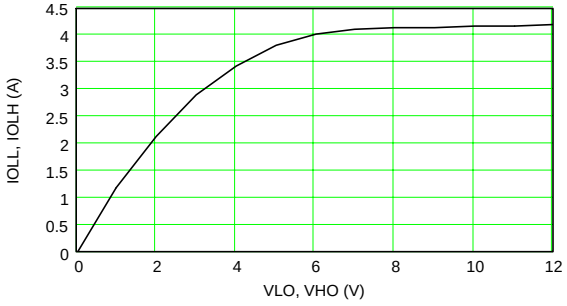



FIGURE 18. PEAK PULL-DOWN CURRENT vs OUTPUT VOLTAGE

## Typical Performance Curves (Continued)

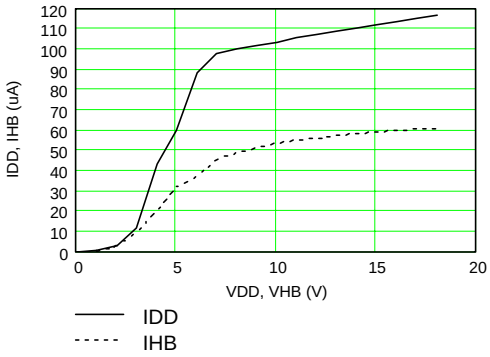



FIGURE 19. ISL2110 QUIESCENT CURRENT vs VOLTAGE

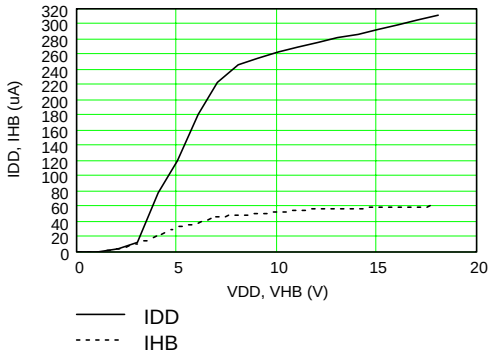



FIGURE 20. ISL2111 QUIESCENT CURRENT vs VOLTAGE

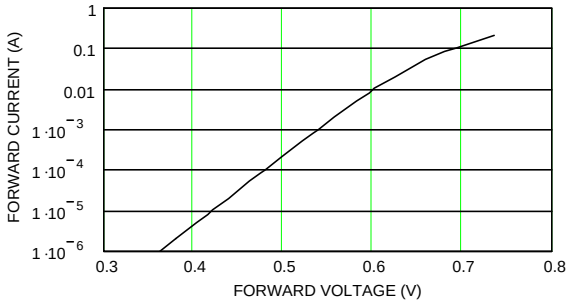



FIGURE 21. BOOTSTRAP DIODE I-V CHARACTERISTICS

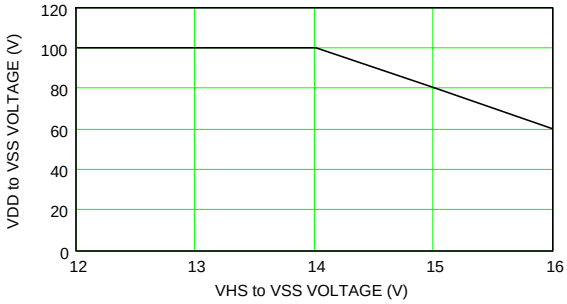
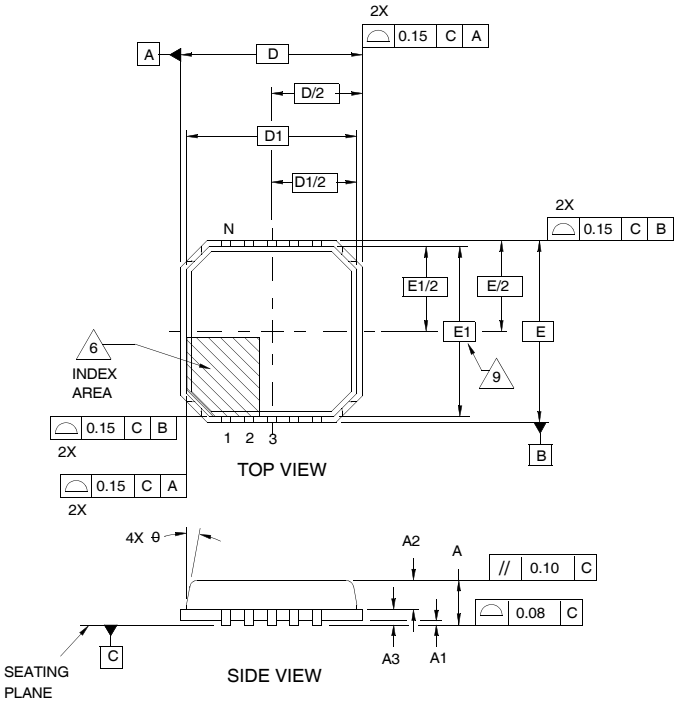
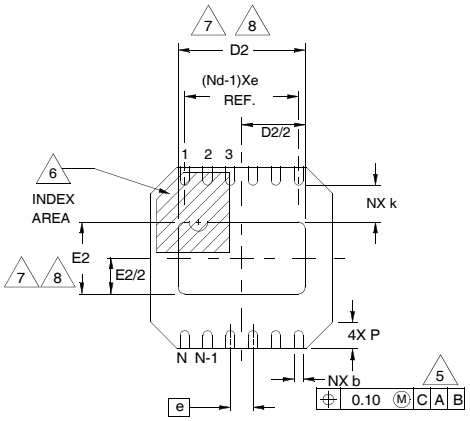
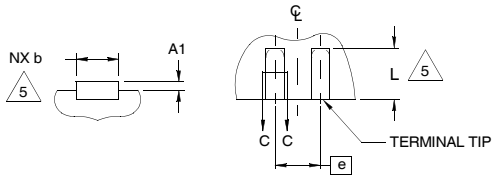



FIGURE 22. VHS VOLTAGE vs VDD VOLTAGE

## Dual Flat No-Lead Plastic Package (DFN)
## Micro Lead Frame Plastic Package (MLFP)




## L12.4x4A

**12 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE**

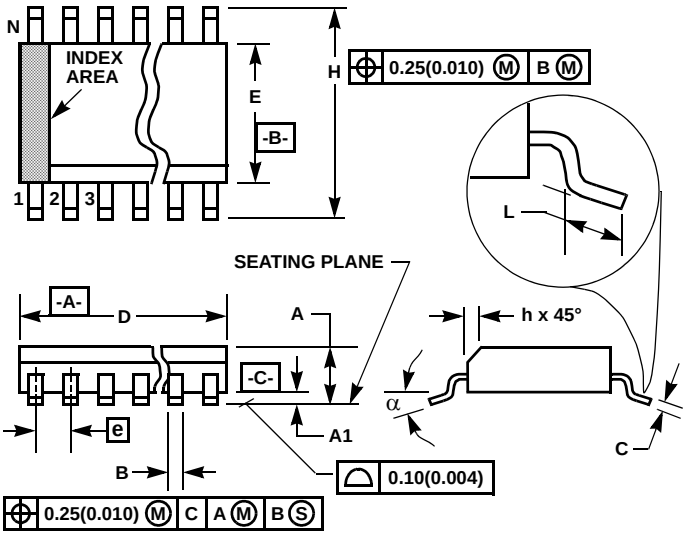
| SYMBOL | MILLIMETERS | | | NOTES |
|---|---|---|---|---|
| | MIN | NOMINAL | MAX | |
| A | - | 0.85 | 0.90 | - |
| A1 | 0.00 | 0.01 | 0.05 | - |
| A2 | - | 0.65 | 0.70 | - |
| A3 | | 0.20 REF | | - |
| b | 0.18 | 0.23 | 0.30 | 5, 8 |
| D | | 4.00 BSC | | - |
| D1 | | 3.75 BSC | | - |
| D2 | 2.65 | 2.80 | 2.95 | 7, 8 |
| E | | 4.00 BSC | | - |
| E1 | | 3.75 BSC | | - |
| E2 | 1.43 | 1.58 | 1.73 | 7, 8 |
| e | | 0.50 BSC | | - |
| k | 0.635 | - | - | - |
| L | 0.30 | 0.40 | 0.50 | 8 |
| N | | 12 | | 2 |
| Nd | | 6 | | 3 |
| P | 0.24 | 0.42 | 0.60 | - |
| θ | - | - | 12 | - |

Rev. 0 8/03

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5M-1994.
2. N is the number of terminals.
3. Nd refer to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. COMPLIANT TO JEDEC MO-229-VGGD-2 ISSUE C except for the L dimension**.**

## Small Outline Plastic Packages (SOIC)




NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

**M8.15 (JEDEC MS-012-AA ISSUE C)**
**8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE**

| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.0532 | 0.0688 | 1.35 | 1.75 | - |
| A1 | 0.0040 | 0.0098 | 0.10 | 0.25 | - |
| B | 0.013 | 0.020 | 0.33 | 0.51 | 9 |
| C | 0.0075 | 0.0098 | 0.19 | 0.25 | - |
| D | 0.1890 | 0.1968 | 4.80 | 5.00 | 3 |
| E | 0.1497 | 0.1574 | 3.80 | 4.00 | 4 |
| e | 0.050 BSC | | 1.27 BSC | | - |
| H | 0.2284 | 0.2440 | 5.80 | 6.20 | - |
| h | 0.0099 | 0.0196 | 0.25 | 0.50 | 5 |
| L | 0.016 | 0.050 | 0.40 | 1.27 | 6 |
| N | 8 | | 8 | | 7 |
| α | 0° | 8° | 0° | 8° | - |

Rev. 1 6/05