

**SINGLE HIGH SIDE DRIVER IC**

**Features**

- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for  $V_{BS}$  and  $V_{CC}$
- 3.3 V and 5 V input logic compatible
- Tolerant to negative transient voltage
- Matched propagation delays for all channels
- RoHS compliant

**Description**

The IRS21851 is a high voltage, high speed power MOSFET and IGBT single high-side driver with propagation delay matched output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The floating logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic and can be operated up to 600 V above the ground. The output driver features a high pulse current buffer stage designed for minimum driver cross-conduction. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high-side configuration, which operates up to 600 V.

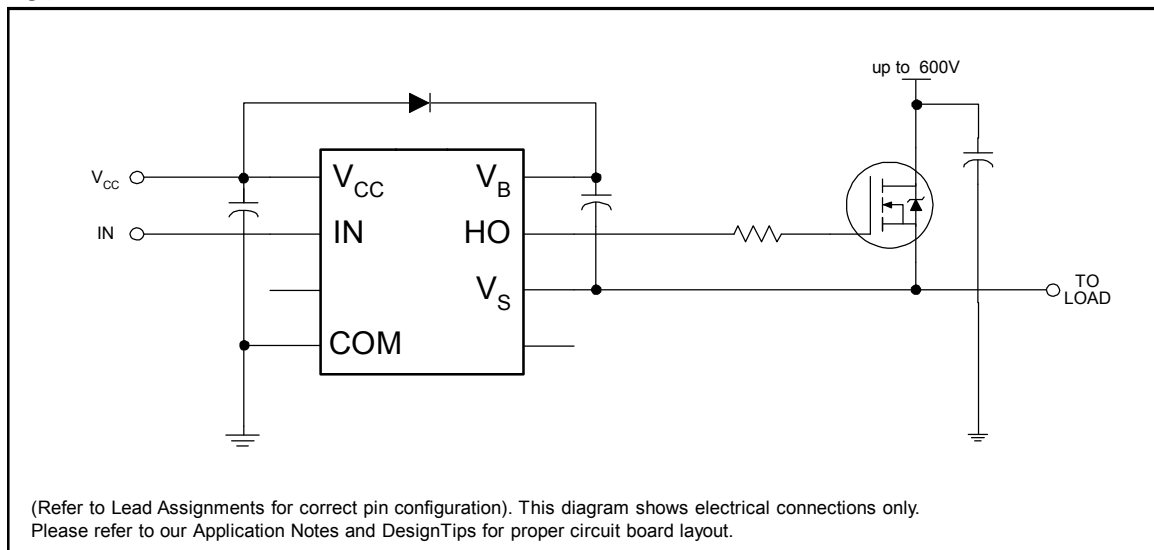
**Product Summary**

$V_{OFFSET}$	600 V max.
$I_{O+/-}$	4 A / 4 A
$V_{OUT}$	10 V - 20 V
$t_{on/off}$ (typ.)	170 ns & 170 ns

**Package**



**Typical Connection**



## Absolute Maximum Ratings

Absolute maximum ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions.

Symbol	Definition	Min.	Max.	Units
V <sub>CC</sub>	Low-side supply voltage	-0.3	20 (Note 1)	V
V <sub>IN</sub>	Logic input voltage (HIN)	COM -0.3	V <sub>CC</sub> + 0.3	
V <sub>B</sub>	High-side floating well supply voltage	-0.3	620 (Note 1)	
V <sub>S</sub>	High-side floating well supply return voltage	V <sub>B</sub> - 20	V <sub>B</sub> + 0.3	
V <sub>HO</sub>	Floating gate drive output voltage	V <sub>S</sub> - 0.3	V <sub>B</sub> + 0.3	
dV <sub>S</sub> /dt	Allowable V <sub>S</sub> offset supply transient relative to COM	—	50	V/ns
P <sub>D</sub>	Package power dissipation @ T <sub>A</sub> ≤ +25 °C	—	1.25	W
R <sub>thJA</sub>	Thermal resistance, junction to ambient	—	100	°C/W
T <sub>J</sub>	Junction temperature	-55	150	°C
T <sub>S</sub>	Storage temperature	-55	150	
T <sub>L</sub>	Lead temperature (soldering, 10 seconds)	—	300	

Note 1: All supplies are fully tested at 25 V. An internal 20 V clamp exists for each supply.

## Recommended Operating Conditions

For proper operation, the device should be used within the recommended conditions. All voltage parameters are absolute voltages referenced to COM. The offset rating are tested with supplies of (V<sub>CC</sub>-COM)=(V<sub>B</sub>-V<sub>S</sub>)=15 V.

Symbol	Definition	Min.	Max.	Units
V <sub>CC</sub>	Low-side supply voltage	10	20	V
V <sub>IN</sub>	HIN input voltage	COM	V <sub>CC</sub>	
V <sub>B</sub>	High-side floating well supply voltage	V <sub>S</sub> + 10	V <sub>S</sub> + 20	
V <sub>S</sub>	High-side floating well supply offset voltage	Note 2	600	
V <sub>HO</sub>	Floating gate drive output voltage	V <sub>S</sub>	V <sub>B</sub>	
T <sub>A</sub>	Ambient temperature	-40	125	°C

Note 2: Logic operational for V<sub>S</sub> of -5 V to 600 V. Logic state held for V<sub>S</sub> of -5 V to -V<sub>BS</sub>. (Please refer to the Design Tip DT97-3 for more details).

## Dynamic Electrical Characteristics

( $V_{CC-COM}$ )=( $V_B-V_S$ )=15 V,  $T_A = 25\text{ }^\circ\text{C}$ .  $C_L = 1000\text{ pF}$  unless otherwise specified. All parameters are referenced to COM.

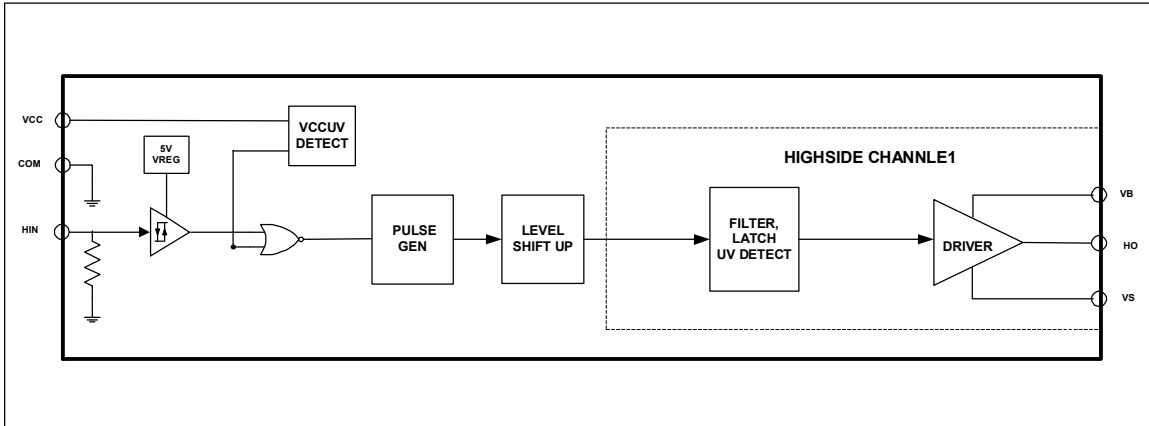
Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$t_{on}$	Turn-on propagation delay	—	160	210	ns	( $V_S - COM$ ) = 0 V
$t_{off}$	Turn-off propagation delay	—	160	210		( $V_S - COM$ ) = 600 V
$t_r$	Turn-on rise time	—	15	40		
$t_f$	Turn-off fall time	—	15	40		

## Static Electrical Characteristics

( $V_{CC-COM}$ )=( $V_B-V_S$ )=15 V. The  $V_{IN}$ ,  $V_{TH}$ , and  $I_{IN}$  parameters are referenced to COM. The  $V_O$  and  $I_O$  parameters are referenced respective  $V_S$  and are applicable to the respective output leads HO. The  $V_{CC}$  parameters are referenced to COM. The  $V_{BSUV}$  parameters are referenced to  $V_S$ .

Symbol	Definition	Min.	Typ.	Max.	Units	Test Conditions
$V_{CCUV+}$	$V_{CC}$ supply undervoltage positive going threshold	8.0	8.9	9.8	V	
$V_{CCUV-}$	$V_{CC}$ supply undervoltage negative going threshold	7.4	8.2	9.0		
$V_{BSUV+}$	$V_{BS}$ supply undervoltage positive going threshold	8.0	8.9	9.8		
$V_{BSUV-}$	$V_{BS}$ supply undervoltage negative going threshold	7.4	8.2	9.0		
$I_{LK}$	High-side floating well offset supply leakage current	—	—	50	$\mu\text{A}$	$V_B = V_S = 600\text{ V}$
$I_{QBS}$	Quiescent $V_{BS}$ supply current	—	80	150		$HIN = 0\text{ V or }5\text{ V}$
$I_{QCC}$	Quiescent $V_{CC}$ supply current	—	120	240	V	
$V_{IH}$	Logic "1" input voltage	2.5	—	—		
$V_{IL}$	Logic "0" input voltage	—	—	0.8	mV	$I_O = 2\text{ mA}$
$V_{OH, HO}$	HO high level output voltage, $V_{BIAS} - V_O$	—	20	60		
$V_{OL, HO}$	HO low level output voltage, $V_O$	—	10	30	$\mu\text{A}$	$V_{HIN} = 5\text{ V}$
$I_{IN+}$	Logic "1" input bias current	—	10	20		$V_{HIN} = 0\text{ V}$
$I_{IN-}$	Logic "0" input bias current	—	0	5	A	$V_O = 0\text{ V}, V_{IN} = 0\text{ V}$ $PW \leq 10\text{ }\mu\text{s}$
$I_{O+, HO}$	Output high short circuit pulsed current HO	—	4	—		$V_O = 15\text{ V}, V_{IN} = 15\text{ V}$ $PW \leq 10\text{ }\mu\text{s}$
$I_{O-, HO}$	Output low short circuit pulsed current HO	—	4	—		

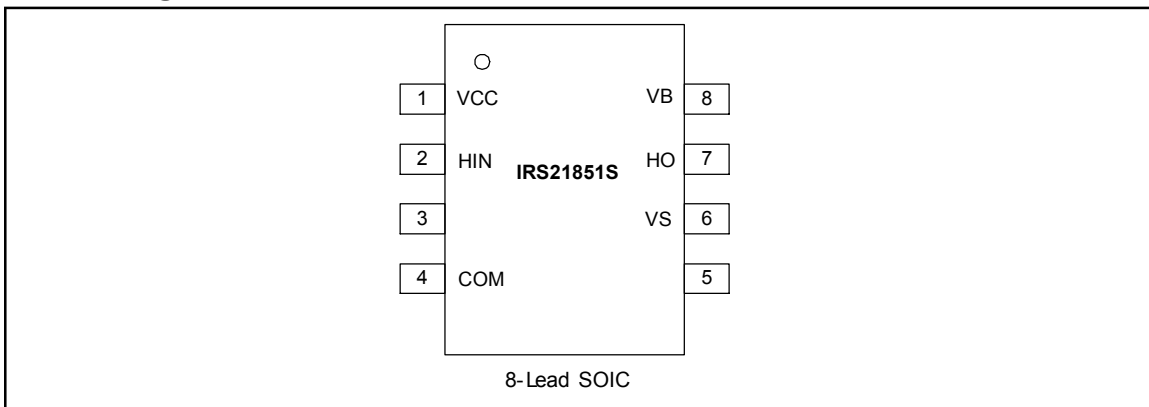
## Functional Block Diagram



## Lead Definitions

Symbol	Description
V <sub>CC</sub>	Low-side supply voltage
COM	Ground
V <sub>B</sub>	High-side drive floating supply
HO	High-side driver outputs
V <sub>S</sub>	High voltage floating supply return
HIN	Logic inputs for high-side gate driver output (in phase)

## Lead Assignments



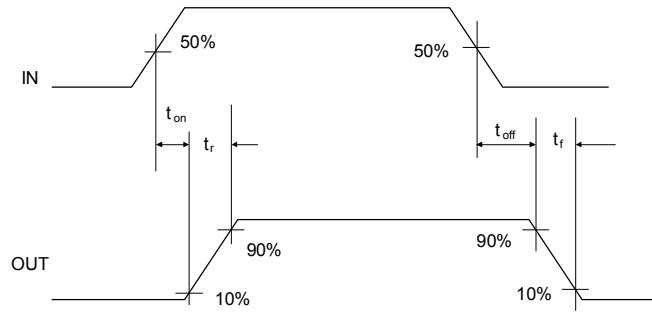


Figure 1. Switching Time Waveforms

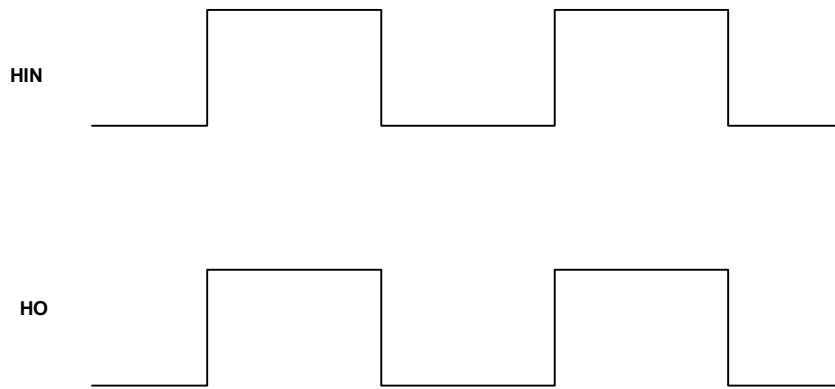
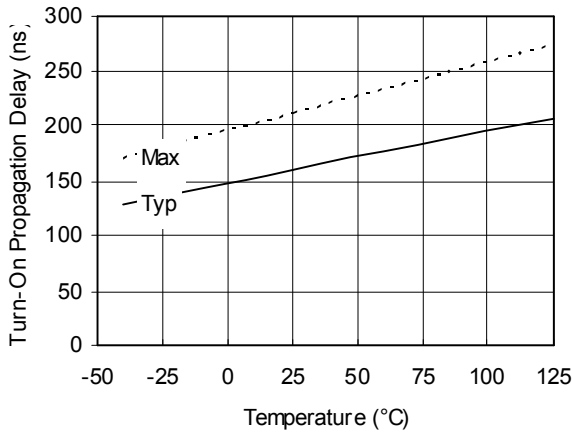
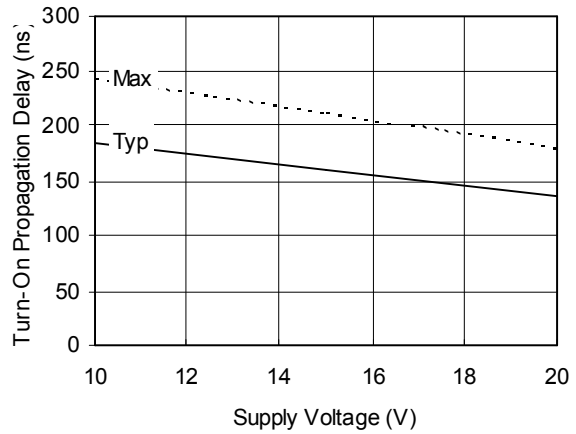


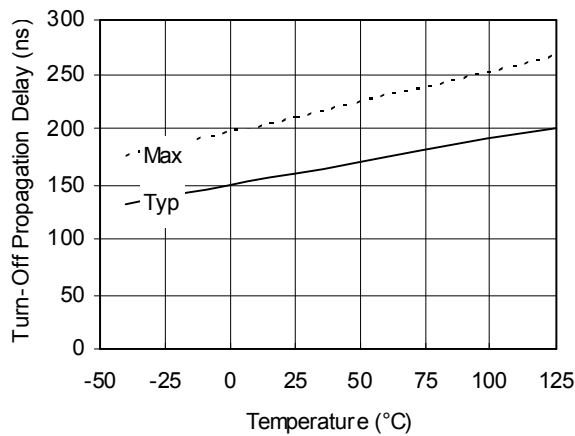
Figure 2. Input/Output Timing Diagram



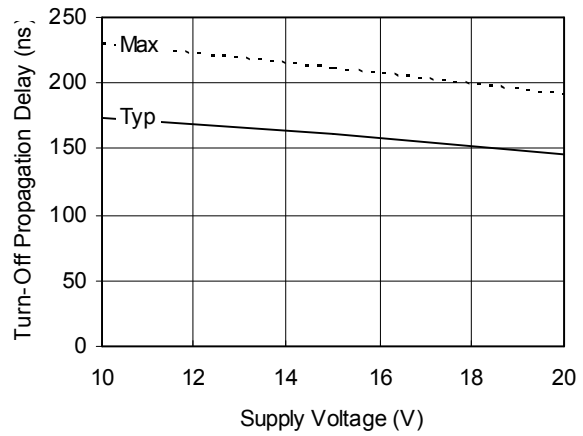
**Figure 3A. Turn-On Propagation Delay vs. Temperature**



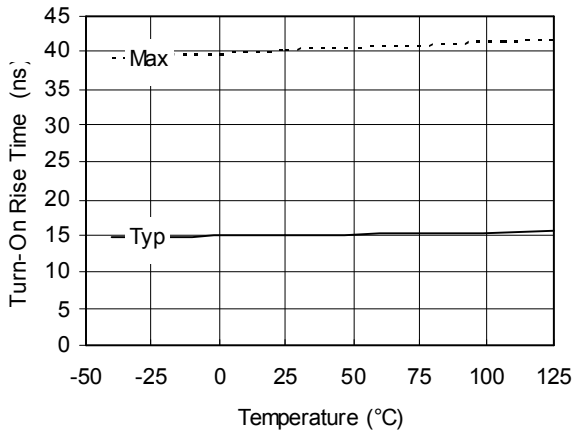
**Figure 3B. Turn-On Propagation Delay vs. Supply Voltage**



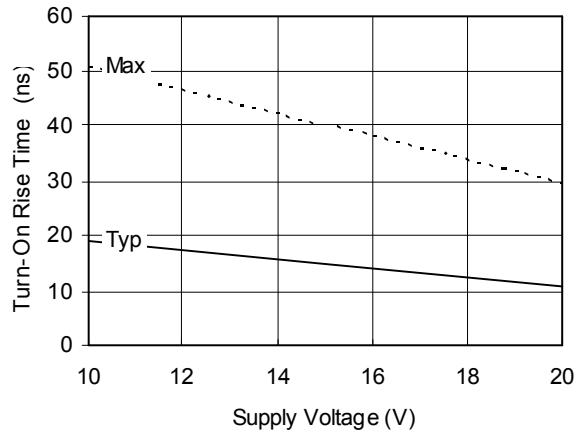
**Figure 4A. Turn-Off Propagation Delay vs. Temperature**



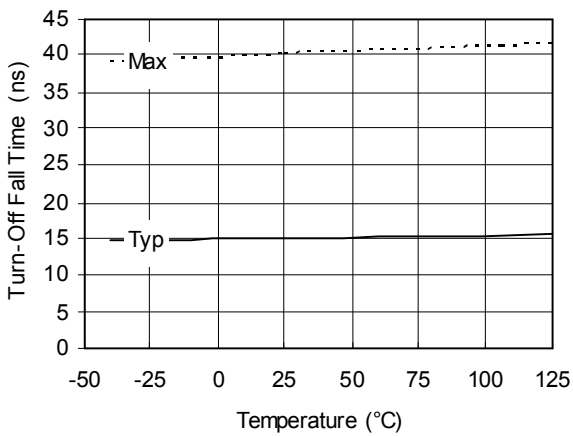
**Figure 4B. Turn-Off Propagation Delay vs. Supply Voltage**



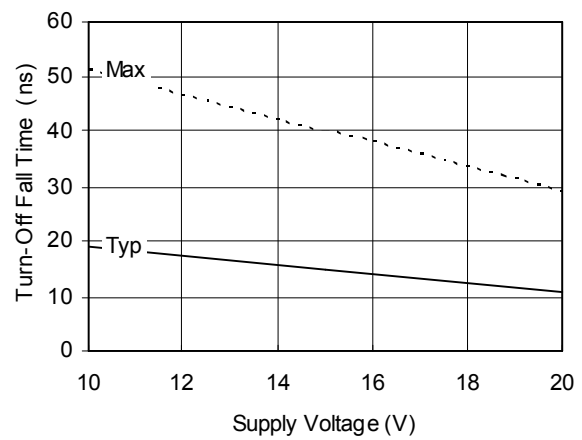
**Figure 5A. Turn-On Rise Time vs. Temperature**



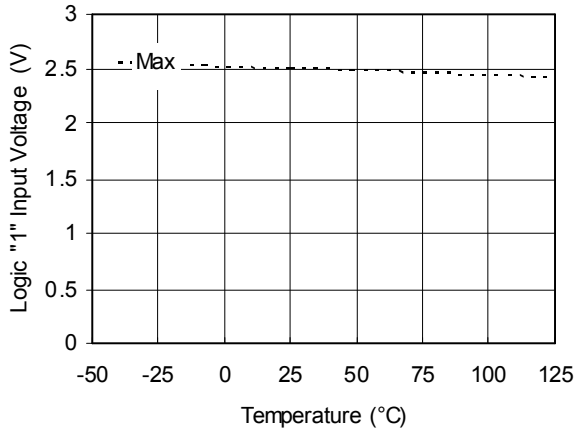
**Figure 5B. Turn-On Rise Time vs. Supply Voltage**



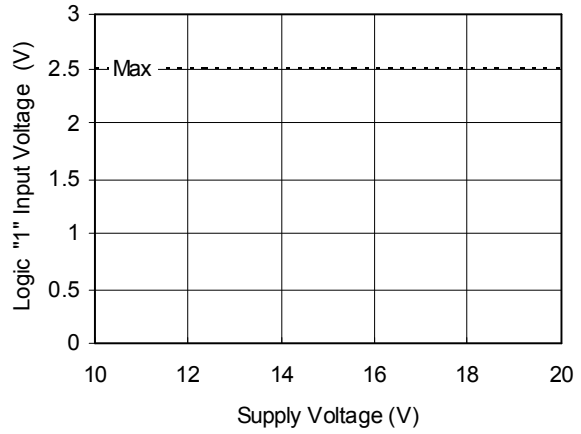
**Figure 6A. Turn-Off Fall Time vs. Temperature**



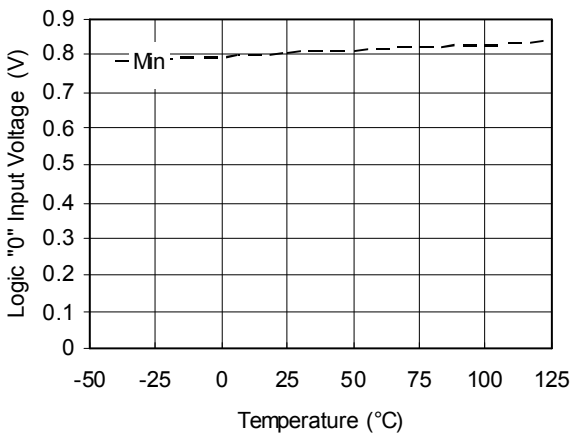
**Figure 6B. Turn-Off Fall Time vs. Supply Voltage**



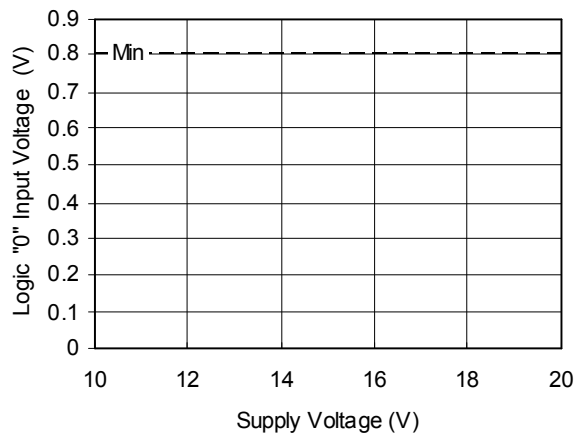
**Figure 7A. Logic "1" Input Voltage vs. Temperature**



**Figure 7B. Logic "1" Input Voltage vs. Supply Voltage**

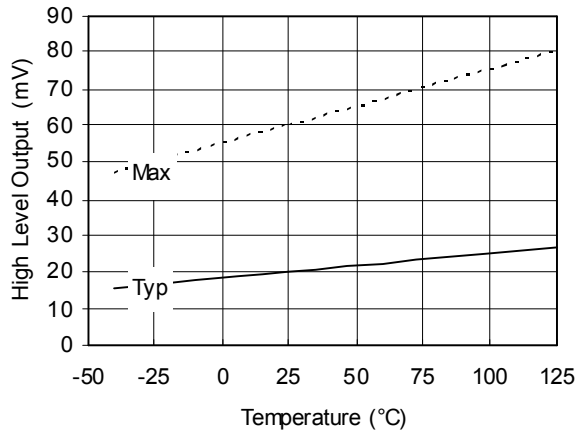


**Figure 8A. Logic "0" Input Voltage vs. Temperature**

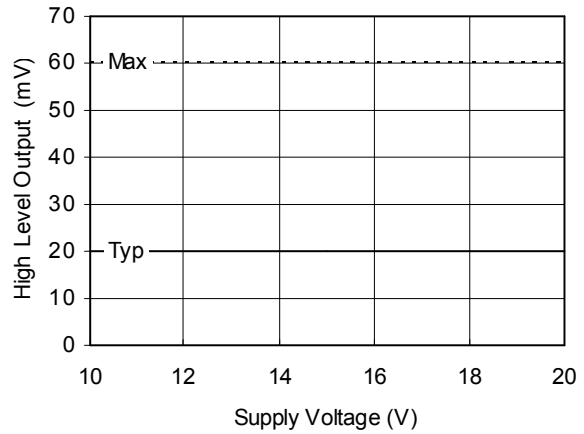


**Figure 8B. Logic "0" Input Voltage vs. Supply Voltage**

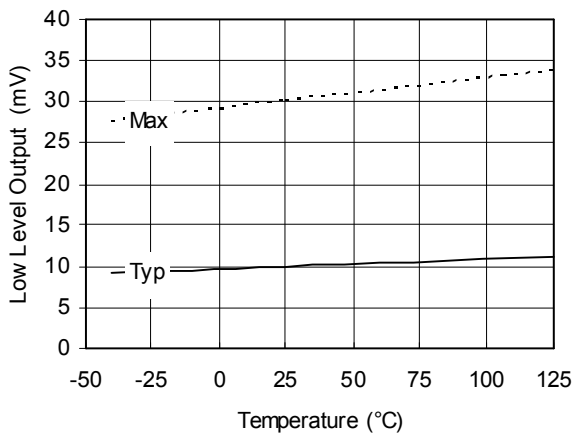




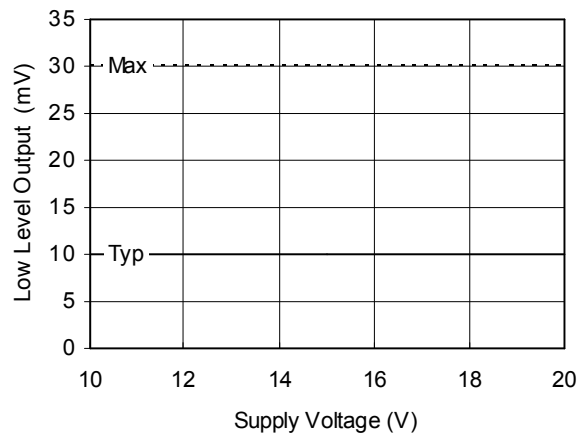
**Figure 9A. High Level Output vs. Temperature (I<sub>O</sub> = 2 mA)**



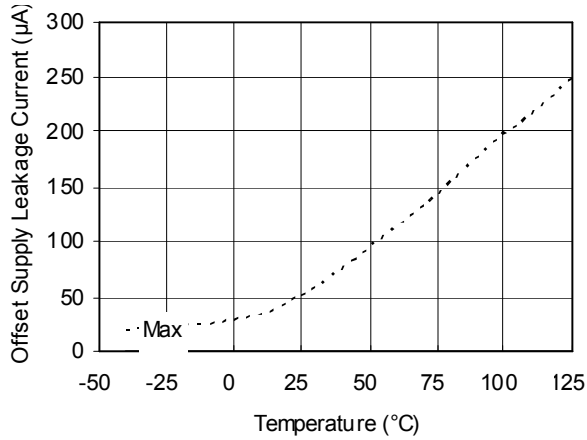
**Figure 9B. High Level Output vs. Supply Voltage (I<sub>O</sub> = 2 mA)**



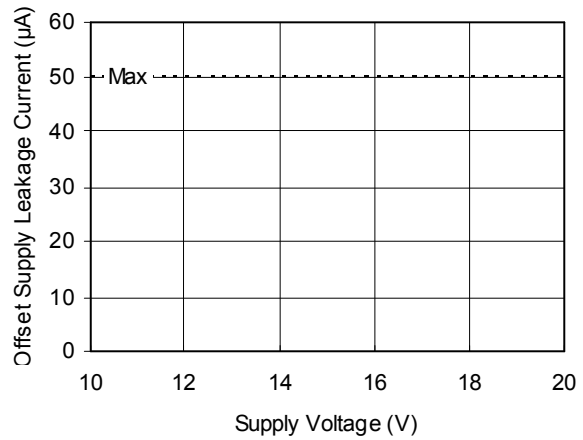
**Figure 10A. Low Level Output vs. Temperature (I<sub>O</sub> = 2 mA)**



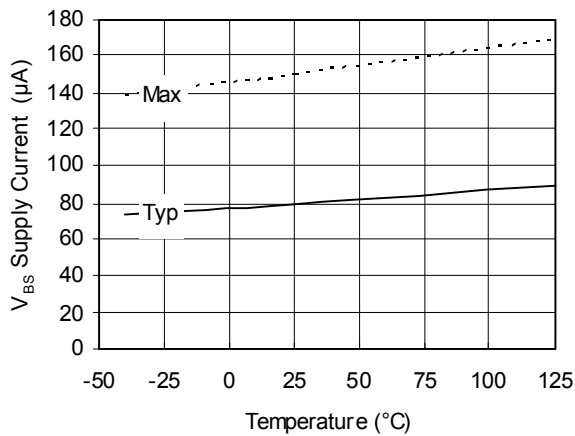
**Figure 10B. Low Level Output vs. Supply Voltage (I<sub>O</sub> = 2 mA)**



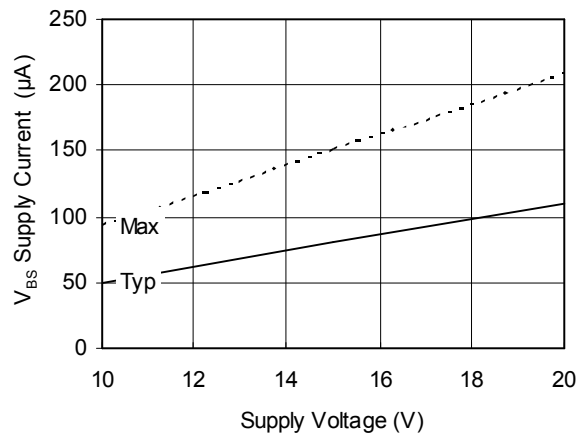
**Figure 11A. Offset Supply Leakage Current vs. Temperature**



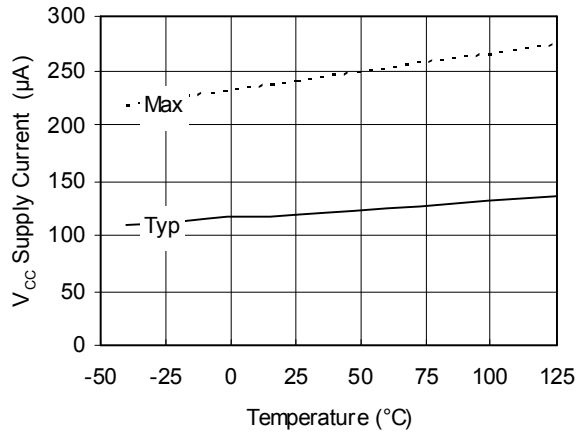
**Figure 11B. Offset Supply Leakage Current vs. Supply Voltage**



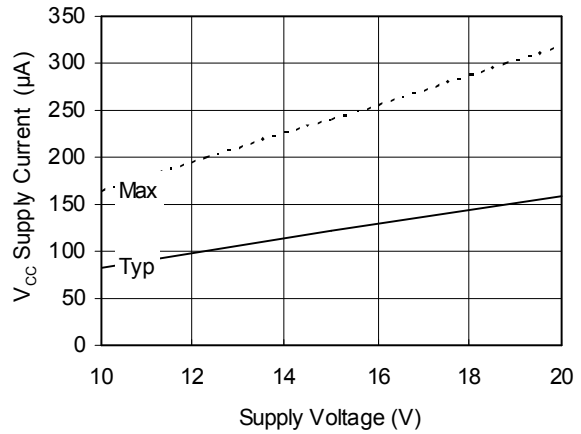
**Figure 12A. V<sub>BS</sub> Supply Current vs. Temperature**



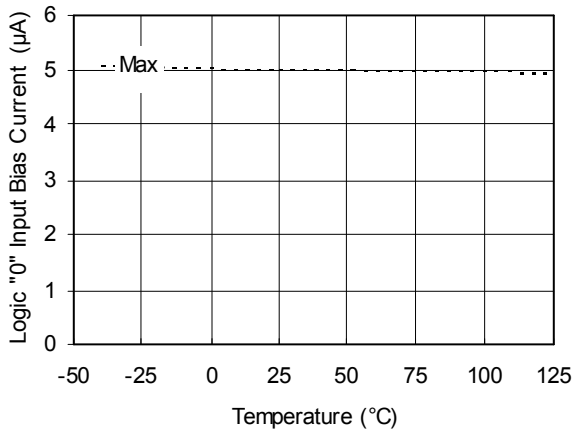
**Figure 12B. V<sub>BS</sub> Supply Current vs. Supply Voltage**



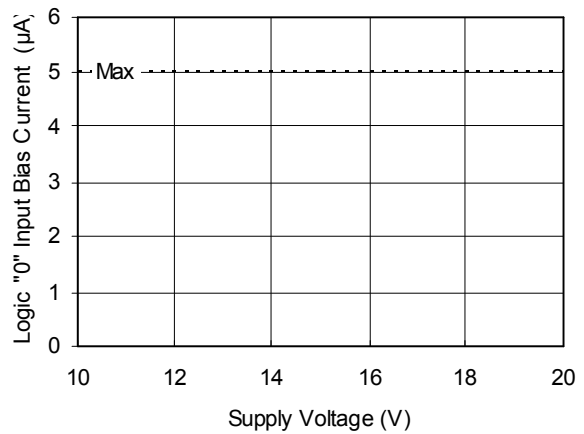
**Figure 13A. V<sub>CC</sub> Supply Current vs. Temperature**



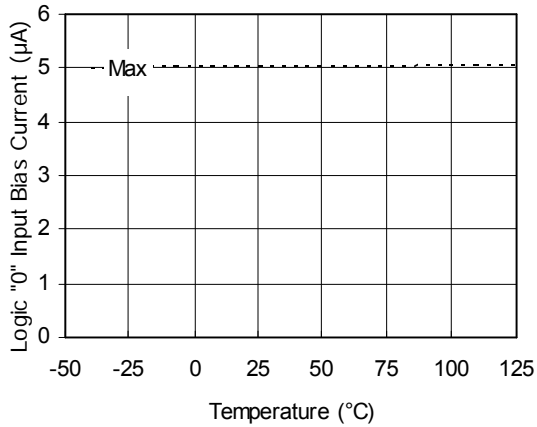
**Figure 13B. V<sub>CC</sub> Supply Current vs. Supply Voltage**



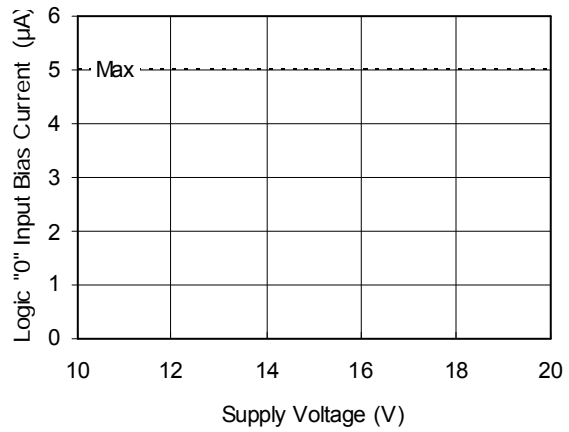
**Figure 14A. Logic "0" Input Bias Current vs. Temperature**



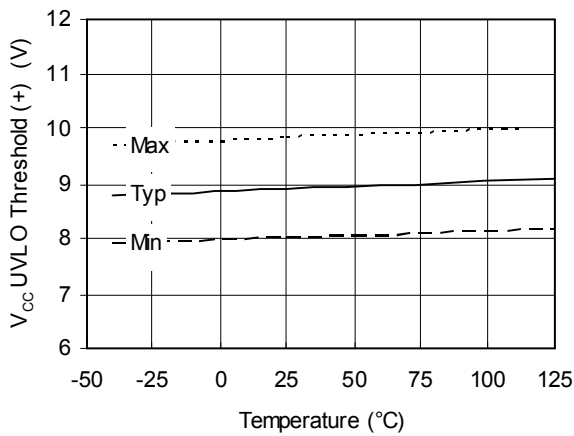
**Figure 14B. Logic "0" Input Bias Current vs. Supply Voltage**



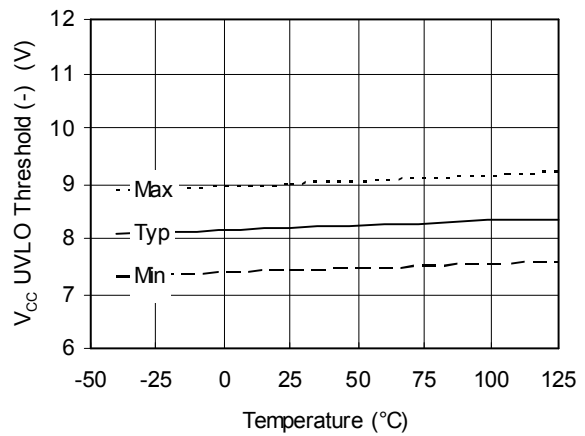
**Figure 15A. Logic "0" Input Bias Current vs. Temperature**



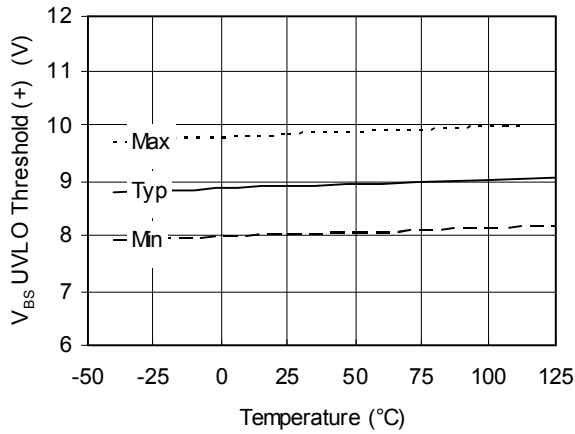
**Figure 15B. Logic "0" Input Bias Current vs. Voltage**



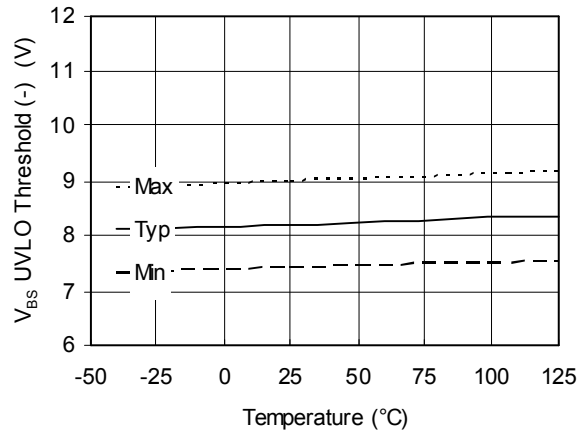
**Figure 16. V<sub>CC</sub> Undervoltage Threshold (+) vs. Temperature**



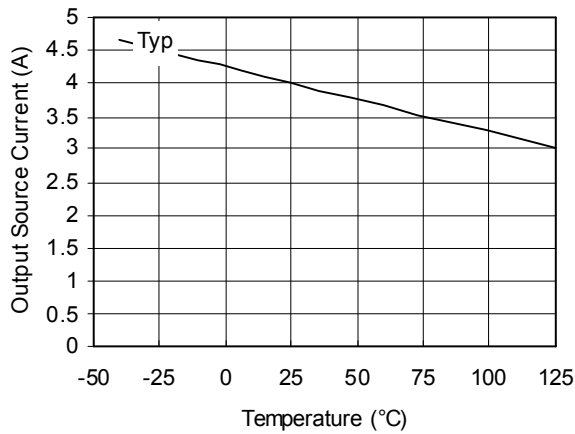
**Figure 17. V<sub>CC</sub> Undervoltage Threshold (-) vs. Temperature**



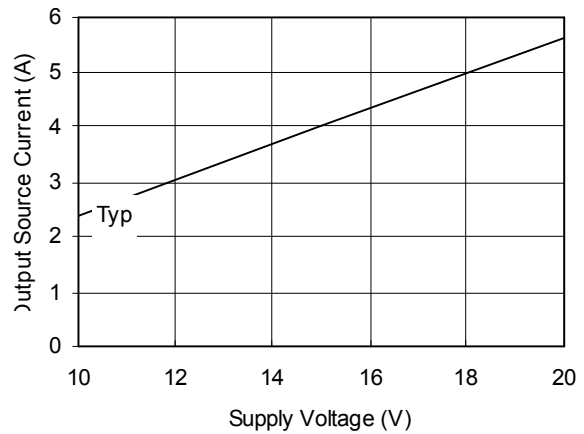
**Figure 18.  $V_{BS}$  Undervoltage Threshold (+) vs. Temperature**



**Figure 19.  $V_{BS}$  Undervoltage Threshold (-) vs. Temperature**



**Figure 20A. Output Source Current vs. Temperature**



**Figure 20B. Output Source Current vs. Supply Voltage**

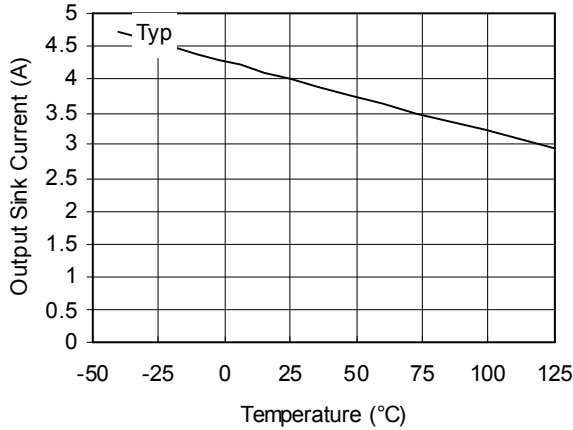


Figure 21A. Output Sink Current vs. Temperature

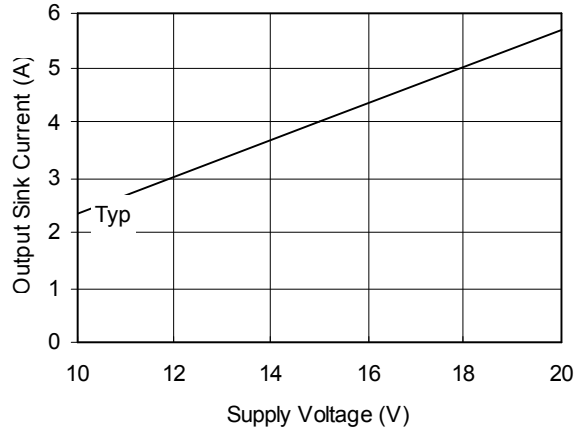


Figure 21B. Output Sink Current vs. Supply Voltage

Case outline

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e 1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°

NOTES:

- DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
- CONTROLLING DIMENSION: MILLIMETER
- DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
- OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA.

⑤ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 [0.06].

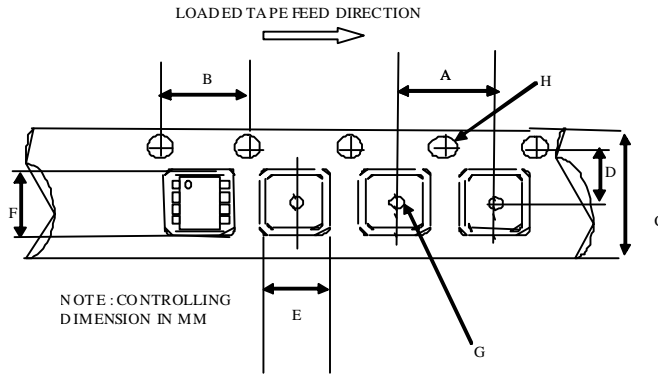
⑥ DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 [0.10].

⑦ DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

01-6027

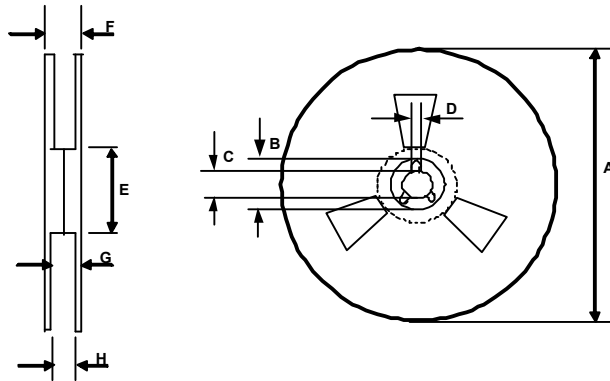
8-Lead SOIC

**Tape & Reel  
 8-lead SOIC**



CARRIER TAPE DIMENSION FOR 8SOICN

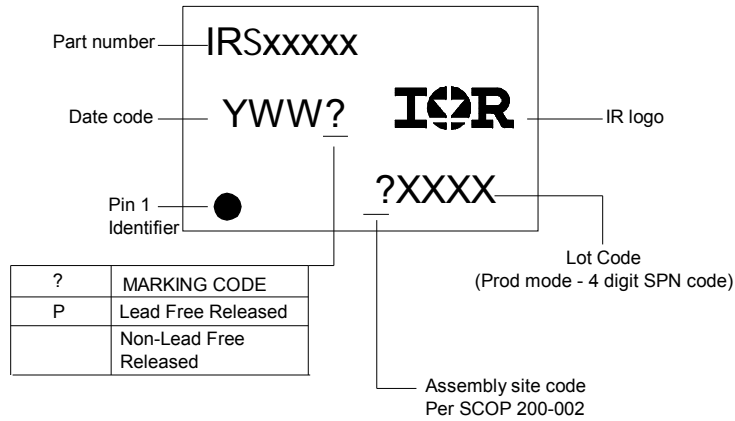
Code	Metric		Imperial	
	Min	Max	Min	Max
A	7.90	8.10	0.311	0.318
B	3.90	4.10	0.153	0.161
C	11.70	12.30	0.46	0.484
D	5.45	5.55	0.214	0.218
E	6.30	6.50	0.248	0.255
F	5.10	5.30	0.200	0.208
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 8SOICN

Code	Metric		Imperial	
	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	18.40	n/a	0.724
G	14.50	17.10	0.570	0.673
H	12.40	14.40	0.488	0.566

**LEADFREE PART MARKING INFORMATION**



**ORDER INFORMATION**

8-Lead SOIC order IRS21851SPbF  
 8-Lead SOIC Tape & Reel IRS21851STRPbF