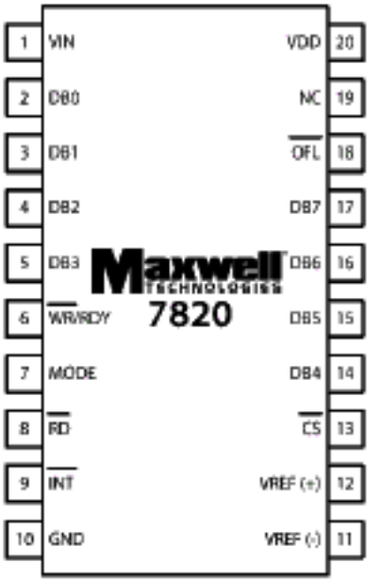
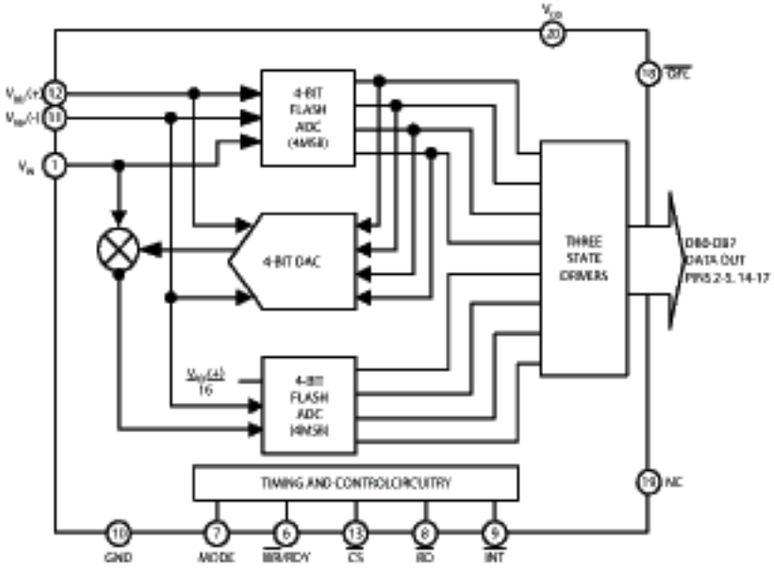
7820
Microprocessor-compatible 8-Bit ADC





Logic Diagram

FEATURES:

- 1.36 µs Conversion Time
- Built-in-Track-and-Hold Function
- Single +5 Volt Supply
- No External Clock Required
- Tri-State Output Buffered
- Total Ionization Dose:
  - > 50 krads (Si), depending upon space mission.
- Excellent Single Event Effects
  - SEL > 80 MeV/mg/cm^2
- Package:
  - 20 pin Rad-Pak DIP

DESCRIPTION:

The 7820 is a microprocessor compatible 8-bit Analog-to-Digital Converter with a 0V to +5V input supply range with a single +5 Volt supply.

The 7820 incorporates internal sample-and-hold circuitry which eliminates the need for an external S/H for signals with slew rates less than 100 mV/µs.

The 7820 was designed to be easiliy interfaced with microprocessors, appearing as either a memory location or I/O port without the need for external interfacing. All outputs are latched and tri-state buffered.

Maxwell Technologies' patented RAD-PAK® packaging technology incorporates radiation shielding in the microcircuit package. It eliminates the need for box shielding while providing the required radiation shielding for a lifetime in orbit or space mission. In a GEO orbit, the RAD-PAK®package provides greater than 50 krad (Si) radiation dose tolerance. This product is available with screening up to Class S.

(858) 503-3300 - Fax: (858) 503-3301 - www.maxwell.com

TABLE 1. PIN DESCRIPTION

PIN	SYMBOL	DESCRIPTION
1	V_{IN}	Analog Input Range: $V_{REF(-)}$ to $V_{REF(+)}$.
2	DB0	Data Output. Three State Output, bit 0 (LSB)
3	DB1	Data Output. Three State Output, bit 1
4	DB2	Data Output. Three State Output, bit 2
5	DB3	Data Output. Three State Output, bit 3
6	$\overline{WR}$/RDY	WRITE control input/READY status output.
7	Mode	Mode Selection Input. It determines whether the device operates in the WR-RD or RD mode. It is internally tied to GND through a 50 µA current source.
8	$\overline{RD}$	READ Input. $\overline{RD}$ must be low to access data from the part.
9	$\overline{INT}$	INTERUPT Output. $\overline{INT}$ going low indicates that the conversion is complete $\overline{INT}$ returns high on rising the edge of $\overline{RD}$ or $\overline{CS}$.
10	GND	Ground
11	V_{REF-}	Lower limit of reference span. Range: GND ≤ $V_{REF(-)}$ ≤ $V_{REF(+)}$
12	V_{REF+}	Upper limit of reference span. Range: GND ≤ $V_{REF(-)}$ ≤ $V_{REF(+)}$ ≤ V_{DD}
13	$\overline{CS}$	Chip Select Input. $\overline{CS}$, the decoded device address, must be low for $\overline{RD}$ or $\overline{WR}$ to be recognized by the converter.
14	DB4	Data Output. Three State Output, bit 4
15	DB5	Data Output. Three State Output, bit 5
16	DB6	Data Output. Three State Output, bit 6
17	DB7	Data Output. Three State Output, bit 7 (MSB)
18	$\overline{OFL}$	Overflow Output. If the analog input is higher than ($V_{REF(+)}$ - 1/2LSB), OFL will be low at the end of conversion. It is a non three state output which can be used to cascade 2 or more devices to increase resolution.
19	NC	No Connection.
20	V_{DD}	Power supply voltage, +5V

TABLE 2. 7820 ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	MIN	MAX	UNIT
V_{DD} to GND	-0	7.0	V
Digital Input Voltage to GND (Pins 6-80, 13)	-0.3	V_{DD} +0.3	V
Digital Output Voltage to GND (Pins 2-5, 9, 14-18)	0.3	V_{DD} +0.3	V
V_{REF} (+) to GND	0	V_{DD} +0.3	V
V_{REF} (-) to GND	V_{SS} -0.3	V_{REF} (+)	V

TABLE 2. 7820 ABSOLUTE MAXIMUM RATINGS[1]

PARAMETER	MIN	MAX	UNIT
V_{IN} to GND	-0.3	V_{DD} +0.3	V
Operating Temperature	-55	125	°C
Storage Temperature Range	-65	150	°C
Power Dissipation to 75°C	--	450	mW
Derates above +75°C	--	6	mW/°C

1. **CAUTION**: ESD (electrostatic discharge) sensitive device. The digital control inputs are diode protected; however, permanent damage may occur on unconnected devices subject to high energy electrostatic fields. Unused devices must be stored in conductive foam or shunts. The protective foam should be discharged to the destination socket before devices are inserted.

TABLE 3. 7820 DC ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V; V_{REF}(+) = +5V; V_{REF}(-) = GND = 0V, UNLESS OTHERWISE SPECIFIED) (RD MODE (PIN 7 = 0V))
(T_A = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	TEST CONDITIONS	SUBGROUPS	MIN	TYP	MAX	UNIT
Accuracy						
Resolution	--		8	--	--	Bits
Total Unadjusted Error[1]	--		--	--	±1.0	LSB
Minimum Resolution for which No Missing Codes are Guaranteed	--		--	--	8	Bits
Reference Input						
Input Resisitance	--	1, 2, 3	1.0	--	4.0	kΩ
V_{REF} (+) Input Voltage Range	--	1, 2, 3	V_{REF}(-)	--	V_{DD}	V
V_{REF} (-) Input Voltage Range	--	1, 2, 3	GND	--	V_{REF}(+)	V
Analog Input						
Input Voltage Range	--	1, 2, 3	V_{REF}(-)	--	V_{REF}(+)	V
Input Leakage Current	--	1, 2, 3	--	--	±3	µA
Input Capacitance[2]	--	1, 2, 3	--	45	--	pF
Logic Inputs						
$\overline{CS}$, $\overline{WR}$, $\overline{RD}$						
V_{INH}	--	1, 2, 3	2.4	--	--	V
V_{INH}	--	1, 2, 3	--	--	0.8	V
I_{INH}($\overline{CS}$, $\overline{RD}$)	--	1, 2, 3	--	--	1	µA
I_{INH}($\overline{WR}$)	--	1, 2, 3	--	--	3	µA
I_{INL}($\overline{WR}$)	--	1, 2, 3	--	--	-1	µA
Input Capacitance[2]	--	1, 2, 3	--	5	8	pF

TABLE 3. 7820 DC ELECTRICAL CHARACTERISTICS

(V_{DD} = +5V; $V_{REF}(+)$ = +5V; $V_{REF}(-)$ = GND = 0V, UNLESS OTHERWISE SPECIFIED) (RD MODE (P_{IN} 7 = 0V))
(T_A = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	TEST CONDITIONS	SUBGROUPS	MIN	TYP	MAX	UNIT
Mode						
V_{INH}	--	1, 2, 3	3.5	--	--	V
I_{INH}	--	1, 2, 3	--	--	200	µA
I_{INL}	--	1, 2, 3	--	--	-1	µA
Input Capacitance[2]	--	1, 2, 3	--	5	8	pF
Logic Outputs $\overline{\text{DB0-DB7}}$, $\overline{\text{OFL}}$, $\overline{\text{INT}}$						
V_{OH}	ISOURCE = 360 µA	1, 2, 3	4	--	--	V
V_{OL}	ISINK = 1.6 mA	1, 2, 3	--	--	0.4	V
I_{OUT}(DB0-DB7)	Floating State Leakage	1, 2, 3	--	--	±3	µA
Output Capacitance[2]	--	1, 2, 3	--	5	8	pF
RDY						
V_{OL}	ISINK = 2.6mA	1, 2, 3	--	--	0.4	V
I_{OUT}	Floating State Leakage	1, 2, 3	--	--	±3	V
Output Capacitance[2]	--	4, 5, 6	--	5	8	pF
Slew Rate, Tracking[2]	--	1, 2, 3	--	0.2	0.1	V/µs
Power Supply						
V_{DD}	±5% for specified performance	1, 2, 3	--	--	5	V
I_{DD}	$\overline{CS}$ = $\overline{RD}$ = $\overline{OV}$	1, 2, 3	--	--	20	mA
Power Dissipation	--	1, 2, 3	--	40	--	mW
Power Supply Sensitivity	VDD = 5V ±5%	1, 2, 3	--	±1/16	±1/4	LSB

1. Total unadjusted error includes offset, full scale and linearity error.
2. Guarenteed by design.

TABLE 4. 7820 AC ELECTRICAL CHARACTERISTICS[1]

(V_{DD} = +5V; $V_{REF}(+)$ = +5V; $V_{REF}(-)$ = GND = 0V, UNLESS OTHERWISE SPECIFIED) (RD MODE (P_{IN} 7 = 0V))

(T_A = -55 TO 125 °C UNLESS OTHERWISE SPECIFIED)

PARAMETER	SUBGROUPS	SYMBOL	MIN	MAX	UNIT
$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ Setup Time	9, 10, 11	t_{CSS}	0	--	ns
$\overline{CS}$ to $\overline{RD}$/$\overline{WR}$ Hold Time	9, 10, 11	t_{CSH}	0	--	ns
$\overline{CS}$ to Delay Time (Pull-up Resistor = 5kΩ	9, 10, 11	t_{RDY}	--	100	ns
Conversion Time (RD Mode)	9, 10, 11	t_{CRD}	--	2.5	µs
Data Access Time (RD Mode)	9, 10, 11	t_{ACCD}	--	t_{CRD} + 50	ns
$\overline{RD}$ to $\overline{INT}$ Delay (RD Mode)	9, 10, 11	t_{INTH}	--	225	ns
Data Hold Time	9, 10, 11	t_{DH}	--	100	ns
Delay Time Between Conversions	9, 10, 11	t_p	600	--	ns
Write Pulse Width	9, 10, 11	t_{WR}	600	--	ns
			--	50	µs
Delay Time Between WR and RD Pulses	9, 10, 11	t_{RD}	700	--	ns
Data Access Time (WR-RD Mode)	9, 10, 11	t_{ACC1}	--	250	ns
RD to INT Delay	9, 10, 11	t_{R1}	--	225	ns
WR to INT Delay	9, 10, 11	t_{INTL}	--	1700	ns
Data Access Time (WR-RD Mode)	9, 10, 11	t_{ACC2}	--	110	ns
WR to INT Delay (Stand-Alone Operation)	9, 10, 11	t_{IHWR}	--	150	ns
Data Access Time After INT (Stand-Alone Operation	9, 10, 11	t_{ID}	--	75	ns

1. Sample tested at 25°C to ensure compliance. Only on process design change.

FIGURE 1. LOAD CIRCUITS FOR DATA ACCESS TIME TEST

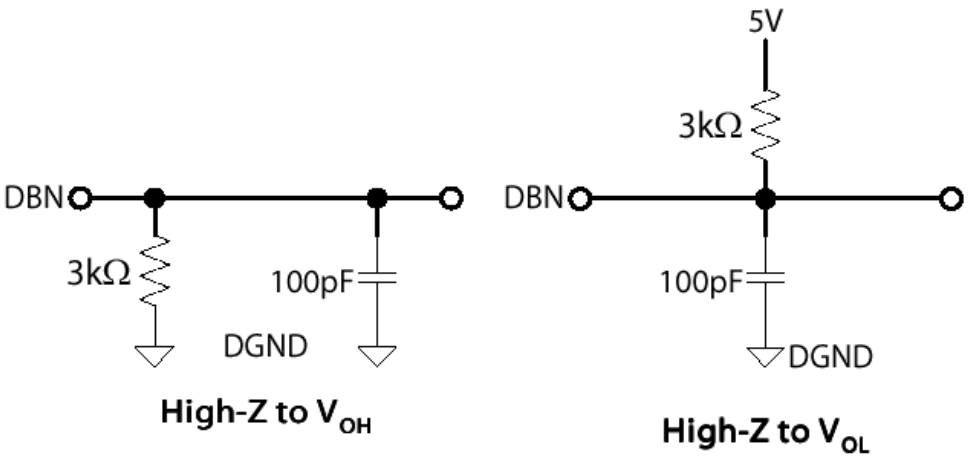


FIGURE 2. LOAD CIRCUITS FOR DATA HOLD TIME RESET

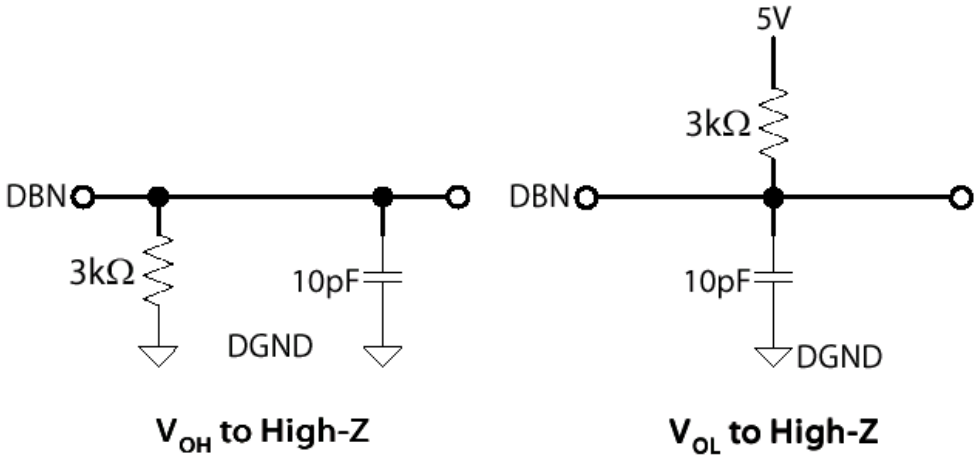


FIGURE 3. LOAD CIRCUIT FOR ACCESS TIME

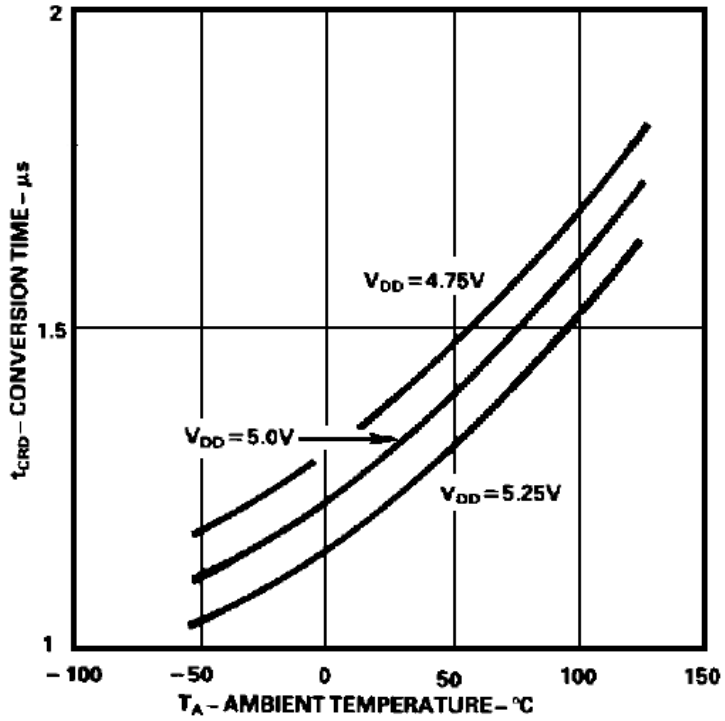


FIGURE 4. LOAD CIRCUIT FOR OUTPUT FLOAT DELAY

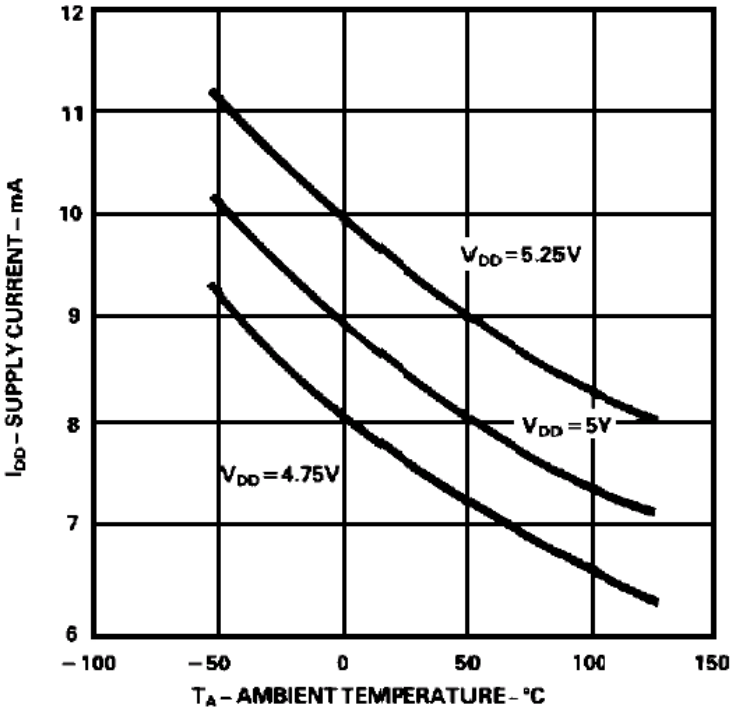


FIGURE 5. ACCURACY VS. T_{WR}

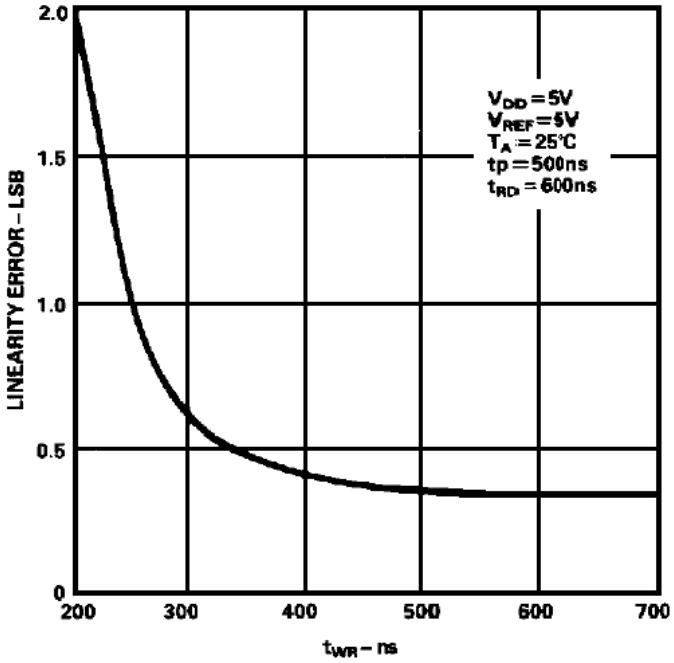


FIGURE 6. ACCURACY VS. T_{RD}

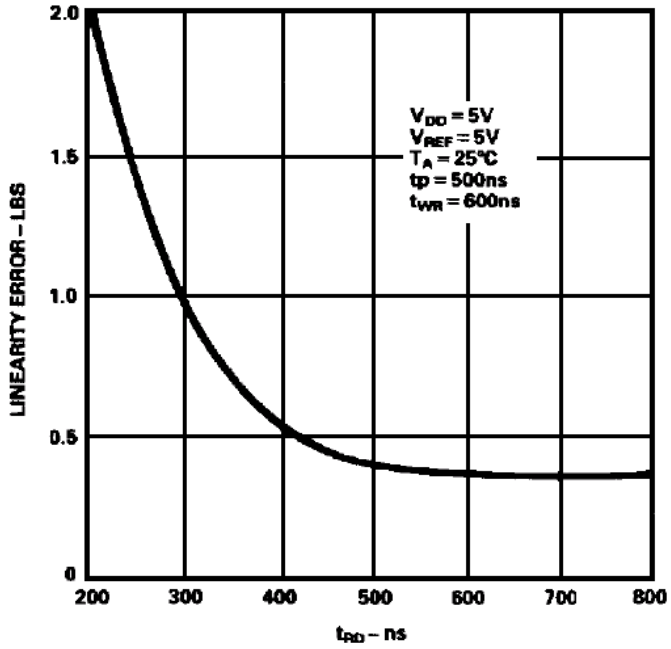


FIGURE 7. ACCURACY VS. T_{SP}

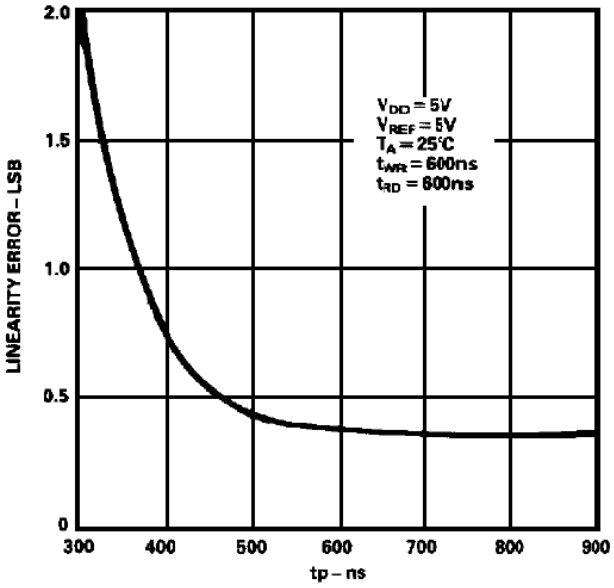


FIGURE 8. ACCURACY VS. T_{REF} [$V_{REF} = V_{REF}(+) - V_{REF}(-)$]

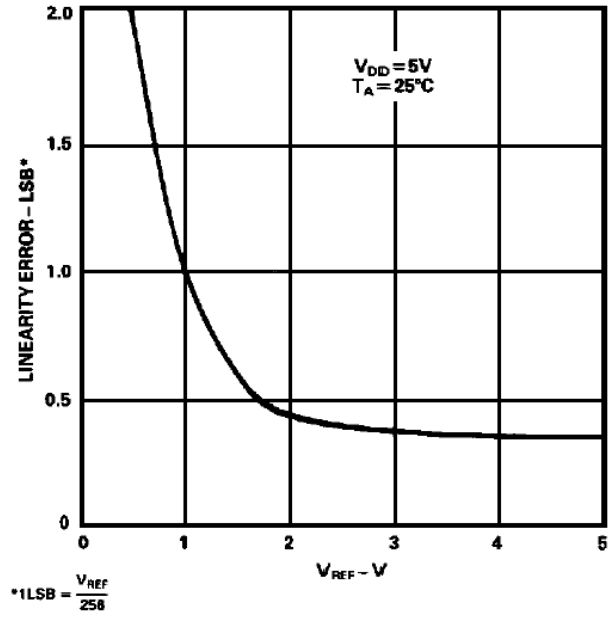


FIGURE 9. SIGNAL-NOISE RATIO VS. INPUT FREQUENCY

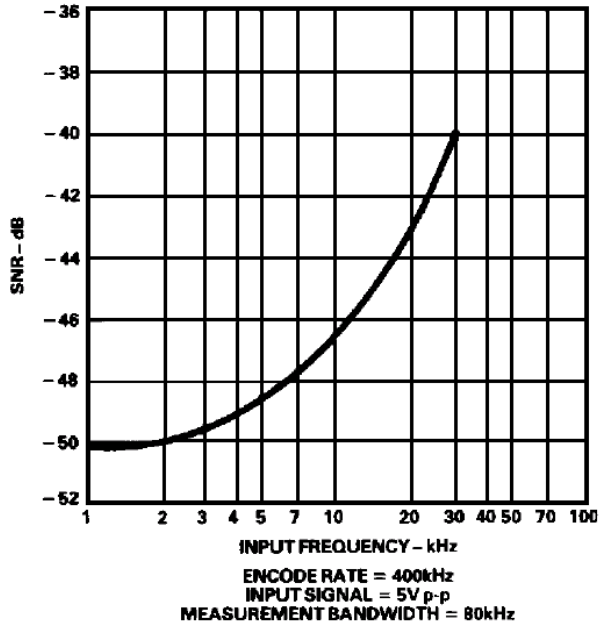


FIGURE 10. T_{INTL} INTERNAL TIME DELAY VS. TEMPERATURE

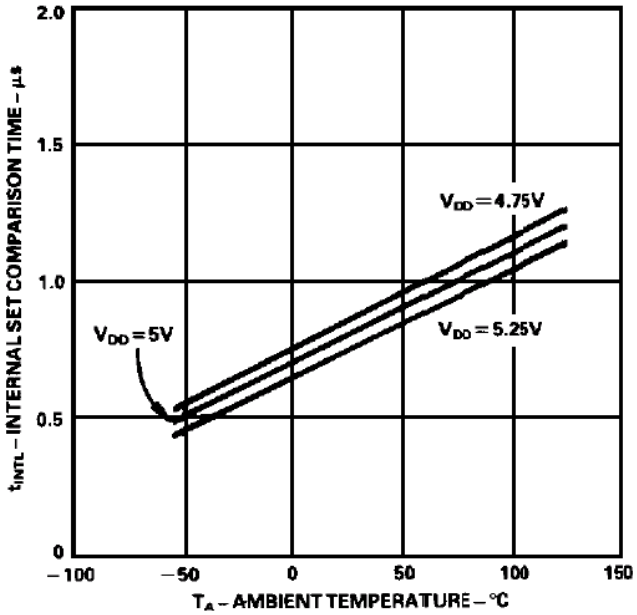


FIGURE 11. OUTPUT CURRENT VS. TEMPERATURE

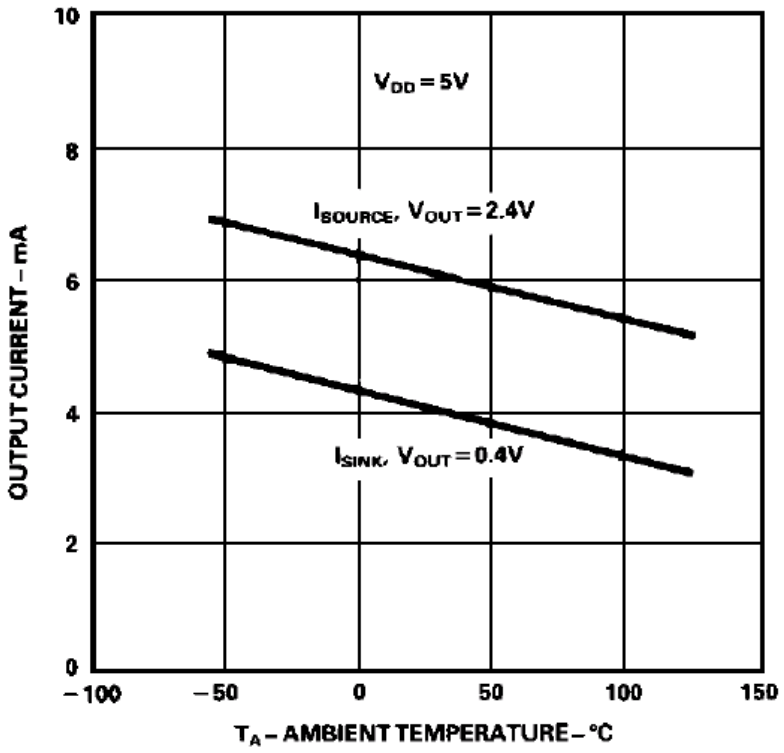


FIGURE 12. OPERATING SEQUENCE (WR-RD MODE)

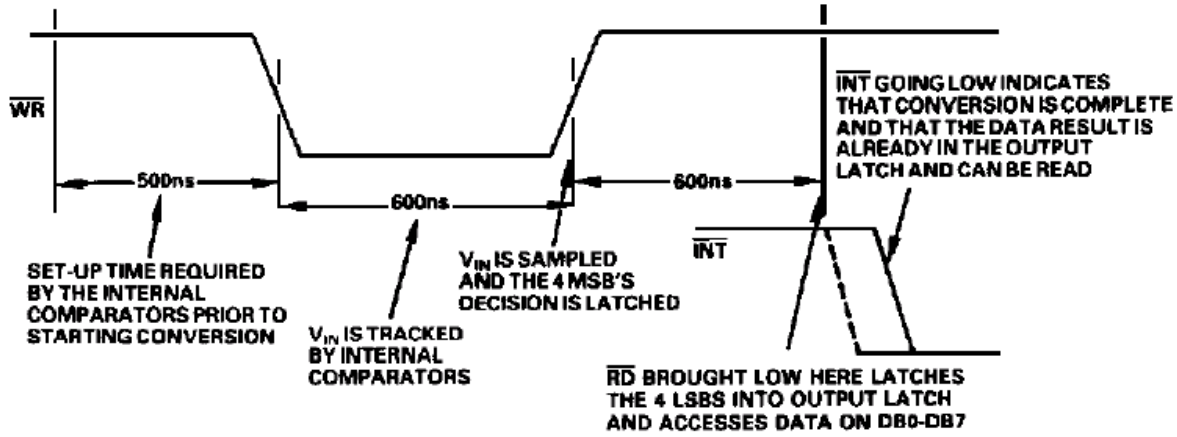


FIGURE 13. RD MODE

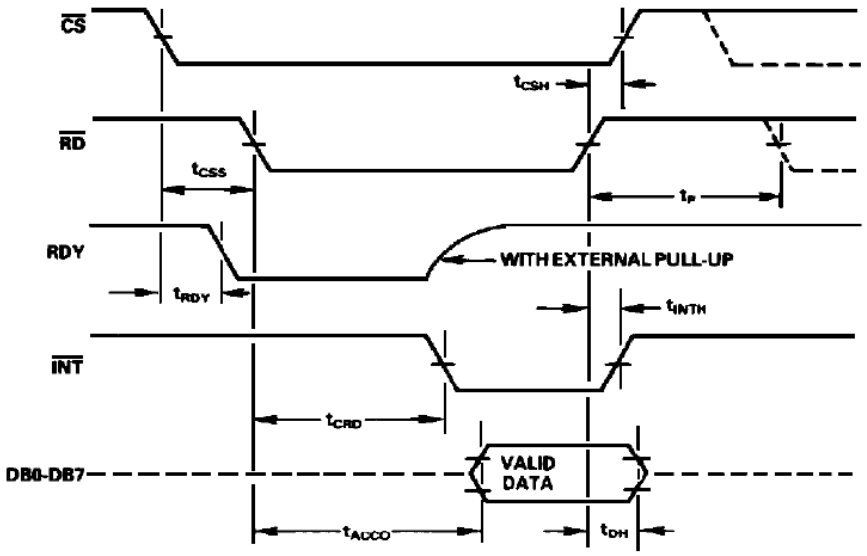


FIGURE 14. WR-RD MODE (TRD>TINTL)

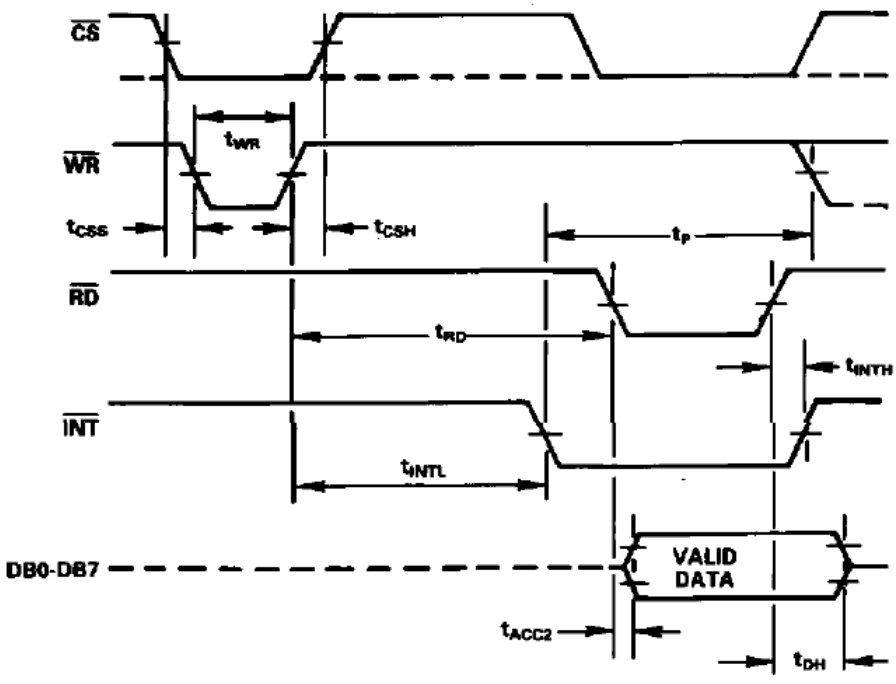


FIGURE 15. WR-RD MODE (T_{RD}<T_{INTL})

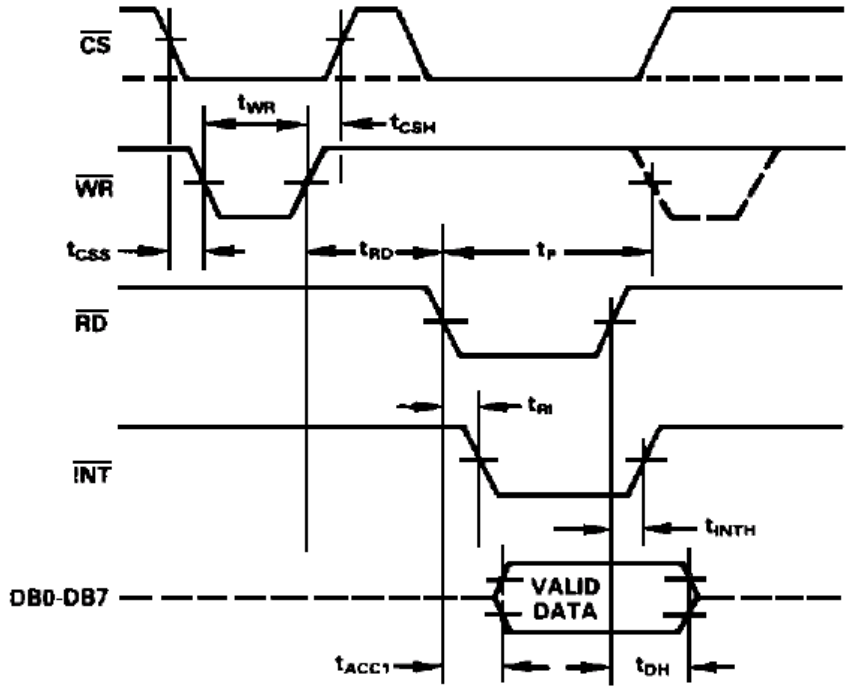


FIGURE 16. WR-RD MODE STAND-ALONE OPERATION ($\overline{CS}$=$\overline{RD}$=0)

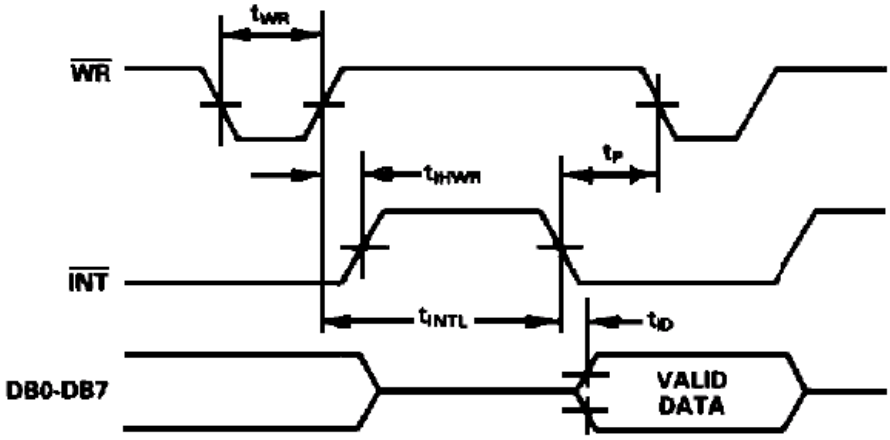


FIGURE 17. POWER SUPPLY AS REFERENCE

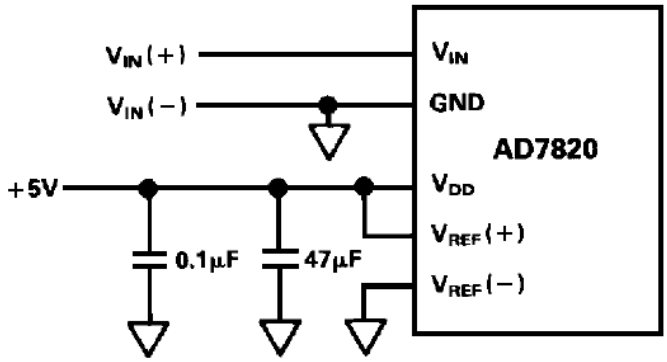


FIGURE 18. INPUT NOT REFERENCED TO GND

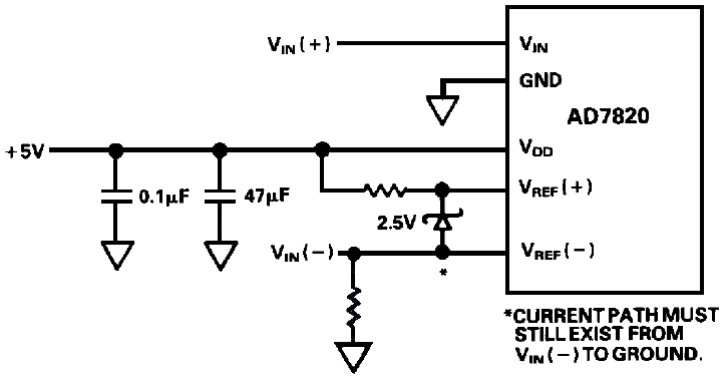


FIGURE 19. EQUIVALENT INPUT CIRCUIT

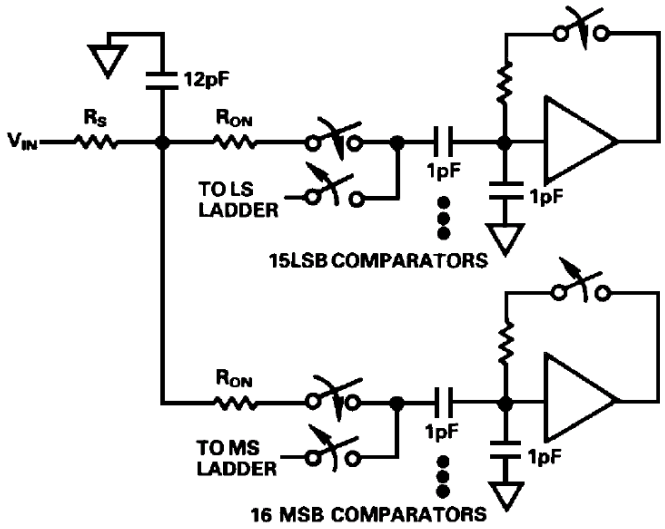
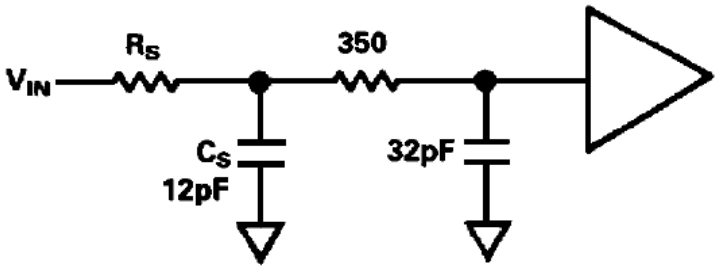
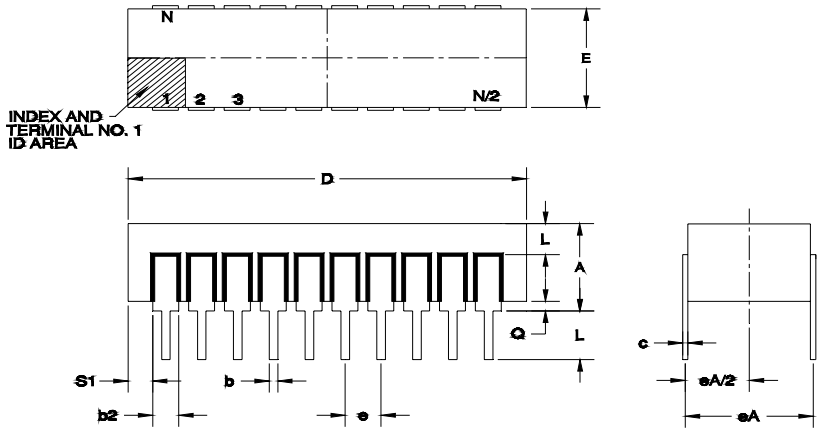


FIGURE 20. RC NETWORK MODEL





20 PIN RAD-PAK® DUAL IN LINE PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	--	0.202	0.230
b	0.014	0.018	0.026
b2	0.045	0.050	0.065
c	0.008	0.010	0.018
D	--	1.000	1.060
E	0.220	0.295	0.310
eA	0.300 BSC		
eA/2	0.150 BSC		
e	0.100 BSC		
L	0.135	0.145	0.155
Q	0.015	0.045	0.070
S1	0.005	0.025	--
S2	0.005	--	--
N	20		

Note: All dimensions in inches

Important Notice:

These data sheets are created using the chip manufacturer's published specifications. Maxwell Technologies verifies functionality by testing key parameters either by 100% testing, sample testing or characterization.

The specifications presented within these data sheets represent the latest and most accurate information available to date. However, these specifications are subject to change without notice and Maxwell Technologies assumes no responsibility for the use of this information.

Maxwell Technologies' products are not authorized for use as critical components in life support devices or systems without express written approval from Maxwell Technologies.

Any claim against Maxwell Technologies must be made within 90 days from the date of shipment from Maxwell Technologies. Maxwell Technologies' liability shall be limited to replacement of defective parts.

Product Ordering Options