APPLIED MICRO CIRCUITS CORPORATION

Ohio

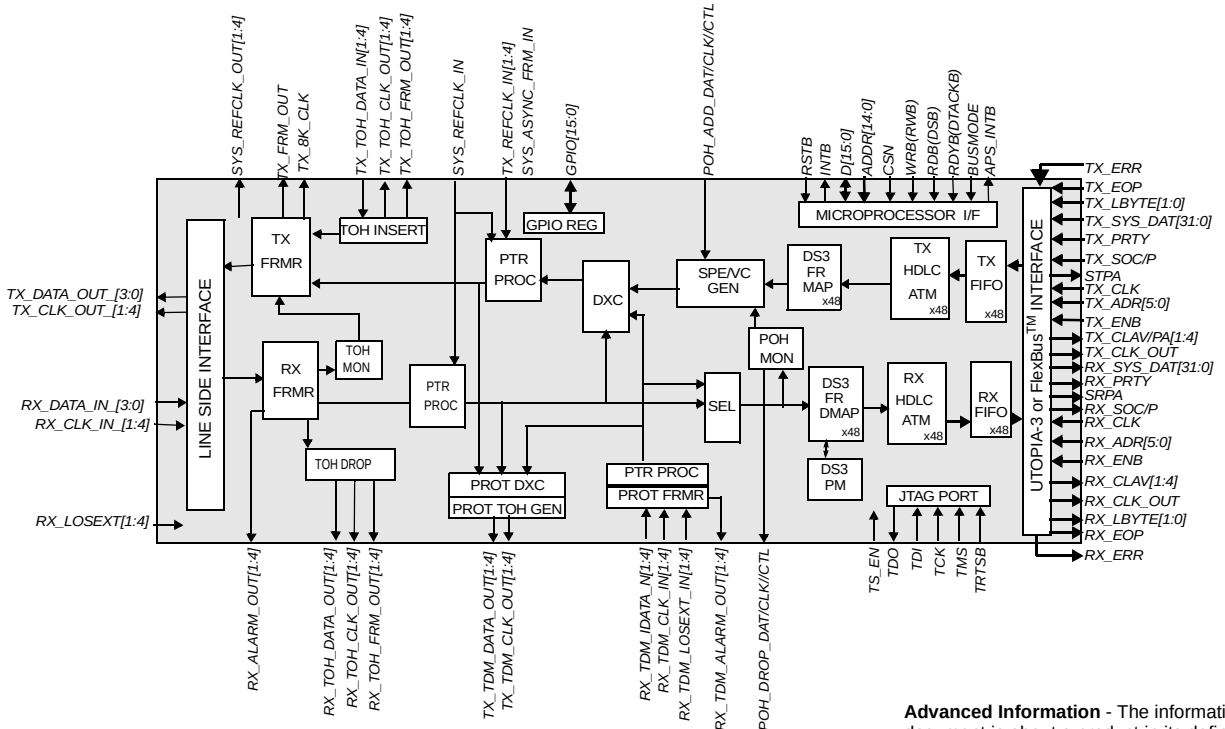
ADVANCED PRODUCT BRIEF

STS-48/STM-16 SONET/SDH Framer and ATM/POS Mapper

Features

- Provides two SONET/SDH line interface modes of operation: single STS-48/STM-16 or quad STS-12/STM-4s.
- Processes any valid combination of SONET/SDH STS-48c/ AU-4-16c, STS-12c/AU-4-4c, STS-3c/AU-4, or STS-1/AU-3 tributaries within an STS-48/STM-16 or STS-12/STM-4.
- Terminates/generates SONET/SDH section, line, and optionally path overhead. SONET/SDH processing of all defined TOH/POH bytes, compliant with Bellcore GR-253 and ANSI T1.105, and ITU G.751, G.783, G.804.
- Performs full-duplex mapping ATM cells or packets for up to 48 payload tributaries. These tributaries can range in size from STS-48c/AU-4-16c down to STS-1/AU-3.
- Supports full-duplex mapping of ATM cells or packets into DS3 tributaries for ATM over DS3 or packet over DS3 applications. DS3 tributaries are then mapped into either STS-1s or STM-1s via AU-3.
- ATM mapping is compliant with the ATM Forum UNI 3.1 specification and ITU-T I.432.1 and I.432.2.
- POS mapping is compliant with IETF RFC 2615.
- Supports simultaneously ATM, POS, TDM and direct-mapped traffic on a per tributary basis.
- Provides a single 4x622 MHz telecom bus type system interface for add/drop of payload tributaries containing TDM traffic. This interface includes a 144x48 STS-1 level cross-connect for grooming of TDM tributaries.
- Alternatively, this TDM port can be used to support protection-switching configurations between two OHIO devices or two fiber optics modules.
- This 4x622MHz APS/TDM drop/add interface supports both synchronous and asynchronous operation.
- Built-in 144x48 cross-connect capability in the TX direction. Supports ring architectures such as add-drop, drop and continue, and hairpinning, as well as APS.
- Provides a four bit 622 MHz line interface on the SONET/SDH side for STS-48/STM-16 applications; four serial 622 MHz signal for STS-12/STM-4 applications
- Supports independent loop timing in quad STS-12/STM-4 line configuration
- Provides a 100 MHz 32-bit Flexbus-3^{TM} system interface; supports Utopia Level 3 mode for ATM applications; for packet operation, can be provisionned either in extended Utopia-3 mode or in OIF SPI-3 mode.
- Programmable Utopia/FlexBus-3^{TM} addresses for multi-PHY operation.
- Loopback capability for SONET/SDH, ATM and POS tributaries
- Packaged in 624 pin CBGA
- 0.18um CMOS, 1.8V core and 2.5V I/O supply

S4806CBI Block Diagram



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ADVANCED PRODUCT BRIEF

Overview and Applications

The S4806 - OHIO is a highly-integrated STS-48/STM-16 SONET/SDH framer and POS/ATM mapper IC.

The line interface can process either a single STS-48/STM-16 or four STS-12/STM-4 signals carrying a mix of ATM, packet or TDM traffic. The S4806 integrates a STS-1 level cross-connect that allows to drop traffic through a dedicated expansion TDM port. Alternatively, the TDM drop port can be used as a second SONET/SDH-compliant line interface to support APS between two OHIO devices or two fiber optics modules.

The S4806 also performs full Path Overhead (POH) generation and monitoring as well as full-duplex mapping of packets, cells or directly mapped traffic into tributaries ranging from DS3 over STS-1/AU-3 to STS-48c. Up to 48 tributaries can be processed simultaneously.

For packets or cell transfers on the system bus, the Flexbus-3^{TM} system interface supports multiple configurations, including UTOPIA 3 and OIF SPI-3 modes.

The high level of integration, versatility and depth of channelization of the S4806 - OHIO make it a perfect fit for aggregation edge equipment as well as multi-service switches.

SONET Processing

The S4806 implements SONET/SDH processing functions for STS-48/STM-16 or four STS-12/STM-4 data streams. It can support any combination of STS-48c/AU-4-16c, STS-12c/AU-4-4c, STS-3c/AU-4, and/or STS-1/AU-3 signals within an STS-48/STM-16, or any combination of STS-12c/AU-4-4c, STS-3c/AU-4 or STS-1/AU-3 signals within the STS-12/STM-4 data streams. The S4806 provides full section, line and path overhead processing of all defined TOH/POH bytes, including framing, scrambling/descrambling, alarm signal (AIS) insertion/detection, remote failure indication insertion/detection (RDI/REI), and bit-interleaved parity (BIP) processing. The OHIO provides programmable Signal Fail (SF) and Signal Degrade (SD) thresholds for each line and path interface.

The S4806 is SONET and SDH standards compliant with Bellcore GR-253 and GR-499, ANSI T1.105 and ITU G.707 and G.783.

ATM Processing

The S4806 can be configured for ATM processing on a per tributary basis. The S4806 can terminate up to 48 data tributaries carrying ATM cells , with data rates anywhere from STS-48c/AU-4-16c down to STS-1/AU-3.

Cells received from or sent to the system interface can be either 52 or 56 bytes long

Transmit ATM Processor

In the transmit direction, the S4806's ATM processor will perform all necessary cell encapsulation including optional HEC generation, cell payload scrambling ($X^{43}+1$), and idle cell insertion to adapt the cell rate to the SPE or DS3 frame rate.

When mapping into DS3 frames, cells are either nibble-aligned with DS3 multiframes or encapsulted in PLCP frames before being mapped into the DS3 frame.

Receive ATM Processor

When receiving data from the line side, it performs cell delineation, HEC checking, descrambling, and receive cell rate adaptation by discarding idle cells.

The S4806 is ATM standards compliant with ATM Forum UNI 3.1, ITU-T I.432.1 and I.432.2.

POS HDLC Processing

The S4806 can be configured for POS HDLC processing on a per tributary basis. The S4806 can terminate up to 48 data tributaries carrying packet traffic, with data rates anywhere from STS-48c/AU-4-16c down to STS-1/AU-3.

Byte-stuffed HDLC processor (POS mode)

In Packet Over SONET mode, the S4806's transmit HDLC processor will provide the insertion of HDLC framed packets into the Synchronous Payload Envelope. It optionally inserts provisionned Address and Control fields and generates a 16 or 32 bit FCS. It also performs transparency processing, optional payload scrambling ($X^{43}+1$) and inter-frame time fill.

The receive HDLC processor provides for the delineation of HDLC frames, de-scrambling (if enabled), transparency removal and FCS error checking. The HDLC Address and Control fields are optionally checked and can be either dropped or passed-through the system interface. The S4806 also provides a robust set of counters and status/control registers for performance montoring via the microprocessor.

Bit-stuffed HDLC processing (DS3 mode)

For packet over DS3, the S4806 supports bit-stuffed HDLC mapping and demapping of packets into DS3 frames. Transparency processing is performed by adding a '0' after each sequence of five contiguous '1' and packets are then mapped bit-by-bit into the DS3 frame. For each frame, a FCS is computed, appended to the frame and transparency processed. During inter-frame fill time, the flag sequence is normally transmitted but the S4806 can optionally be provisioned to transmit 15 or more mark idle bits as required by some circuit-switched links.

The receive bit-stuffed HDLC processor performs removal of inter-frame flags, transparency processing and FCS checking.

The S4806 is POS/HDLC standards compliant with IETF RFC 1662/2615. Additionally, the S4806 HDLC processor support IP and Ethernet mapping over SONET/SDH using Link Access Procedure -SDH (LAPS) as proposed by ITU X.85 and X.86.

Direct Map Mode

The S4806 provides with the ability to directly map the traffic received from the Flexbus-3^{TM} system interface into the Synchronous Payload envelope (SONET/SDH tributaries) or DS3 frames (DS3 over STS-1/AU-3 mode). In this mode, the ATM and HDLC processors are by-passed and other protocols like Ethernet can be mapped into SONET/SDH.

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DS3 Processing

The S4806 can be configured to support DS3 mapping/demapping of ATM, HDLC or directly-mapped payloads on a per tributary basis. The S4806 supports the C-bit parity and M23 DS3 frame formats.

DS3 frame generation (Transmit)

In the Transmit direction, the S4806 maps the data received from the ATM or HDLC processor into the payload of a DS3 frame. It also generates DS3 Overhead bits and, for channels operating in C-bit mode, inserts the Terminal to Terminal Data Link information. Additionally, the OHIO can be provisionned to generate IDLE or AIS signals on any active DS3 channel. The DS3 frames are subsequently mapped into SONET STS-1 SPE or in SDH VC3 Virtual Container.

DS3 framing and demapping (Receive)

In the RX direction, the S4806 frames the DS3 signals and monitors the signal for Errors, Alarms or Idle conditions detection. In C-bit mode, it extracts the Data Link channels and makes it available to the user through an external interface. The data payload is demapped and passed through the ATM, HDLC or Direct Map Mode processors.

For testing purposes, the S4806 includes a Pseudo Random Bit Sequence generator (Tx) and monitor (Rx) and any one DS3 can be replaced by a PRBS sequence.

TDM/Circuit Drops

In addition to the FlexBus™ system interface, the S4806 also provides a single telecom-type interface to allow for add/drop of TDM tributaries. This TDM interface can operate as either a 4-bit wide STS-48/STM-16 signal, or as 4xSTS-12/STM-4 SONET/SDH signals, both operating at 622.08 MHz. The signal format adheres to the SONET/SDH frame structure, with valid A1A2, B1 and H1H2H3 pointer bytes.

For backplane applications, the TDM port's High Speed Serial Link mode provides clock recovery for the 622MHz signals as long as a low speed (78MHz) reference clock that is frequency synchronous to the data stream is supplied to the device.

The TDM port can interface directly to the AMCC S1204 Orinoco device, or the S2509. The S1204 Orinoco will interface with the STS-12/STM-4 TDM ports of the S4806, and provide insertion/extraction of DS3, E3 or clear channel STS-1/STM-0 tributaries to/from these TDM add/drop signals. The S2509 provides the capability to serialize a 4-bit wide STS-48 signal into a single 2.5 Gb/s serial backplane signal.

Redundancy Features

The 4x622 Mb/s TDM ports can also be used as APS input and output interfaces to convey signals between two S4806 devices configured for APS operation. This configuration supports 1+1 and 1:1 protection in linear, UPSR and BLSR configurations. The TDM interface provides fully compliant SONET/SDH transmit and receive TOH monitoring/generation for both 4-bit wide STS-48/STM-16 and 4xSTS-12/STM-4 modes of operation. This enables the use of the TDM port as a redundant line interface, allowing a single OHIO device to support linear 1+1 and 1:1 protection.

Cross-Connect

The S4806 provides integrated cross-connection functionality, to support all types of ring configurations, including hairpinning, drop-add, drop-and-continue, and broadcast/multicast. A 144x48 STS-1 level cross-connect is placed in the transmit direction of the S4806. The inputs to the cross-connect block come from the 48 transmit ATM/HDLC processing blocks, the receive data path, and the input TDM/APS port.

Additionally, the S4806 provides a 144x48 STS-1 level cross-connect capability in front of the TDM/APS output port, to allow for grooming of the TDM/APS interface signals. The inputs to this cross-connect come from the receive data path, the receive TDM port and the SPE / VC generator.

Line-side Interface

For STS-48/STM-16 operation, the S4806 supports a 4-bit parallel line-side interface which operates at 622.08 MHz. In this mode, the device is connected to the S3455 mux/demux and clock recovery device. (See figure below.) For STS-12/STM-4 operation, the S4806 supports four serial line interfaces which operate at 622.08 MHz. In this application, the device is connected to four S3024 clock recovery devices.

System Interface

The S4806 provides a FlexBus-3™ system interface to allow the transfer of ATM cells or packet data between the S4806 and a link layer device. For ATM cell transfer, the Flexbus-3™ interface operates as a 100 MHz 32 bit UTOPIA Level 3 interface. The S4806 supports multi-PHY operation for up to 48 tributaries. It also provides multiple TX/RX_CLAV signals for multiplexed polling operation.

For packet/direct data transfer, the FlexBus-3™ interface extends the UTOPIA framework to accomodate the variable length nature of packet traffic. In this mode, the S4806 also supports multi-PHY operation for up to 48 tributaries with multiple TX/RX_PA signals for multiplexed polling operation. Alternatively, it can be configured to operate in SPI-3 mode as defined by the Optical Internetworking Forum (OIF). The Flexbus-3™ interface also has extensions to support Direct Map Mode operation.

Microprocessor Interface

The user of the S4806 can select between an 8-bit asynchronous or a 16-bit synchronous microprocessor interface for device control and monitoring. The interface supports both Intel and Motorola type microprocessors, and is capable of operating in either an interrupt driven or polled-mode configurations.

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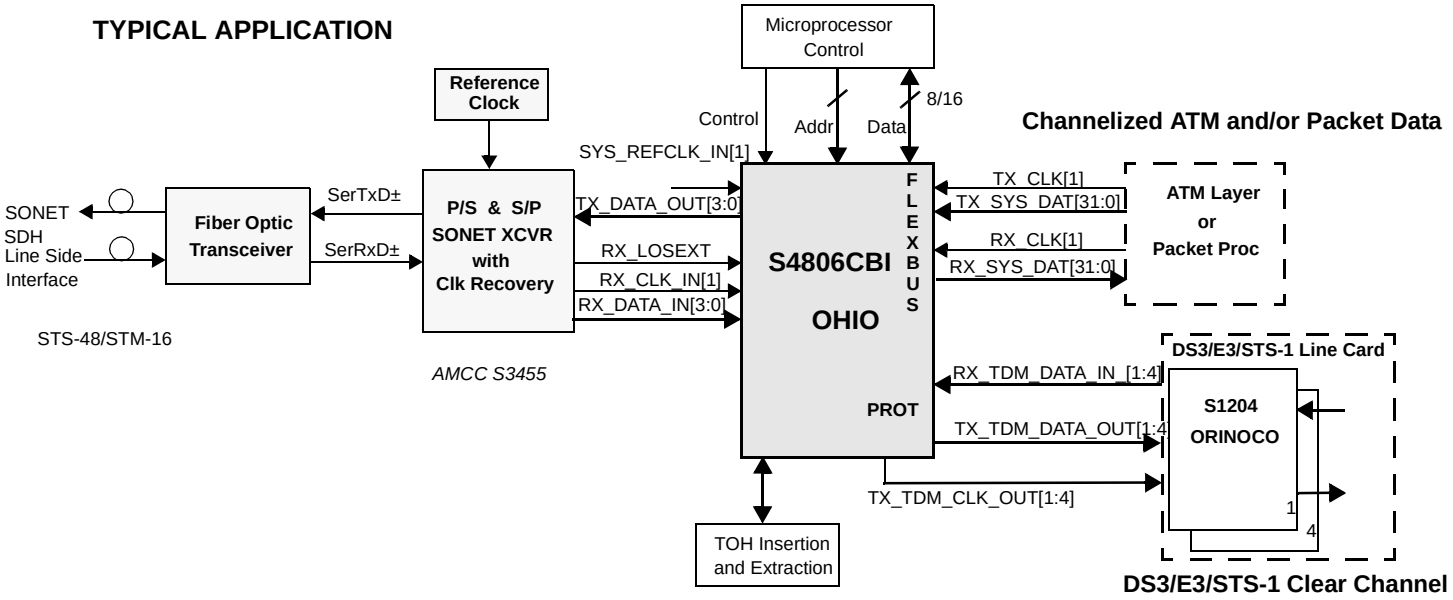
Applications

- Termination of mixed TDM and Data traffic in Multi-service switches
- Dense traffic aggregation in ATM switches and IP Routers
- Multi-service metropolitan access nodes
- SONET/SDH Multiplexers, including 2 fiber BLSR architectures.
- Mapping of Ethernet traffic into SONET/SDH using LAPS

TYPICAL APPLICATION



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