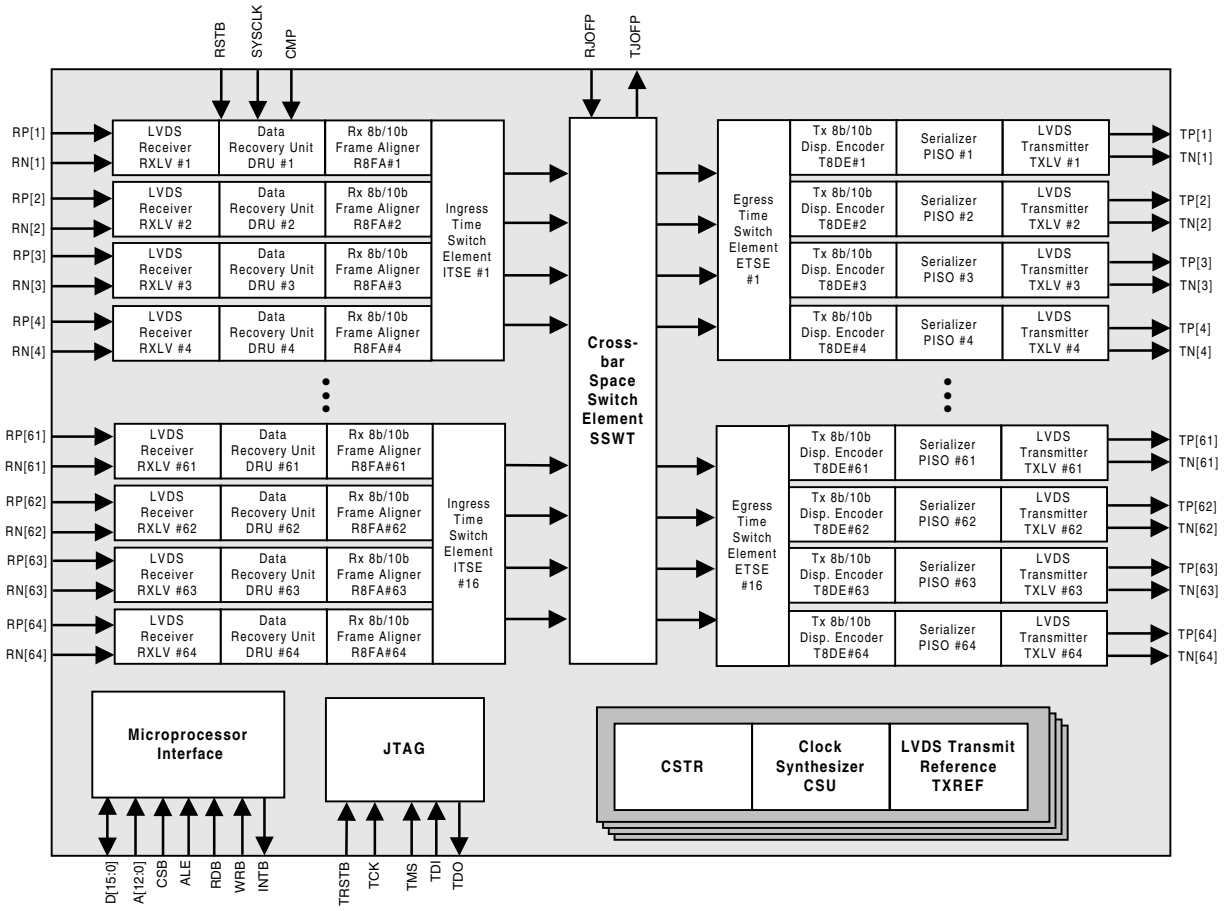
40 Gbit/s Transport Switching Element

FEATURES

- Implements a Time-Space-Time fabric with STS-1/AU-3 granularity.
- Provides 64 ingress STS-12 equivalent ports for a total of 64*12 = 768 STS-1 flows.
- Supports non-blocking permutation switching of 768 STS-1 flows at STS-1 granularity.
- Provides 64 egress STS-12 equivalent ports consisting of 768 STS-1 flows.
- Interfaces to STS-48 and STS-192 devices by aggregating 4 and 16 STS-12 equivalent flows respectively.
- Supports multicast and broadcast of STS-1 streams.
- Supports STS-12 equivalent flows with an extended 8B/10B protocol over 777.6 MHz LVDS links.
- Supports multi-plane (inverse multiplexed) switch architectures in conjunction with the PM5310 TBS device and PM7390 S/UNI®-MACH48.
- Recovers clock and data at each ingress port, synchronizes with an internal 77.76 MHz clock, and produces egress streams with a common 777.6 MHz clock.
- Detects and reports inactive or erred LVDS links via the microprocessor interface.
- Supports two sets of switch settings and a controlled method of changing settings on STS-1 frame boundaries.
- Supports multiple fabric architectures that range from 40 Gbit/s (1 TSE) to 160 Gbit/s (4 TSE devices) in a single stage, and up to 2.5 Tbit/s using multi-stage fabrics.
- Ingress to egress STS-1 switching latency of approximately 900 ns.
- Supported by an efficient algorithm to compute control settings for all permutation loads for all supported fabric architectures. Algorithms are also available for multicast/broadcast allocation.
- 1.8 V CMOS core and 3.3 V CMOS/LVDS input/output.
- Requires no external RAMs or logic parts.
- Provides a standard IEEE 1149.1 JTAG port.
- Power Consumption of 13 W (maximum).
- Packaged in a 520 pin 40mm by 40mm UltraBGA.
- Supports a 16-bit microprocessor interface which is used to initialize the device, to write switch settings into on-chip control tables, and to monitor device performance.

BLOCK DIAGRAM



40 Gbit/s Transport Switching Element

APPLICATIONS

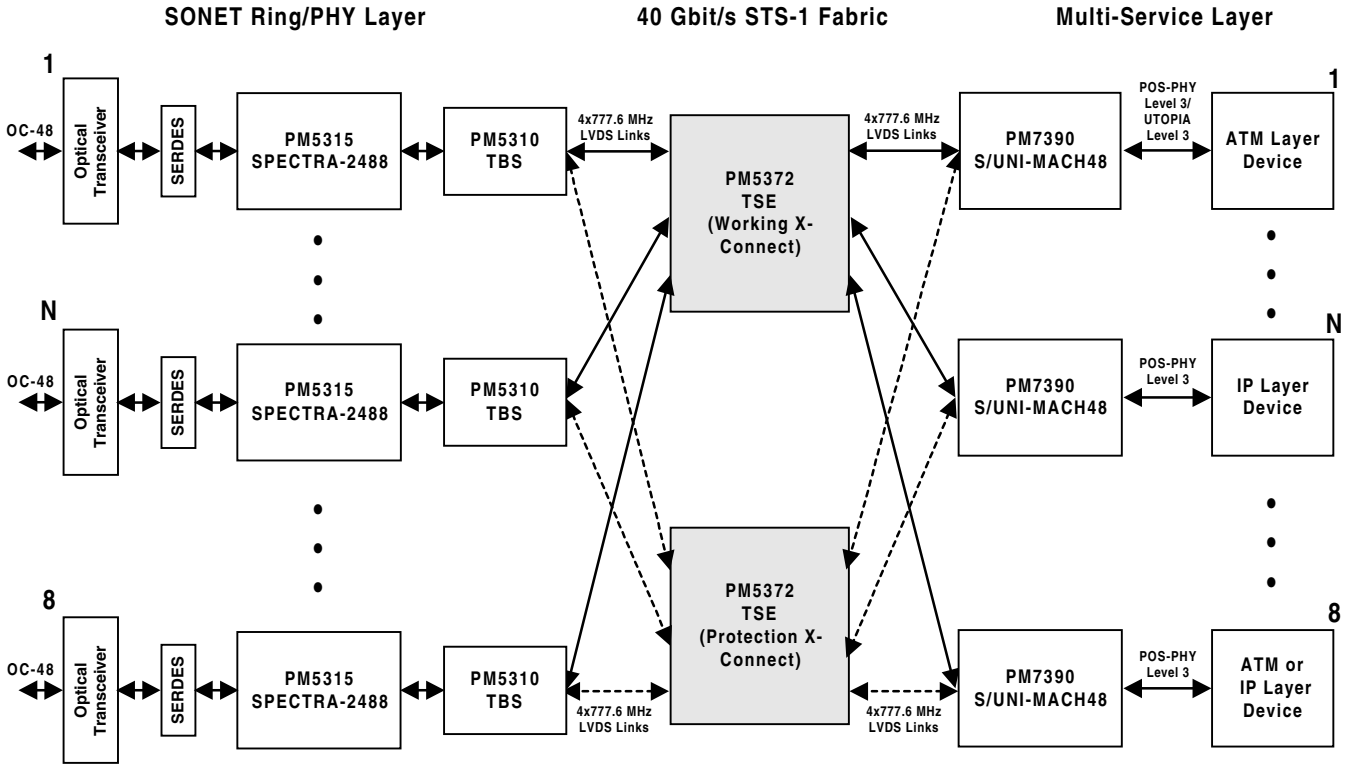
In combination with the PM5310 TBS (TelecomBus Serializer and Time-Space switching stage), the PM5315 SPECTRA-2488, the PM5316 SPECTRA-4X155, and the PM7390 S/UNI-MACH48, the PM5372 TSE supports a variety of flexible Layer 1 / Layer 2 architectures. These architectures can implement features commonly found in DCS, ADM, and multi-service switch/router equipment.

The PM5372 TSE provides the functionality that enables networking equipment to:

- Connect to (multiple) SONET rings.
- Participate in mesh-connected architectures.
- Serve as SONET-connected terminal multiplexers.
- Groom traffic at STS-1/AU-3 granularity.
- Support channelization of OC-3/12/48/192 line rates.
- Support concatenated lines rates including STS-1 (DS-3), STS-3c, STS-12c, STS-48c and STS-192c.
- Support add, drop, and drop-and-continue.
- Support UPSR, 2-BLSR, 4-BLSR, and 1+1 or 1:N APS.
- Support mesh-based APS systems.

TYPICAL APPLICATIONS

MULTI-SERVICE ATM/POS SWITCH PORT APPLICATION



Head Office:
PMC-Sierra, Inc.
#105 - 8555 Baxter Place
Burnaby, B.C. V5A 4V7
Canada
Tel: 604.415.6000
Fax: 604.415.6200

To order documentation, send email to: document@pmc-sierra.com or contact the head office, Attn: Document Coordinator

All product documentation is available on our web site at: http://www.pmc-sierra.com For corporate information, send email to: info@pmc-sierra.com

PMC-2000328 (P1)

March 2000