FUJITSU SEMICONDUCTOR
DATA SHEET

DS07-08201-1E

FR-V™ Family

FR450 Series
VLIW Embedded Microprocessor

MB93461

■ DESCRIPTION

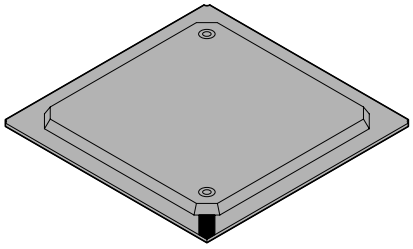
MB93461 realizes excellent performance in the field by combining advanced general processing and media processing for Digital AV equipments such as Television, Advanced Projector, IP TV Phone, Portable Media Player, etc.

The processor core embedded in MB93461 can combine maximum two instructions out of integer operation instruction, media instruction, and branch instruction and can issue them in units of VLIW (Very Long Instruction Word) instruction per cycle. Moreover, peripheral resource modules including MMU (Memory Management Unit) , SDRAM controller (SDRAMC) , interrupt controller (IRC) , DMA controller (DMAC) , asynchronous transfer module (UART) , TIMER/COUNTER, general-purpose input/output (GPIO) , video display controller (VDC) , video capture controller (VCC) , audio interface, serial interface (I^2C*) , USB interface (Full Speed Host/Function) , Memory Stick interface, and SD-IO interface are embedded in MB93461.

* : Purchase of Fujitsu I^2C components conveys a license under the Philips I^2C Patent Rights to use, these components in an I^2C system provided that the system conforms to the I^2C Standard Specification as defined by Philips.

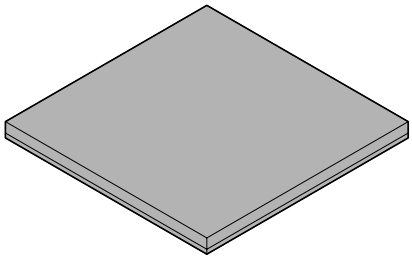
■ PACKAGES

420-ball plastic BGA



(BGA-420P-M25)

400-ball plastic PFBGA



(BGA-400P-M04)

FUJITSU

■ FEATURES

FR450 CPU Core

- 2-way VLIW Processor Core
- Core Frequency : 400 MHz/360 MHz
- MMU is embedded
- Peak Performance (Core Frequency : 400 MHz)
  800 MIPS (Integer operation performance) ,
  3200 MOPS + 400 MIPS (Media operation performance, 4MAC + Integer)
- 64 32-bit registers (32GR + 32FR)

Cache

- Instruction cache 32 KB (2way) , line size 32 Byte
- Data cache 32 KB (2way) , line size 32 Byte
- Non-blocking cache (Data Cache)
- 64-byte store buffer (Data Cache)

SDRAM interface

- SDRAM compliant with PC133 standard can be connected, Variable 32-bit/16-bit data bus and 4 CS

Local bus interface

- 32-bit address/32-bit, 16-bit, or 8-bit data
- Directly connecting SRAM/ROM, etc. is possible

JTAG

- Boundary scan function compliant with IEEE1149.1 is supported

AV peripheral resource

- Video Display Controller (VDC)
  Scan method : progressive/interlace
  Horizontal resolution : 320 to 1920 pixels, Vertical resolution : 240 to 1200 pixels
  OSD display : Max 1920x1200 pixels , 255/15 colors + transparent
- Video Capture Controller (VCC)
  Scan method : progressive/interlace
  Horizontal resolution : 320 to 1920 pixels, Vertical resolution : 240 to 1200 pixels
  Reduce Scaler
- Audio output
  3-line serial (SPD-IF, I^2S, MSB-Justified) , PCM highway, and Digital volume are supported
- Audio input
  3-line serial (I^2S, MSB-Justified) and PCM highway are supported
- Serial interface (I^2C, 2 channels)
  Standard transfer (100 Kbps) and high-speed transfer (400 Kbps) are supported
- USB interface
  USB 2.0 FS Host/Function
- MS1.4 Interface
- SD-IO interface
- AV-DMAC (8 channels)
- GPIO (32-bit)

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General-purpose peripheral resource

- Interrupt Controller (IRC)
- DMAC (8 channels)
- UART (2 channels)
- Timer (3 channels)
- GPIO (22-bit)

Recommended operation condition and external shape

- Power supply voltage and current
  Externally 3.3 V ± 0.15 V, Internally 1.4 V ± 0.07 V (at 400 MHz) , Internally 1.3 V ± 0.065 V (at 360 MHz)
- Operating temperature range from 0 °C to + 70 °C

■ PRODUCT LINEUP

These specifications have indicated four kinds of following products.

1) MB93461PB-GE1

2) MB93461-40PB-GE1

3) MB93461BGL-GE1

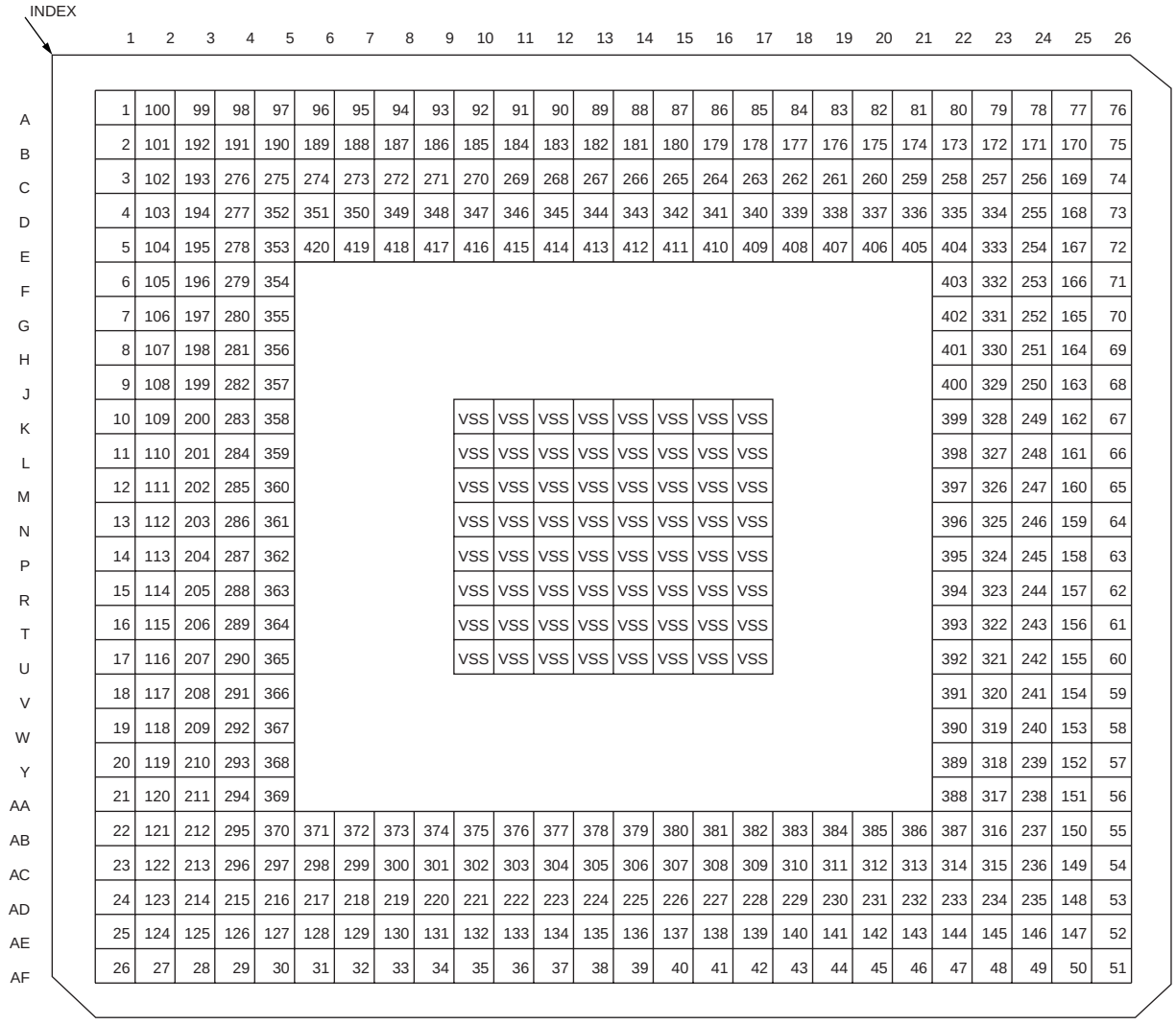
4) MB93461-40BGL-GE1

Part number	MB93461PB-GE1	MB93461-40PB-GE1	MB93461BGL-GE1	MB93461-40BGL-GE1
Core Frequency	360 MHz	400 MHz	360 MHz	400 MHz
Voltage external/ internal	3.3 V ± 0.15 V/ 1.3 V ± 0.065 V	3.3 V ± 0.15 V/ 1.4 V ± 0.07 V	3.3 V ± 0.15 V/ 1.3 V ± 0.065 V	3.3 V ± 0.15 V/ 1.4 V ± 0.07 V
Ta	0 °C to + 70 °C			
Package (code)	BGA420 (BGA-420P-M25)		PFBGA400 (BGA-400P-M04)	
Thermal resistance Rth (ja)	19 °C/W (0 m/s)		42 °C/W (0 m/s)	
Remarks	Lead-free Solder ball			

■ PIN ASSIGNMENT

1. BGA420

64 pins from K10 to U17 are for thermal. Connect them to VSS.



(BGA-420P-M25)

Pin No.	Position	Pin name	Pin No.	Position	Pin name	Pin No.	Position	Pin name
1	A1	N.C.	37	AF12	VSS	73	D26	N.C.
2	B1	N.C.	38	AF13	DA[0]	74	C26	N.C.
3	C1	N.C.	39	AF14	DA[1]	75	B26	N.C.
4	D1	N.C.	40	AF15	DA[4]	76	A26	N.C.
5	E1	HPWREN	41	AF16	DA[9]	77	A25	N.C.
6	F1	VCG[0]	42	AF17	DBA[1]	78	A24	N.C.
7	G1	VCG[5]	43	AF18	DDQM[3]	79	A23	N.C.
8	H1	VSS	44	AF19	DDQ[17]	80	A22	A[23]
9	J1	VCR[1]	45	AF20	DDQ[22]	81	A21	A[26]
10	K1	VCR[6]	46	AF21	DDQ[25]	82	A20	VSS
11	L1	VCB[1]	47	AF22	DDQ[30]	83	A19	BSTREQ#
12	M1	VCB[6]	48	AF23	N.C.	84	A18	BSTACK#
13	N1	VDR[0]	49	AF24	N.C.	85	A17	BS#
14	P1	VDR[1]	50	AF25	N.C.	86	A16	CS#[1]
15	R1	VDR[6]	51	AF26	N.C.	87	A15	CS#[6]
16	T1	VDG[1]	52	AE26	N.C.	88	A14	PP[00]
17	U1	VDG[6]	53	AD26	N.C.	89	A13	PP[01]
18	V1	VDB[1]	54	AC26	N.C.	90	A12	PP[04]
19	W1	VDB[6]	55	AB26	TRST#	91	A11	PP[09]
20	Y1	ENABLE	56	AA26	VSS	92	A10	PP[12]
21	AA1	VDE	57	Y26	PRST#	93	A9	PP[17]
22	AB1	VSS	58	W26	CMODE[3]	94	A8	PP[13]
23	AC1	N.C.	59	V26	VDD	95	A7	SDCMD
24	AD1	N.C.	60	U26	D[2]	96	A6	VSS
25	AE1	N.C.	61	T26	D[7]	97	A5	VDD
26	AF1	N.C.	62	R26	D[10]	98	A4	N.C.
27	AF2	N.C.	63	P26	D[15]	99	A3	N.C.
28	AF3	N.C.	64	N26	D[16]	100	A2	N.C.
29	AF4	N.C.	65	M26	D[19]	101	B2	N.C.
30	AF5	VDD	66	L26	D[24]	102	C2	N.C.
31	AF6	DDQ[2]	67	K26	D[27]	103	D2	N.C.
32	AF7	DDQ[7]	68	J26	BE[0]	104	E2	VDD
33	AF8	DDQ[9]	69	H26	BCLKO	105	F2	VDD
34	AF9	DDQ[14]	70	G26	A[5]	106	G2	VCG[4]
35	AF10	DCAS#	71	F26	A[8]	107	H2	VCVSYNC
36	AF11	DCS#[2]	72	E26	A[13]	108	J2	VCR[0]

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Pin No.	Position	Pin name	Pin No.	Position	Pin name	Pin No.	Position	Pin name
109	K2	VCR[5]	143	AE21	DDQ[26]	177	B18	A[31]
110	L2	VCB[0]	144	AE22	DDQ[31]	178	B17	WE#
111	M2	VCB[5]	145	AE23	TEST-MODE	179	B16	CS#[0]
112	N2	VCB[7]	146	AE24	N.C.	180	B15	CS#[5]
113	P2	VDR[2]	147	AE25	N.C.	181	B14	CPUHOLD
114	R2	VDR[7]	148	AD25	N.C.	182	B13	PP[02]
115	T2	VDG[2]	149	AC25	N.C.	183	B12	PP[05]
116	U2	VDG[7]	150	AB25	TMS	184	B11	PP[10]
117	V2	VDB[2]	151	AA25	ED	185	B10	PP[15]
118	W2	VDB[7]	152	Y25	VDE	186	B9	PP[20]
119	Y2	TOPFIELD	153	W25	CMODE[2]	187	B8	PP[16]
120	AA2	DISABLE	154	V25	CLKIN	188	B7	SDDAT[0]
121	AB2	VDE	155	U25	D[1]	189	B6	SDCKI
122	AC2	N.C.	156	T25	D[6]	190	B5	USCKI
123	AD2	N.C.	157	R25	D[9]	191	B4	UDM
124	AE2	N.C.	158	P25	D[14]	192	B3	N.C.
125	AE3	N.C.	159	N25	D[17]	193	C3	N.C.
126	AE4	SDA[1]	160	M25	D[20]	194	D3	VDE
127	AE5	VSS	161	L25	D[25]	195	E3	VSS
128	AE6	DDQ[1]	162	K25	D[28]	196	F3	VDE
129	AE7	DDQ[6]	163	J25	BE[1]	197	G3	VCG[3]
130	AE8	DDQ[8]	164	H25	BE[3]	198	H3	VCHSYNC
131	AE9	DDQ[13]	165	G25	A[6]	199	J3	VDD
132	AE10	DWE#	166	F25	A[9]	200	K3	VCR[4]
133	AE11	DCS#[1]	167	E25	A[14]	201	L3	VCR[7]
134	AE12	DCLKFB	168	D25	A[16]	202	M3	VCB[4]
135	AE13	DRAS#	169	C25	N.C.	203	N3	VSS
136	AE14	DA[2]	170	B25	N.C.	204	P3	VDR[3]
137	AE15	DA[5]	171	B24	N.C.	205	R3	VDG[0]
138	AE16	DA[10]	172	B23	N.C.	206	T3	VDG[3]
139	AE17	DA[11]	173	B22	A[22]	207	U3	VDB[0]
140	AE18	DDQ[16]	174	B21	A[25]	208	V3	VDB[3]
141	AE19	DDQ[18]	175	B20	A[30]	209	W3	VDCLK-OUT
142	AE20	DDQ[23]	176	B19	IBW	210	Y3	VDD

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Pin No.	Position	Pin name	Pin No.	Position	Pin name	Pin No.	Position	Pin name
211	AA3	FSCKI	246	N24	D[18]	281	H4	VCG[7]
212	AB3	LRCKI	247	M24	D[21]	282	J4	VDE
213	AC3	SDO	248	L24	D[26]	283	K4	VCR[3]
214	AD3	N.C.	249	K24	D[29]	284	L4	VDE
215	AD4	SDA[0]	250	J24	BE[2]	285	M4	VCB[3]
216	AD5	SCL[1]	251	H24	A[2]	286	N4	VDE
217	AD6	DDQ[0]	252	G24	A[7]	287	P4	VDR[4]
218	AD7	DDQ[5]	253	F24	A[10]	288	R4	VSS
219	AD8	VDD	254	E24	A[15]	289	T4	VDG[4]
220	AD9	DDQ[12]	255	D24	A[17]	290	U4	VSS
221	AD10	DDQ[15]	256	C24	N.C.	291	V4	VDB[4]
222	AD11	DCS#[0]	257	C23	A[19]	292	W4	VDHSYNC
223	AD12	VSS	258	C22	A[21]	293	Y4	VSS
224	AD13	DCS#[3]	259	C21	A[24]	294	AA4	SDI
225	AD14	DA[3]	260	C20	A[29]	295	AB4	BCKO
226	AD15	DA[6]	261	C19	BREQ#	296	AC4	VDE
227	AD16	DBA[0]	262	C18	VDE	297	AC5	SCL[0]
228	AD17	DA[12]	263	C17	RD#	298	AC6	VDE
229	AD18	VSS	264	C16	BGNT#	299	AC7	DDQ[4]
230	AD19	DDQ[19]	265	C15	CS#[4]	300	AC8	VDE
231	AD20	DDQ[24]	266	C14	CS#[7]	301	AC9	DDQ[11]
232	AD21	DDQ[27]	267	C13	PP[03]	302	AC10	VDE
233	AD22	VSS	268	C12	PP[06]	303	AC11	DDQM[1]
234	AD23	TDC	269	C11	PP[11]	304	AC12	DCLK
235	AD24	N.C.	270	C10	PP[18]	305	AC13	VSS
236	AC24	TDO	271	C9	PP[21]	306	AC14	VSS
237	AB24	TDI	272	C8	SDCLK	307	AC15	DA[7]
238	AA24	ERST#	273	C7	SDDAT[1]	308	AC16	VSS
239	Y24	RAM-BOOT#	274	C6	VDE	309	AC17	DCKE
240	W24	CMODE[1]	275	C5	VDD	310	AC18	VDE
241	V24	VSS	276	C4	UDP	311	AC19	DDQ[20]
242	U24	D[0]	277	D4	VDE	312	AC20	VSS
243	T24	D[5]	278	E4	UDM1	313	AC21	DDQ[28]
244	R24	D[8]	279	F4	VSS	314	AC22	VDE
245	P24	D[13]	280	G4	VCG[2]	315	AC23	MTEST-MODE

(Continued)

Pin No.	Position	Pin name	Pin No.	Position	Pin name	Pin No.	Position	Pin name
316	AB23	TCK	349	D8	SDWP	382	AB17	DDQM[2]
317	AA23	HRST#	350	D7	SDDAT[2]	383	AB18	VDD
318	Y23	VSS	351	D6	SDCD	384	AB19	DDQ[21]
319	W23	CMODE[0]	352	D5	VSS	385	AB20	VDE
320	V23	VSS	353	E5	UDP1	386	AB21	DDQ[29]
321	U23	RSTOUT#	354	F5	HOVR-CUR#	387	AB22	VDD
322	T23	D[4]	355	G5	VCG[1]	388	AA22	ECV
323	R23	VDE	356	H5	VCG[6]	389	Y22	ECLK
324	P23	D[12]	357	J5	VCD-CLKIN	390	W22	VDD
325	N23	VSS	358	K5	VCR[2]	391*	V22	VDD
326	M23	D[22]	359	L5	VSS	392	U22	VDE
327	L23	VSS	360	M5	VCB[2]	393	T22	D[3]
328	K23	D[30]	361	N5	VSS	394	R22	VSS
329	J23	VSS	362	P5	VDR[5]	395	P22	D[11]
330	H23	A[3]	363	R5	VDE	396	N22	VDE
331	G23	VSS	364	T5	VDG[5]	397	M22	D[23]
332	F23	A[11]	365	U5	VDE	398	L22	VDE
333	E23	VSS	366	V5	VDB[5]	399	K22	D[31]
334	D23	A[18]	367	W5	VDVSYNC	400	J22	VDE
335	D22	A[20]	368	Y5	VDP-CLKIN	401	H22	A[4]
336	D21	VDE	369	AA5	BCKI	402	G22	VDE
337	D20	A[28]	370	AB5	LRCKO	403	F22	A[12]
338	D19	ERR#	371	AB6	VSS	404	E22	VDD
339	D18	VDD	372	AB7	DDQ[3]	405	E21	VSS
340	D17	RDY#	373	AB8	VSS	406	E20	A[27]
341	D16	VDE	374	AB9	DDQ[10]	407	E19	VDD
342	D15	CS#[3]	375	AB10	VSS	408	E18	VSS
343	D14	VDE	376	AB11	DDQM[0]	409	E17	DIR
344	D13	VSS	377	AB12	VDD	410	E16	VSS
345	D12	PP[07]	378*	AB13	VDD	411	E15	CS#[2]
346	D11	VSS	379	AB14	VDE	412	E14	VSS
347	D10	PP[19]	380	AB15	DA[8]	413	E13	VDE
348	D9	VSS	381	AB16	VDE	414	E12	PP[08]

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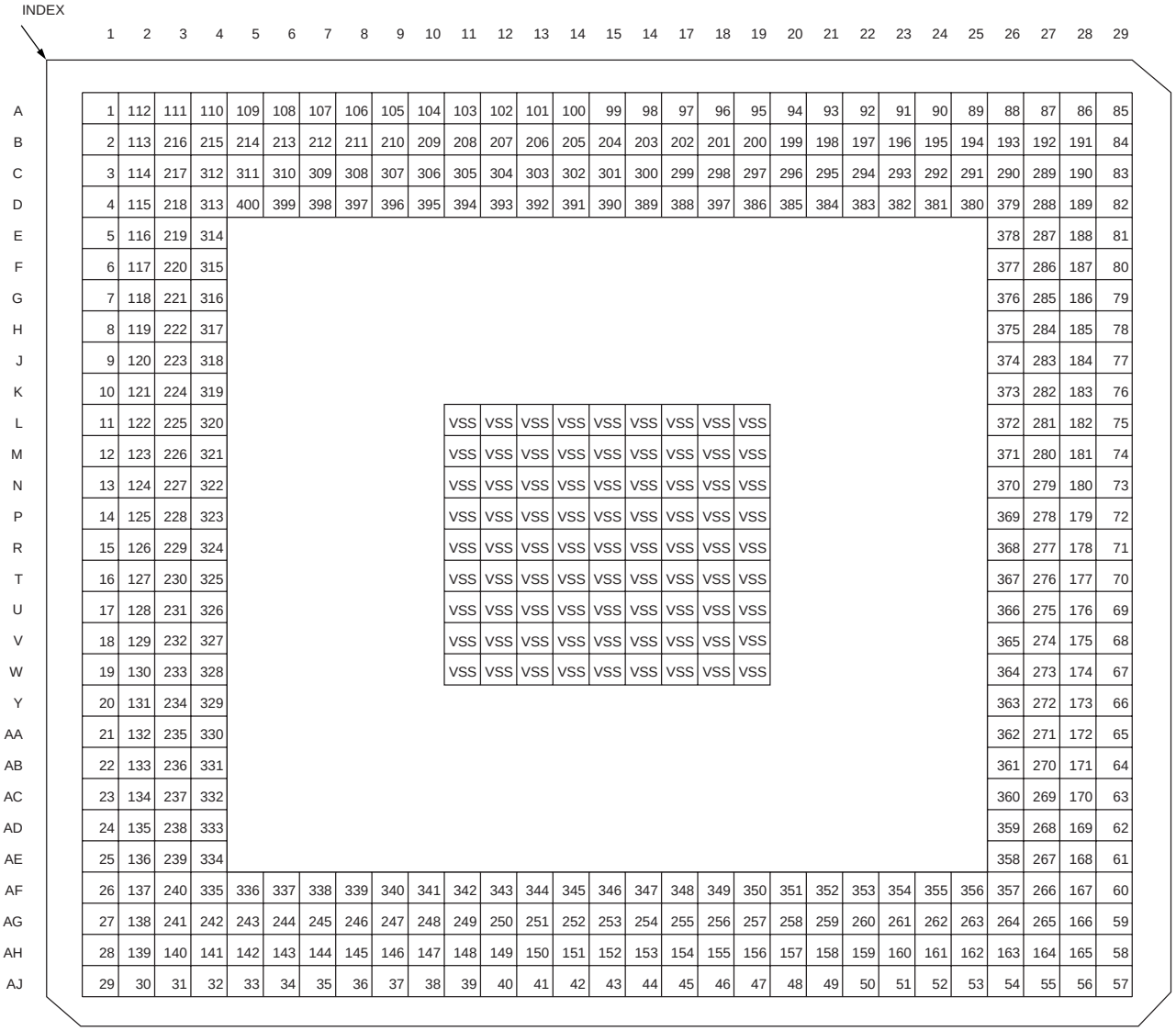
Pin No.	Position	Pin name
415	E11	VDE
416	E10	PP[14]
417	E9	VDD
418	E8	MSDIRP
419	E7	SDDAT[3]
420	E6	SDMSSE-LECT

* : Pin No. 378 and 391 are the analog power supply pins of PLL.

2. PFBGA400

81 pins from L11 to W19 are for thermal. Connect them to VSS.

(TOP VIEW)



(BGA-400P-M04)

Pin No.	Position	Pin name	Pin No.	Position	Pin name	Pin No.	Position	Pin name
1	A1	N.C.	35	AJ7	VDE	69	U29	D[12]
2	B1	N.C.	36	AJ8	DDQ[10]	70	T29	D[16]
3	C1	UDP1	37	AJ9	DDQ[14]	71	R29	VDE
4	D1	HPWREN	38	AJ10	DWE#	72	P29	D[22]
5	E1	VDD	39	AJ11	DCS#[0]	73	N29	D[26]
6	F1	VCG[3]	40	AJ12	DCLK	74	M29	D[28]
7	G1	VCG[7]	41*	AJ13	VDD	75	L29	BE[0]
8	H1	VCD-CLKIN	42	AJ14	DA[0]	76	K29	VDE
9	J1	VCR[1]	43	AJ15	VSS	77	J29	A[3]
10	K1	VCR[5]	44	AJ16	DA[6]	78	H29	A[7]
11	L1	VCR[7]	45	AJ17	DA[10]	79	G29	A[9]
12	M1	VCB[3]	46	AJ18	DBA[1]	80	F29	A[13]
13	N1	VSS	47	AJ19	DDQM[2]	81	E29	VDD
14	P1	VDR[0]	48	AJ20	VDE	82	D29	A[18]
15	R1	VDR[4]	49	AJ21	DDQ[19]	83	C29	N.C.
16	T1	VDG[0]	50	AJ22	DDQ[23]	84	B29	N.C.
17	U1	VDG[2]	51	AJ23	DDQ[25]	85	A29	N.C.
18	V1	VDG[6]	52	AJ24	DDQ[29]	86	A28	N.C.
19	W1	VDE	53	AJ25	VDE	87	A27	A[20]
20	Y1	VDB[4]	54	AJ26	TDC	88	A26	VSS
21	AA1	VDCLK-OUT	55	AJ27	N.C.	89	A25	A[26]
22	AB1	TOPFIELD	56	AJ28	N.C.	90	A24	A[30]
23	AC1	VDE	57	AJ29	N.C.	91	A23	BREQ#
24	AD1	BCKI	58	AH29	N.C.	92	A22	VDD
25	AE1	BCKO	59	AG29	TCK	93	A21	DIR
26	AF1	N.C.	60	AF29	ECV	94	A20	BS#
27	AG1	N.C.	61	AE29	VSS	95	A19	CS#[0]
28	AH1	N.C.	62	AD29	VDE	96	A18	CS#[4]
29	AJ1	N.C.	63	AC29	CMODE[1]	97	A17	VDE
30	AJ2	N.C.	64	AB29	VSS	98	A16	PP[01]
31	AJ3	SDA[1]	65	AA29	VDE	99	A15	VDE
32	AJ4	VDD	66	Y29	D[2]	100	A14	PP[07]
33	AJ5	DDQ[1]	67	W29	D[6]	101	A13	PP[11]
34	AJ6	DDQ[5]	68	V29	D[8]	102	A12	PP[15]

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Pin No.	Position	Pin name	Pin No.	Position	Pin name	Pin No.	Position	Pin name
103	A11	PP[17]	136	AE2	LRCKI	169	AD28	RAM-BOOT#
104	A10	VDD	137	AF2	SDO	170	AC28	CMODE[0]
105	A9	SDWP	138	AG2	N.C.	171	AB28*	VDD
106	A8	SDDAT[1]	139	AH2	N.C.	172	AA28	VDD
107	A7	SDCKI	140	AH3	SDA[0]	173	Y28	D[1]
108	A6	VDD	141	AH4	VSS	174	W28	D[5]
109	A5	UDM	142	AH5	DDQ[0]	175	V28	VDE
110	A4	N.C.	143	AH6	DDQ[4]	176	U28	D[11]
111	A3	N.C.	144	AH7	VSS	177	T28	D[15]
112	A2	N.C.	145	AH8	DDQ[9]	178	R28	VSS
113	B2	N.C.	146	AH9	DDQ[13]	179	P28	D[21]
114	C2	VDE	147	AH10	DDQ[15]	180	N28	D[25]
115	D2	VDD	148	AH11	DDQM[1]	181	M28	D[27]
116	E2	VDE	149	AH12	VDD	182	L28	D[31]
117	F2	VCG[2]	150	AH13	VSS	183	K28	VSS
118	G2	VCG[6]	151	AH14	DRAS#	184	J28	A[2]
119	H2	VSS	152	AH15	DA[3]	185	H28	A[6]
120	J2	VCR[0]	153	AH16	DA[5]	186	G28	A[8]
121	K2	VCR[4]	154	AH17	DA[9]	187	F28	A[12]
122	L2	VDE	155	AH18	VDE	188	E28	VSS
123	M2	VCB[2]	156	AH19	DCKE	189	D28	A[17]
124	N2	VCB[6]	157	AH20	VSS	190	C28	N.C.
125	P2	VCB[7]	158	AH21	DDQ[18]	191	B28	N.C.
126	R2	VDR[3]	159	AH22	DDQ[22]	192	B27	A[19]
127	T2	VDR[7]	160	AH23	VDE	193	B26	A[23]
128	U2	VDG[1]	161	AH24	DDQ[28]	194	B25	A[25]
129	V2	VDG[5]	162	AH25	VSS	195	B24	A[29]
130	W2	VSS	163	AH26	TEST-MODE	196	B23	ERR#
131	Y2	VDB[3]	164	AH27	N.C.	197	B22	VSS
132	AA2	VDB[7]	165	AH28	N.C.	198	B21	BSTACK#
133	AB2	ENABLE	166	AG28	TDO	199	B20	WE#
134	AC2	VDP-CLKIN	167	AF28	TRST#	200	B19	BGNT#
135	AD2	SDI	168	AE28	ED	201	B18	CS#[3]

(Continued)

Pin No.	Position	Pin name	Pin No.	Position	Pin name	Pin No.	Position	Pin name
202	B17	VSS	236	AB3	VDVSYNC	270	AB27	CMODE[3]
203	B16	PP[00]	237	AC3	VSS	271	AA27	CLKIN
204	B15	VSS	238	AD3	FSCKI	272	Y27	D[0]
205	B14	PP[06]	239	AE3	VDE	273	W27	D[4]
206	B13	PP[10]	240	AF3	LRCKO	274	V27	VSS
207	B12	PP[12]	241	AG3	VDE	275	U27	D[10]
208	B11	PP[14]	242	AG4	SCL[1]	276	T27	D[14]
209	B10	VSS	243	AG5	VDE	277	R27	D[18]
210	B9	SDCLK	244	AG6	DDQ[3]	278	P27	D[20]
211	B8	SDDAT[0]	245	AG7	DDQ[7]	279	N27	D[24]
212	B7	VSS	246	AG8	DDQ[8]	280	M27	VDE
213	B6	SDMSSE-LECT	247	AG9	DDQ[12]	281	L27	D[30]
214	B5	VSS	248	AG10	VDE	282	K27	BE[2]
215	B4	VDE	249	AG11	DDQM[0]	283	J27	BE[3]
216	B3	N.C.	250	AG12	DCS#[2]	284	H27	A[5]
217	C3	N.C.	251	AG13	DCLKFB	285	G27	VDE
218	D3	VSS	252	AG14	DCS#[3]	286	F27	A[11]
219	E3	VSS	253	AG15	DA[2]	287	E27	A[15]
220	F3	VCG[1]	254	AG16	DA[4]	288	D27	A[16]
221	G3	VCG[5]	255	AG17	DA[8]	289	C27	N.C.
222	H3	VCVSYNC	256	AG18	VSS	290	C26	A[22]
223	J3	VDD	257	AG19	DA[12]	291	C25	A[24]
224	K3	VCR[3]	258	AG20	DDQ[16]	292	C24	A[28]
225	L3	VSS	259	AG21	DDQ[17]	293	C23	VDD
226	M3	VCB[1]	260	AG22	DDQ[21]	294	C22	BSTREQ#
227	N3	VCB[5]	261	AG23	VSS	295	C21	A[31]
228	P3	VSS	262	AG24	DDQ[27]	296	C20	RD#
229	R3	VDR[2]	263	AG25	DDQ[31]	297	C19	VDE
230	T3	VDR[6]	264	AG26	VDD	298	C18	CS#[2]
231	U3	VDE	265	AG27	MTEST-MODE	299	C17	CS#[6]
232	V3	VDG[4]	266	AF27	TMS	300	C16	CPUHOLD
233	W3	VDB[0]	267	AE27	ERST#	301	C15	PP[03]
234	Y3	VDB[2]	268	AD27	VSS	302	C14	PP[05]
235	AA3	VDB[6]	269	AC27	VDD	303	C13	PP[09]

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Pin No.	Position	Pin name	Pin No.	Position	Pin name	Pin No.	Position	Pin name
304	C12	VDE	338	AF7	DDQ[6]	372	L26	D[29]
305	C11	PP[19]	339	AF8	VDD	373	K26	BE[1]
306	C10	PP[21]	340	AF9	DDQ[11]	374	J26	BCLKO
307	C9	PP[16]	341	AF10	VSS	375	H26	A[4]
308	C8	SDCMD	342	AF11	DCAS#	376	G26	VSS
309	C7	SDDAT[3]	343	AF12	DCS#[1]	377	F26	A[10]
310	C6	SDCD	344	AF13	VSS	378	E26	A[14]
311	C5	VDD	345	AF14	VSS	379	D26	A[21]
312	C4	UDP	346	AF15	DA[1]	380	D25	VDE
313	D4	UDM1	347	AF16	VDE	381	D24	A[27]
314	E4	HOVR-CUR#	348	AF17	DA[7]	382	D23	VSS
315	F4	VCG[0]	349	AF18	DBA[0]	383	D22	IBW
316	G4	VCG[4]	350	AF19	DA[11]	384	D21	VDE
317	H4	VCHSYNC	351	AF20	DDQM[3]	385	D20	RDY#
318	J4	VDE	352	AF21	VDD	386	D19	VSS
319	K4	VCR[2]	353	AF22	DDQ[20]	387	D18	CS#[1]
320	L4	VCR[6]	354	AF23	DDQ[24]	388	D17	CS#[5]
321	M4	VCB[0]	355	AF24	DDQ[26]	389	D16	CS#[7]
322	N4	VCB[4]	356	AF25	DDQ[30]	390	D15	PP[02]
323	P4	VDE	357	AF26	TDI	391	D14	PP[04]
324	R4	VDR[1]	358	AE26	HRST#	392	D13	PP[08]
325	T4	VDR[5]	359	AD26	ECLK	393	D12	VSS
326	U4	VSS	360	AC26	PRST#	394	D11	PP[18]
327	V4	VDG[3]	361	AB26	CMODE[2]	395	D10	PP[20]
328	W4	VDG[7]	362	AA26	VSS	396	D9	PP[13]
329	Y4	VDB[1]	363	Y26	RSTOUT#	397	D8	MSDIRP
330	AA4	VDB[5]	364	W26	D[3]	398	D7	SDDAT[2]
331	AB4	VDHSYNC	365	V26	D[7]	399	D6	VDE
332	AC4	VDD	366	U26	D[9]	400	D5	USCKI
333	AD4	VDCDIS-ABLE	367	T26	D[13]			
334	AE4	VSS	368	R26	D[17]			
335	AF4	SCL[0]	369	P26	D[19]			
336	AF5	VSS	370	N26	D[23]			
337	AF6	DDQ[2]	371	M26	VSS			

* : Pin No. 41 and 171 are the analog power supply pins of PLL.

■ PIN DESCRIPTION

1. Format

Pin No.	Pin name	Direction	Type	BS	Description

Pin name : Indicates name of external pin

If several signals share the same pin, the names are separated by a slash (/) .

“#” in a signal line name indicates “active low.”

Direction : Indicates I/O of signal with reference to LSI chip

Input : Indicates pin for input signal to LSI chip

Output : Indicates pin for output signal from LSI chip

Input/output : Indicates pin for bidirectional signal

Type : Indicates pin input/output circuit type

Each symbol has the following meaning :

Symbol	Description
SD	Solid Drive Type of output pin. Normal output. The pin never becomes high impedance.
TS	Tri-State Type of output or input/output pin. The pin may become high impedance.
PU	Pull-up Type of input pin or input/output pin. A pull-up resistor is built into the circuit.
PD	Pull-down Type of input pin or input/output pin. A pull-down resistor is built into the circuit.
OD	Open-drain Type of output pin. The pin may become high impedance.

Note : Explains outline of function and relationship with other pins.

BS : Indicates whether the target of boundary-scan or not.

2. Local Bus Interface

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
261	91	BREQ#	Input	—	Yes	Bus Request This signal inputs a bus release request from the bus master device.
264	200	BGNT#	Output	SD	Yes	Bus Grant This signal indicates that the local bus is released.
177	295	A[31]	Input/ output	TS	Yes	Address A word address is output. When the local bus is released, this pin becomes input.
175	90	A[30]				
260	195	A[29]				
337	292	A[28]				
406	381	A[27]				
81	89	A[26]				
174	194	A[25]				
259	291	A[24]				
80	193	A[23]				
173	290	A[22]				
258	379	A[21]				
335	87	A[20]				
257	192	A[19]				
334	82	A[18]				
255	189	A[17]				
168	288	A[16]				
254	287	A[15]				
167	378	A[14]				
72	80	A[13]				
403	187	A[12]				
332	286	A[11]				
253	377	A[10]				
166	79	A[9]				
71	186	A[8]				
252	78	A[7]				
165	185	A[6]				
70	284	A[5]				
401	375	A[4]				
330	77	A[3]				
251	184	A[2]				

(Continued)

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
399	182	D[31]	Input/ output	TS	Yes	<u>Data</u> This is the data bus; D[31] is MSB. When connecting a 16-bit slave device to this signal, connect it to D[31 : 16] (higher) . When connecting a 8-bit slave device to this signal, connect it to D[31 : 24] (higher) . If all of the CS# that allowed to assert are configured to 8-bit or 16-bit (by LCR0-7.BW) , D[15 : 00] are not driven.
328	281	D[30]				
249	372	D[29]				
162	74	D[28]				
67	181	D[27]				
248	73	D[26]				
161	180	D[25]				
66	279	D[24]				
397	370	D[23]				
326	72	D[22]				
247	179	D[21]				
160	278	D[20]				
65	369	D[19]				
246	277	D[18]				
159	368	D[17]				
64	70	D[16]				
63	177	D[15]				
158	276	D[14]				
245	367	D[13]				
324	69	D[12]				
395	176	D[11]				
62	275	D[10]				
157	366	D[9]				
244	68	D[8]				
61	365	D[7]				
156	67	D[6]				
243	174	D[5]				
322	273	D[4]				
393	364	D[3]				
60	66	D[2]				
155	173	D[1]				
242	272	D[0]				

(Continued)

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
68 163 250 164	75 373 282 283	BE[0]/BE#[0] BE[1]/BE#[1] BE[2]/BE#[2] BE[3]/BE#[3]	Input/ output	TS	Yes	Byte Enable This specifies byte lanes for data transfer. The correspondence between this signal and the data bus when accessing the 32-bit slave device is shown below (The CS area can be set only to the big endian (LCRx.LE = 0) .) : BE[0] → D [31 : 24] BE[1] → D [23 : 16] BE[2] → D [15 : 08] BE[3] → D [07 : 00] BE[0 : 1] is used to access a 16-bit slave device; the correspondence between this signal and the data bus is shown below : 1) The CS area set to big endian (LCRx.LE = 0) BE[0] → D [31 : 24] (higher byte) BE[1] → D [23 : 16] (lower byte) 2) The CS area set to little endian (LCRx.LE = 1) BE[0] → D [23 : 16] (higher byte) BE[1] → D [31 : 24] (lower byte) BE[2] is used to access halfword address. BE[2] → A[1] BE[0] is used to access a 8-bit slave device; the correspondence between this signal and the data bus is shown below : BE[0] → D [31 : 24] BE[2 : 3] is used to access byte address. BE[2] → A[1] BE[3] → A[0] These pins become input when the bus is released. To access this LSI as the slave device when this bus is released, it must be treated as a 32-bit slave device. BE[0] must be pulled-down/pulled-up according to BE/#BE polarity (When RSTOUT# is asserted, the value of BE[0] is reflected in LGCR.BED) .
85	94	BS#	Input/ output	TS	Yes	Bus Cycle Start This is asserted for only 1 CLKIN cycle at the beginning of a bus cycle to indicate the start of the bus cycle. This pin is input when the bus is released.
263	296	RD#	Output	TS	Yes	Read This pin is asserted during the second or later CLKIN cycles of read local bus cycles. This pin becomes high impedance when the local bus is released.

(Continued)

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
178	199	WE#	Output	TS	Yes	Write Enable This pin is asserted during a write cycles. It can be used as a strobe pulse for write data. This pin becomes high impedance when the bus is released.
409	93	DIR	Input/ output	TS	Yes	Direction Indicates transfer direction of D[31 : 00] pins L : input (read) , H : output (write) This pin becomes input when the bus is released. This LSI determines whether the local bus cycles that performed by external devices are reads or writes, based on the DIR signal. This pin becomes “L” when bus is idle.
340	385	RDY#	Input/ output	TS	Yes	Ready This pin is in the input state while the bus is not released; the bus cycle completion notice is “input” from the slave device to this pin. This pin becomes output while this LSI is operating as the slave bus when the bus released; it notifies the bus master device of the bus cycle completion. When RSTOUT# is asserted, the value of RDY# is reflected in LCR0.RC.
338	196	ERR#	Input	—	Yes	Error This is sampled at the end of the bus cycle; the error notice is input from the slave device to this pin. This pin is ignored when the bus is released.
342 411 86 179	201 298 387 95	CS#[3] CS#[2] CS#[1] CS#[0]	Output	SD	Yes	Chip Select This signal selects slave device under control of MB93461. The corresponding address is determined from the settings of the programmable address decoder built into MB93461. Connect the boot ROM to the CS#[0] pin.
266 87 180 265	389 299 388 96	CS#[7]/IRQ#[7] CS#[6]/IRQ#[6] CS#[5]/IRQ#[5] CS#[4]/IRQ#[4]	Input/ output	TS/ PU	Yes	Chip Select/Interrupt Request 7-4 This signal is used as chip select or interrupt request. Chip select selects slave device under control of this LSI. This signal works as IRQ#[7 : 4] after power-on reset and need to set LGCR.CSE to use as CS#. When use as CS#, the corresponding address is determined from the setting of the programmable address decoder built into this LSI.

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Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
176	383	IBW	Input	—	Yes	Initial Bus Width This pin is used to specify the data bus width of the boot ROM to be connected to the CS#[0] pin. The data bus width specified for this signal can be changed later via software. 16 bits : Input low level 32 bits : Input high level
83	294	BSTREQ#	Input/ output	TS	Yes	Burst Request This pin is used to request burst transfer.
84	198	BSTACK#	Input/ output	TS	Yes	Burst Acknowledge This pin is used to enable burst transfer.
69	374	BCLKO	Output	SD	Yes	Bus Clock Out This clock is supplied to the device connected with the local bus. Output stops during power-on reset.

3. SDRAM Interface

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
224 36 133 222	252 250 343 39	DCS#[3] DCS#[2] DCS#[1] DCS#[0]	Output	SD	Yes	Chip Select This signal is output based on the setting of the programmable address decoder incorporated in this LSI. DCS#[2] and DCS#[3] are only used for connecting the 168-pin registered DIMM.
42 227	46 349	DBA[1] DBA[0]	Output	SD	Yes	Bank Address The bank address is output.
228 139 138 41 380 307 226 137 40 225 136 39 38	257 350 45 154 255 348 44 153 254 152 253 346 42	DA[12] DA[11] DA[10] DA[9] DA[8] DA[7] DA[6] DA[5] DA[4] DA[3] DA[2] DA[1] DA[0]	Output	SD	Yes	Multiplexed Address The address multiplexed for SDRAM is output.
135	151	DRAS#	Output	SD	Yes	Row Address Strobe Row Address Strobe signal to SDRAM.
35	342	DCAS#	Output	SD	Yes	Column Address Strobe Column Address Strobe signal to SDRAM.
132	38	DWE#	Output	SD	Yes	Write Enable Write Enable signal to SDRAM.
309	156	DCKE	Output	SD	Yes	Clock Enable Clock Enable signal to SDRAM.
376 303 382 43	249 148 47 351	DDQM[0] DDQM[1] DDQM[2] DDQM[3]	Output	SD	Yes	Data Mask These pins (signal) are combined with other signals to specify the byte lane to be written. At read, all the bits are driven Low. The correspondence between this signal and the data bus when connecting 32-bit SDRAM is shown below : DDQM[0] → DDQ[31 : 24] DDQM[1] → DDQ[23 : 16] DDQM[2] → DDQ[15 : 08] DDQM[3] → DDQ[07 : 00] The correspondence between this signal and the data bus when connecting 16-bit SDRAM is shown below : DDQM[0] → DDQ[31 : 24] DDQM[1] → DDQ[23 : 16]

(Continued)

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Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
144 47 386 313 232 143 46 231 142 45 384 311 230 141 44 140 221 34 131 220 301 374 33 130 32 129 218 299 372 31 128 217	263 356 52 161 262 355 51 354 50 159 260 353 49 158 259 258 147 37 146 247 340 36 145 246 245 338 34 143 244 337 33 142	DDQ[31] DDQ[30] DDQ[29] DDQ[28] DDQ[27] DDQ[26] DDQ[25] DDQ[24] DDQ[23] DDQ[22] DDQ[21] DDQ[20] DDQ[19] DDQ[18] DDQ[17] DDQ[16] DDQ[15] DDQ[14] DDQ[13] DDQ[12] DDQ[11] DDQ[10] DDQ[9] DDQ[8] DDQ[7] DDQ[6] DDQ[5] DDQ[4] DDQ[3] DDQ[2] DDQ[1] DDQ[0]	Input/ output	TS	Yes	Data This signal is connected to the SDRAM data bus; DDQ[31] is MSB. When connecting 16-bit SDRAM, connect it to DDQ[31 : 16] When the bus width is set to 16 bits by DCFG.BW, DDQ[15 : 00] is fixed to the high-impedance state.
304	40	DCLK	Output	SD	Yes	SDRAM Clock This is the output of the clock signal supplied to SDRAM. The output is halted while the PLL is halted. The output is also halted during a power-on reset.
134	251	DCLKFB	Input	—	Yes	Feedback for SDRAM Clock To adjust the DCLK phase, feedback input to the PLL built into this LSI chip.

4. General-purpose Peripheral Resource

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
88 89 182 267	203 98 390 301	IRQ#[0]/PP[00] IRQ#[1]/PP[01] IRQ#[2]/PP[02] IRQ#[3]/PP[03]	Input/ output	TS	Yes	Interrupt Request 0 to 3/GPIO 0 to 3 These pins are used as the interrupt input and as a general-purpose I/O port (GPIO) .
90	391	TOUT[0]/ GATE[0]/PP[04]	Input/ output	TS	Yes	Timer ch 0 Output/Timer ch 0 Gate/GPIO 4 This pin is used as the timer ch 0 pin and as a general-purpose I/O port (GPIO) .
183	302	TOUT[1]/ GATE[1]/PP[05]	Input/ output	TS	Yes	Timer ch 1 Output/Timer ch 1 Gate/GPIO 5 This pin is used as the timer ch 1 pin and as a general-purpose I/O port (GPIO) .
268	205	RXD[0]/PP[06]	Input/ output	TS	Yes	UART ch 0 Receive Data/GPIO 6 This pin is used as the UART ch 0 receive data and as a general-purpose I/O port (GPIO) .
345	100	TXD[0]/PP[07]	Input/ output	TS	Yes	UART ch 0 Transmit Data/GPIO 7 This pin is used as the UART ch 0 transmit data and as a general-purpose I/O port (GPIO) .
414	392	CTS#[0]/PP[08]	Input/ output	TS	Yes	UART ch 0 Clear To Send Signal/GPIO 8 This pin is used as the UART ch 0 CTS signal and as a general-purpose I/O port (GPIO) .
91	303	RTS#[0]/PP[09]	Input/ output	TS	Yes	UART ch 0 Request To Send Signal/GPIO 9 This pin is used as the UART ch 0 RTS signal and as a general-purpose I/O port (GPIO) .
184	206	RXD[1]/PP[10]	Input/ output	TS	Yes	UART ch 1 Receive Data/GPIO 10 This pin is used as the UART ch 1 receive data and as a general-purpose I/O port (GPIO) .
269	101	TXD[1]/PP[11]	Input/ output	TS	Yes	UART ch 1 Transmit Data/GPIO 11 This pin is used as the UART ch 1 transmit data and as a general-purpose I/O port (GPIO) .
92	207	DREQ#[0]/PP[12]	Input/ output	TS	Yes	DMAC ch 0 Transfer Request/GPIO 12 This pin is used as the UART ch 0 transfer request and as a general-purpose I/O port (GPIO) .
94	396	DACK#[0]/PP[13]	Input/ output	TS	Yes	DMAC ch 0 Acknowledge/GPIO 13 This pin is used as the DMAC ch 0 transfer acknowledge signal and as a general-purpose I/O port (GPIO) .

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(Continued)

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
416	208	DONE#[0]/ DREQ#[4]/PP[14]	Input/ output	TS	Yes	DMAC ch 0 Transfer Done/DMAC ch4 Transfer Request/GPIO 14 This pin is used as the DMAC ch 0 transfer end signal, as the DMAC ch 4 transfer request, and as a general-purpose I/O port (GPIO) .
185	102	DREQ#[1]/PP[15]	Input/ output	TS	Yes	DMAC ch 1 Transfer Request/GPIO 15 This pin is used as the DMAC ch 1 transfer request and as a general-purpose I/O port (GPIO) .
187	307	DACK#[1]/PP[16]	Input/ output	TS	Yes	DMAC ch 1 Acknowledge/GPIO 16 This pin is used as the DMAC ch 1 transfer acknowledge signal and as a general-purpose I/O port (GPIO) .
93	103	DONE#[1]/ DREQ#[5]/ PP[17]	Input/ output	TS	Yes	DMAC ch 1 Transfer Done/DMAC ch 5 Transfer Request/GPIO 17 This pin is used as the DMAC ch 1 transfer end signal, as the DMAC ch 5 transfer request, and as a general-purpose I/O port (GPIO) .
270	394	DREQ#[2]/PP[18]	Input/ output	TS	Yes	DMAC ch 2 Transfer Request/GPIO 18 This pin is used as the DMAC ch 2 transfer request and as a general-purpose I/O port (GPIO) .
347	305	DREQ#[3]/PP[19]	Input/ output	TS	Yes	DMAC ch 3 Transfer Request/GPIO 19 This pin is used as the DMAC ch 3 transfer request and as a general-purpose I/O port (GPIO) .
186	395	DACK#[2]/ DREQ#[6]/ PP[20]	Input/ output	TS	Yes	DMAC ch 2 Transfer Acknowledge/DMAC ch 6 Transfer Request/GPIO 20 This pin is used as the DMAC ch 2 transfer acknowledge signal, as the DMAC ch 6 transfer request, and as a general-purpose I/O port (GPIO) .
271	306	DACK#[3]/ DREQ#[7]/ PP[21]	Input/ output	TS	Yes	DMAC ch 3 Transfer Acknowledge/DMAC ch 7 Transfer Request/GPIO 21 This pin is used as the DMAC ch 3 transfer acknowledge signal, as the DMAC ch 7 transfer request, and as a general-purpose I/O port (GPIO) .

5. ICE Interface

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
238	267	ERST#	Input	PD	Yes	ESB Reset For the printed circuit board using the ICE, connect the connector intended for the ICE to this pin; for the printed circuit board not using the ICE, open this pin.
317	358	HRST#	Input	—	Yes	Hard Reset This is the reset input dedicated to the ICE. This pin function is equivalent to reset by the debugger hardware reset command. Reset by this pin will not reset debug related settings, so this pin can be used for debugging the reset sequence, etc. When using this pin, connect the reset switch signal to this pin; when not using this pin, fix it to the High level.
388	60	ECV	Input	PU	Yes	ESB Command Valid Command valid signal for ICE interface. For the printed circuit board using the ICE, connect the connector intended for the ICE to this pin; for the printed circuit board not using the ICE, open this pin.
151	168	ED	Input/ output	TS/ PD	Yes	ESB Data Data I/O signal for ICE interface. For the printed circuit board using the ICE, connect the connector intended for the ICE to this pin; for the printed circuit board not using the ICE, open this pin.
389	359	ECLK	Output	TS	Yes	ESB Clock Clock signal (output) for ICE interface. For the printed circuit board using the ICE, connect the connector intended for the ICE to this pin; for the printed circuit board not using the ICE, open this pin.

6. Reset-related Pin

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
57	360	PRST#	Input	—	Yes	Power-on Reset This is the level trigger initialization signal. Apply the L level to this pin for 16 CLKIN clock cycles or more. This pin is used to cause a power-on reset; it initializes all registers and sequencers except cache and GR/FR.
321	363	RSTOUT#	Output	SD	Yes	Reset Output This signal is asserted during a power-on reset. The power-on reset operation is prolonged in the LSI until the oscillation stabilization wait time for the internal PLL has elapsed. Consequently, use this signal to detect that the power-on reset operation has been completed in the LSI. When HRST# is asserted with the ICE used, this signal (RSTOUT#) is asserted as in the power-on reset.
239	169	RAMBOOT#	Input	—	Yes	RAM Boot A software reset can be caused by applying a Low level to this pin. When this signal and the PRST# pin are asserted simultaneously, the power-on reset operation is preferred. At a power-on reset, the level input to this pin is reflected in the SA bit of the register HSR0, and then the reset vector address is determined as shown below based on the SA bit. Low level : 0x00000000 High level : 0xFF000000

7. CPU Status

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
181	300	CPUHOLD	Output	SD	Yes	CPU Hold Signal indicating that CPU stops in hold state.

8. Clock

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
154	271	CLKIN	Input	—	Yes	Clock Input External clock are input to this pin.
58 153 240 319	270 361 63 170	CMODE[3] CMODE[2] CMODE[1] CMODE[0]	Input	—	Yes	Clock Mode Determines operating frequency of each section in LSI.

9. Pin Related to JTAG

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
237	357	TDI	Input	PU	No	Test Data Input This is the test data input pin. This signal is sampled on the rising edge of TCK.
236	166	TDO	Output	TS	No	Test Data Output This is the test data output pin. This drives active when the ATP controller is the Shift-IR or Shift-DR state. This signal changes on the falling edge of TCK.
150	266	TMS	Input	PU	No	Test Mode Select This is the test mode select pin. This signal is sampled on the rising edge of TCK.
316	59	TCK	Input	PU	No	Test Clock This is the test clock pin.
55	167	TRST#	Input	PU	No	Test Reset This is the TAP controller asynchronous reset. This pin initializes the TAP controller. When not using the JTAG function on the printed circuit board, input the same signal as PRST# to this pin.

10. Test

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
145	163	TESTMODE	Input	—	Yes	Test Mode Input Fix it at Low level on the printed circuit board.
234	54	TDC	Input	—	No	Test Input Fix it at Low level on the printed circuit board.
315	265	MTESTMODE	Input	—	Yes	UITEST MODE Input Fix it at Low level on the printed circuit board.

11. VDC Pin

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
114 15 362 287 204 113 14 13	127 230 325 15 126 229 324 14	VDR[7]/VDCR[7]/AVPP[23] VDR[6]/VDCR[6]/AVPP[22] VDR[5]/VDCR[5]/AVPP[21] VDR[4]/VDCR[4]/AVPP[20] VDR[3]/VDCR[3]/AVPP[19] VDR[2]/VDCR[2]/AVPP[18] VDR[1]/VDCR[1]/AVPP[17] VDR[0]/VDCR[0]/AVPP[16]	Input/ output	TS	Yes	R component output/Cr component output/GPIO These pins are display video data output pins. In the RGB mode, the red component is output. In the 24-bit YC mode, Cr component is output. These pins are shared by GPIO unit and set as GPIO input setting after reset.
116 17 364 289 206 115 16 205	328 18 129 232 327 17 128 16	VDG[7]/VDY[7]/VDX[7] VDG[6]/VDY[6]/VDX[6] VDG[5]/VDY[5]/VDX[5] VDG[4]/VDY[4]/VDX[4] VDG[3]/VDY[3]/VDX[3] VDG[2]/VDY[2]/VDX[2] VDG[1]/VDY[1]/VDX[1] VDG[0]/VDY[0]/VDX[0]	Output	TS	Yes	G Component output/Y component output/YC multiplexed output These pins are display video data output pins. In the RGB mode, the green component is output. Also, in the 16-bit or 24-bit YC mode, the Y component is output. When 8-bit YC mode is selected, multiplexed pixel data is output.
118 19 366 291 208 117 18 207	132 235 330 20 131 234 329 233	VDB[7]/VDCX[7]/VDCB[7]/ AVPP[39] VDB[6]/VDCX[6]/VDCB[6]/ AVPP[38] VDB[5]/VDCX[5]/VDCB[5]/ AVPP[37] VDB[4]/VDCX[4]/VDCB[4]/ AVPP[36] VDB[3]/VDCX[3]/VDCB[3]/ AVPP[35] VDB[2]/VDCX[2]/VDCB[2]/ AVPP[34] VDB[1]/VDCX[1]/VDCB[1]/ AVPP[33] VDB[0]/VDCX[0]/VDCB[0]/ AVPP[32]	Input/ output	TS	Yes	B Component output/C component output/Cb component output/ GPIO These pins are display video data output pins. In the RGB mode, the blue component is output. In the 16-bit YC mode, the Cb component and the C_r component are time-shared and output. Moreover, in the 24-bit YC mode, Cb component is output. These pins are shared by GPIO unit and set as GPIO input setting after reset.
292	331	VDHSYNC/VDHSYNC#	Output	TS	Yes	Horizontal synchronous signal output This pin is for display synchronous signal output. Its polarity is programmable.
367	236	VDVSYNC/VDVSYNC#	Output	TS	Yes	Vertical synchronous signal output This pin is for display synchronous signal output. Its polarity is programmable.

(Continued)

(Continued)

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
368	134	VDPCLKIN	Input	—	Yes	Vertical pixel clock input This pin inputs a basic clock to generate display pixel clock output.
209	21	VDCLKOUT	Output	TS	Yes	Display pixel clock output Pixel data is output in synchronization with this signal.
20	133	ENABLE/ENABLE#	Output	TS	Yes	Pixel output enable This signal shows that effective pixel data is output. Its polarity is programmable.
119	22	TOPFIELD/TOPFIELD#	Output	TS	Yes	Top field This pin shows that the top field is displayed. Its polarity is programmable.
120	333	DISABLE	Input	—	Yes	Video output disable When this signal is asserted, VDR[7 : 0]/VDCR[7 : 0], VDG[7 : 0]/VDY[7 : 0], VDB[7 : 0]/VDCX[7 : 0]/VDCB[7 : 0], VDHSYNC, VDVSYNC, and VDCLKOUT go in to the high-impedance state. However, ordinary operation continues inside.

12. VCC Pin

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
201 10 109 200 283 358 9 108	11 320 10 121 224 319 9 120	VCR[7]/VCCR[7]/AVPP[15] VCR[6]/VCCR[6]/AVPP[14] VCR[5]/VCCR[5]/AVPP[13] VCR[4]/VCCR[4]/AVPP[12] VCR[3]/VCCR[3]/AVPP[11] VCR[2]/VCCR[2]/AVPP[10] VCR[1]/VCCR[1]/AVPP[9] VCR[0]/VCCR[0]/AVPP[8]	Input/ output	TS	Yes	R component input/Cr component input/GPIO These pins are capture video data input pins. In the RGB mode, the red component is input. In the 24-bit YC mode, Cr component is input. These pins are shared by GPIO unit and set as GPIO input setting after reset.
281 356 7 106 197 280 355 6	7 118 221 316 6 117 220 315	VCG[7]/VCY[7]/VCX[7] VCG[6]/VCY[6]/VCX[6] VCG[5]/VCY[5]/VCX[5] VCG[4]/VCY[4]/VCX[4] VCG[3]/VCY[3]/VCX[3] VCG[2]/VCY[2]/VCX[2] VCG[1]/VCY[1]/VCX[1] VCG[0]/VCY[0]/VCX[0]	Input	—	Yes	G Component input/Y component input/YC multiplexed input These pins are capture video data input pins. In the RGB mode, the green component is input. Also, in the 24-bit YC mode, the Y component is input. When 8-bit YC mode is selected, multiplexed pixel data is output.
112 12 111 202 285 360 11 110	125 124 227 322 12 123 226 321	VCB[7]/VCCX[7]/VCCB[7]/ AVPP[31] VCB[6]/VCCX[6]/VCCB[6]/ AVPP[30] VCB[5]/VCCX[5]/VCCB[5]/ AVPP[29] VCB[4]/VCCX[4]/VCCB[4]/ AVPP[28] VCB[3]/VCCX[3]/VCCB[3]/ AVPP[27] VCB[2]/VCCX[2]/VCCB[2]/ AVPP[26] VCB[1]/VCCX[1]/VCCB[1]/ AVPP[25] VCB[0]/VCCX[0]/VCCB[0]/ AVPP[24]	Input/ output	TS	Yes	B component input/C component input/Cb component input/GPIO These pins are capture video data input pins. In the RGB mode, the blue component is input. Also, in the 16-bit YC mode, Cb component and Cr component are time-shared and input. Moreover, in the 24-bit YC mode, Cb component is input. These pins are shared by GPIO unit and set as GPIO input setting after reset.
198	317	VCHSYNC/VCHSYNC#	Input	—	Yes	Horizontal synchronous signal input This pin is a capture synchronous signal input pin. Its polarity is programmable.
107	222	VCVSYNC/VCVSYNC#	Input	—	Yes	Vertical synchronous signal input This pin is a capture synchronous signal input pin. Its polarity is programmable.
357	8	VCDCLKIN	Input	—	Yes	Capture pixel clock input This pin is a sampling clock for capture. The edge to use is programmable.

13. Audio Pin

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
213	137	SDO/DX	Output	TS	Yes	Audio data output Audio serial data is output.
370	240	LRCKO/FS0	Output	SD	Yes	LR clock output/CH0 synchronous signal LR clock is output when it is I²S and MSB-Justified output. Moreover, if it is output that supports PCM highway, CH0 synchronous signal FS0 is output.
295	25	BCKO/MCLK	Output	SD	Yes	Bit clock output This pin is for bit clock output for audio input/output. Input/output that supports PCM highway always operates in the master mode, therefore, MCLK output by MB93461 is used for input as well.
294	135	SDI/DR	Input	—	Yes	Audio data input This pin is for audio serial data input.
212	136	LRCKI/FS1	Input/output	TS	Yes	LR clock input/CH1 synchronous signal output In the case of I²S and MSB-Justified input, it becomes LR clock input. Moreover, in the case of input/output that supports PCM highway, CH1 synchronous signal FS1 is output.
369	24	BCKI	Input	—	Yes	Bit clock input This pin is for the input of bit clock used for I²S and MSB-justified audio input.
211	238	FSCKI	Input	—	Yes	Basic clock input for audio output This pin is for the input of basic clocks (256f_S/384f_S/512f_S/756f_S) to generate bit clock of MSB-justified or I²S audio output, LR clock and MCLK, FS0 and FS1 at supporting PCM highway.

14. USB/USB-Host

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
276	312	UDP	Input/ output	TS	No	USB D+ signal This pin is for differential signal (+) of USB function.
191	109	UDM	Input/ output	TS	No	USB D– signal This pin is for differential signal (–) of USB function.
190	400	USCKI	Input	—	Yes	USB clock input This pin inputs 48 MHz clock that is required by USB interface.
353	3	UDP1	Input/ output	TS	No	USB D+ signal This pin is for differential signal (+) of USB host.
278	313	UDM1	Input/ output	TS	No	USB D- signal This pin is for differential signal (–) of USB host.
354	314	HOVRCUR#	Input	—	Yes	USB Over Current Detection This signal is asserted when over current occurs in the down stream. It is read to the Over Current Indicator of HcRhstatus. Over-Current mode is set by No Over Current Protection of HcRh Descriptor A and Over CurrentProtection Mode. In the Individual over-current mode, it is read into Port Over Current Indicator of HcRh Port Status. This pin must be pulled up on the printed circuit board if not used.
5	4	HPWREN	Output	SD	Yes	USB Port Power Enable Global power to the USB port is controlled by this signal. When No Power Switching is set, this signal is always active.

15. I^2C Pin

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
216 297	242 335	SCL[1] SCL[0]	Input/output	OD	No	I^2C clock These pins are used for a clock signal of the I^2C bus. SCL[0] corresponds to I^2C ch 0; SCL[1] corresponds to I^2C ch 1.
126 215	31 140	SDA[1] SDA[0]	Input/output	OD	No	I^2C data These pins are used for data signals for the I^2C bus. SDA[0] corresponds to I^2C ch 0; SDA[1] corresponds to I^2C ch 1.

16. SD/MS Pin

Pin No.		Pin name	Direction	Type	BS	Description
BGA	PFBGA					
189	107	SDCKI/ MSCKI	Input	—	Yes	Clock input for the SD/Memory Stick If both of SD and MS are not used, set this pin to the “H” level on the printed circuit board.
349	105	SDWP/ MSDIRS	Input/ output	—	Yes	Data direction output of SDDAT[0]/MSDIO[0] If both of SD and MS are not used, set this pin to the “H” level on the printed circuit board.
418	397	MSDIRP	Input/ output	—	Yes	Data direction output of SDDAT[3 : 1]/ MSDIO[3 : 1] If both of SD and MS are not used, set this pin open on the printed circuit board.
351	310	SDCD/MSCD	Input	—	Yes	SD/Memory Stick insertion/extraction detection signal If both of SD and MS are not used, set this pin to the “H” level on the printed circuit board.
95	308	SDCMD/MSBS	Input/ output	SD	Yes	SD command I/O/Memory Stick bus state signal If both of SD and MS are not used, set this pin to the “H” level on the printed circuit board.
272	210	SDCLK/MSCLK	Output	SD	Yes	Transfer clock output for SD/Memory Stick If both of SD and MS are not used, set this pin open on the printed circuit board.
188	211	SDDAT[0]/MSDIO[0]	Input/ output	TS	Yes	Data signal for SD/Memory Stick (at serial) If both of SD and MS are not used, set this pin to the “H” level on the printed circuit board.
419 350 273	309 398 106	SDDAT[3]/MSDIO[3] SDDAT[2]/MSDIO[2] SDDAT[1]/MSDIO[1]	Input/ output	TS	Yes	Data signal for SD/Memory Stick (at parallel) If both of SD and MS are not used, set this pin to the “H” level on the printed circuit board.
420	213	SDMSSELECT	Input	—	Yes	SD/Memory Stick selection signal input If both of SD and MS are not used, set this pin to the “H” level on the printed circuit board.

Note : Customers are advised to consult with our sales representatives, if you use SD or MS.

■ PIN STATE

H : Indicates high level
L : Indicates low level
HiZ : Indicates high-impedance state
X : Indicates either high level or low level
A : Indicates output of clock

Note : Initial value : Indicates pin state immediately after power-on reset. The meaning of each symbol is given below :

Pin Name	Initial state	Core sleep mode	Bus sleep mode	PLL operation mode	PLL stop mode
BREQ#	—	—	—	—	—
BGNT#	H	Operation	H	H	H
A[31 : 2]	HiZ	Operation	X	X	X
D[31 : 0]	HiZ	Operation	HiZ	HiZ	HiZ
BE[0 : 3]/BE#[0 : 3]	HiZ	Operation	X	X	X
BS# , RD# , WE#	HiZ	Operation	H	H	H
DIR	HiZ	Operation	X	X	X
RDY#	HiZ	Operation	HiZ	HiZ	HiZ
ERR#	—	—	—	—	—
CS#[3 : 0]	H	Operation	H	H	H
CS#[7 : 4]/IRQ#[7 : 4]	HiZ	Operation	H or HiZ	H or HiZ	H or HiZ
IBW	—	—	—	—	—
BSTREQ#	HiZ	Operation	H	H	H
BSTACK#	HiZ	Operation	HiZ	HiZ	HiZ
BCLKO	L	Operation	Operation	L	L
DCS#[3 : 0]	H	Operation	L	L	L
DBA[1 : 0]	L	Operation	X	X	X
DA[12 : 0]	X	Operation	X	X	X
DRAS# , DCAS#	H	Operation	L	L	L
DWE#	H	Operation	H	H	H
DCKE	H	Operation	L	L	L
DDQM[0 : 3]	H	Operation	H	H	H
DDQ[31 : 0]	HiZ	Operation	HiZ	HiZ	HiZ
DCLK	L	Operation	Operation	Operation	L
DCLKFB	—	—	—	—	—
IRQ#[3 : 0]/PP[03 : 00]	HiZ	Operation	Operation	X or HiZ	X or HiZ
TOUT[0]/GATE[0]/PP[04]	HiZ	Operation	Operation	X or HiZ	X or HiZ
TOUT[1]/GATE[1]/PP[05]	HiZ	Operation	Operation	X or HiZ	X or HiZ

(Continued)

Pin Name	Initial state	Core sleep mode	Bus sleep mode	PLL operation mode	PLL stop mode
RXD[0]/PP[06]	HiZ	Operation	Operation	X or HiZ	X or HiZ
TXD[0]/PP[07]	HiZ	Operation	Operation	X or HiZ	X or HiZ
CTS#[0]/PP[08]	HiZ	Operation	Operation	X or HiZ	X or HiZ
RTS#[0]/PP[09]	HiZ	Operation	Operation	X or HiZ	X or HiZ
RXD[1]/PP[10]	HiZ	Operation	Operation	X or HiZ	X or HiZ
TXD[1]/PP[11]	HiZ	Operation	Operation	X or HiZ	X or HiZ
DREQ#[0]/PP[12]	HiZ	Operation	X or HiZ	X or HiZ	X or HiZ
DACK#[0]/PP[13]	HiZ	Operation	X or HiZ	X or HiZ	X or HiZ
DONE#[0]/DREQ#[4]/PP[14]	HiZ	Operation	X or HiZ	X or HiZ	X or HiZ
DREQ#[1]/PP[15]	HiZ	Operation	X or HiZ	X or HiZ	X or HiZ
DACK#[1]/PP[16]	HiZ	Operation	X or HiZ	X or HiZ	X or HiZ
DONE#[1]/DREQ#[5]/PP[17]	HiZ	Operation	X or HiZ	X or HiZ	X or HiZ
DREQ#[2]/PP[18]	HiZ	Operation	X or HiZ	X or HiZ	X or HiZ
DREQ#[3]/PP[19]	HiZ	Operation	X or HiZ	X or HiZ	X or HiZ
DACK#[2]/DREQ#[6]/PP[20]	HiZ	Operation	X or HiZ	X or HiZ	X or HiZ
DACK#[3]/DREQ#[7]/PP[21]	HiZ	Operation	X or HiZ	X or HiZ	X or HiZ
ERST# , HRST#	—	—	—	—	—
ECV	—	—	—	—	—
ED	HiZ	HiZ	HiZ	HiZ	HiZ
ECLK	L	L	L	L	L
PRST#	—	—	—	—	—
RSTOUT#	L	Operation	Operation	Operation	Operation
RAMBOOT#	—	—	—	—	—
CPUHOLD	L	X	X	X	X
CLKIN	—	—	—	—	—
CMODE[3 : 0]	—	—	—	—	—
TDI	—	—	—	—	—
TDO	HiZ	HiZ	HiZ	HiZ	HiZ
TMS , TCK , TRST#	—	—	—	—	—
TESTMODE , TDC , MTESTMODE	—	—	—	—	—
VDR[7 : 0]/VDCR[7 : 0] /AVPP[23 : 16]	—	Operation	X or HiZ	X or HiZ	X or HiZ
VDG[7 : 0]/VDY[7 : 0]/VDX[7 : 0]	—	Operation	X	X	X

(Continued)

Pin Name	Initial state	Core sleep mode	Bus sleep mode	PLL operation mode	PLL stop mode
VDB[7 : 0]/VDCX[7 : 0]/ VDCB[7 : 0]/AVPP[39 : 32]	—	Operation	X or HiZ	X or HiZ	X or HiZ
VDHSYNC/VDHSYNC#	—	Operation	X	X	X
VDVSYNC/VDVSYNC#	—	Operation	X	X	X
VDPCLKIN	—	—	—	—	—
VDCLKOUT	—	Operation	Operation	Operation	Operation
ENABLE/ENABLE#	—	Operation	X	X	X
TOPFIELD/TOPFIELD#	—	Operation	X	X	X
DISABLE	—	—	—	—	—
VCR[7 : 0]/VCCR[7 : 0]/ AVPP[15 : 8]	—	Operation	X or HiZ	X or HiZ	X or HiZ
VCG[7 : 0]/VCY[7 : 0]/VCX[7 : 0]	—	—	—	—	—
VCB[7 : 0]/VCCX[7 : 0]/ VCCB[7 : 0]/AVPP[31 : 24]	—	Operation	X or HiZ	X or HiZ	X or HiZ
VCHSYNC/VCHSYNC#	—	—	—	—	—
VCVSYNC/VCVSYNC#	—	—	—	—	—
VCDCLKIN	—	—	—	—	—
SDO/DX	—	Operation	X	X	X
LRCKO/FS0	—	Operation	Operation	Operation	Operation
BCKO/MCLK	—	Operation	Operation	Operation	Operation
SDI/DR	—	—	—	—	—
LRCKI/FS1	—	Operation	X or HiZ	X or HiZ	X or HiZ
BCKI	—	—	—	—	—
FSCKI	—	—	—	—	—
UDP	—	Operation	HiZ	HiZ	HiZ
UDM	—	Operation	HiZ	HiZ	HiZ
USCKI	—	—	—	—	—
UDP1	—	Operation	HiZ	HiZ	HiZ
UDM1	—	Operation	HiZ	HiZ	HiZ
HOVRCUR#	—	—	—	—	—
HPWREN	—	Operation	X	X	X
SCL[1 : 0]	—	HiZ	HiZ	HiZ	HiZ
SDA[1 : 0]	—	HiZ	HiZ	HiZ	HiZ
SDCKI/MSCKI	—	—	—	—	—
SDWP/MSDIRS	—	Operation	X or HiZ	X or HiZ	X or HiZ
MSDIRP	—	Operation	X	X	X

(Continued)

(Continued)

Pin Name	Initial state	Core sleep mode	Bus sleep mode	PLL operation mode	PLL stop mode
SDCD/MSCD	—	—	—	—	—
SDCMD/MSBS	—	Operation	X or HiZ	X or HiZ	X or HiZ
SDCLK/MSCLK	—	Operation	Operation	Operation	Operation
SDDAT[0]/MSDIO[0]	—	Operation	X or HiZ	X or HiZ	X or HiZ
SDDAT[3 : 1]/MSDIO[3 : 1]	—	Operation	X or HiZ	X or HiZ	X or HiZ
SDMSSELECT	—	—	—	—	—

■ HANDLING DEVICES

• Preventing latch-up

CMOS IC chips may suffer latch-up under the following conditions :

- A voltage higher than V_{DE} or lower than V_{SS} is applied to an input or output pin.
- A voltage higher than the rated voltage is applied between VDE pin and VSS pin.

Latch-up may increase the power supply current drastically, causing thermal damage to the device.

For the same reason, care must also be taken in not allowing the analog power-supply voltage (V_{DD}) to exceed the digital power-supply voltage.

• Handling unused pins

Leaving unused input pins open may result in misbehavior or latch-up and possible permanent damage of the device. Therefore they must be pulled up or pulled down through resistors. In this case those resistors should be more than 2 kΩ.

Unused bi-directional pins should be set to the output state and can be left open, or the input state with the above described connection.

When not using USB/USB-Host pin, fix both UDP1 and UDM1 to the opposite level for each other.

• Power supply pins

In products with multiple VDE, VDD, or VSS pins, the pins of a same potential are internally connected in the device to avoid abnormal operations including latch-up. However you must connect the pins to an external power and a ground line to lower the electro-magnetic emission level, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total current rating.

Make sure to connect VDE, VDD, and VSS pins via the lowest impedance to power lines.

It is recommended to provide a bypass capacitor of around 0.1 μF between VDE, VDD, and VSS pins near the device.

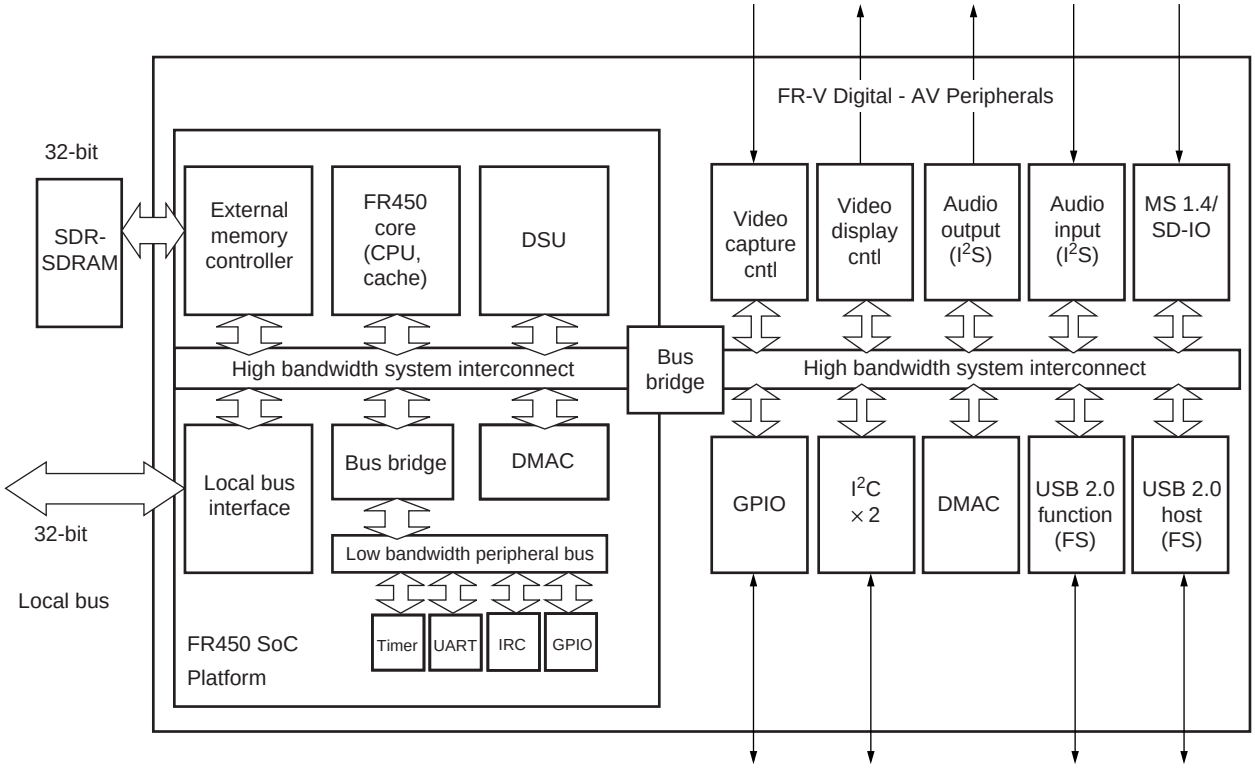
• Pull-up/down resistors

The MB93461 does not support internal pull-up/down resistors (except PU/PD Pin Type) . Use external components where needed.

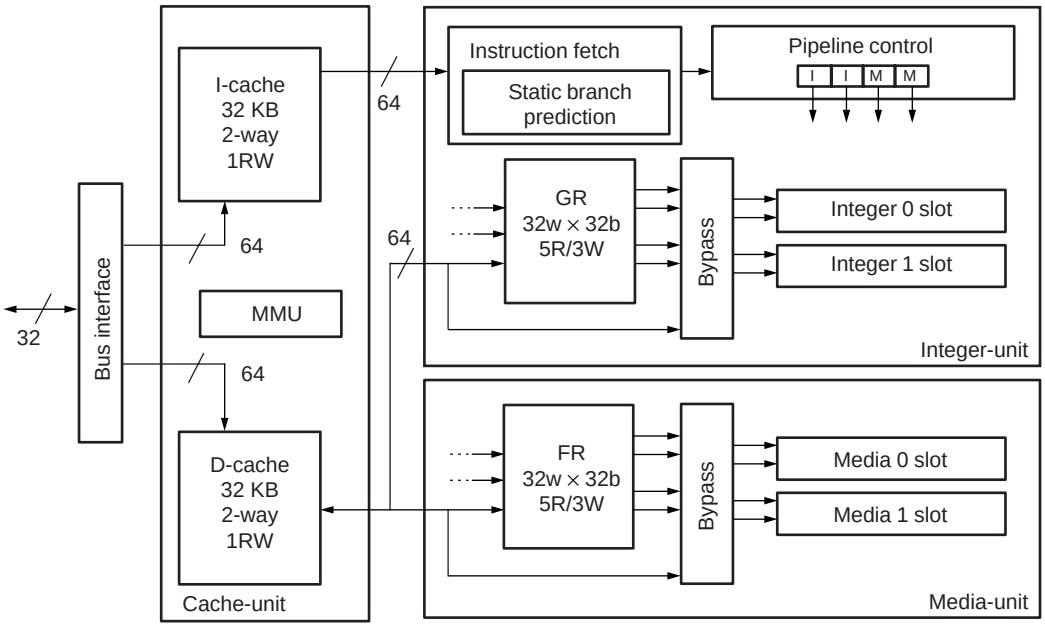
• N.C. Pin

The N.C. (internally connected) pin must be opened for use.

■ BLOCK DIAGRAM



FR450 core block diagram



■ ELECTRICAL CHARACTERISTICS

1. Absolute Maximum Ratings

Parameter	Symbol	Rating		Unit
		Min	Max	
Power supply voltage (External)	V_{DE}	V_{SS} – 0.5	V_{SS} + 4.0	V
Power supply voltage (Internal)	V_{DD}	V_{SS} – 0.5	V_{SS} + 1.8	V
Input voltage	V_I	V_{SS} – 0.5	V_{DE} + 0.5 (≤ 4.0)	V
Storage temperature	T_{STG}	–55	+ 125	°C

Note : V_{SS} = 0 V

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

2. Recommended Operating Conditions

[V_{SS} = 0 V]

Parameter	Symbol		Value			Unit
			Min	Typ	Max	
Power supply voltage (External)	V_{DE}	360 MHz	3.15	3.3	3.45	V
		400 MHz	3.15	3.3	3.45	V
Power supply voltage (Internal)	V_{DDI}	360 MHz	1.235	1.3	1.365	V
		400 MHz	1.33	1.4	1.47	V
“L” level input voltage	V_{IL}		–0.3	—	0.8	V
“H” level input voltage	V_{IH}		2.0	—	V_{DE} + 0.3	V
Operating temperature	T_a		0	25	70	°C

USB

[V_{SS} = 0 V]

Parameter	Symbol	Value			Unit
		Min	Typ	Max	
“H” level input voltage	V_{IHU}	2.0	—	—	V
“L” level input voltage	V_{ILU}	—	—	0.8	V
Differential input sensitivity	V_{DIU}	0.2	—	—	V
Differential common mode range	V_{CMU}	0.8	—	2.5	V
“H” level output voltage	V_{OHU}	2.8	—	3.45	V
“L” level output voltage	V_{OLU}	0.0	—	0.3	V
Output signal crossover voltage	V_{CRSU}	1.3	—	2.0	V
Bus pull-up/down resistor on upstream port	Rpu *1	1.425	—	1.575	kΩ
	Rpd *2	14.25	—	15.75	kΩ
Termination voltage on upstream port pull-up	V_{TERM}	3.15	—	3.45	V

*1 : If USB function is used , it is necessary to attach “Rpu” outside to D+ or D–.
*2 : If USB host is used , it is necessary to attach “Rpd” outside to D+ and D–.

Notes : Board Wiring

- For connecting the power supply and ground (GND) , use multiple VDD and VSS pins. The system board based on the MB93461 must be a multi-layer board containing power supply (V_{DD}) and GND (V_{SS}) layers for stable power supply.
- Insert sufficient decoupling capacitors (condensers) near the MB93461. Changes to the output levels of many of the output pins on the MB93461 (in particular, those with large load capacitance) may cause variation in power supply.
- For those systems which run at a high frequency, low-inductance capacitors and mutual wiring are recommended. Inductance can be lowered by shortening the distance between the processor and decoupling capacitor.

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device’s electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their FUJITSU representatives beforehand.

3. DC Characteristics

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Parameter	Symbol		Condition	Value			Unit
				Min	Typ	Max	
"L" level input voltage	V_{IL}		—	0	—	0.8	V
"H" level input voltage	V_{IH}		—	2.0	—	V_{DE}	V
"L" level output voltage	V_{OL}		I_{OL} = 100 µA	0	—	0.2	V
"H" level output voltage	V_{OH}		I_{OH} = –100 µA	V_{DE} – 0.2	—	V_{DE}	V
Input leakage current	I_{LI}		V_{IN} = 0 or V_{DE}	–5	—	5	µA
Tri-state output leakage current	I_{LZ}		V_{OUT} = 0 or V_{DE}	–5	—	5	µA
Power supply current (V_{DE})	I_{DE}	360 MHz	CMODE = 0x3, CLKIN = 60 MHz, (Dhrystone2.1 + DMA transfer) No Load	0	40	80	mA
		400 MHz	CMODE = 0x3, CLKIN = 66MHz, (Dhrystone2.1 + DMA transfer) No Load	0	44	88	mA
Power supply current (V_{DD})	I_{DD}	360 MHz	CMODE = 0x3, CLKIN = 60 MHz, (Dhrystone2.1 + DMA transfer)	—	196	420	mA
		400 MHz	CMODE = 0x3, CLKIN = 66 MHz, (Dhrystone2.1 + DMA transfer)	—	245	520	mA
At sleep power supply current	$I_{CORESLEEP}$	360 MHz	Core sleep mode, CLKIN = 60 MHz	—	70	—	mA
		400 MHz	Core sleep mode, CLKIN = 66 MHz	—	87	—	mA
	$I_{BUSSLEEP}$	360 MHz	Bus sleep mode, CLKIN = 60 MHz	—	32.4	—	mA
		400 MHz	Bus sleep mode, CLKIN = 66 MHz	—	40.6	—	mA
	I_{PLLON}	360 MHz	PLL On mode, CLKIN = 60 MHz	—	18.2	—	mA
		400 MHz	PLL On mode, CLKIN = 66 MHz	—	22.4	—	mA
	I_{PLLOFF}		PLL Stop mode, CLKIN = 0 MHz	—	5	—	mA
Capacity of pins	C_{PIN}		V_{DE} = V_I = 0, f = 1 MHz	—	—	16	pF

USB

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
“L” level output voltage	V_{OL}	I_{OL} = 20 mA	0	—	0.4	V
“H” level output voltage	V_{OH}	I_{OH} = –20 mA	V_{DE} – 0.5	—	V_{DE}	V
“L” level output current	I_{OL}	V_{OL} = 0.4 V	20	—	—	mA
“H” level output current	I_{OH}	V_{OH} = V_{DE} – 0.4 V	–20	—	—	mA
Output short-circuit current	I_{OS}	—	—	—	300	mA

I²C

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Parameter	Symbol	Conditions	Value			Unit
			Min	Typ	Max	
“L” level input voltage	V_{IL}	—	–0.5	—	0.3 × V_{DE}	V
“H” level input voltage	V_{IH}	—	0.7 × V_{DE}	—	V_{DE}	V
“L” level output voltage 1	V_{OL1}	I_{OL} = 3 mA	0	—	0.4	V
Schmitt trigger hysteresis	V_{HYS}	—	0.05 × V_{DE}	—	—	V
Data line leakage	I_I	—	–10	—	10	µA

4. AC Characteristics

(1) Local Bus Interface

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Item	Parameter		Reference Signal	360 MHz		400 MHz		Unit
				Min	Max	Min	Max	
CLKIN input	CLKIN period (T_{CLKIN})		—	15*	27*	15*	23.5*	ns
	CLKIN high time		—	6.0	—	6.0	—	ns
	CLKIN low time		—	6.0	—	6.0	—	ns
	CLKIN rise time		—	—	1.0	—	1.0	ns
	CLKIN fall time		—	—	1.0	—	1.0	ns
Local-bus I/F output	BGNT#	Output valid delay time	CLKIN rise	1.5	6.5	1.5	6.5	ns
	A [31 : 2]	Output valid delay time	CLKIN rise	1.5	6.5	1.5	6.5	ns
		Output hold time	CLKIN rise	1.5	—	1.5	—	ns
	D [31 : 0]	Output valid delay time	CLKIN rise	1.5	6.5	1.5	6.5	ns
		Output hold time	CLKIN rise	1.5	—	1.5	—	ns
	BE/BE# [0 : 3]	Output valid delay time	CLKIN rise	1.5	6.5	1.5	6.5	ns
		Output hold time	CLKIN rise	1.5	—	1.5	—	ns
	BS#	Output valid delay time	CLKIN rise	1.5	6.5	1.5	6.5	ns
		Output hold time	CLKIN rise	1.5	—	1.5	—	ns
	RD#	Output valid delay time	CLKIN rise	1.5	6.5	1.5	6.5	ns
	WE#	Output valid delay time	CLKIN fall	1.0	7.0	1.0	7.0	ns
	DIR	Output valid delay time	CLKIN rise	1.5	6.5	1.5	6.5	ns
		Output hold time	CLKIN rise	1.5	—	1.5	—	ns
	RDY#	Output valid delay time	CLKIN rise	1.5	6.5	1.5	6.5	ns
		Output hold time	CLKIN rise	1.5	—	1.5	—	ns
	CS# [3 : 0]	Output valid delay time	CLKIN rise	1.5	6.5	1.5	6.5	ns
	CS# [7 : 4]/ IRQ# [7 : 4]	Output valid delay time	CLKIN rise	1.5	6.5	1.5	6.5	ns
		Output hold time	CLKIN rise	1.5	—	1.5	—	ns
	BSTREQ#	Output valid delay time	CLKIN rise	1.5	6.5	1.5	6.5	ns
		Output hold time	CLKIN rise	1.5	—	1.5	—	ns
	BSTACK#	Output valid delay time	CLKIN rise	1.5	6.5	1.5	6.5	ns
		Output hold time	CLKIN rise	1.5	—	1.5	—	ns

* : Refer to “5. Clock Setting” for details.

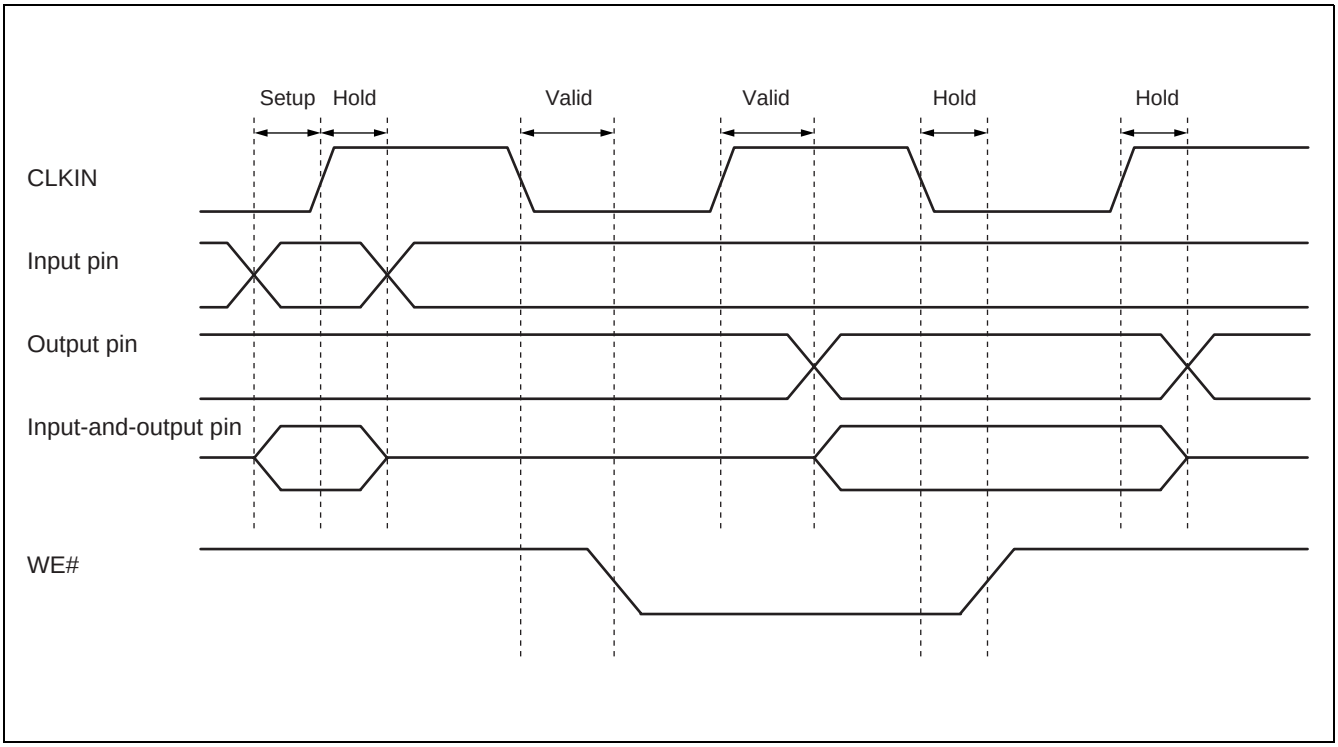
(Continued)

(Continued)

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Item	Parameter		Reference Signal	360MHz		400MHz		Unit
				Min	Max	Min	Max	
Local-bus I/F input	BREQ#	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	A [31 : 2]	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	D [31 : 0]	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	BE/BE# [0 : 3]	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	BS#	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	DIR	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	RDY#	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	ERR#	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	CS# [7 : 4]/ IRQ# [7 : 4]	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	IBW	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	BSTREQ#	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	BSTACK#	Input setup time	CLKIN rise	3.0	—	3.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns

Notes :
- Each parameter is valid within the specified ranges of temperature and supply voltages unless otherwise noted.
  Each voltage value is based on the GND (V_{SS} = 0.0 V) level. The timing measurement reference point is 1.5 V, the input level is 0.4 V to 2.4 V, and the input rise time and fall time are 1.5 ns or less.
  The external output load capacitance is 30 pF.
- Maximum frequency of CLKIN varies depending on the setting of CMODE [0] to [3] pins. Please refer to " 5. Clock Setting."


Setup
Hold
Valid
Valid
Hold
Hold
CLKIN
Input pin
Output pin
Input-and-output pin
WE#

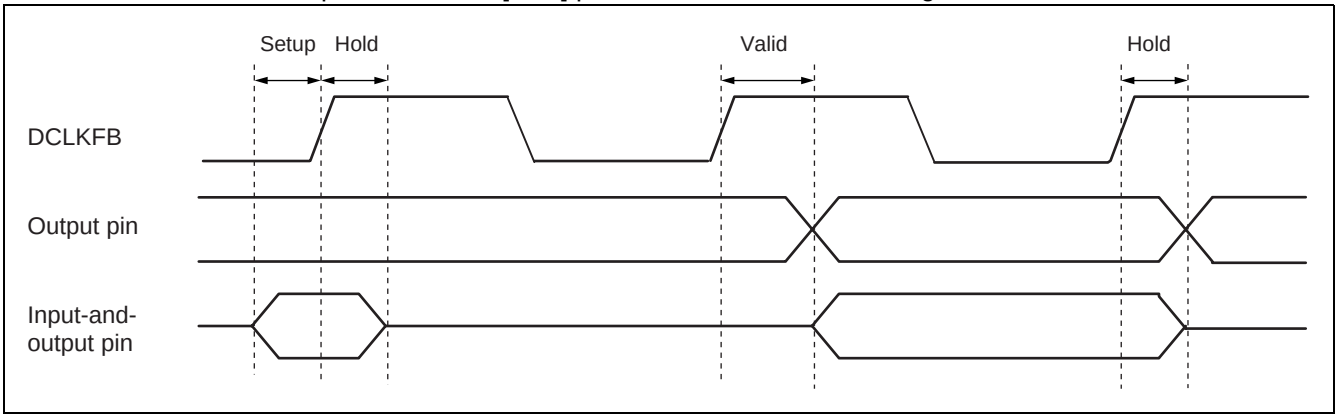
(2) SDRAM Interface

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Item	Parameter		Reference Signal	360 MHz		400 MHz		Unit
				Min	Max	Min	Max	
DCLKFB input	DCLKFB period (T_{DCLKFB})		—	7.5*	20*	7.5*	17.5*	ns
	DCLKFB high time		—	2.5	—	2.5	—	ns
	DCLKFB low time		—	2.5	—	2.5	—	ns
	DCLKFB rise time		—	—	1.0	—	1.0	ns
	DCLKFB fall time		—	—	1.0	—	1.0	ns
SDRAM I/F output	DCS# [3 : 0]	Output valid delay time	DCLKFB rise	1.0	4.5	1.0	4.5	ns
	DBA [1 : 0]	Output valid delay time	DCLKFB rise	1.0	4.5	1.0	4.5	ns
	DA [12 : 0]	Output valid delay time	DCLKFB rise	1.0	4.5	1.0	4.5	ns
	DRAS#	Output valid delay time	DCLKFB rise	1.0	4.5	1.0	4.5	ns
	DCAS#	Output valid delay time	DCLKFB rise	1.0	4.5	1.0	4.5	ns
	DWE#	Output valid delay time	DCLKFB rise	1.0	4.5	1.0	4.5	ns
	DCKE	Output valid delay time	DCLKFB rise	1.0	4.5	1.0	4.5	ns
	DDQM [0 : 3]	Output valid delay time	DCLKFB rise	1.0	4.5	1.0	4.5	ns
	DDQ [31 : 0]	Output valid delay time	DCLKFB rise	1.0	4.5	1.0	4.5	ns
		Output hold time	DCLKFB rise	1.0	—	1.0	—	ns
SDRAM I/F input	DDQ [31 : 0]	Input setup time	DCLKFB rise	1.0	—	1.0	—	ns
		Input hold time	DCLKFB rise	1.0	—	1.0	—	ns

* : This value is decided by CMODE.

Notes :
- Each parameter is valid within the specified ranges of temperature and supply voltages unless otherwise noted.
  Each voltage value is based on the GND (V_{SS} = 0.0 V) level. The timing measurement reference point is 1.5 V, the input level is 0.4 V to 2.4 V, and the input rise time and fall time are 1.5 ns or less unless otherwise noted.
  The external output load capacitance is 30 pF unless otherwise noted.
- The frequency of the input to DCLKFB and the output from DCLK is decided by the input frequency to CLKIN, and setup of a CMODE [3 : 0] pins. Refer to “5. Clock Setting” for details.



- This LSI outputs DCLK which is supplied to SDRAM as a clock. PLL is built into this LSI. Adjust the phase of DCLK so that the CLK pin of SDRAM and the internal phase in this LSI may be nearly equal. Therefore, when connecting, adjust the delay time of the feedback path from DCLK to DCLKFB, so that the phase of the clock input to DCLKFB which is the feedback signal to PLL and the phase of the clock (wave shape on the reception edge of DCLK) input to CLK of SDRAM may be nearly equal.

(3) General-purpose Peripheral Resource

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Item	Parameter		Reference Signal	360 MHz		400 MHz		Unit
				Min	Max	Min	Max	
Resources output	IRQ# [3 : 0]/ PP [03 : 00]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	TOUT[0]/ GATE[0]/ PP[04]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	TOUT[1]/ GATE[1]/ PP[05]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	RXD[0]/ PP[06]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	TXD[0]/PP[07]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	CTS# [0]/ PP[08]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	RST# [0]/ PP[09]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	RXD[1]/ PP[10]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	TXD[1]/PP[11]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	DREQ# [0]/ PP[12]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	DACK# [0]/ PP[13]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	DONE# [0]/ DREQ# [4]/ PP[14]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	DREQ# [1]/ PP[15]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	DACK# [1]/ PP[16]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	DONE# [1]/ DREQ# [5]/ PP[17]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns

(Continued)

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Item	Parameter		Reference Signal	360 MHz		400 MHz		Unit
				Min	Max	Min	Max	
Resources output	DREQ#[2]/ PP[18]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	DREQ#[3]/ PP[19]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	DACK#[2]/ DREQ#[6]/ PP[20]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
	DACK#[3]/ DREQ#[7]/ PP[21]	Output valid delay time	CLKIN rise	2.0	10.0	2.0	10.0	ns
		Output hold time	CLKIN rise	2.0	—	2.0	—	ns
Resources input	IRQ#[3 : 0]/ PP [03 : 00]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	TOUT[0]/ GATE[0]/ PP[04]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	TOUT[1]/ GATE[1]/ PP[05]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	RXD[0]/ PP[06]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	TXD[0]/PP[07]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	CTS#[0]/ PP[08]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	RST#[0]/ PP[09]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	RXD[1]/ PP[10]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	TXD[1]/PP[11]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	DREQ#[0]/ PP[12]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	DACK#[0]/ PP[13]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns

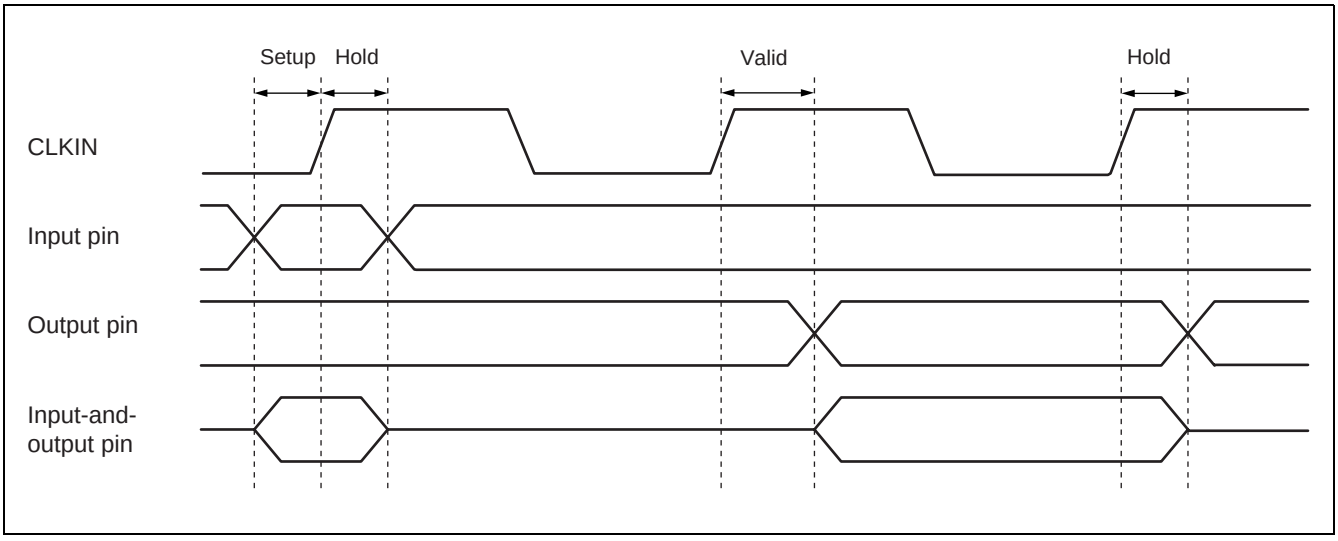
(Continued)

(Continued)

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Item	Parameter		Reference Signal	360 MHz		400 MHz		Unit
				Min	Max	Min	Max	
Resources input	DONE#[0]/ DREQ#[4]/ PP[14]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	DREQ#[1]/ PP[15]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	DACK#[1]/ PP[16]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	DONE#[1]/ DREQ#[5]/ PP[17]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	DREQ#[2]/ PP[18]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	DREQ#[3]/ PP[19]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	DACK#[2]/ DREQ#[6]/ PP[20]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns
	DACK#[3]/ DREQ#[7]/ PP[21]	Input setup time	CLKIN rise	4.0	—	4.0	—	ns
		Input hold time	CLKIN rise	1.5	—	1.5	—	ns

Note : Each parameter is valid within the specified ranges of temperature and supply voltages unless otherwise noted.
Each voltage value is based on the GND (V_{SS} = 0.0 V) level. The timing measurement reference point is 1.5 V, the input level is 0.4 V to 2.4 V, and the input rise time and fall time are 1.5 ns or less.
The external output load capacitance is 30 pF unless otherwise noted.



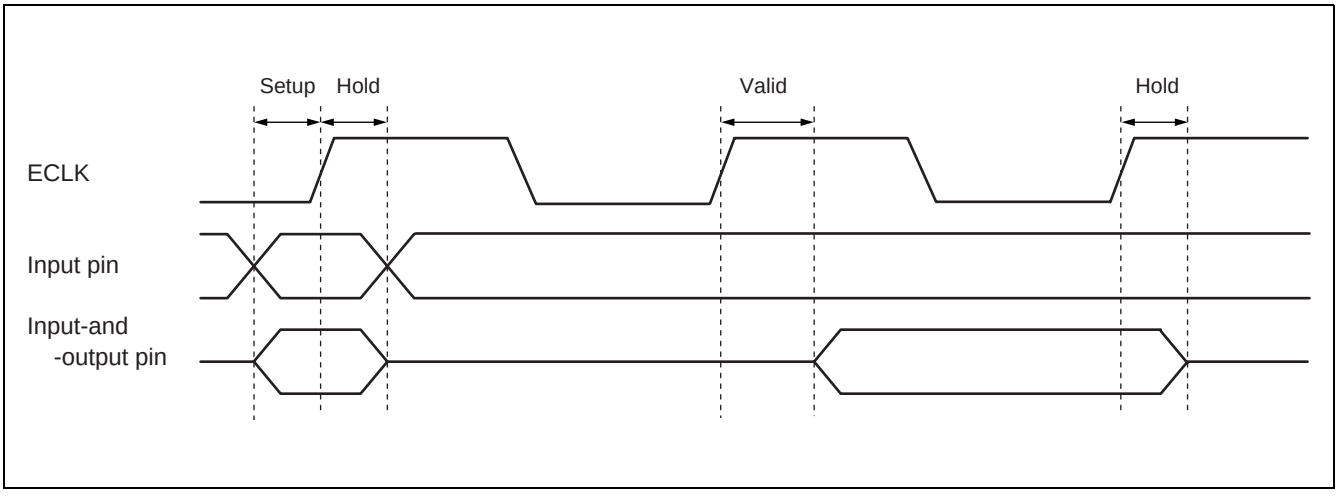
(4) ICE Interface

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Item	Parameter		Reference Signal	360 MHz		400 MHz		Unit
				Min	Max	Min	Max	
ECLK output	ECLK output period		—	30	—	30	—	ns
	ECLK output high time		—	13.0	—	13.0	—	ns
	ECLK output low time		—	13.0	—	13.0	—	ns
	ECLK output rise time		—	—	2.0	—	2.0	ns
	ECLK output fall time		—	—	2.0	—	2.0	ns
ICE output	ED	Output valid delay time	ECLK rise	—	8.0	—	8.0	ns
		Output hold time	ECLK rise	0.0	—	0.0	—	ns
ICE input	ERST#	Input setup time	ECLK rise	5.0	—	5.0	—	ns
		Input hold time	ECLK rise	0.0	—	0.0	—	ns
	HRST#	Low pulse width	—	16	—	16	—	T_{CLKIN}*
	ECV	Input setup time	ECLK rise	5.0	—	5.0	—	ns
		Input hold time	ECLK rise	0.0	—	0.0	—	ns
	ED	Input setup time	ECLK rise	5.0	—	5.0	—	ns
		Input hold time	ECLK rise	0.0	—	0.0	—	ns

* : Unit of T_{CLKIN} is CLKIN period. Please refer to “4. (1) Local Bus Interface”.

Note : Each parameter is valid within the specified ranges of temperature and supply voltages unless otherwise noted.
Each voltage value is based on the GND (V_{SS} = 0.0 V) level. The timing measurement reference point is 1.5 V, and the input level is 0.4 V to 2.4 V. The input rise time and fall time are 1.5 ns or less. The external output load capacitance is 30 pF unless otherwise noted.



(5) Reset-related Pin

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Item	Parameter		Reference Signal	360 MHz		400 MHz		Unit
				Min	Max	Min	Max	
Reset output	RSTOUT#	Output valid delay time	CLKIN rise	0	8.0	0	8.0	ns
Reset input	PRST#	Low pulse width	—	16	—	16	—	T_{CLKIN}*
Boot input	RAMBOOT#	Low pulse width	—	16	—	16	—	T_{CLKIN}*

* : Unit of T_{CLKIN} is CLKIN period. Please refer to “4. (1) Local Bus Interface”.

(6) CPU Status

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Item	Parameter		Reference Signal	360 MHz		400 MHz		Unit
				Min	Max	Min	Max	
CPU output	CPUHOLD	Output valid delay time	CLKIN rise	0	8.0	0	8.0	ns

(7) Clock

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Item	Parameter		Reference Signal	360 MHz		400 MHz		Unit
				Min	Max	Min	Max	
Clock mode input	CMODE[3 : 0]	Input setup time	—	Must be fixed to “H” or “L”				—
		Input hold time	—	Must be fixed to “H” or “L”				—

(8) Test

[360 MHz : V_{DE} = 3.3 V ± 0.15, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Item	Parameter		Reference Signal	360 MHz		400 MHz		Unit
				Min	Max	Min	Max	
Test mode input	TESTMODE	Input setup time	—	Must be fixed to “L”				—
		Input hold time	—	Must be fixed to “L”				—
	TDC	Input setup time	—	Must be fixed to “L”				—
		Input hold time	—	Must be fixed to “L”				—
	MTESTMODE	Input setup time	—	Must be fixed to “L”				—
		Input hold time	—	Must be fixed to “L”				—

(9) Video Display Controller (VDC)

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Item	Parameter		Reference Signal	360 MHz/400 MHz		Unit
				Min	Max	
VDC clock input	VDPCLKIN period		—	12.5	125	ns
	VDPCLKIN high time		—	4	—	ns
	VDPCLKIN low time		—	4	—	ns
VDC I/F output	VDR [7 : 0]/VDCR [7 : 0]	Output valid delay time	VDCLKOUT fall	–2	3	ns
		Output hold time	VDCLKOUT fall	–2	—	ns
	VDG [7 : 0]/VDY [7 : 0]/ VDX[7 : 0]	Output valid delay time	VDCLKOUT fall	–2	3	ns
	VDB [7 : 0]/VDCX[7 : 0]/ VDCB [7 : 0]	Output valid delay time	VDCLKOUT fall	–2	3	ns
		Output hold time	VDCLKOUT fall	–2	—	ns
	VDHSYNC/ VDHSYNC#	Output valid delay time	VDCLKOUT fall	–2	3	ns
	VDVSYNC/ VDVSYNC#	Output valid delay time	VDCLKOUT fall	–2	3	ns
	ENABLE/ENABLE#	Output valid delay time	VDCLKOUT fall	–2	3	ns
	TOPFIELD/ TOPFIELD#	Output valid delay time	VDCLKOUT fall	–2	3	ns
	VDCLKOUT*	Output valid delay time	VDPCLKIN rise	7	11	ns
VDC I/F input	DISABLE	Input setup time	VDPCLKIN rise	2.5	—	ns
		Input hold time	VDPCLKIN rise	1.5	—	ns

* : The falling edge of VDCLKOUT is synchronous with respect to the rising edge of VDPCLKIN.

Note : Each parameter is valid within the specified ranges of temperature and supply voltage unless otherwise noted. Each voltage value is based on the GND (V_{SS} = 0.0 V) level. The timing measurement reference point is 1.5 V, and the input level is 0.4 V to 2.4 V.
The external output load capacitance is 15 pF.

(10) Video Capture Controller (VCC)

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Item	Parameter		Reference Signal	360 MHz/400 MHz		Unit
				Min	Max	
VCC clock input	VCDCLKIN period		—	12.5	125	ns
	VCDCLKIN high time		—	4	—	ns
	VCDCLKIN low time		—	4	—	ns
VCC I/F input	VCR [7 : 0]/VCCR [7 : 0]	Input setup time	VCDCLKIN edge*	2.5	—	ns
		Input hold time	VCDCLKIN edge*	1.5	—	ns
	VCG[7 : 0]/VCY[7 : 0]/ VCX[7 : 0]	Input setup time	VCDCLKIN edge*	2.5	—	ns
		Input hold time	VCDCLKIN edge*	1.5	—	ns
	VCB[7 : 0]/VCCX[7 : 0]/ VCCB[7 : 0]	Input setup time	VCDCLKIN edge*	2.5	—	ns
		Input hold time	VCDCLKIN edge*	1.5	—	ns
	VCHSYNC/ VCHSYNC#	Input setup time	VCDCLKIN edge*	2.5	—	ns
		Input hold time	VCDCLKIN edge*	1.5	—	ns
	VCVSYNC/ VCVSYNC#	Input setup time	VCDCLKIN edge*	2.5	—	ns
		Input hold time	VCDCLKIN edge*	1.5	—	ns

*: The reference signal of VCC interface is decided by the setting of register in the VCC unit.
RCC.ES = 0 : falling edge of VCDCLKIN
RCC.ES = 1 : rising edge of VCDCLKIN
Please refer to MB93461 LSI specification.

Note : Each parameter is valid within the specified ranges of temperature and supply voltages unless otherwise noted.
Each voltage value is based on the GND (V_{SS} = 0.0 V) level. The timing measurement reference point is 1.5 V, and the input level is 1.0 V to 2.0 V.
The external output load capacitance is 30 pF.

(11) Audio

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Item	Parameter		Reference Signal	360 MHz/400 MHz		Unit
				Min	Max	
Audio clock input	FSCKI period		—	25	—	ns
	FSCKI high time		—	10.5	—	ns
	FSCKI low time		—	10.5	—	ns
	BCKI period		—	100	—	ns
	BCKI high time		—	42	—	ns
	BCKI low time		—	42	—	ns
Audio I/F output	SDO*	Output valid delay time	FSCKI rise	3	11	ns
	LRCKO*	Output valid delay time	FSCKI rise	3	11	ns
	BCKO*	Output valid delay time	FSCKI rise	3	11	ns
	LRCKI	Output valid delay time	FSCKI rise	3	11	ns
Audio I/F input	SDI	Input setup time	BCKI rise	15	—	ns
		Input hold time	BCKI rise	15	—	ns
	LRCKI	Input setup time	BCKI rise	15	—	ns
		Input hold time	BCKI rise	15	—	ns

* : LRCKO and SDO signals are generated with respect to the falling edge of BCKO (duty 50%) .

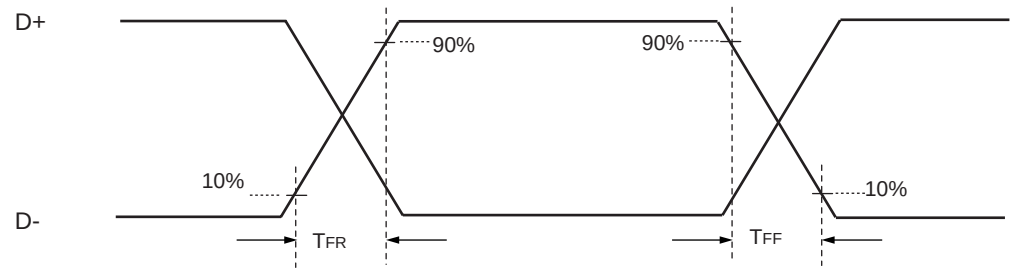
Note : Each parameter is valid within the specified ranges of temperature and supply voltages unless otherwise noted.
Each voltage value is based on the GND (V_{SS} = 0.0 V) level. The timing measurement reference point is 1.5 V, and the input level is 0.4 V to 2.4 V.
The external output load capacitance is 30 pF.

(12) USB Interface

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Item	Parameter		Reference Signal	360 MHz/400 MHz		Unit
				Min	Max	
USB clock input	USCKI period		—	20	—	ns
	USCKI high time		—	8	—	ns
	USCKI low time		—	8	—	ns
USB driver	D+/D− rise time	T_{FR}	—	4	20	ns
	D+/D− fall time	T_{FF}	—	4	20	ns
	Differential rise and fall time matching		—	90	111.11	%
	Driver output resistance		—	28	44	Ω

Notes :
- Frequency of USCKI is set to 48 MHz in order to carry out operation based on the standard of USB 2.0 FS. Furthermore, it is necessary to put in a clock with a frequency accuracy of 2500 ppm.
- In order to fulfill the standard of USB 2.0 FS, it is necessary to add 25 Ω to 30 Ω in-series resistance outside.



(13) I²C

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Item	Parameter		Reference Signal	360 MHz/400 MHz		Unit
				Min	Max	
I²C I/F output	SCL[1 : 0]	Output fall time	—	23*	250	ns
		Output rise time	—	23*	300	ns
	SDA[1 : 0]	Output fall time	—	23*	250	ns
		Output rise time	—	23*	300	ns

* : 20 + 0.1 × C (C = Capacitance of one bus line in pF)

Notes :
- Each parameter is valid within the specified ranges of temperature and supply voltages unless otherwise noted.
- Each voltage value is based on the GND (V_{SS} = 0.0 V) level. The timing measurement reference point is 1.5 V, the input level is 0.4 V to 2.4 V, and the input rise time and fall time are 1.5 ns or less.
- The external output load capacitance is 30 pF.

(14) GPIO

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Item	Parameter		Reference Signal	360 MHz/400 MHz		Unit
				Min	Max	
GPIO I/F output	AVPP[39 : 8]	Output valid delay time	—	—	—	ns
		Output hold time	—	—	—	ns
GPIO I/F input	AVPP[39 : 8]	Input setup time	—	—	—	ns
		Input hold time	—	—	—	ns

Notes :
- AVPP[39 : 8] is an asynchronous pin.
- Each parameter is valid within the specified ranges of temperature and supply voltages unless otherwise noted.
  Each voltage value is based on the GND (V_{SS} = 0.0 V) level. The timing measurement reference point is 1.5 V, and the input level is 0.4 V to 2.4 V.
  The external output load capacitance is 30 pF.

(15) Memory Stick Interface

Note : Customers are advised to consult with our sales representatives , if you use MS.

(16) SD-IO Interface

Note : Customers are advised to consult with our sales representatives , if you use SD.

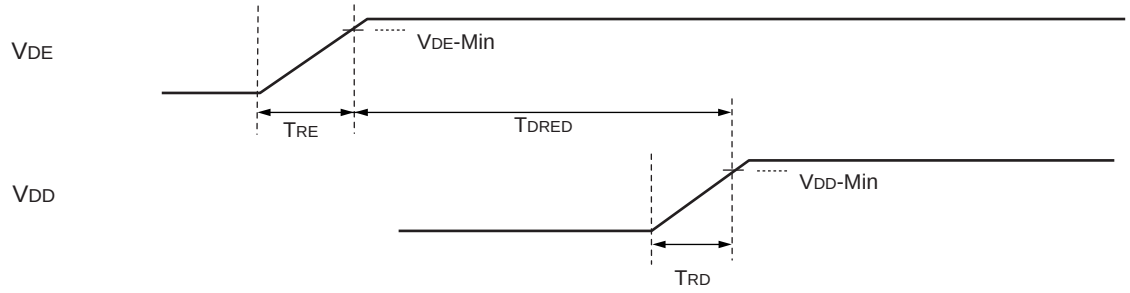
(17) Power Sequence

[360 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.3 V ± 0.065 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]
[400 MHz : V_{DE} = 3.3 V ± 0.15 V, V_{DD} = 1.4 V ± 0.07 V, V_{SS} = 0 V, Ta = 0 °C to + 70 °C]

Item	Parameter		Reference Signal	360 MHz/400 MHz		Unit
				Min	Max	
Power-on	VDE rise time	T_{RE}	—	—	30	ms
	VDD rise time	T_{RD}	—	—	15	ms
	Delay time from V_{DE} rise to V_{DD} rise	T_{DRED}	—	–100	100	ms

Note : Power-off Sequence is not defined.

- Power-on Sequence



5. Clock Setting

In this LSI, the clock signal inputted into CLKIN is multiplied by internal PLL, and it has distributed to each part in LSI.

The multiplication rate for each clock is decided using the CMODE [3 : 0] pins. Depending on this setup, the maximum frequency of CLKIN may be restricted.

The maximum frequency that can be inputted into CLKIN and the frequency of each part of LSI are shown below.

CMODE [0] to [3]				Ratio	CLKIN Freq.	Internal operating clock of this LSI					CLKIN input				
											360 MHz or 400 MHz	Period (T_{CLKIN}) [ns]		Freq. [MHz]	
3	2	1	0			External bus	SDRAM	Core bus	Core	DSU		Min	Max	Min	Max
0	0	0	0	Ratio	×1	×1	×1	×1	×1	×0.5	360 MHz	15.0	18.0	55.6	66.7
											400 MHz	15.0	15.5	64.5	66.7
0	0	0	1	Ratio	×1	×1	×1	×1	×3	×0.25	360 MHz	15.0	20.0	50.0	66.7
											400 MHz	15.0	17.5	57.1	66.7
0	0	1	0	Ratio	×1	×1	×1	×2	×6	×0.5	360 MHz	16.7	20.0	50.0	60.0
											400 MHz	15.0	17.5	57.1	66.7
0	0	1	1	Ratio	×1	×1	×2	×2	×6	×0.5	360 MHz	16.7	20.0	50.0	60.0
											400 MHz	15.0	17.5	57.1	66.7
0	1	0	0	Ratio	×1	×1	×1	×2	×2	×0.16	360 MHz	15.0	18.0	55.6	66.7
											400 MHz	15.0	15.5	64.5	66.7
0	1	0	1	Reserved											
0	1	1	0	Reserved											
0	1	1	1	Reserved											
1	0	0	0	Ratio	×1	×1	×1	×1	×2	×0.16	360 MHz	15.0	18.0	55.6	66.7
											400 MHz	15.0	15.5	64.5	66.7

(Continued)

(Continued)

CMODE [0] to [3]				Ratio	CLKIN Freq.	Internal operating clock of this LSI					CLKIN input				
											360 MHz or 400 MHz	Period (T_{CLKIN}) [ns]		Freq. [MHz]	
3	2	1	0			External bus	SDRAM	Core bus	Core	DSU		Min	Max	Min	Max
1	0	0	1	Ratio	×1	×1	×2	×2	×4	×0.33	360 MHz	15.0	18.0	55.6	66.7
											400 MHz	15.0	15.5	64.5	66.7
1	0	1	0	Reserved											
1	0	1	1	Reserved											
1	1	0	0	Ratio	×1	×1	×1	×2	×4	×0.33	360 MHz	15.0	18.0	55.6	66.7
											400 MHz	15.0	15.5	64.5	66.7
1	1	0	1	Reserved											
1	1	1	0	Ratio	×1	×1	×3	×3	×9	×0.75	360 MHz	25.0	27.0	37.0	40.0
											400 MHz	22.5	23.5	42.6	44.4
1	1	1	1	Ratio	×1	×1	×1.5	×1.5	×4.5	×0.375	360 MHz	15.0	20.0	50.0	66.7
											400 MHz	15.0	17.5	57.1	66.7

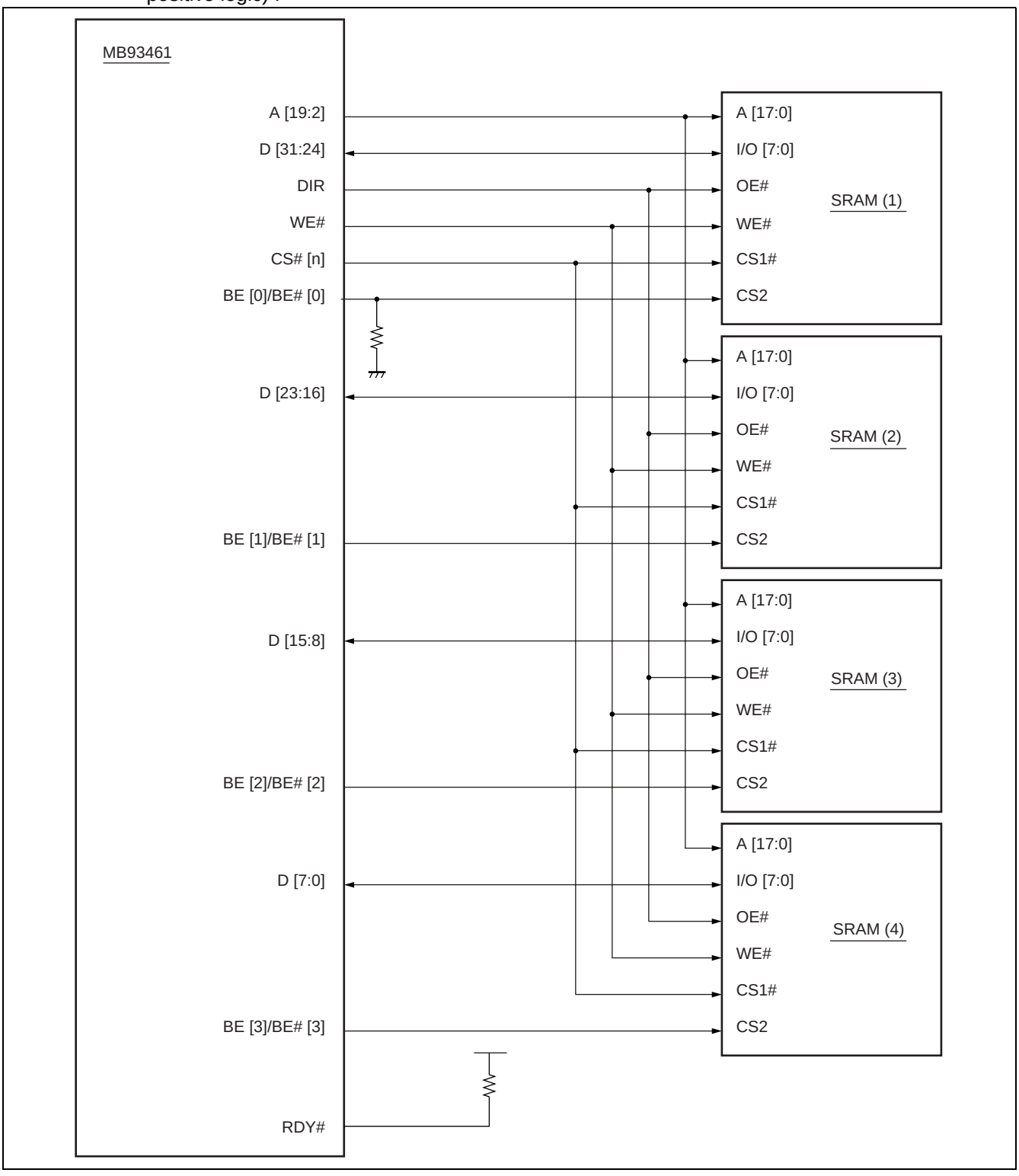
Notes :
- "×" indicates the frequency ratio for the external input clock.
- By default, the operating frequency of the resource bus clock is the same as that of the external bus.
- When CLKC.p0 is set to "1", the operating frequency of the resource bus clock is half that of the external bus. However, the frequency of the resource bus clock is fixed to 1/2 operating frequency of the external bus when CMODE = F regardless of the setting of CLKC.p0.
- As the setting of CMODE = 5, 6, 7, A, B, D that is the hatched part in the table is not confirmed for operation guarantee, do not set them.

■ CONNECTION WITH MEMORY

1. Connection with ROM or SRAM

An example of connection between this processor and ROM or SRAM, etc. is shown below.

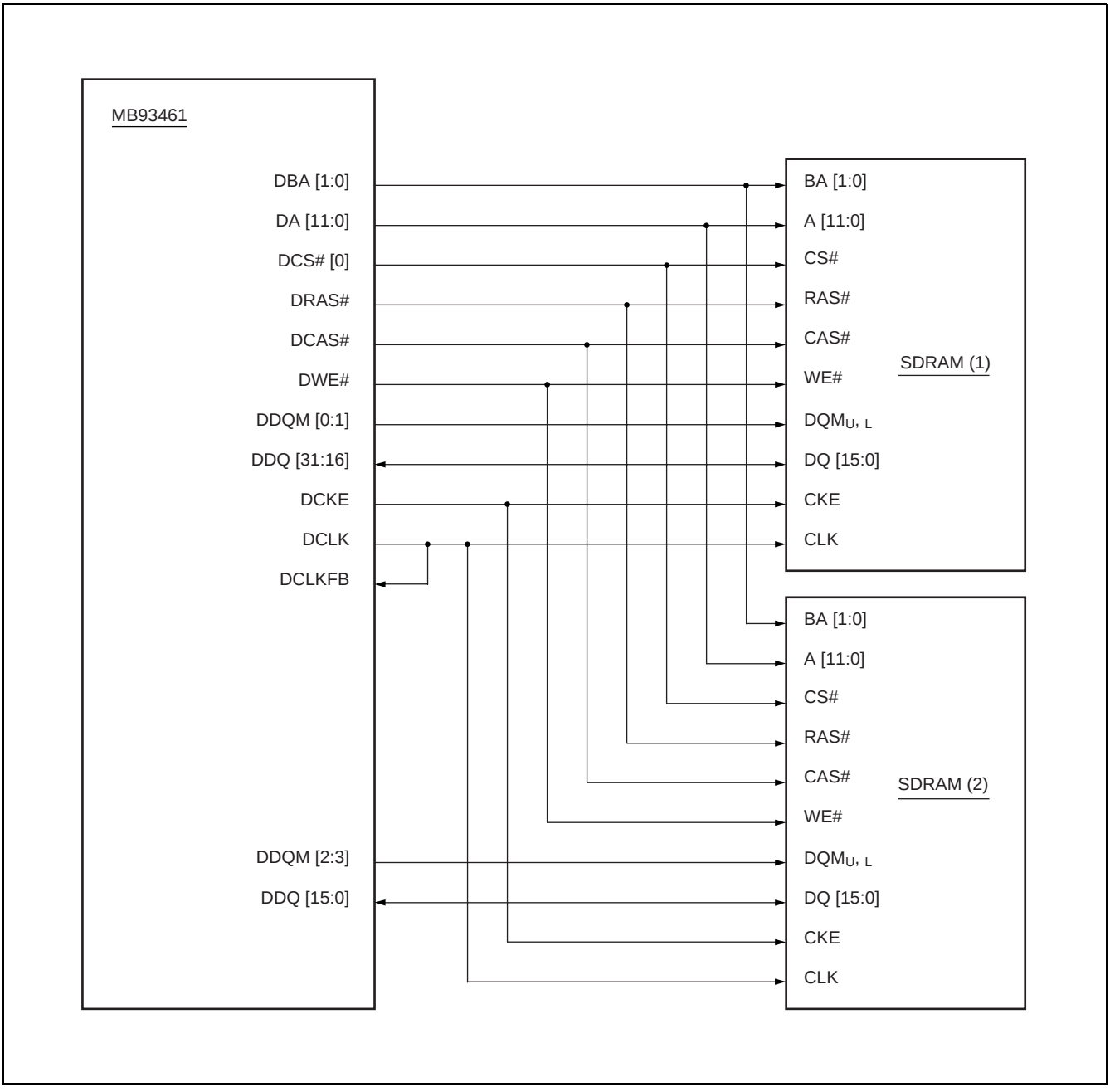
Example : Four SRAMs (each of “256 K × 8 bits”) are connected to the 32-bit bus (The polarity of BE/BE# is positive logic) .



2. Connection with SDRAM

SDRAM can be connected directly to DCS# [0] or DCS# [1].

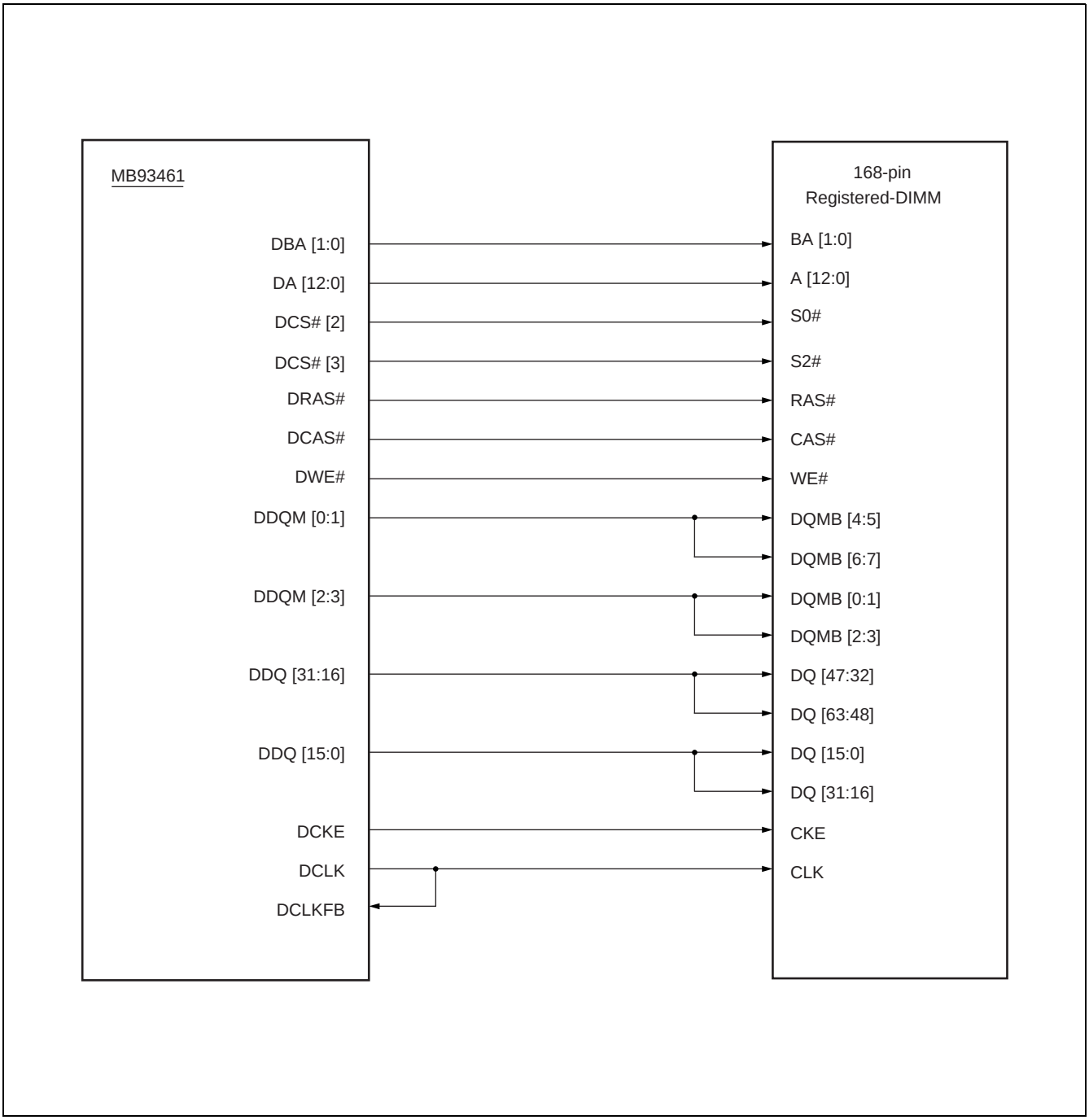
An example in which two SDRAMs (each of “1 M × 4 banks × 16 bits”) are connected to the 32-bit bus is shown below.



Note : This LSI outputs DCLK which is supplied to SDRAM as a clock. PLL is built into this LSI. Adjust the phase of DCLK so that the CLK pin of SDRAM and the internal phase in this LSI may be nearly equal. Therefore, when connecting, adjust the delay time of the feedback path from DCLK to DCLKFB, so that the phase of the clock input to DCLKFB which is the feedback signal to PLL and the phase of the clock (wave shape on the reception edge of DCLK) input to CLK of SDRAM may be nearly equal.

Example : Connecting Registered-DIMM to DCS#[3 : 2]

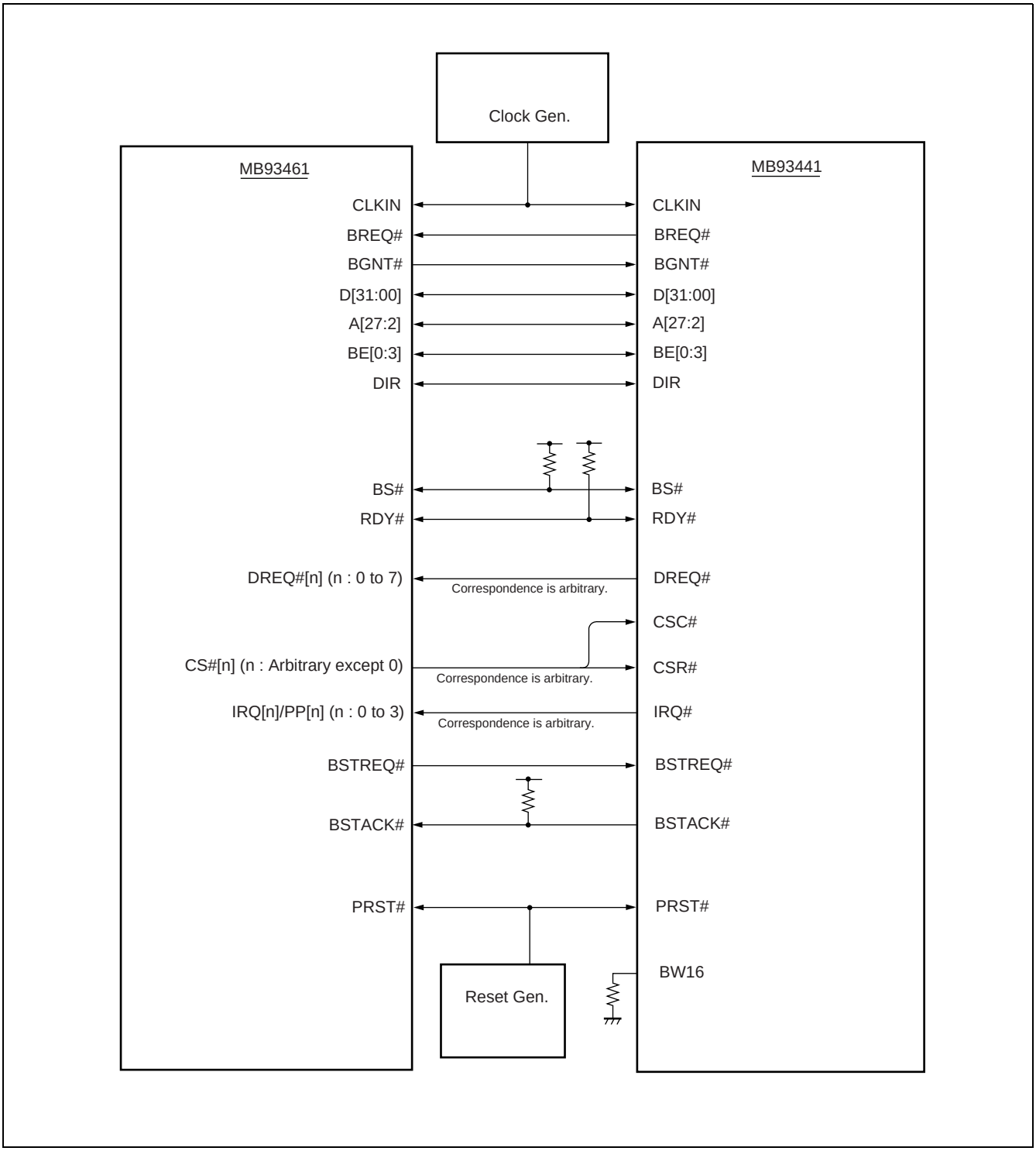
DCS#[2] and DCS#[3] are only used for connecting the 168-pin registered DIMM. Connect the 168-pin registered DIMM as follows. The DIMM must be “registered”. In the registered DIMM, it is assumed that the module connected to DCS#[2] or DCS#[3] is used after DCS#, DBA, DA, DRAS#, DCAS#, DWE#, DDQM, and DCKE are latched once at the rising of DCLK signal. When using DCS#[2] or DCS#[3], the bus width must be set to the 32-bit mode.



■ CONNECTION WITH PERIPHERAL DEVICE

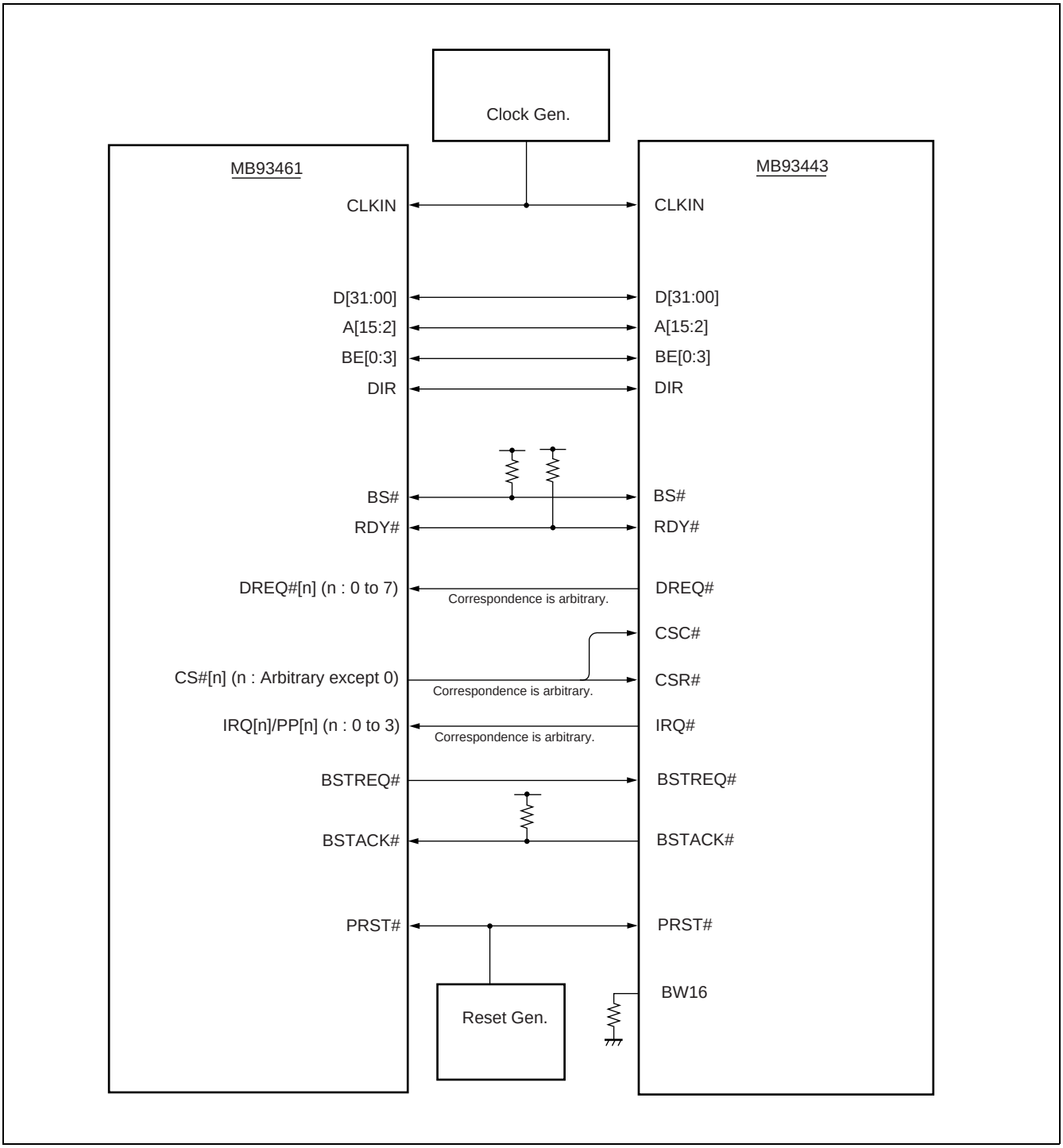
1. Connection with MB93441 (PCI Bridge Chip)

An example of connection between this processor and peripheral device is shown below.



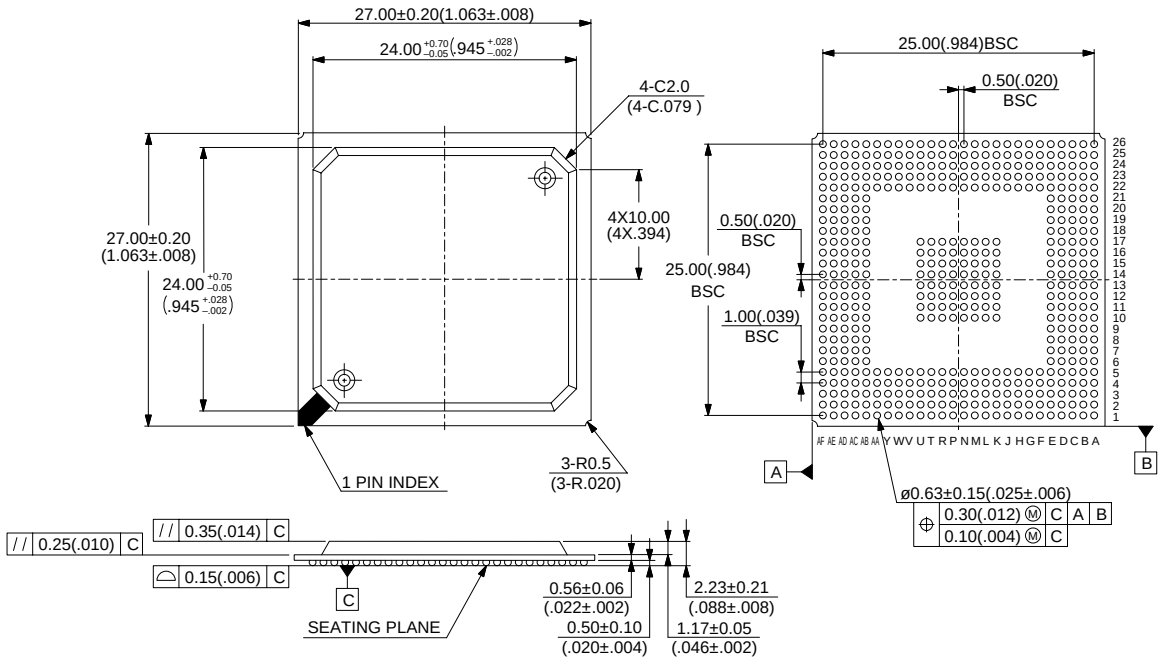
2. Connection with MB93443 (IDE/PC-Card Host Controller)

An example of connection between this processor and peripheral device is shown below.



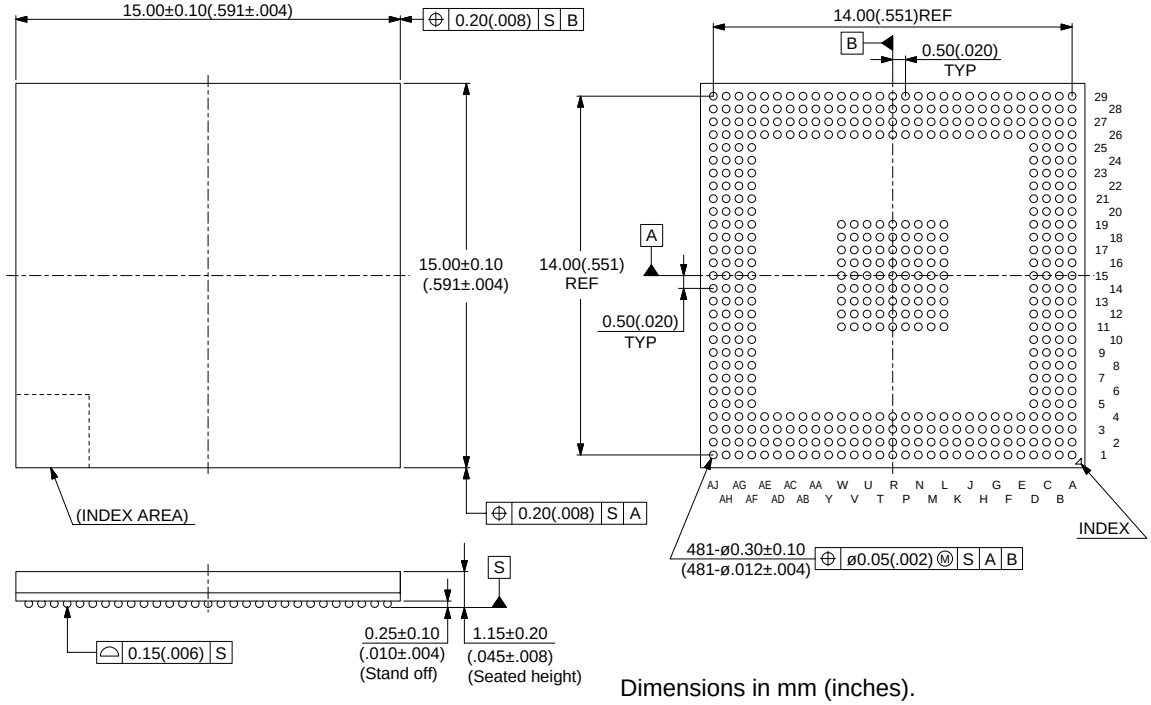
■ PACKAGE DIMENSIONS

420-ball plastic BGA
(BGA-420P-M25)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

400-ball plastic PFBGA
(BGA-400P-M04)



Dimensions in mm (inches).
Note: The values in parentheses are reference values.

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Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.

If any products described in this document represent goods or technologies subject to certain restrictions on export under the Foreign Exchange and Foreign Trade Law of Japan, the prior authorization by Japanese government will be required for export of those products from Japan.

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