CDB42L52

Evaluation Board for CS42L52

Features

- Stereo Analog Inputs
  - 4 Stereo Audio Jack Inputs, 2 of which can be Differential Microphone Inputs
  - Channel Mixer
- MUX'd Analog Output and Speaker Outputs
  - Headphone/Line Out Jack
  - Stereo Headphone Jack
  - Stereo Speaker Outputs w/Banana Jacks
- 8- to 96-kHz S/PDIF Interface
  - CS8416 Digital Audio Receiver
  - CS8406 Digital Audio Transmitter
- I/O Stake Headers
  - External Control Port Accessibility
  - External DSP Serial Audio I/O Accessibility
- Independent, Regulated Power Supplies
- 1.65 V to 3.3 V Logic Interface
- FlexGUI S/W Control - Windows® Compatible
  - Pre-Defined & User-Configurable Scripts

Description

Using the CDB42L52 evaluation board is an ideal way to evaluate the CS42L52 CODEC. Use of the board requires an analog/digital signal source, an analyzer and power supplies. A Windows PC-compatible computer is also needed in order to configure the CS42L52 and the board functionality.

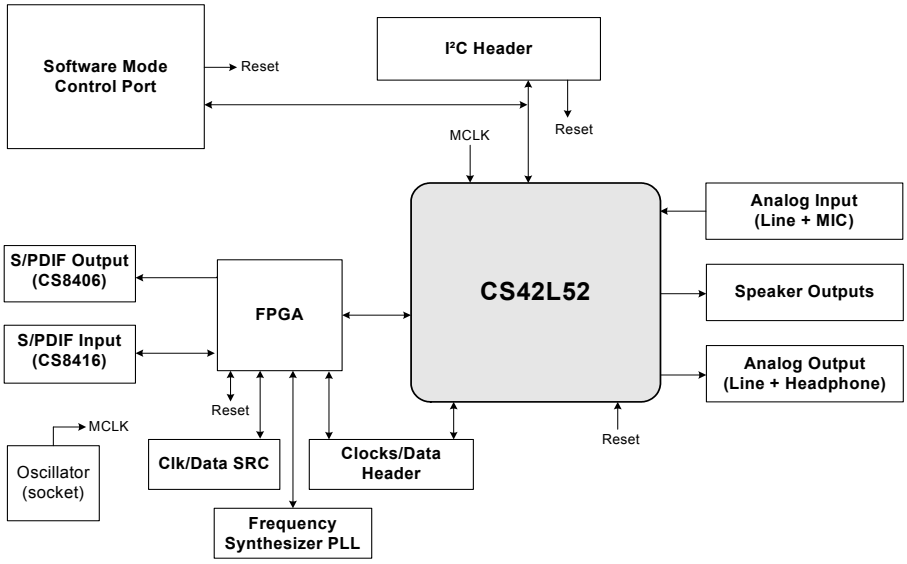
System timing can be provided by the CS8416, by the CS42L52 with supplied master clock, or via an I/O stake header with a DSP connected.

1/8th inch audio jacks are provided for the CS42L52 analog inputs and HP/Line outputs. Speaker driver outputs are via Banana jacks. Digital data I/O connections are via RCA phono or optical connectors to the CS8416 and CS8406 (S/PDIF Rx and Tx).

The Windows-based software GUI provided makes configuring the CDB42L52 easy. The software communicates through the PC's USB to configure board and FPGA registers so that all features of the CS42L52 can be evaluated. The evaluation board may also be configured to accept external timing and data signals for operation in a user application during system development.

ORDERING INFORMATION

CDB42L52	Evaluation Board



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1. SYSTEM OVERVIEW

The CDB42L52 platform provides analog and digital interfaces to the CS42L52 and allows for external DSP and I²C® interconnect. On board power regulators are provided so that only an external +5 V power supply is necessary. Board configuration is done using the Windows PC-compatible GUI to read/write device registers. An FPGA on the board helps make clock/data routing and CS42L52 configuration easy.

The CDB42L52 schematic set has been partitioned into seven pages and is shown in Figures 4 through 11. "System Connections and Jumpers" on page 13 provides a description of all stake headers and connectors, including the default factory settings for all jumpers. Section 2. "Software Mode Control" on page 6 provides further configuration details.

1.1 Power

Power is supplied to the evaluation board via the USB connection or by applying +5.0 V to TP2. Jumper J34 allows the user to select the power source. Power (VP) and ground (GND) for the PWM output stages in the CS42L52 is supplied via binding posts J35 and J4 (respectively) or by standard AAA batteries in locations BT1, BT2 and BT3. The VP voltage level can be in the range of +1.6 V to +5.25 V. On board regulators and jumpers allow the user to connect the CODEC's supplies to +1.65 V, 2.5 V or +3.3 V for VL and +1.65 V or 2.5 V for VD, VA and VA_HP. All voltage inputs must be referenced to ground using the black binding post J4.

Stake headers/Jumpers and parallel resistors provide a convenient way to measure supply currents to the CS42L52 for VD, VA, VL, VA_HP and VP supplies. The current is easily calculated by measuring the voltage drop across this resistor with its associated jumper removed. **NOTE:** The stake headers connected in parallel with these resistors must be shunted with the supplied jumper during normal operation.

WARNING: Please refer to the CS42L52 data sheet for allowable voltage levels.

1.2 Grounding and Power Supply Decoupling

The CS42L52 requires careful attention to power supply and grounding arrangements to optimize performance. The CDB42L52 demonstrates these optimal arrangements. Figure 7 on page 16 provides an overview of the connections to the CS42L52. Figure 12 on page 21 shows the component placement, Figure 13 on page 22 shows the top layout, and Figure 16 on page 25 shows the bottom layout. Power supply decoupling capacitors are located as close as possible to the CS42L52. Extensive use of ground plane fill helps reduce radiated noise.

1.3 FPGA

The FPGA controls digital signal routing between the CS42L52, CS8406, CS8416, SRC, PLL and the I/O stake header. It also provides routing control of the system master clock from an on-board oscillator, the CS8416 and the I/O stake header. The Cirrus FlexGUI software provides full control of the FPGA's routing and configuration options. Section 2. "Software Mode Control" on page 6 provides configuration details.

1.4 CS42L52 Audio CODEC

A complete description of the CS42L52 (Figure 4 on page 17) can be found in the CS42L52 product data sheet.

The CS42L52 is configured using the Cirrus FlexGUI. The device configuration registers are accessible via the "Register Maps" tab of the Cirrus FlexGUI software. This tab provides low-level control of each bit. For easier configuration, additional tabs provide high-level control. Section 2. "Software Mode Control" on page 6 provides configuration details.

1.5 CS8406 Digital Audio Transmitter

A complete description of the CS8406 transmitter (Figure 4 on page 17) and a discussion of the digital audio interface can be found in the CS8406 data sheet.

The CS8406 converts the PCM data generated by the CS42L52 to the standard S/PDIF data stream and routes this signal to the optical and RCA connectors on the CDB42L52.

Selections are made by using the “Board Configuration” tab of the Cirrus FlexGUI software. Section 2. “Software Mode Control” on page 6 provide configuration details.

1.6 CS8416 Digital Audio Receiver

A complete description of the CS8416 receiver (Figure 4 on page 17) and a discussion of the digital audio interface can be found in the CS8416 data sheet.

The CS8416 converts the input S/PDIF data stream from the optical or RCA connector into PCM data that is input to the CS42L52.

Selections are made by using the “Board Configuration” tab of the Cirrus FlexGUI software. Section 2. “Software Mode Control” on page 6 provides configuration details.

1.7 Oscillator

The socketed on-board oscillator can be selected as the system master clock source by using the selections on the “Board Configuration” tab of the Cirrus FlexGUI. Section 2. “Software Mode Control” on page 6 provides configuration details.

The oscillator is mounted in pin sockets, allowing easy removal or replacement. The device footprint on the board will accommodate full- or half-can-sized oscillators.

1.8 I/O Stake Headers

The evaluation board has been designed to allow interfacing with external systems via a serial port header (reference designation J8) and a control port header (reference designation J109). The serial port header provides access to the serial audio signals required to interface with a DSP (Figure 10 on page 19). Selections are made by using the “Board Configuration” tab of the Cirrus FlexGUI software. Section 2. “Software Mode Control” on page 6 provides configuration details.

The control port header provides bidirectional access to the I²C control port signals by simply removing all the shunt jumpers from the “USB” position. The user may then connect a ribbon cable connector to the “Ext Sys Connect” pins for external control of board functions. A single row of “GND” pins are provided to maintain signal ground integrity. Two unpopulated pull-up resistors are also available should the user choose to use the CDB42L52 logic supply (VL) externally.

1.9 Analog Inputs

Four stereo jack connectors supply the AC coupled line-level analog inputs to the CS42L52. Differential or single ended microphone inputs may be connected to J45 or J50 in place of line inputs. Stake headers J46 J38, J51 and J49 allow the user to select (with jumpers installed) the CS42L52 as the microphone bias source for each microphone input.

Figure 8 on page 17 illustrates how the analog inputs are connected and routed. Table 2 on page 14 details the jumper selections. The CS42L52 data sheet specifies the allowed full scale input voltage level.

1.10 Analog Outputs

The CDB42L52 has a Stereo Headphone/Line output jack and a separate Stereo Headphone (HP) output jack for the ground centered DAC output. Stake headers are provided to allow the user to select a 16 Ω or a 32 Ω resistive load connected to the DAC output or a filtered or unfiltered output for the HP/Line jack output. The resistive load can be selected to evaluate the CS42L52 drive capabilities. When connecting headphones to either output jack, the resistive load should be disconnected by removing the jumpers on each stake header.

The CDB42L52 also has A/B speaker output banana jacks (2 per A or B channel) and 1/8“ jack outputs. (1 per A or B channel). Stake headers on each channel (A or B) connect the CS42L52 Class D speaker driver amp outputs to either banana jack or 1/8” jack output in a number of configurations. Audio jack stake header selections include RC filtered or unfiltered outputs. Banana jack output selections include RLC filtered, unfiltered and either full or half bridge output modes. The red banana jacks designate the positive speaker terminal connection and the black jacks designate the negative terminal connection.

1.11 Control Port Connectors

The graphical user interface for the CDB42L52 (Cirrus Logic Flex GUI) allows the user to configure the CS42L52 registers and other component registers via the onboard I²C control bus. The GUI interfaces with the CDB via the USB connection to a PC. Section 2. “Software Mode Control” on page 6 provides a description of the Graphical User Interface (GUI).

1.11.1 USB Connector

Connecting a USB port cable from a PC to the USB connector on the board and launching the Cirrus FlexGUI software enables the CDB42L52. Note: The USB port connection also provides DC power to the board (except for VP). The minimum current required is approximately 300 mA. It may, therefore, be necessary to connect the CDB42L52 directly to the USB port on the PC as opposed to a hub or keyboard port where current may be limited.

2. SOFTWARE MODE CONTROL

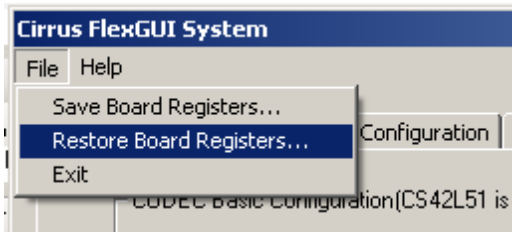
The CDB42L52 may be used with the Microsoft Windows®-based FlexGUI graphical user interface, allowing software control of the CS42L52, FPGA and CS8421 registers. The latest control software may be downloaded from www.cirrus.com/msasoftware. Step-by-step instructions for setting up the FlexGUI are provided as follows:

1. Download and install the FlexGUI software as instructed on the Website.
2. Connect and apply power to the +5.0 VP binding post.
3. Connect the CDB to the host PC using a USB cable.
4. Launch the Cirrus FlexGUI. *Once the GUI is launched successfully, all registers are set to their default reset state.*
5. Refresh the GUI by clicking on the “Update” button. *The default state of all registers are now visible.*

For standard set-up:

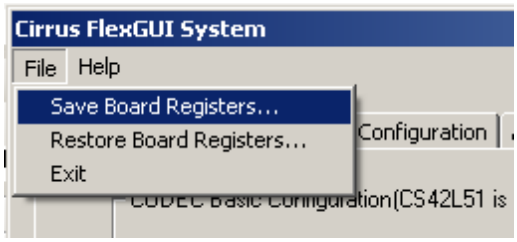
6. Set up the signal routing in the “Board Configuration” tab as desired.
7. Set up the CS42L52 in the “CODEC Configuration”, “Analog Input Volume”, “DSP Engine” and “Analog and PWM Output Volume” tab as desired.
8. Begin evaluating the CS42L52.

For quick set-up, the CDB42L52 may, alternatively, be configured by loading a predefined sample script file:



9. On the File menu, click "Restore Board Registers..."
10. Browse to Boards\CDB42L52\Scripts\.
11. Choose any one of the provided scripts to begin evaluation.

To create personal scripts files:



12. On the File menu, click "Save Board Registers..."
13. Enter any name that sufficiently describes the created setup.
14. Choose the desired location and save the script.
15. To load this script, follow the instructions from step 9 above.

2.1 Board Configuration Tab

The “Board Configuration” tab provides high-level control of signal routing on the CDB42L52. This tab also includes basic controls that allow “quick setup” in a number of simple board configurations. Status text detailing the CODEC’s specific configuration appears directly below the associated control. This text may change depending on the setting of the associated control. A description of each control group is outlined below:

CS42L52 CODEC Basic Configuration - Register controls for CS42L52 basic setup like interface format, clocking functions and analog input signal routing. See Section 2.2 through Section 2.5 for more controls in the CS42L52.

CS8416 S/PDIF Receiver Control - Register controls for setting up the CS8416.

CS8406 S/PDIF Transmitter Control - Register controls for setting up the CS8406.

Clock/Data Routing and Selection - Includes controls used for routing clocks and data between the CS42L52, CS8416, oscillator, I/O stake header, SRC and PFD. Also includes a reset control for the CS42L52.

Update - Reads all registers in the FPGA, CS42L52 and CS8421 and shows the current values in the GUI.

Reset - Resets FPGA to default routing configuration.

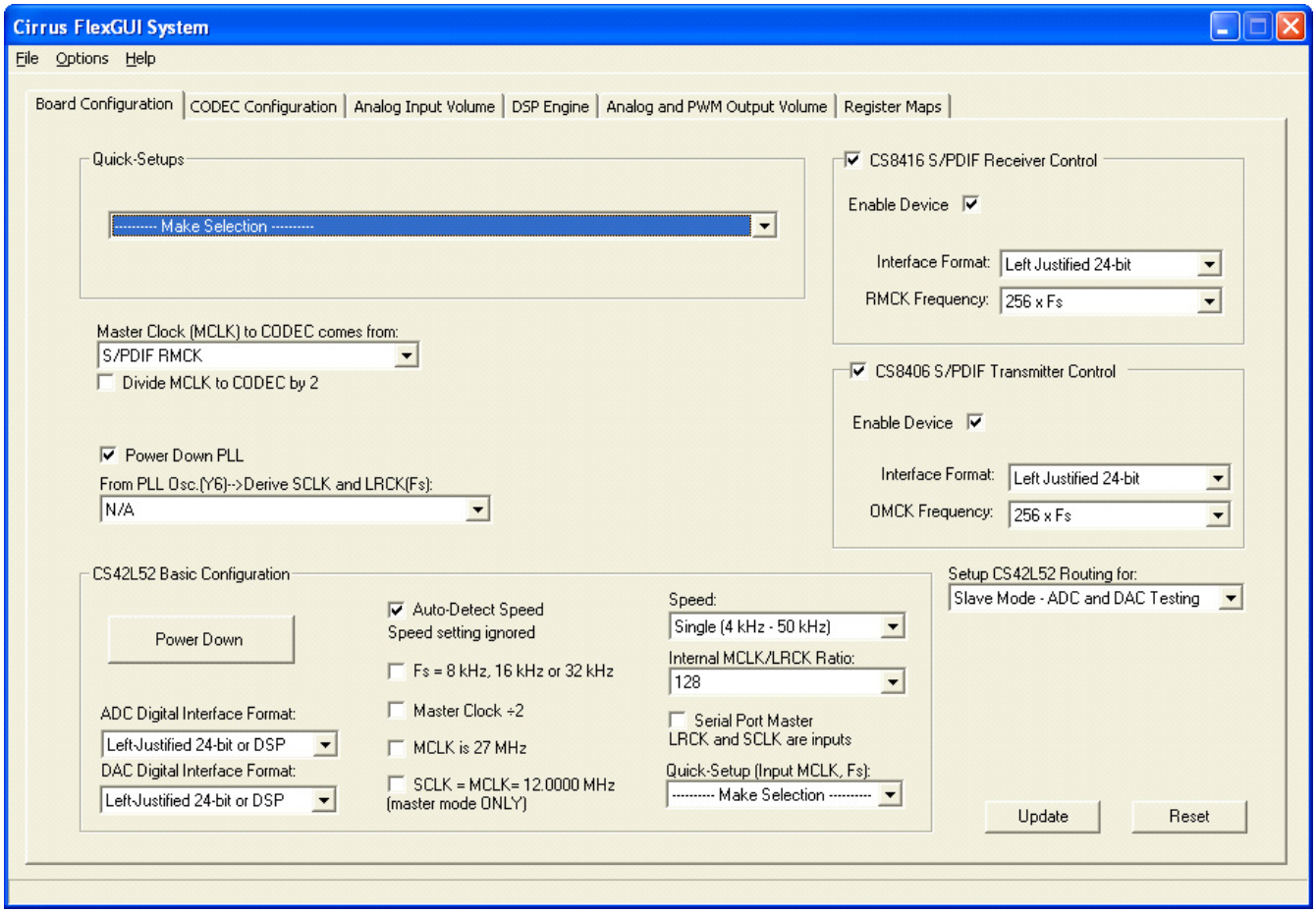


Figure 1. Board Configuration Tab

2.2 CODEC Configuration Tab

The “CODEC Configuration” tab provides high-level control of the CS42L52 register settings. Status text detailing the CODEC’s specific configuration is shown in parenthesis or appears directly below the associated control. This text will change depending on the setting of the associated control. A description of each control group is outlined below. See the CS42L52 data sheet for complete register descriptions.

Power Control - Register controls for powering down each device within the CODEC.

ADC Configuration - Controls for the input MUXs, input mixer (summing amp), microphone bias output, and ADC/SPE mixer.

Serial Port Configuration - Controls for all settings related to the serial I/O data and clocks on the board.

DAC Configuration - Control for the signal source to the DAC and analog output mux.

Update - Reads all registers in the CS42L52 and reflects the current values in the GUI.

Reset - Resets the CS42L52.

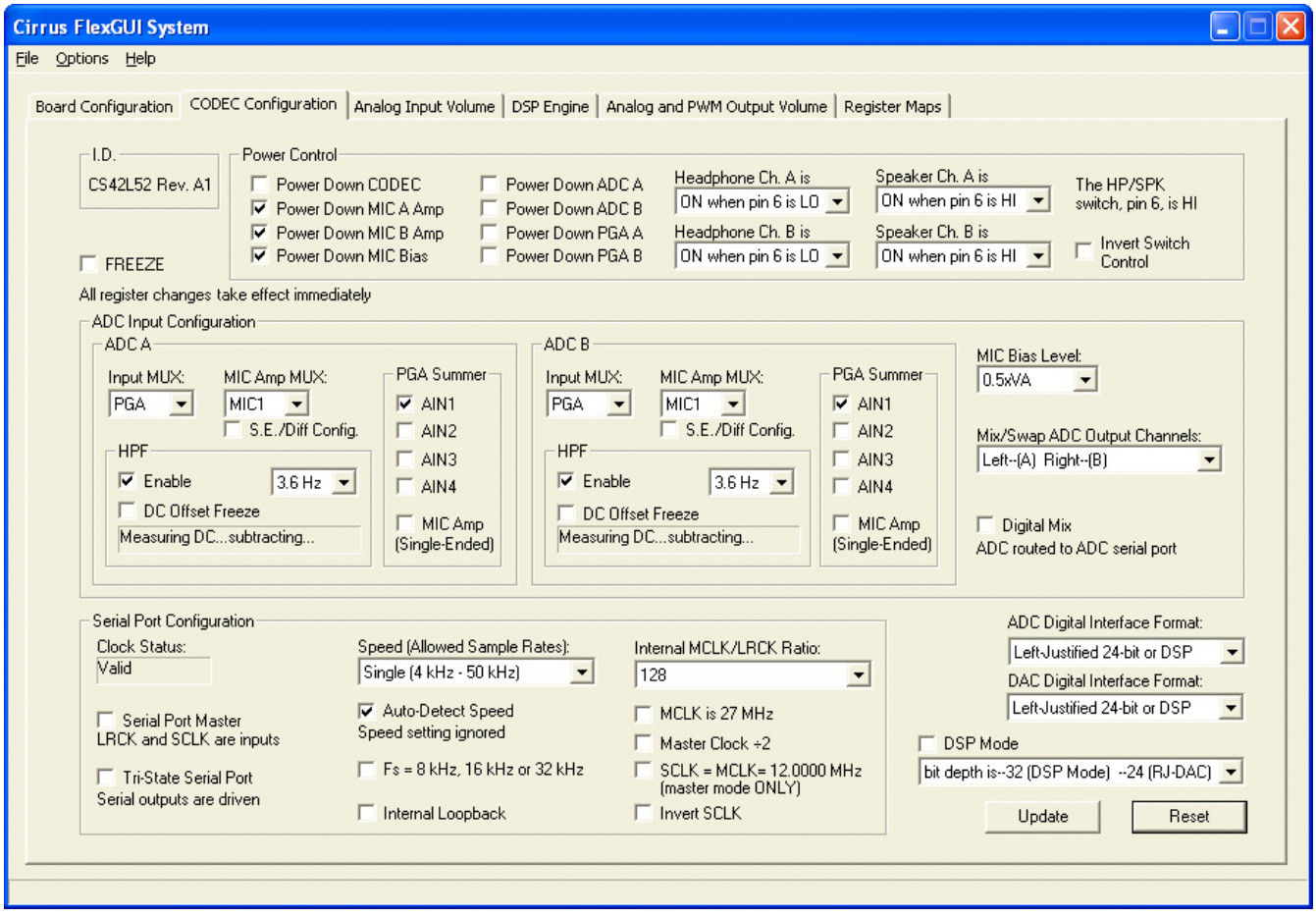


Figure 2. CODEC Configuration Tab

2.3 Analog Input Volume Tab

The “Analog Input Volume” tab provides high-level control of all volume settings in the ADC of the CS42L52. Status text detailing the CODEC’s specific configuration is shown in parenthesis or inside the control group of the affected control. This text will change depending on the setting of the associated control. A description of each control group is outlined below (a description of each register is included in the CS42L52 data sheet):

Digital Volume Control - Digital volume controls and adjustments (ADC output).

ALC Configuration - Configuration settings for the Automatic Level Control (ALC).

Analog Volume Control - Analog volume controls and adjustments (PGA and MIC amps).

Noise Gate Configuration - All configuration settings for the noise gate.

Update - Reads all registers in the CS42L52 and reflects the current values in the GUI.

Reset - Resets the CS42L52.

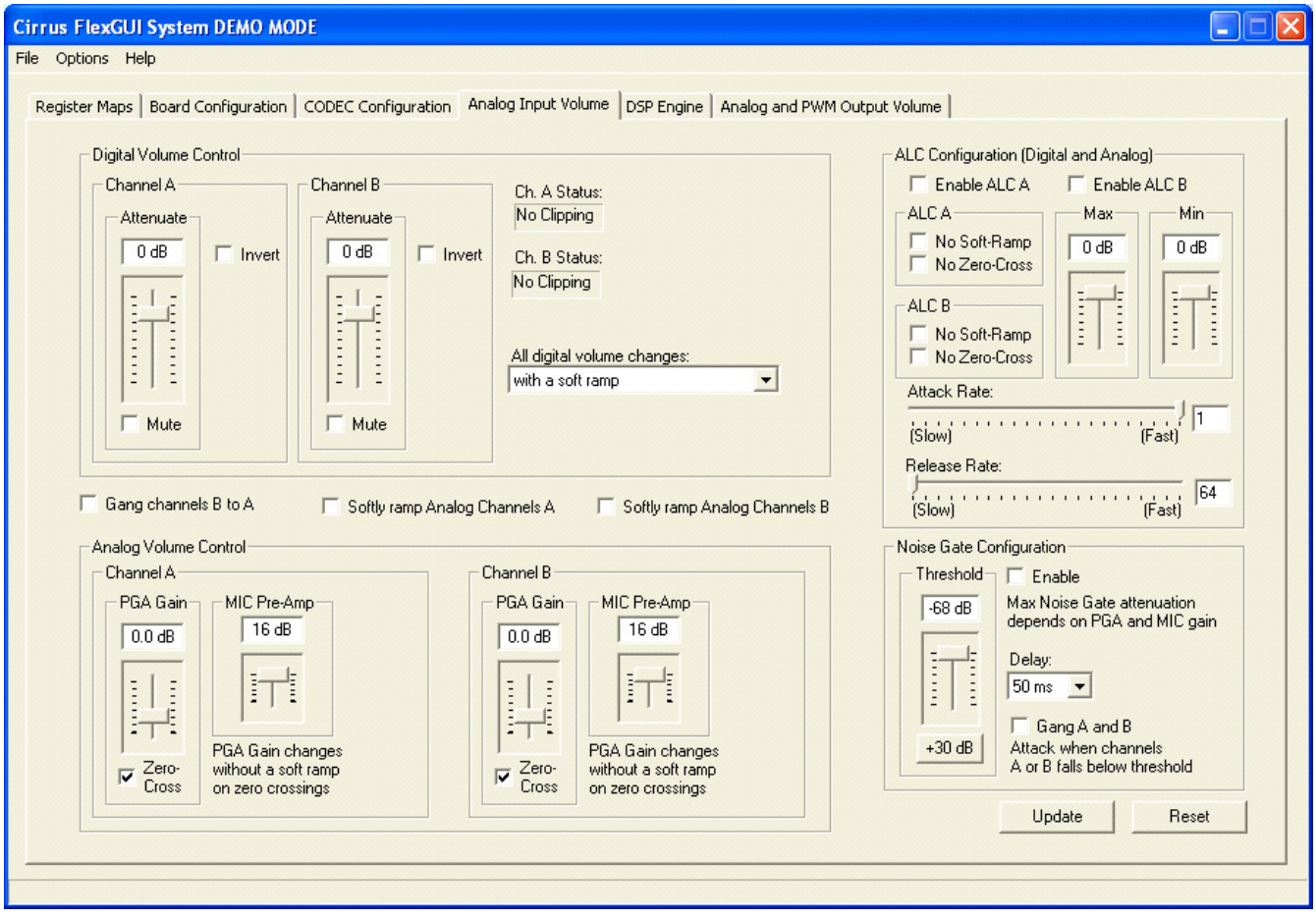


Figure 3. ADC Channel Volume Tab

2.4 DSP Engine Tab

The “DSP Engine” tab provides high-level control of the SDIN (PCM) data volume level, the ADC output/SDIN mix volume level and the overall DAC/PWM channel volume level. DAC/PWM channel Limiter, Tone Control and Beep Generator control functions are also provided. Status text detailing the CODEC’s specific configuration is shown in parenthesis or inside the control group of the affected control. This text will change depending on the setting of the associated control. A description of each control group is outlined below (a description of each register is included in the CS42L52 data sheet):

Digital Volume Control - Digital volume controls and adjustments for the SDIN data, ADC out data and overall channel volume. Mute, gang, invert and de-emphasis functions are also available.

Limiter - Configuration settings for the Automatic Level Control (ALC).

Tone Control - Bass and treble volume controls and filter corner frequencies.

Beep Generator - On/Off time, frequency, volume, mix and repeat beep functions.

Update - Reads all registers in the CS42L52 and reflects the current values in the GUI.

Reset - Resets the CS42L52.

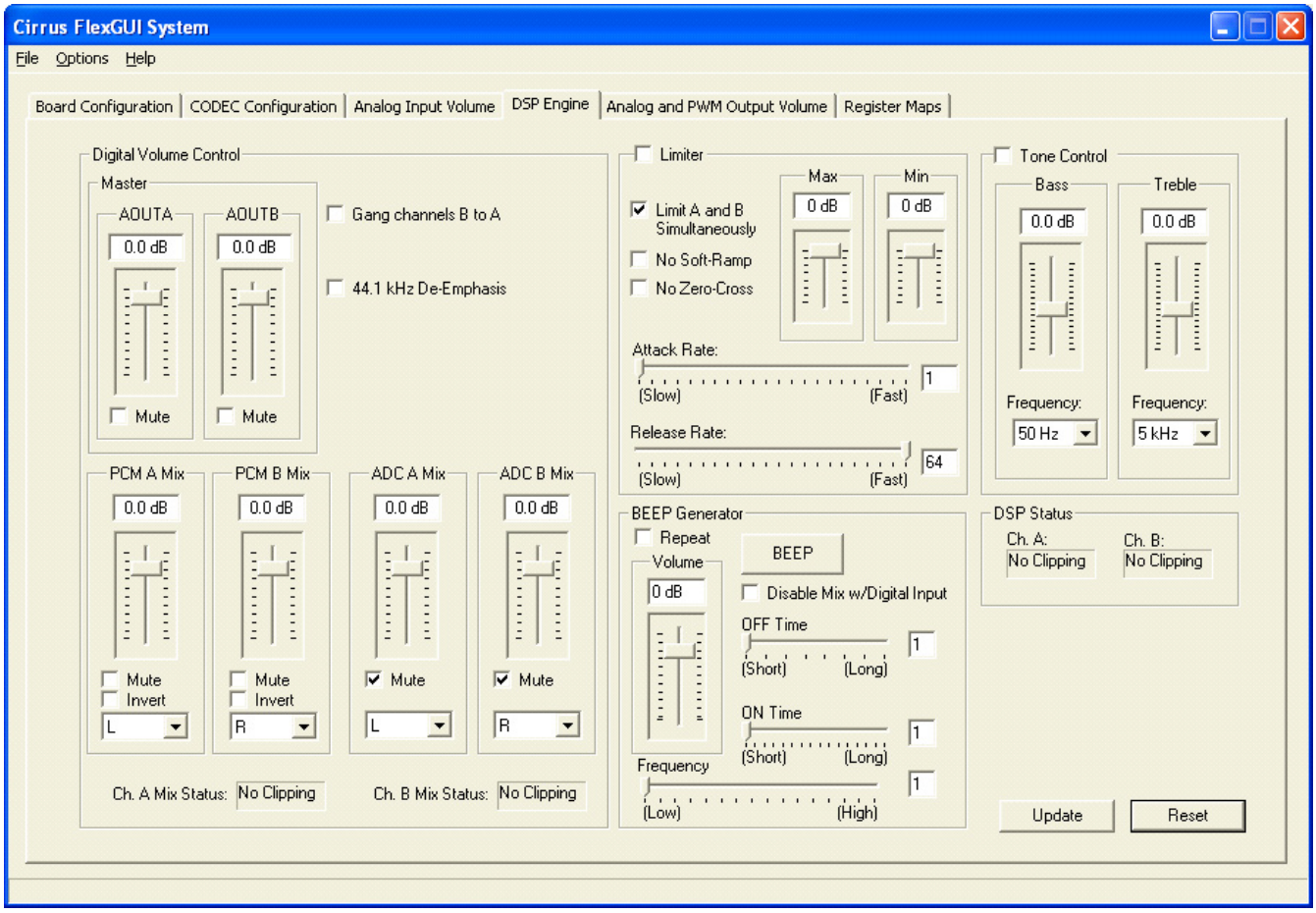


Figure 4. ADC Channel Volume Tab

2.5 Analog and PWM Output Volume Tab

The “Analog and PWM Output Volume” tab provides high-level control of the CS42L52 DAC output analog MUX, Input pass-through volume, HP/Line output volume levels and charge pump frequency. This tab also provides controls for the PWM output including speaker volume, PWM gain and modulation index. Temperature and Battery monitoring controls for the PWM/Speaker outputs are also on this tab. Status text detailing the CODEC’s specific configuration is shown in read-only edit boxes, in parenthesis or appears directly below the associated control. This text will change depending on the setting of the associated control. A description of each control group is outlined below (register descriptions are in the CS42L52 data sheet).

Headphone/Line Analog Output - Digital and analog volume controls and adjustments for the DAC channel (outside of the SPE) and for the input pass-through. Gain, Modulation Index, current limit and charge pump frequency adjustment are also provided and affect the FS output levels.

PWM Output - Volume, mute, power down and other functional controls for the PWM speaker outputs.

Temperature and Battery Monitor/Control - Battery Compensation, Thermal Foldback, Temperature Shutdown and Battery Monitor for the PWM/Speaker outputs.

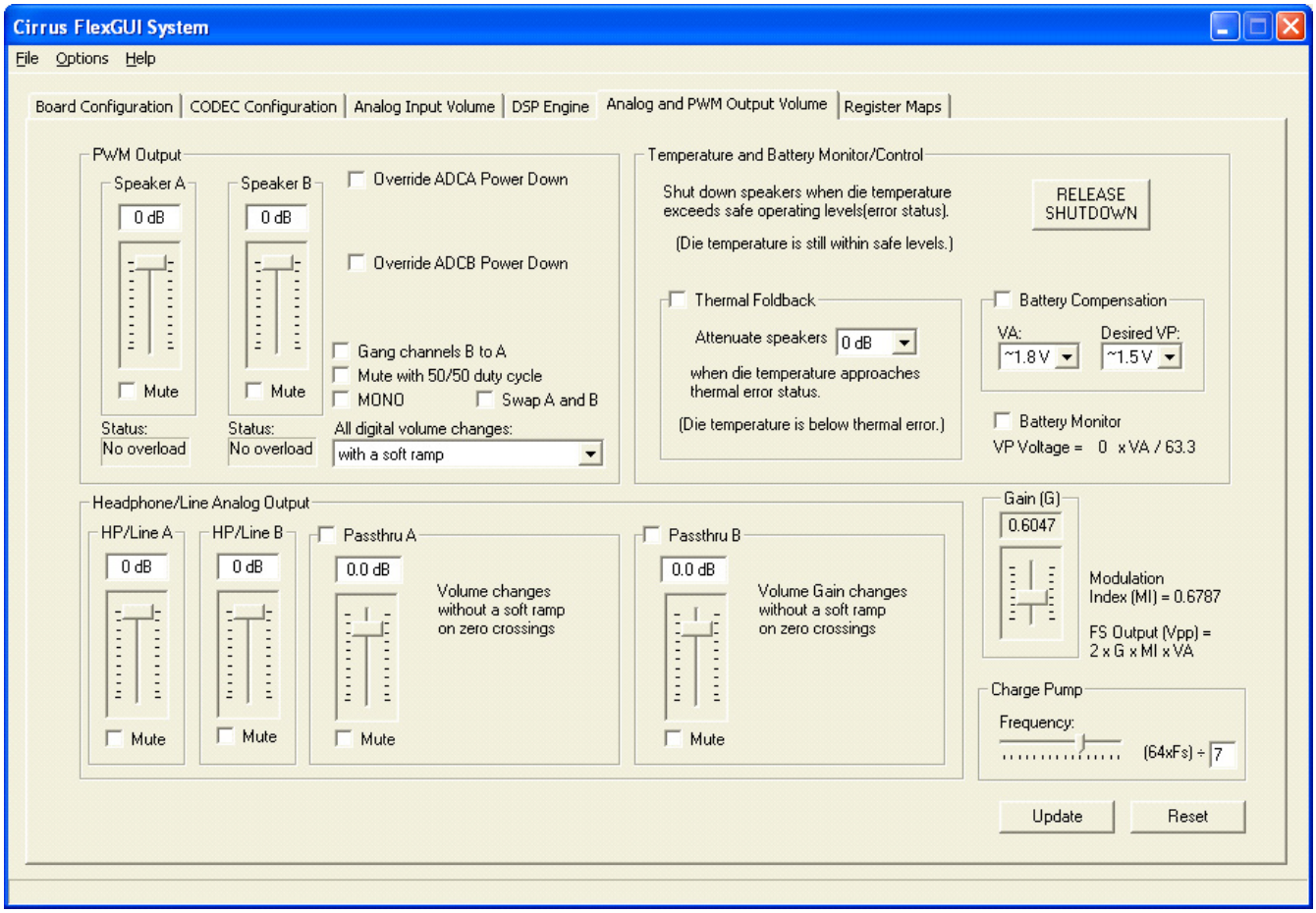


Figure 5. Analog and PWM Output Volume Tab

2.6 Register Maps Tab

The Register Maps tabs provide low-level control of the CS42L52, CS8416, CS8406, CS8421, FPGA and GPIO register settings. Register values can be modified bit-wise or byte-wise. “Left-clicking” on a particular register accesses that register and shows its contents at the bottom. The user can change the register contents by using the push-buttons, by selecting a particular bit and typing in the new bit value or by selecting the register in the map and typing in a new hex value.

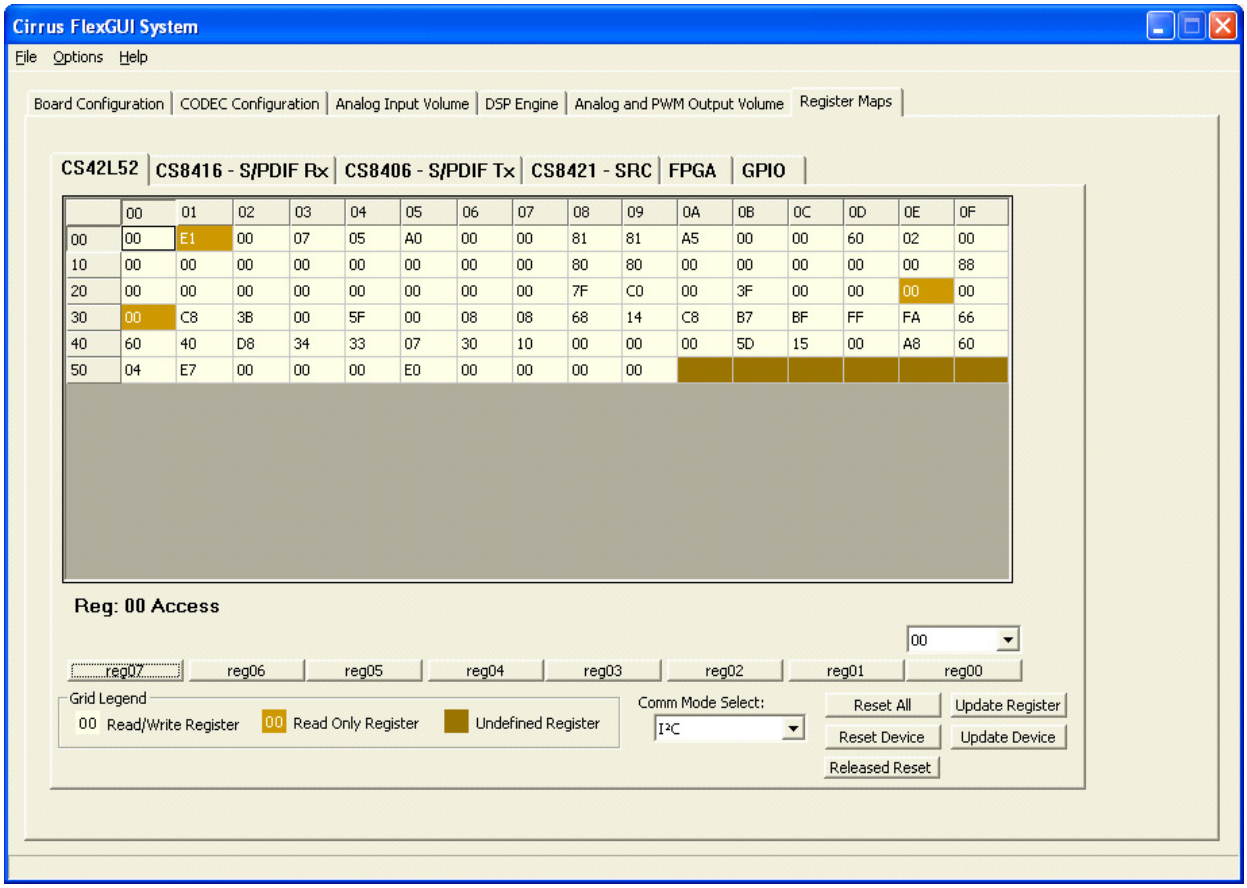


Figure 6. Register Maps Tab - CS42L52

3. SYSTEM CONNECTIONS AND JUMPERS

CONNECTOR	REF	INPUT/OUTPUT	SIGNAL PRESENT
VP	J35	Input	+1.6 V to +5.25 V Power Supply.
GND	J4	Input	Ground Reference .
USB	J94	Input/Output	USB connection to PC for I²C control port signals.
SPDIF OPTICAL OUT	OPT2	Output	CS8406 digital audio output via optical cable.
SPDIF COAX OUT	J68	Output	CS8406 digital audio output via coaxial cable.
SPDIF OPTICAL IN	OPT3	Input	CS8416 digital audio input via optical cable.
SPDIF COAX IN	J61	Input	CS8416 digital audio input via coaxial cable.
I/O Header	J8	Input/Output	I/O for Clocks & Data.
S/W CONTROL	J109	Input/Output	I/O for external I²C control port signals.
MICRO JTAG	J110	Input/Output	I/O for programming the micro controller (U84).
FPGA JTAG	J75	Input/Output	I/O for programming the FPGA (U5).
MICRO RESET	S4	Input	Reset for the micro controller (U5).
FPGA PROGRAM	S2	Input	Reload Xilinx program into the FPGA from Flash (U14).
H/W BOARD RESET	S1	Input	Reset for the CS42L52 (U1).
LINE1A/1B LINE2A/2B	J33 J37	Input Input	1/8” audio jacks for analog input signal to CS42L52.
LINE3A_MIC1- /3B_MIC2- LINE4A_MIC1+ /4B_MIC2+	J45 J50	Input	1/8” audio jacks for Line or MIC analog input signals to CS42L52.
SPEAKER A-/A+ SPEAKER B-/B+	J6 J18	Output	1/8” audio jack speaker A-/A+ outputs.
SPEAKER A- SPEAKER A+ SPEAKER B- SPEAKER B+	J60 J59 J101 J99	Output	Binding Post speaker outputs.
HP/Line Output	J40	Output	Stereo 1/8” jack for DAC outputs. When headphones are plugged in to HP Connect, this output is disconnected.
HP Connect	J21	Output	Stereo headphone jack for DAC outputs.
PCM I/O	J78	Input/Output	Digital Audio and Clocks to/from a DSP device.

Table 1. System Connections

JMP	LABEL	PURPOSE	POSITION	FUNCTION SELECTED
J31	VL	Selects source of voltage for the VL supply	*+1.8V	Voltage source is +1.8 V regulator.
			+2.5V	Voltage source is +2.5 V regulator.
			+3.3V	Voltage source is +3.3 V regulator.
J36	VA_HP	Selects source of voltage for the VA_HP supply	*+1.8V	Voltage source is +1.8 V regulator.
			+2.5V	Voltage source is +2.5 V regulator. .
J25	VA	Selects source of voltage for the VA supply	*+1.8V	Voltage source is +1.8 V regulator.
			+2.5V	Voltage source is +2.5 V regulator. .
J28	VD	Selects source of voltage for the VD supply	*+1.8V	Voltage source is +1.8 V regulator.
			+2.5V	Voltage source is +2.5 V regulator. .
J52 J47 J74 J53 J48	VL +VA_HP VA VD VP	Current Measurement	*SHUNTED	1 Ω series resistor is shorted.
			OPEN	1 Ω series resistor in power supply path.
J39	AIN1A_AC_DC	Selects either AC or DC couple for AIN1A Input	*OPEN	AIN1A input is AC coupled to ADC.
			SHUNTED	AIN1A input is DCcoupled to ADC.
J7	AIN1A_AC_DC	Selects either AC or DC couple for AIN1B Input	*OPEN	AIN1A input is AC coupled to ADC.
			SHUNTED	AIN1A input is DCcoupled to ADC.
J38	MIC1-_BIAS	Selects MICBIAS for MIC1- Input	*OPEN	AIN3A/MIC1- Input from Audio Jack.
			SHUNTED	AIN3A/MIC1- Input is MICBIAS.
J46	MIC2-_BIAS	Selects MICBIAS for MIC1- Input	*OPEN	AIN3B/MIC2- Input from Audio Jack.
			SHUNTED	AIN3B/MIC2- Input is MICBIAS.
J49	MIC1+_BIAS	Selects MICBIAS for MIC1+ Input	*OPEN	AIN4A/MIC1+ Input from Audio Jack.
			SHUNTED	AIN4A/MIC1+ Input is MICBIAS.
J51	MIC2+_BIAS	Selects MICBIAS for MIC2+ Input	*OPEN	AIN4B/MIC2+ Input from Audio Jack.
			SHUNTED	AIN4B/MIC2+ Input is MICBIAS.
J13	SPKRA-_FLT/NOFLT	Selects FLT or NOFLT output for SPKOUTA-	1 - 2	No filtered output selected for SPKOUTA-.
			*2 - 3	LC filtered output selected for SPKOUTA-.
J16	SPKRA+_FLT/NOFLT	Selects FLT or NOFLT output for SPKOUTA+	1 - 2	No filtered output selected for SPKOUTA+.
			*2 - 3	LC filtered output selected for SPKOUTA+.
J11	SPKRB-_FLT/NOFLT	Selects FLT or NOFLT output for SPKOUTB-	1 - 2	No filtered output selected for SPKOUTB-.
			*2 - 3	LC filtered output selected for SPKOUTB-.
J20	SPKRB+-_FLT/NOFLT	Selects FLT or NOFLT output for SPKOUTB+	1 - 2	No filtered output selected for SPKOUTB+.
			*2 - 3	LC filtered output selected for SPKOUTB+.
J14	SPKR_A-_CONN	Selects LCFLT or RCFLT output for SPKOUTA-	1 - 2	RC filtered SPKOUTA- to J6.
			*2 - 3	LC filtered SPKOUTA- to J6 and J60.
J17	SPKR_A+_CONN	Selects LCFLT or RCFLT output for SPKOUTA+	1 - 2	RC filtered SPKOUTA+ to J6.
			*2 - 3	LC filtered SPKOUTA+ to J6 and J59.
J12	SPKR_B-_CONN	Selects LCFLT or RCFLT output for SPKOUTB-	1 - 2	RC filtered SPKOUTB- to J18.
			*2 - 3	LC filtered SPKOUTB- to J18 and J101.
J23	SPKR_B+_CONN	Selects LCFLT or RCFLT output for SPKOUTB+	1 - 2	RC filtered SPKOUTB+ to J18.
			*2 - 3	LC filtered SPKOUTB+ to J18 and J99.
J15	MONO	Selects Full or Half Bridge output for SPKOUTA-/+	*OPEN	Stereo Full Bridge outputs to J60 and J59.
			SHUNTED	Mono Full Bridge output to J60 and J59.
J19	MONO	Selects Full or Half Bridge output for SPKOUTB-/+	*OPEN	Stereo Full Bridge outputs to J101 and J99.
			SHUNTED	Mono Full Bridge output to J101 and J99.

Table 2. Jumper Settings

J3	HP/LINEB_R_LOAD	Selects 32 or 16 ohm load for HP/LINE_OUTB (DAC out)	1 - 2	16 ohm load selected.
			2 - 3	32 ohm load selected.
J9	HP/LINEA_R_LOAD	Selects 32 or 16 ohm load for HP/LINE_OUTA (DAC out)	1 - 2	16 ohm load selected.
			2 - 3	32 ohm load selected.
J1	HP/LINEA_FLT	Selects filtered or non filtered HP/LINE_OUTA (DAC out)	1 - 2	Non-filtered HP/LINE_OUTA to HP/Line Jack.
			*2 - 3	Filtered HP/LINE_OUTA to HP/Line Jack.
J2	HP/LINEB_FLT	Selects filtered or non filtered HP/LINE_OUTB (DAC out)	1 - 2	Non-filtered HP/LINE_OUTA to HP/Line Jack.
			*2 - 3	Filtered HP/LINE_OUTA to HP/Line Jack.
J22	SW/SPKR_HP_DET	Selects either FPGA DET or HP Jack generated DET signal	1 - 2	FPGA generated HP_DET signal selected.
			*2 - 3	HP Jack generated HP_DET signal selected.
J34	Board Power	Selects either USB or External +5 V power to the board	1 - 2	External +5 V power.
			*2 - 3	USB generated +5 V power.
J5	VP Power	Selects either External or Battery VP power to the board	*1 - 2	External VP power.
			2 - 3	Battery VP power.
J10	1.65 V or 1.8 V Select	Selects either 1.65 V or 1.8 V from the onboard regulator U6	1 - 2	1.65 V select.
			*2 - 3	1.8 V select.

*Default factory settings

Table 2. Jumper Settings

CDB42L51 BLOCK DIAGRAM

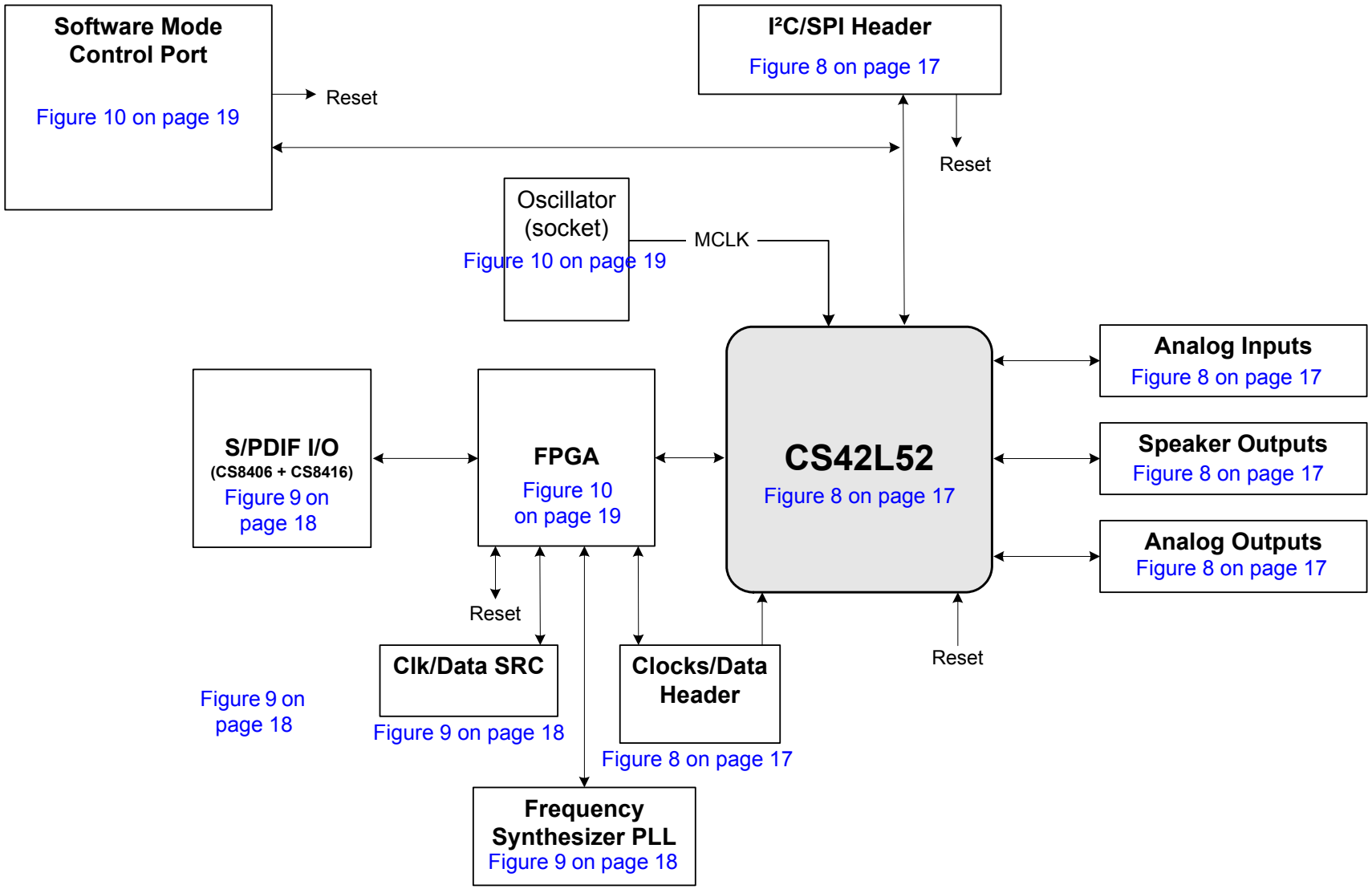


Figure 7. Block Diagram

4. CDB42L51 SCHEMATICS

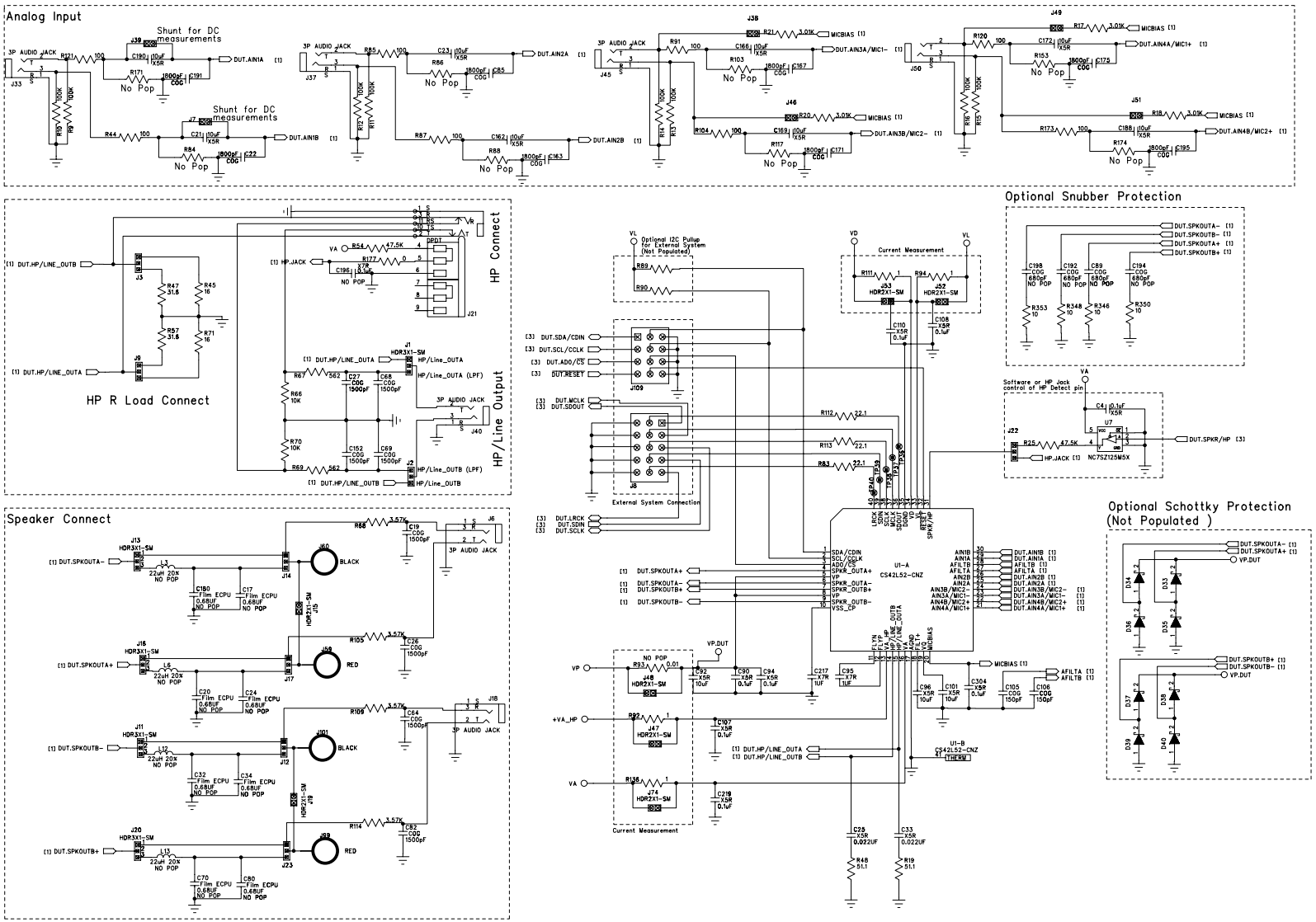
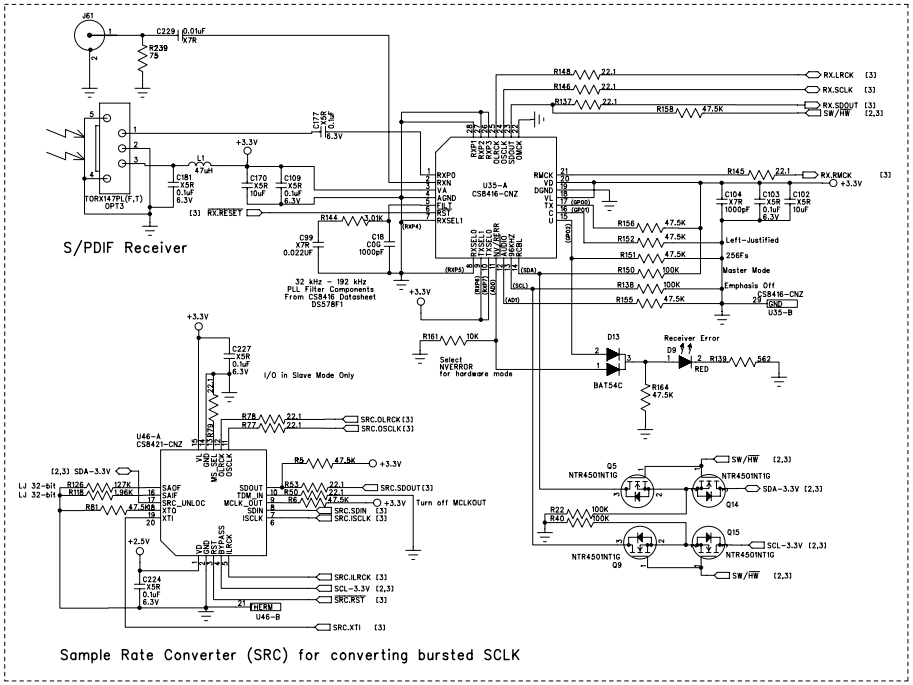
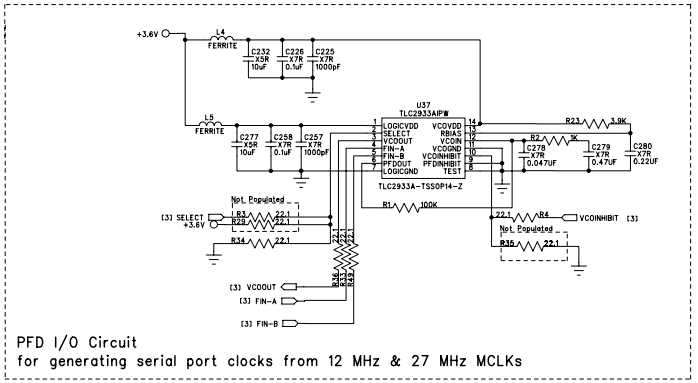
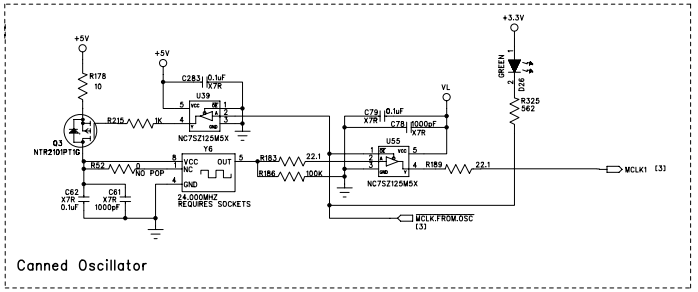
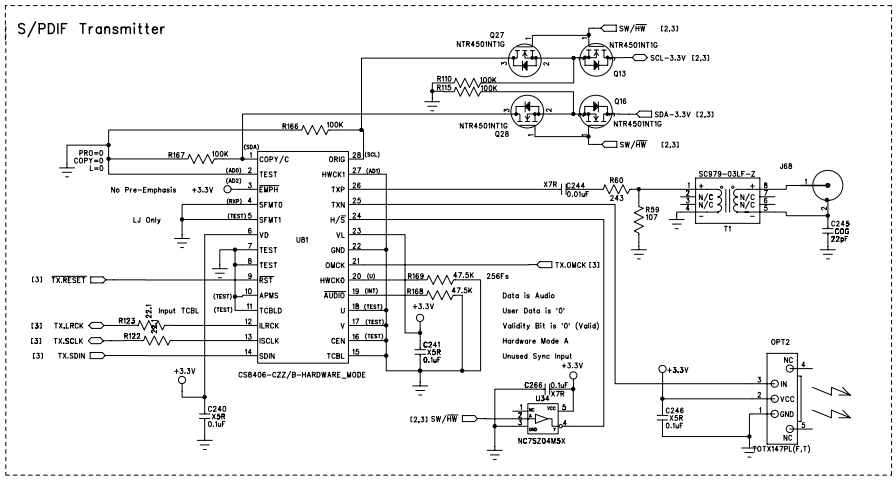


Figure 8. CS42L52 & Analog I/O (Schematic Sheet 1)









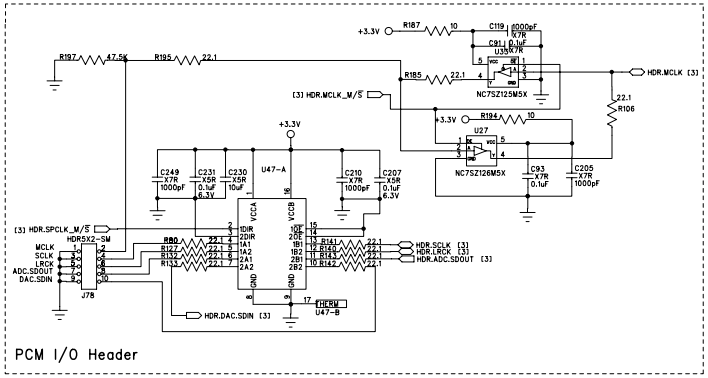


Figure 9. S/PDIF & Digital Interface (Schematic Sheet 2)

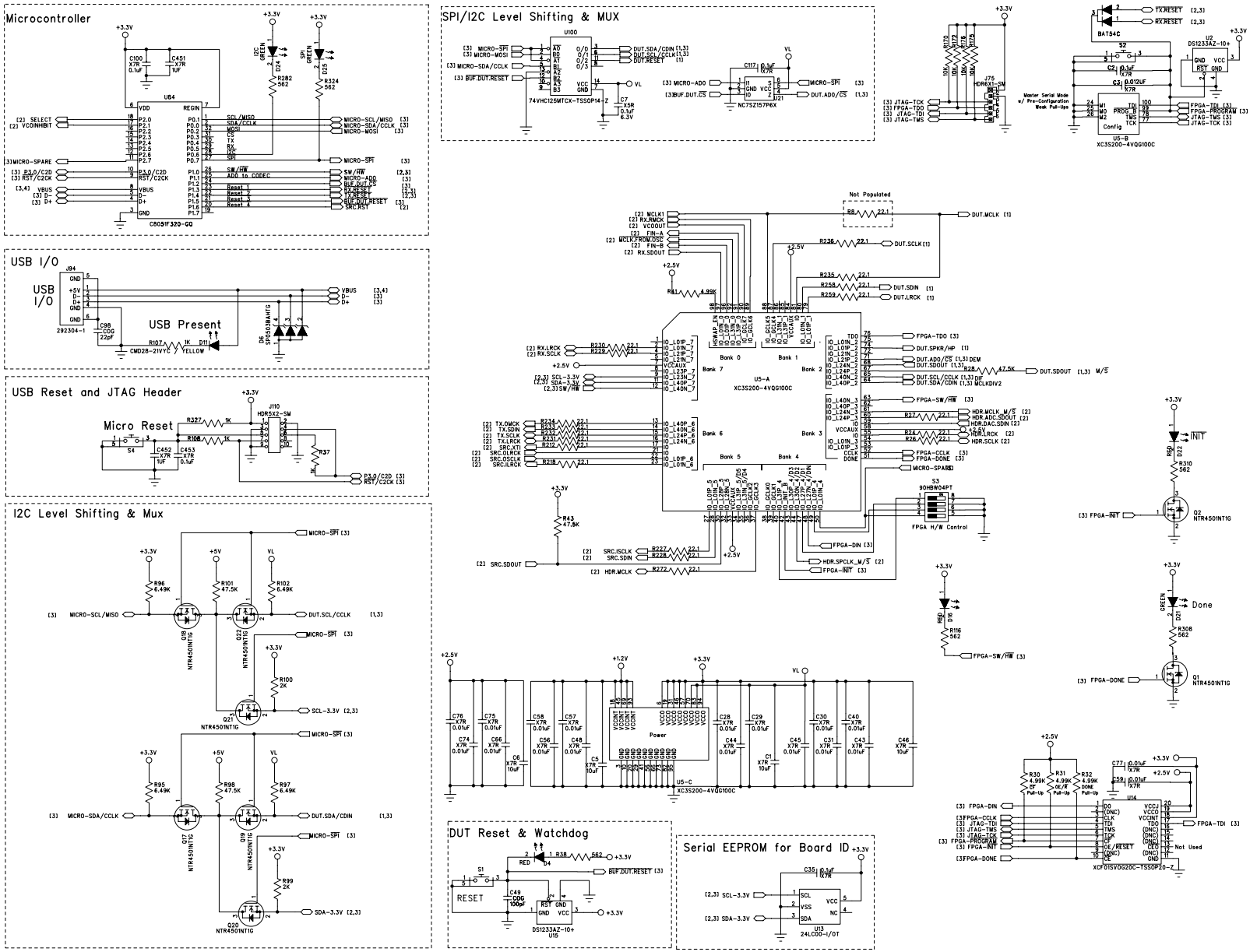


Figure 10. Micro & FPGA Control (Schematic Sheet 3)

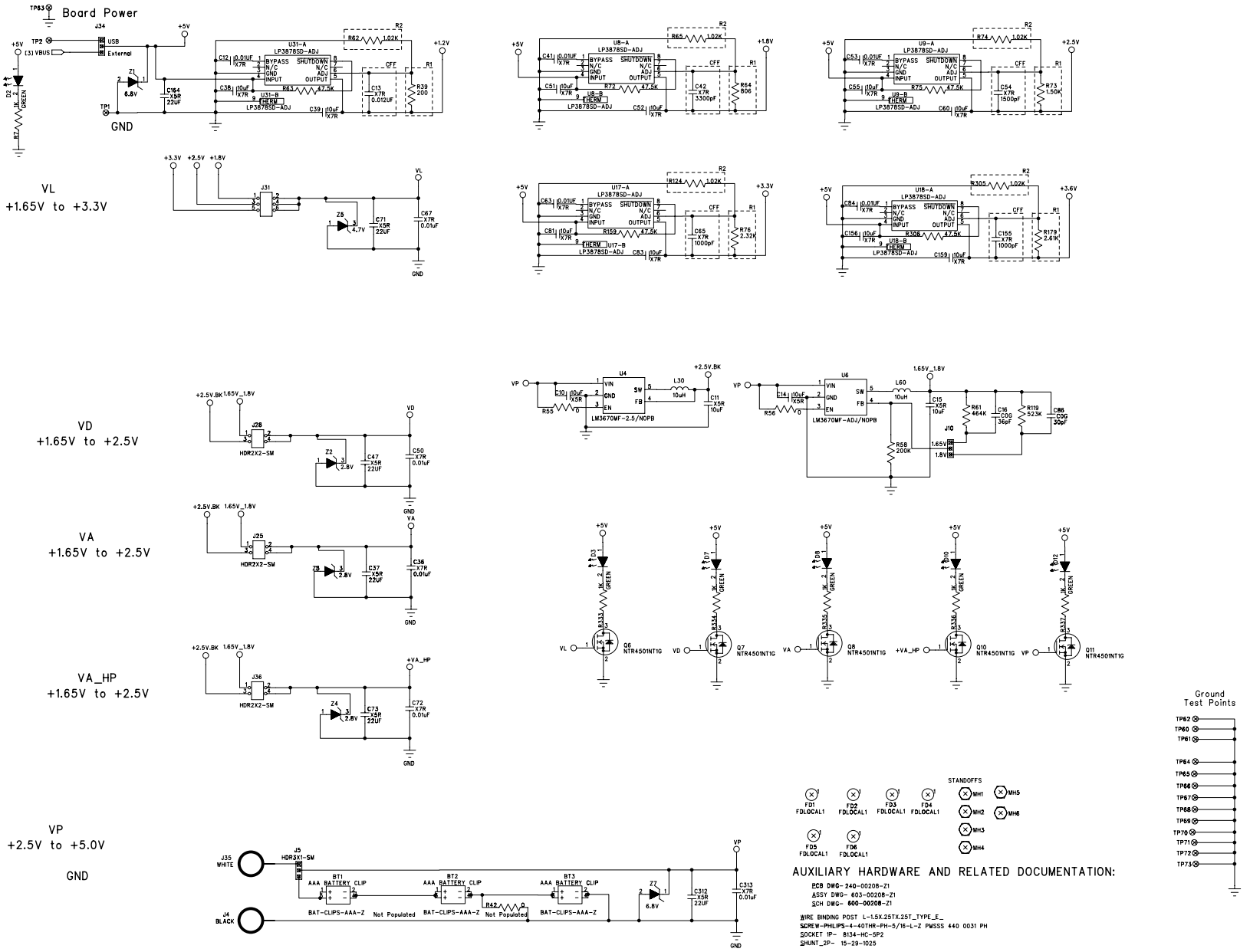


Figure 11. Power (Schematic Sheet 4)

5. CDB42L51 LAYOUT

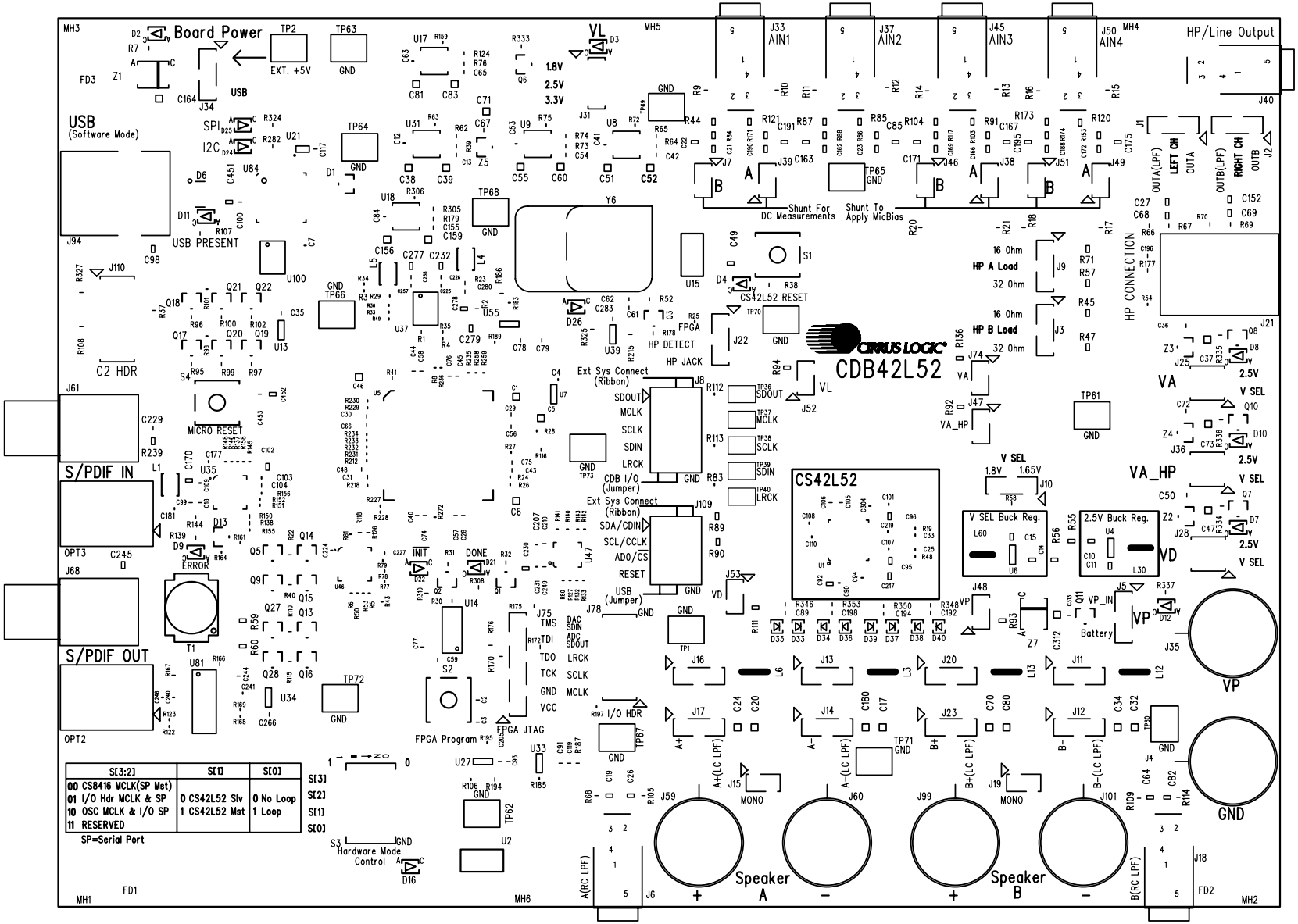


Figure 12. Silk Screen

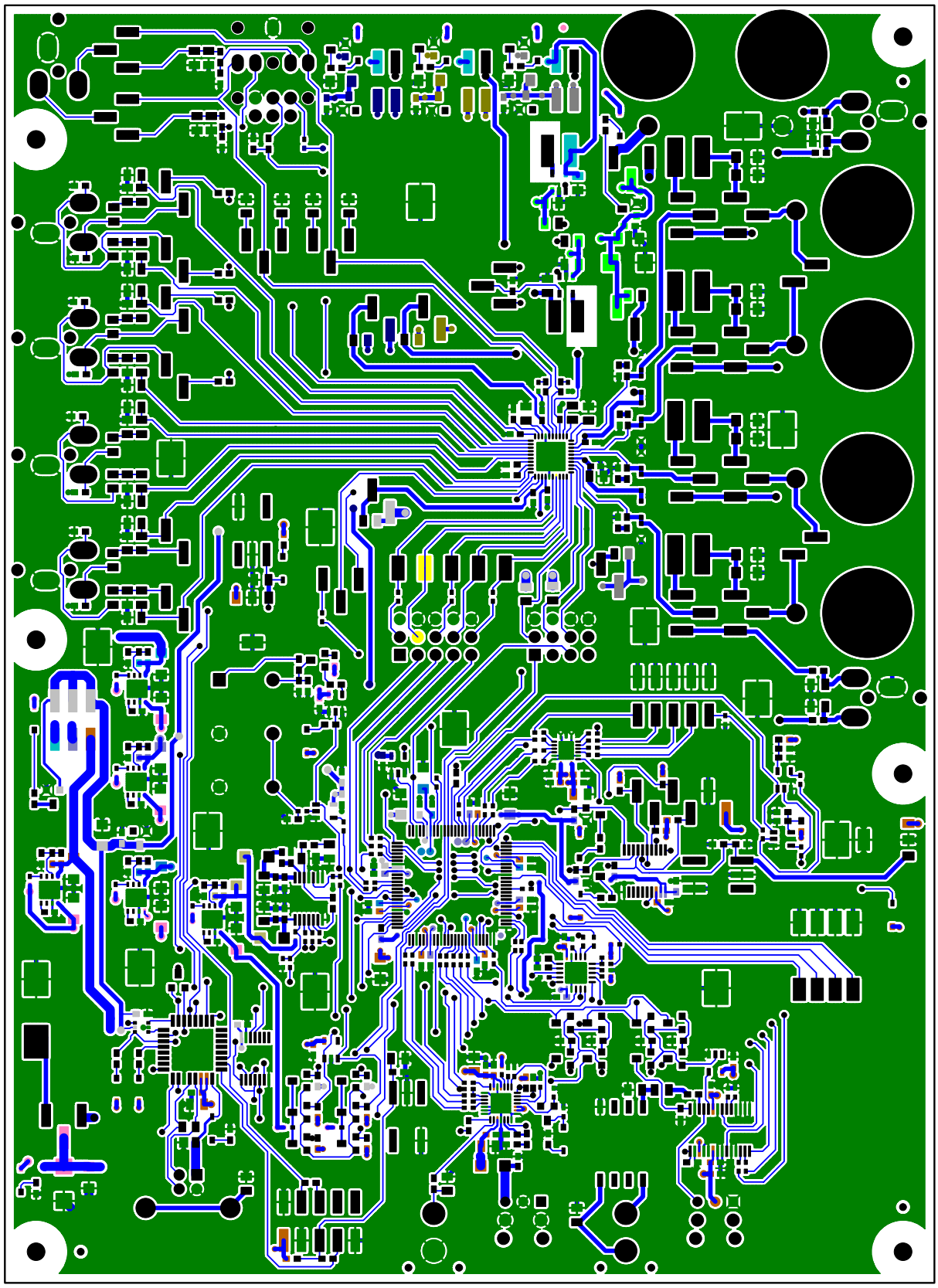


Figure 13. Top-Side Layer

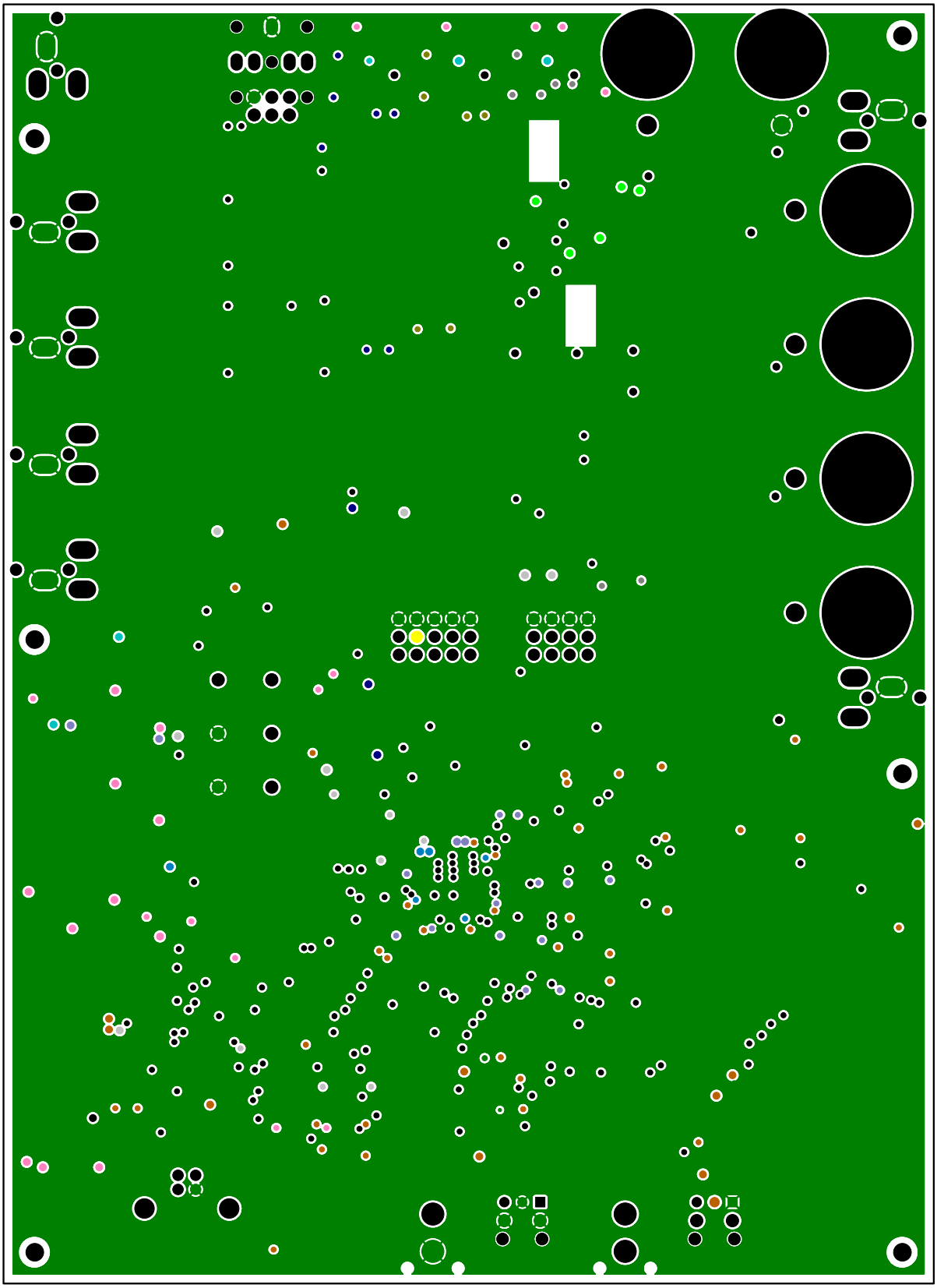


Figure 14. GND (Layer 2)

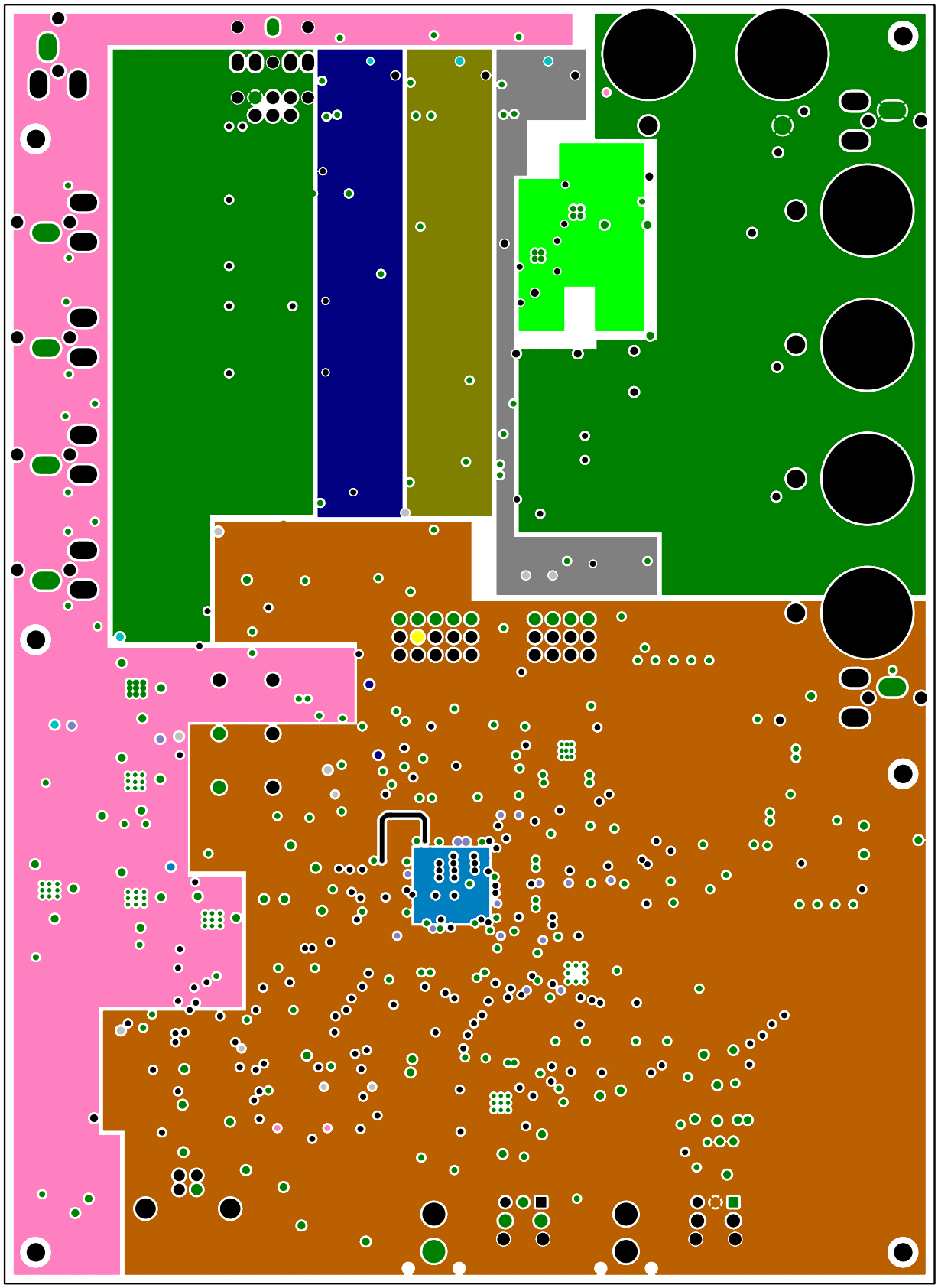


Figure 15. Power (Layer 3)

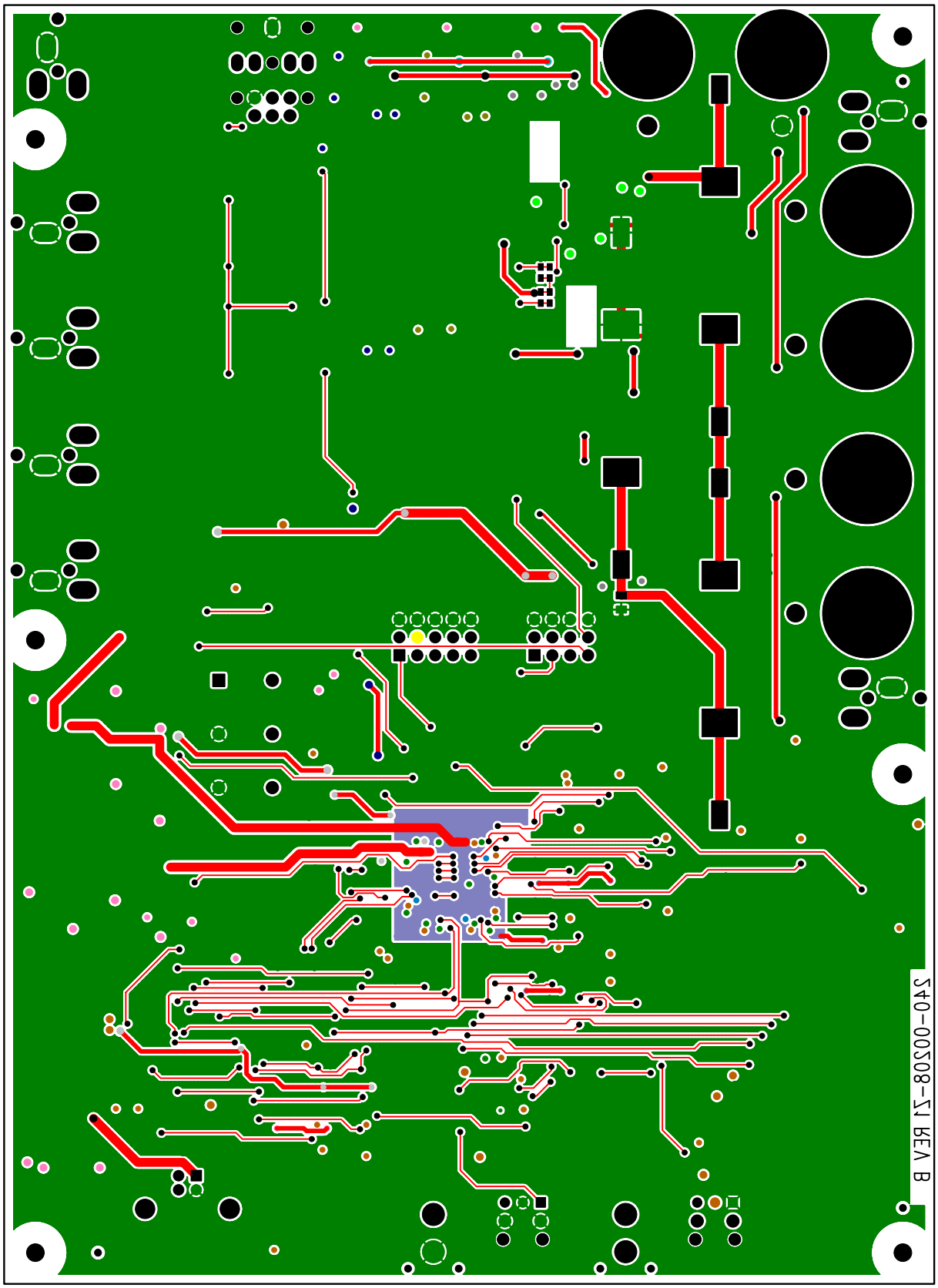


Figure 16. Bottom Side Layer

6. REVISION HISTORY

Revision	Changes
DB1	Initial Release

Contacting Cirrus Logic Support

For all product questions and inquiries, contact a Cirrus Logic Sales Representative.
To find the one nearest you, go to www.cirrus.com.