SECTION 11
ELECTRICAL SPECIFICATIONS

11.1 Introduction

This section contains electrical and timing specifications.

11.2 Maximum Ratings

This device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, it is advised that normal precautions be taken to avoid application of any voltage higher than maximum-rated voltages to this high-impedance circuit. For proper operation, it is recommended that V_{IN} and V_{OUT} be constrained to the range $V_{SS} \le (V_{IN}$ or $V_{OUT}) \le V_{DD}$. Reliability of operation is enhanced if unused inputs are connected to an appropriate logic voltage level (for example, either V_{SS} or V_{DD}). Internal I/O pulldowns may be used.

Table 11-1. Maximum Ratings*

Rating	Symbol	Value	Unit
Supply Voltage	V_{DD}	−0.3 to +7.0	V
Input Voltage	V_{IN}	V_{SS} −0.3 to V_{DD} +0.3	V
$\overline{IRQ}/V_{PP}$ Pin	V_{IN}	V_{SS} −0.3 to $2V_{DD}$ +0.3	V
Current Drain Per Pin Excluding V_{DD}, V_{SS}, and PA4–PA7	I	25	mA
Storage Temperature Range	T_{STG}	−65 to +150	°C

*Voltages are referenced to V_{SS}

11.3 Thermal Characteristics

Table 11-2. Thermal Characteristics

Rating	Symbol	Value	Unit
Thermal Resistance MC68HC705J1AP(1) MC68HC705J1ADW(2)	 θ_{JA} θ_{JA}	 60 60	 °C/W °C/W
Operating Temperature Range MC68HC705J1A (Standard) MC68HC705J1A (Extended)	T_A	T_L to T_H 0 to +70 −40 to +85	°C

NOTES:
1. P = Plastic dual-in-line package (PDIP)
2. DW = Small outline integrated circuit (SOIC)

11.4 Power Considerations

The average chip-junction temperature, T_J, can be obtained in °C from:

$$T_J = T_A + (P_D \times \theta_{JA}) \quad (1)$$

where:

T_A = Ambient temperature, °C

θ_{JA} = Package thermal resistance, junction -to-ambient, °C/W

$P_D = P_{INT} + P_{I/O}$

$P_{INT} = I_{DD} \times V_{DD}$ watts (chip internal power)

$P_{I/O}$ = Power dissipation on input and output pins (user-determined)

For most applications, $P_{I/O} \ll P_{INT}$ and can be neglected.

The following is an approximate relationship between P_D and T_J (neglecting $P_{I/O}$):

$$P_D = K + (T_J + 273°C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \times (T_A + 273°C) + \theta_{JA} \times (P_D)^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D at equilibrium for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

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11.5 DC Electrical Characteristics

Table 11-3. DC Electrical Characteristics (V_{DD} = 5 V)[1]

Characteristic	Symbol	Min	Typ[2]	Max	Unit
Output Voltage I_{LOAD} = 10.0 µA I_{LOAD} = 10.0 µA	 V_{OL} V_{OH}	 — V_{DD} –0.1	 — —	 0.1 —	 V V
Output High Voltage (I_{LOAD} = –0.8 mA) PA0-PA7, PB0-PB5	V_{OH}	V_{DD} –0.8	—	—	V
Output Low Voltage (I_{LOAD} = 1.6 mA) PA0-PA3, PB0-PB5 (I_{LOAD} = 10.0 mA) PA4-PA7	 V_{OL} V_{OL}	 — —	 — —	 0.4 0.4	 V V
Input High Voltage PA0-PA7, PB0-PB5, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input Low Voltage PA0-PA7, PB0-PB5, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply Current Run[4] Wait[3, 4, 5, 7] Stop[5, 6] 25°C –40°C to +85°C	 I_{DD} I_{DD} I_{DD} I_{DD}	 — — — —	 3.5 0.45 0.2 2.0	 6.0 2.75 10 20	 mA mA µA µA
I/O Ports Hi-Z Leakage Current PA0-PA7, PB0-PB5 (without individual pulldown activated)	I_{IL}	—	—	±10	µA
Input Pulldown Current PA0-PA7, PB0-PB5 (with individual pulldown activated)	I_{IL}	40	80	200	µA
Input Pullup Current $\overline{RESET}$	I_{IL}	–15	–35	–80	µA
Input Current[8] $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1	I_{IN}	—	—	±1	µA
Capacitance Ports (as Input or Output) $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1, OSC2	 C_{OUT} C_{IN}	 — —	 — —	 12 8	 pF pF
Crystal/Ceramic Resonator Oscillator Mode Internal Resistor OSC1 to OSC2	R_{OSC}	1.0	2.0	3.0	MΩ

NOTES:

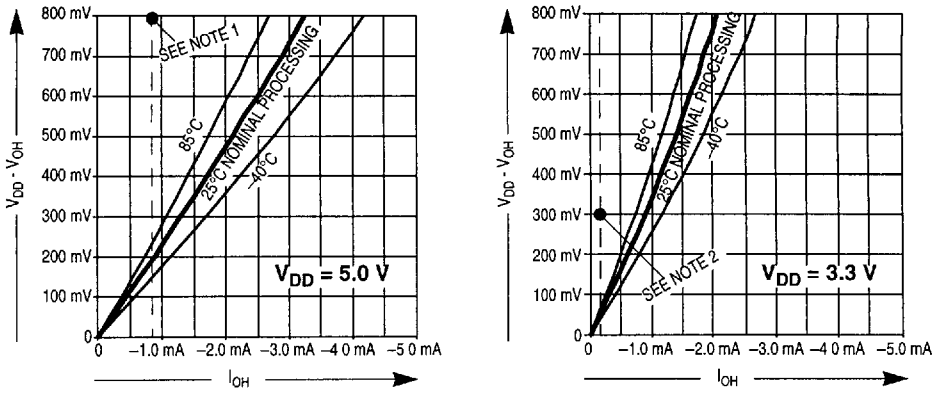
1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted
2. Typical values reflect average measurements at midpoint of voltage range, 25°C.
3. Wait I_{DD}: Only timer system active.
4. Run (Operating) I_{DD}, Wait I_{DD}: Measured using external square wave clock source (f_{OP} = 2.1 MHz), all inputs 0.2 V from rail; no dc loads, less than 50 pF on all outputs, C_L = 20 pF on OSC2.
5. Wait, Stop I_{DD}: All ports configured as inputs, V_{IL} = 0.2 V, V_{IH} = V_{DD} -0.2 V.
6. Stop I_{DD} measured with OSC1 = V_{SS}.
7. Wait I_{DD} is affected linearly by the OSC2 capacitance.
8. Only input high current rated to +1 µA on $\overline{RESET}$.

Table 11-4. DC Electrical Characteristics (V_{DD} = 3.3 V)[1]

Characteristic	Symbol	Min	Typ[2]	Max	Unit
Output Voltage I_{LOAD} = 10.0 µA I_{LOAD} = 10.0 µA	 V_{OL} V_{OH}	 — V_{DD} –0.1	 — —	 0.1 —	 V V
Output High Voltage (I_{LOAD} = –0.2 mA) PA0-PA7, PB0-PB5	V_{OH}	V_{DD} –0.3	—	—	V
Output Low Voltage (I_{LOAD} = 0.4mA) PA0-PA3, PB0-PB5 (I_{LOAD} = 5.0mA) PA4-PA7	 V_{OL} V_{OL}	 — —	 — —	 0.3 0 3	 V V
Input High Voltage PA0-PA7, PB0-PB5, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IH}	0.7 × V_{DD}	—	V_{DD}	V
Input Low Voltage PA0-PA7, PB0-PB5, $\overline{IRQ}$/V_{PP}, $\overline{RESET}$, OSC1	V_{IL}	V_{SS}	—	0.2 × V_{DD}	V
Supply Current Run[4] Wait[3, 4, 5, 7] Stop[5, 6] 25°C –40°C to +85°C	 I_{DD} I_{DD} I_{DD} I_{DD}	 — — — —	 1.2 0 25 0 1 1	 4.0 1 5 5 10	 mA mA µA µA
I/O Ports Hi-Z Leakage Current PA0-PA7, PB0-PB5 (without individual pulldown activated)	I_{IL}	—	—	±10	µA
Input Pulldown Current PA0-PA7, PB0-PB5 (with individual pulldown activated)	I_{IL}	15	30	100	µA
Input Pullup Current $\overline{RESET}$	I_{IL}	–10	–20	–40	µA
Input Current[8] $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1	I_{IN}	—	—	±1	µA
Capacitance Ports (as Input or Output) $\overline{RESET}$, $\overline{IRQ}$/V_{PP}, OSC1, OSC2	 C_{OUT} C_{IN}	 — —	 — —	 12 8	 pF pF
Crystal/Ceramic Resonator Oscillator Mode Internal Resistor OSC1 to OSC2	R_{OSC}	1.0	2.0	3.0	MΩ

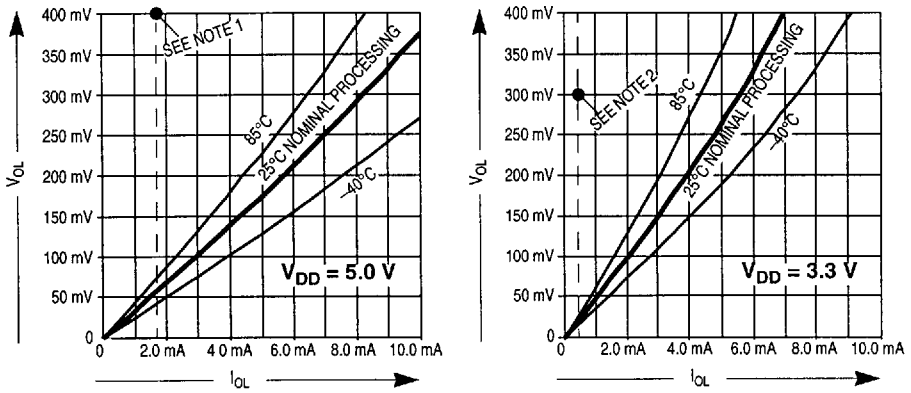
NOTES:

1. V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted
2. Typical values reflect average measurements at midpoint of voltage range, 25°C.
3. Wait I_{DD}: Only timer system active.
4. Run (Operating) I_{DD}, Wait I_{DD}: Measured using external square wave clock source (f_{OP} = 1.0 MHz), all inputs 0.2 V from rail; no dc loads, less than 50 pF on all outputs, C_L = 20 pF on OSC2.
5. Wait, Stop I_{DD}: All ports configured as inputs, V_{IL} = 0.2 V, V_{IH} = V_{DD} -0.2 V.
6. Stop I_{DD} measured with OSC1 = V_{SS}.
7. Wait I_{DD} is affected linearly by the OSC2 capacitance.
8. Only input high current rated to +1 µA on $\overline{RESET}$.



NOTES:
1. At V_{DD} = 5.0 V, devices are specified and tested for ($V_{DD} - V_{OH}$) ≤ 800 mV @ I_{OL} = –0.8 mA.
2. At V_{DD} = 3.3 V, devices are specified and tested for ($V_{DD} - V_{OH}$) ≤ 300 mV @ I_{OL} = –0.2 mA.

Figure 11-1. PA0–PA7, PB0–PB5 Typical High-Side Driver Characteristics



NOTES:
1. At V_{DD} = 5.0 V, devices are specified and tested for V_{OL} ≤ 400 mV @ I_{OL} = 1.6 mA.
2. At V_{DD} = 3.3 V, devices are specified and tested for V_{OL} ≤ 300 mV @ I_{OL} = 0.4 mA.

Figure 11-2. PA0–PA3, PB0–PB5 Typical Low-Side Driver Characteristics

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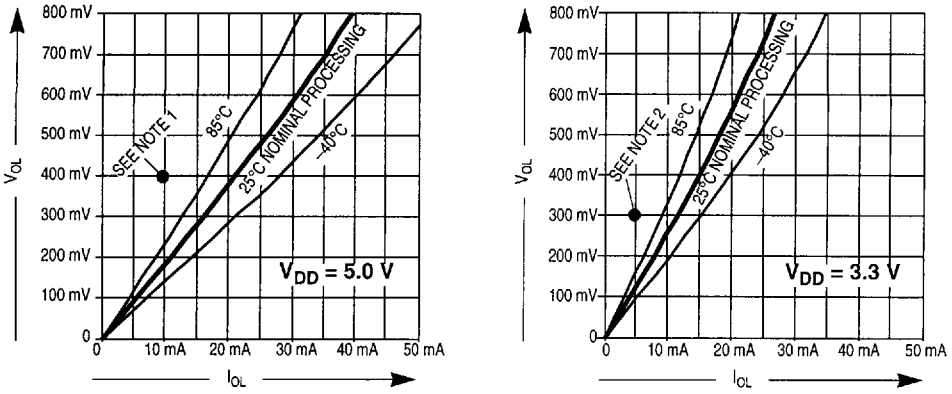
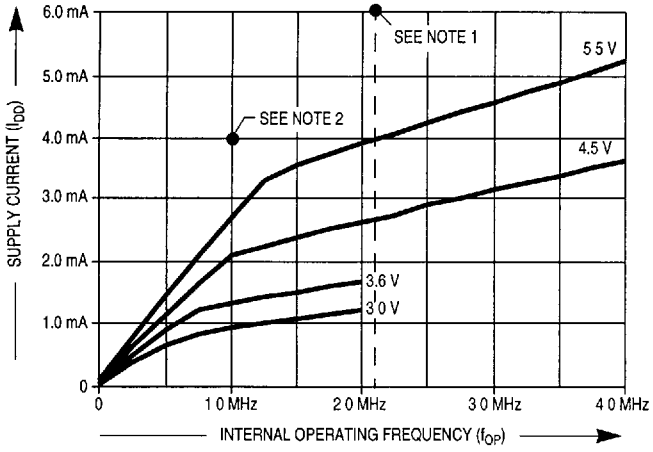


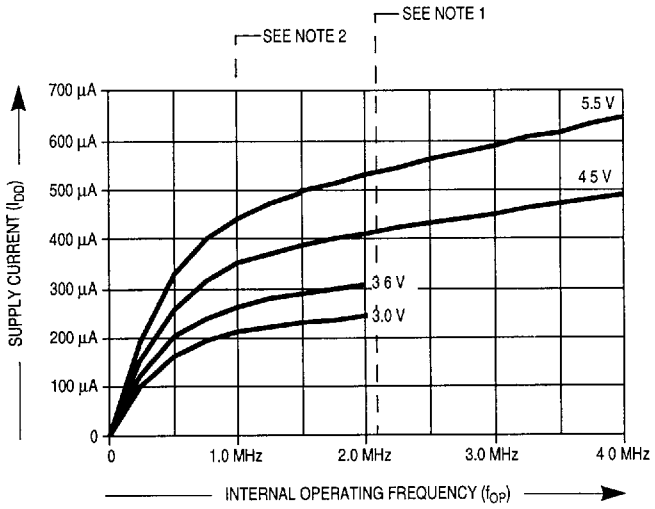
NOTES:
1. At V_{DD} = 5.0 V, devices are specified and tested for $V_{OL} \leq 400$ mV @ I_{OL} = 10.0 mA.
2. At V_{DD} = 3.3 V, devices are specified and tested for $V_{OL} \leq 300$ mV @ I_{OL} = 5.0 mA.

Figure 11-3. PA4–PA7 Typical Low-Side Driver Characteristics



NOTES:
1. At V_{DD} = 5.0 V, devices are specified and tested for $I_{DD} \leq 6.0$ mA @ f_{OP} = 2.1 MHz.
2. At V_{DD} = 3.3 V, devices are specified and tested for $I_{DD} \leq 4.0$ mA @ f_{OP} = 1.0 MHz.

Figure 11-4. Typical Operating I_{DD} (25°C)



NOTES:
1. At V_{DD} = 5.0 V, devices are specified and tested for $I_{DD} \leq 2.75$ mA @ f_{OP} = 2.1 MHz.
2. At V_{DD} = 3.3 V, devices are specified and tested for $I_{DD} \leq 1.5$ mA @ f_{OP} = 1.0 MHz.

Figure 11-5. Typical Wait Mode I_{DD} (25°C)

11.6 EPROM Programming Characteristics

Table 11-5. EPROM Programming Characteristics(1)

Characteristic	Symbol	Min	Typ	Max	Unit
Programming Voltage $\overline{IRQ}/V_{PP}$	V_{PP}	16.0	16.5	17.0	V
Programming Current $\overline{IRQ}/V_{PP}$	I_{PP}	—	3.0	10.0	mA
Programming Time Per Array Byte MOR	 t_{EPGM} t_{MPGM}	 4 4	 — —	 — —	 ms ms

NOTE: 1 V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = −40°C to +85°C, unless otherwise noted.

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11.7 Control Timing

Table 11-6. Control Timing (5 V)[1]

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation Crystal Oscillator Option External Clock Source	 f_{OSC} f_{OSC}	 — DC	 4.2 4.2	 MHz MHz
Internal Operating Frequency Crystal Oscillator ($f_{OSC} \div 2$) External Clock ($f_{OSC} \div 2$)	 f_{OP} f_{OP}	 — DC	 2.1 2.1	 MHz MHz
Cycle Time ($1/f_{OP}$)	t_{CYC}	476	—	ns
$\overline{\text{RESET}}$ Pulse Width Low	t_{RL}	1.5	—	t_{CYC}
$\overline{\text{IRQ}}$ Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	1.5	—	t_{CYC}
$\overline{\text{IRQ}}$ Interrupt Pulse Width (Edge and Level Triggered)	t_{ILIL}	1.5	Note 2	t_{CYC}
PA0 through PA3 Interrupt Pulse Width High (Edge-Triggered)	t_{IHIL}	1.5	—	t_{CYC}
PA0 through PA3 Interrupt Pulse Width (Edge and Level Triggered)	t_{IHIH}	1.5	Note 2	t_{CYC}
OSC1 Pulse Width	t	200	—	ns

NOTES:

1. V_{DD} = 5.0 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted
2. The maximum width t_{ILIL} or t_{IHIH} should not be more than the number of cycles it takes to execute the interrupt service routine plus 19 t_{CYC} or the interrupt service routine will be re-entered.

Table 11-7. Control Timing (3.3 V)[1]

Characteristic	Symbol	Min	Max	Unit
Frequency of Operation Crystal Oscillator Option External Clock Source	 f_{OSC} f_{OSC}	 — DC	 2.0 2.0	 MHz MHz
Internal Operating Frequency Crystal Oscillator ($f_{OSC} \div 2$) External Clock ($f_{OSC} \div 2$)	 f_{OP} f_{OP}	 — DC	 1.0 1.0	 MHz MHz
Cycle Time ($1/f_{OP}$)	t_{CYC}	1000	—	ns
$\overline{\text{RESET}}$ Pulse Width Low	t_{RL}	1.5	—	t_{CYC}
$\overline{\text{IRQ}}$ Interrupt Pulse Width Low (Edge-Triggered)	t_{ILIH}	1.5	—	t_{CYC}
$\overline{\text{IRQ}}$ Interrupt Pulse Width (Edge and Level Triggered)	t_{ILIL}	1.5	Note 2	t_{CYC}
PA0 through PA3 Interrupt Pulse Width High (Edge-Triggered)	t_{IHIL}	1.5	—	t_{CYC}
PA0 through PA3 Interrupt Pulse Width (Edge and Level Triggered)	t_{IHIH}	1.5	Note 2	t_{CYC}
OSC1 Pulse Width	t	400	—	ns

NOTES:

1. V_{DD} = 3.3 Vdc ± 10%, V_{SS} = 0 Vdc, T_A = –40°C to +85°C, unless otherwise noted
2. The maximum width t_{ILIL} or t_{IHIH} should not be more than the number of cycles it takes to execute the interrupt service routine plus 19 t_{CYC} or the interrupt service routine will be re-entered.

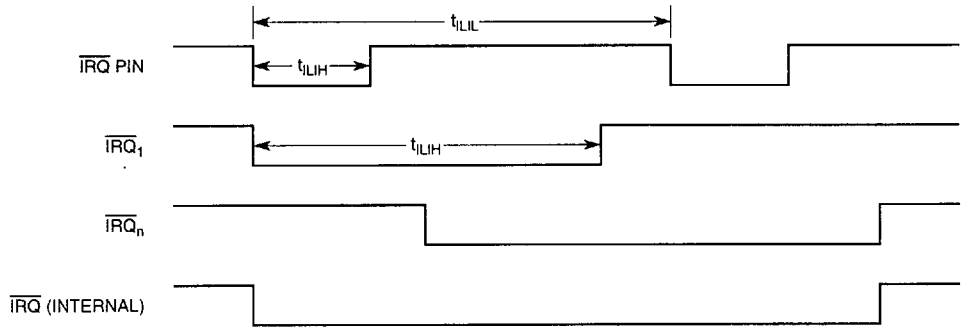
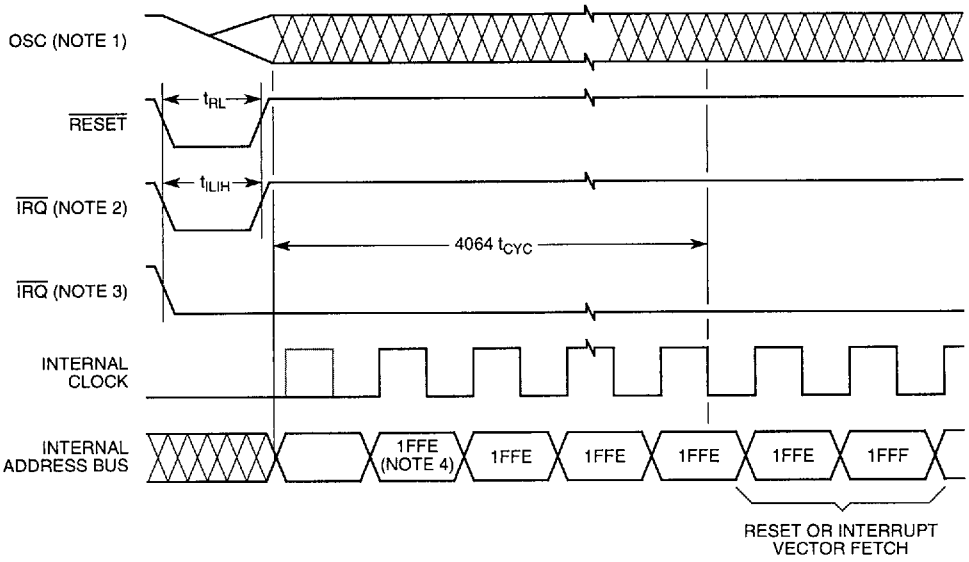


Figure 11-6. External Interrupt Timing



NOTES:

1. Internal clocking from OSC1 pin.
2. Edge-triggered external interrupt mask option.
3. Edge- and level-triggered external interrupt mask option.
4. Reset vector shown as example.

Figure 11-7. Stop Mode Recovery Timing

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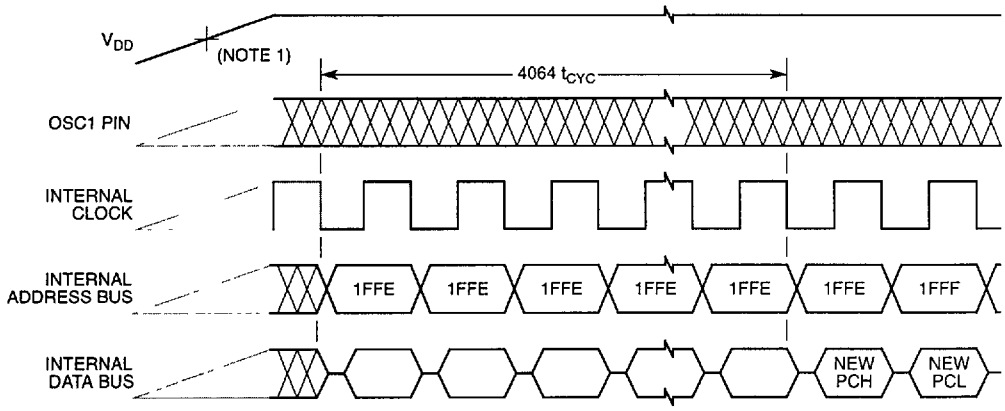
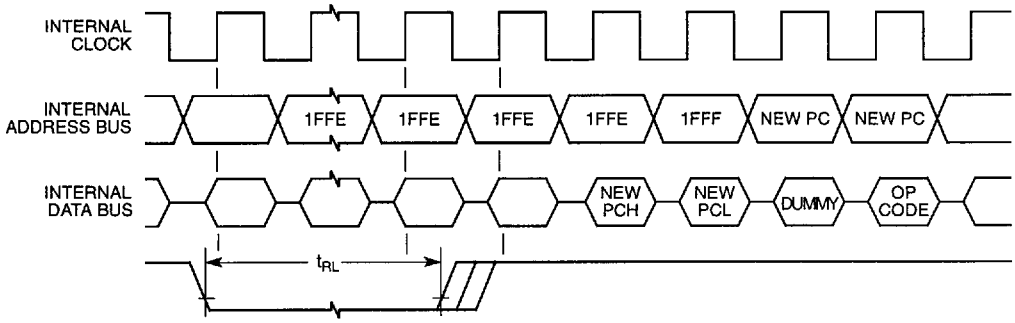


NOTES:

1. Power-on reset threshold is typically between 1 V and 2 V.
2. Internal clock, internal address bus, and internal data bus are not available externally.

Figure 11-8. Power-On Reset Timing



NOTES:

1. Internal clock, internal address bus, and internal data bus are not available externally.
2. The next rising edge of the internal clock after the rising edge of $\overline{\text{RESET}}$ initiates the reset sequence.

Figure 11-9. External Reset Timing

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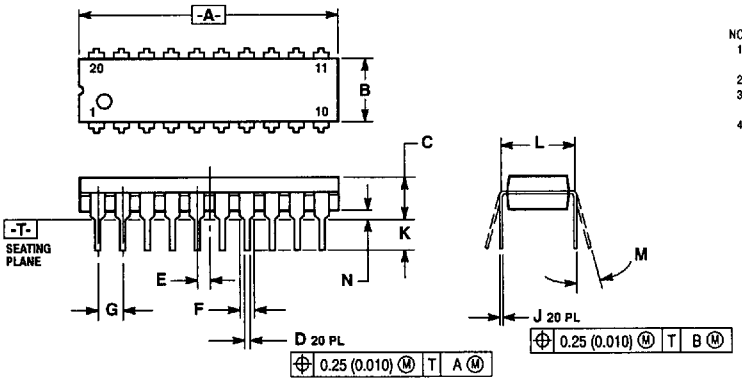
SECTION 12
MECHANICAL SPECIFICATIONS

12.1 Introduction

This section gives the dimensions of the plastic dual in-line package (PDIP) and the small outline integrated circuit (SOIC) package.

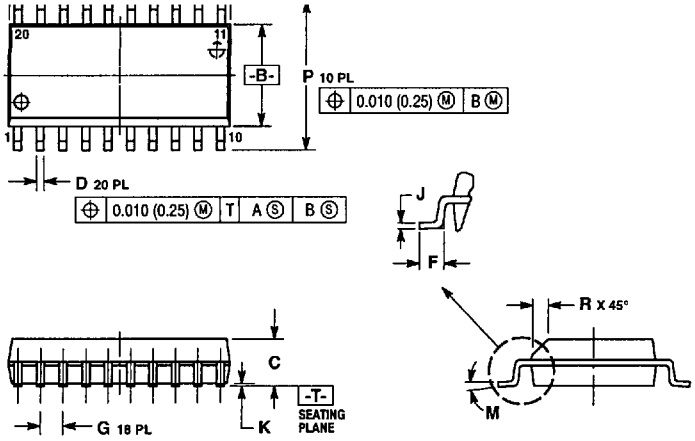
12.2 PDIP Package (Case 738-03)



NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

12.3 SOIC Package (Case 751D-04)



NOTES
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029