Preliminary Data Sheet
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microelectronics group

Lucent Technologies
Bell Labs Innovations

LU5X34F
Quad Gigabit Ethernet Transceiver

Overview

The LU5X34F is a low-cost, low-power quad transceiver. It is used for data transmission over fiber or coaxial media in conformance with *IEEE** 802.3z Gigabit Ethernet specification and Fibre Channel *ANSI*† X3T11 at 1.0 Gbits/s and 1.25 Gbits/s.

Each of the four transceivers independently provides complete serialize/deserialize (SERDES) and transmit and receive functions. The device is available in a 217-pin PBGA package.

The transmitter section accepts TTL compatible data at the 10-bit parallel input port. The parallel input data is latched on the rising edge of TXCLKx. It also accepts the low-speed, TTL compatible system clock, REFCLK, and uses this clock to synthesize the internal high-speed serial bit clock. The serialized data is then available at the differential PECL outputs, terminated in 50 Ω or 75 Ω to drive either an optical transmitter or coaxial media.

The receive section receives high-speed serial data at its differential PECL input port. This data is fed to the digital clock recovery section, which generates a recovered clock and retimes the data. The retimed data is deserialized and presented as 10-bit parallel data on the output port. A divided-down version of the recovered clock, synchronous with parallel data bytes, is also available as a TTL compatible output. The receive section recognizes the comma character and aligns the comma-containing byte on the word boundary, when ENCDET = 1.

Features

- Designed to operate in Ethernet, fibre channel, *Firewire*‡, or backplane applications.
- Operationally compliant to *IEEE* 802.3z Gigabit Ethernet specification.
- Operationally compliant to Fibre Channel *ANSI* X3T11. Provides FC-0 services at 1.0 Gbits/s—1.25 Gbits/s (10-bit encoded data rate).
- 100 MHz—125 MHz differential or single-ended reference clock.
- 10-bit parallel, TTL-compatible I/O interface.
- 8-bit/10-bit encoded data.
- High-speed comma character recognition (K28.1, K28.5, K28.7) for latency-sensitive applications and alignment to word boundary.
- Two 50 MHz—62.5 MHz receive-byte clocks.
- Single analog PLL design requires no external components for the frequency synthesizer.
- Novel digital data lock in receiver avoids the need for multiple analog PLLs.
- Expandable beyond four serializer/deserializers.
- PECL high-speed interface I/O for use with optical transceiver or coaxial copper media.
- Requires one external resistor for PECL output reference-level definition.
- Low-power digital CMOS technology.
- Less than 2 W total power dissipation per quad transceiver.
- 3.3 V ± 5% power supply.
- 0 °C—70 °C ambient temperature.
- Stand-alone transceiver product.
- Transceiver macrocell template.
- Available in 217-pin PBGA package.

* *IEEE* is a registered trademark of The Institute of Electrical and Electronics Engineers, Inc.
† *ANSI* is a registered trademark of American National Standards Institute.
‡ *FireWire* is a registered trademark of Apple Computer, Inc.

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Functional Description

The LU5X34F transceiver provides for data transmission over fiber or coaxial media at 1.0 Gbits/s to 1.25 Gbits/s. The block diagram of the quad transceiver is shown in Figure 1 and the four-channel application pinout for the 217-pin PBGA package is given in Figure 3 and Table 3.

Transmitter Section

The transmitter accepts 8b/10b encoded bits in 10-bit parallel form and converts to serial format for up to 1.25 Gbits/s transmission. The serial nonreturn to zero (NRZ) bits are then shifted out of the device at a maximum rate of 1.25 Gbits/s. Internally, the device uses two parallel shift registers that operate at half rate (i.e., a maximum of 625 MHz) for reduced power consumption. The two shift registers drive the PECL output buffer in an interleaved manner to construct the 1.25 Gbits/s output data stream.

The typical transmit-and-receive, high-speed I/O interfacing for a single-channel backplane application is shown in Figure 9.

The transmit shift register and other circuits are driven with clocks generated from a 500 MHz—625 MHz internal clock. This internal clock is sourced from a voltage-controlled oscillator (VCO) that is locked to the external reference of 100 MHz—125 MHz. The internal transmit phase- lock loop multiplies the frequency of the input reference clock by a factor of 5, and controls the transmit jitter bandwidth with appropriate design of the jitter transfer function. The transmit phase-lock loop generates multiple clock phases that are all used by each of the four receiver circuits. The clock phases are derived from the transmit VCO.

Receiver Section

Each of the quad receiver circuits recovers clock from and retimes the serial input data. The data is input to the receiver on differential PECL buffers. External termination resistors are supplied by the user in accordance with *ANSI* standard, X3T11. The serial differential inputs, HDINP and HDINN, are ac-coupled to the device and internally biased to the PECL input common-mode range center. See Figure 9 for the typical application and termination of the transmission lines.

The receiver data-retiming circuit uses a digital timing recovery loop that compares the phase of the input data to multiple phases of the on-device VCO in the transmit section. One of the phases is chosen to retime the receive data. A digital low-pass filter is used in the timing recovery loop to reject jitter from the data input. A novel phase interpolation circuit permits the retiming clock's phase to be stepped with fine resolution for precise alignment of the sampling clock within the data eye. Use of this digital data locking scheme for each receiver advantageously avoids the use of multiple analog phase-lock loops on-device that can potentially injection lock to one another. Additionally, the digital data locking loop maintains precise loop dynamics, hence, the jitter transfer function is process and temperature independent.

Lock to Reference

The receive circuit has two modes of operation: lock to reference, and lock to data with retiming. When no data or invalid data is present on the HDINP and HDINN input pins, the user can program the device to ignore the input data by setting LCKREFN equal to logic 0. In this mode, neither the PECL input buffer nor the RX parallel data bus toggles. In normal operation, the LCKREFN is a logic 1 and the receiver attempts to lock to the incoming data. If the input data is invalid or outside the nominal ± frequency range, the receive digital PLL will simply ramp the phase of the output clock until it locks to data.

Table 1. Receive Circuit Operating Modes*

Mode	Lock to Reference	Lock to Receive Data
LCKREFN = 1 (normal operation)	Not applicable.	Continually attempts to lock to data.
LCKREFN = 0	Lock to clock, output data does not toggle. Disable PECL input buffer.	Not applicable.

* REFCLK requirements are given in Table 4, and receive PLL specifications are given in Table 5.

Functional Description (continued)

Byte Alignment

When ENCDET = 1, the LU5X34F recognizes the comma character and aligns this 10-bit character to the word boundary, bits RX[0:9].

COMDET =1 when the parallel output word contains a byte-aligned comma character. The COMDET flag will continue to pulse a logic 1 whenever a byte-aligned comma character is at the parallel output port, independent of ENCDET. When ENCDET = 0, there are two possible scenarios depending upon when the comma character is received.

1. If byte alignment had been previously achieved when ENCDET had been a logic 1, the COMDET flag will continue to pulse a logic 1 whenever a byte-aligned comma character is at the parallel output port. If a comma character occurs that is not on the word boundary, no attempt will be made to align this comma character and the COMDET flag will remain at a logic 0.
2. If byte alignment had **not** been previously achieved when ENCDET had been a logic 1, then the first (and only the first) comma character received will be aligned to the word boundary. COMDET will pulse when the comma character is aligned to the word boundary.

Parallel Output Port

Timing for the parallel output data and the 50 MHz to 62.5 MHz receive-byte clock is given in Table 14.

Two low data rate receive-byte clocks are available as TTL compatible outputs during use of the parallel output port in 10-bit mode. RXCLK1 is the receive byte clock used by the protocol device to register bytes 0 and 2. RXCLK0 is the receive-byte clock used by the protocol device to register bytes 1 and 3, and it is 180 degrees out of phase with RXCLK1. Both RXCLK1 and RXCLK0 can be stretched during byte alignment but not truncated or slivered. The maximum allowable frequency of these two clocks under all circumstances, excluding start-up, will not exceed 80 MHz. The start-up time is specified as 1 ms.

Loopback Mode Operation

A control signal input, EWRAP, selects between two possible sets of inputs: normal data (HDINP, HDINN) or internal loopback data. When EWRAP = 1, the serial output ports, HDOUTP and HDOUTN, remain active. The serial transmit data prior to the PECL output driver is directed to the data recovery circuit, where clock is recovered and data is resynchronized to the recovered clock. Retimed data and clock then go to the serial-to-parallel converter.

Table 2. Definition of Bit Transmission/Reception Order*

Serial Transmit/ Receive Rate	TXx[9:0]	RXx[9:0]
1.0 Gbits/s to 1.25 Gbits/s	TXx[0] bit serially transmitted first at HDOUTxP, HDOUTxN	RXx[0] bit received first at serial inputs HDINxP, HDINxN

* Lower case x signifies channel A, B, C, or D.

Functional Description (continued)

Powerup Sequence

The power ramp time for the LU5X34F is specified at V_{DD} > 2.7 V within 20 µs of start-up. Once 2.7 V is reached, the device is held in reset for 15 µs—70 µs. The REFCLK must be active and within specification at this point and remain active while the device is powered up, unless in Reset.

When signals RESET, BYPPLL, and LPWR are all low, the following start-up sequence occurs:

1. 0 µs—32 µs, the analog PLL is held at minimum frequency to allow dc bias to settle.
2. 32 µs—262 µs, the analog PLL has locked-in and receiver analog circuits start to lock-in.
3. 262 µs—326 µs, the receiver analog circuits are locked; receiver starts to lock onto incoming data.
4. After 358 µs, the receiver is locked onto incoming data and can be viewed at the parallel output ports. The comma-detect circuit is enabled at this point, allowing byte alignment if ENCDET = 1.

If LCKREFN goes low after the 358 µs, the receiver will sit idle. When LCKREFN goes high, the receiver will be locked onto data after 2 µs.

Device Reset

The RESETN input to the device is active-low. When activated with a pulse duration of 1 µs, the RESETN signal globally resets the device and the following is performed:

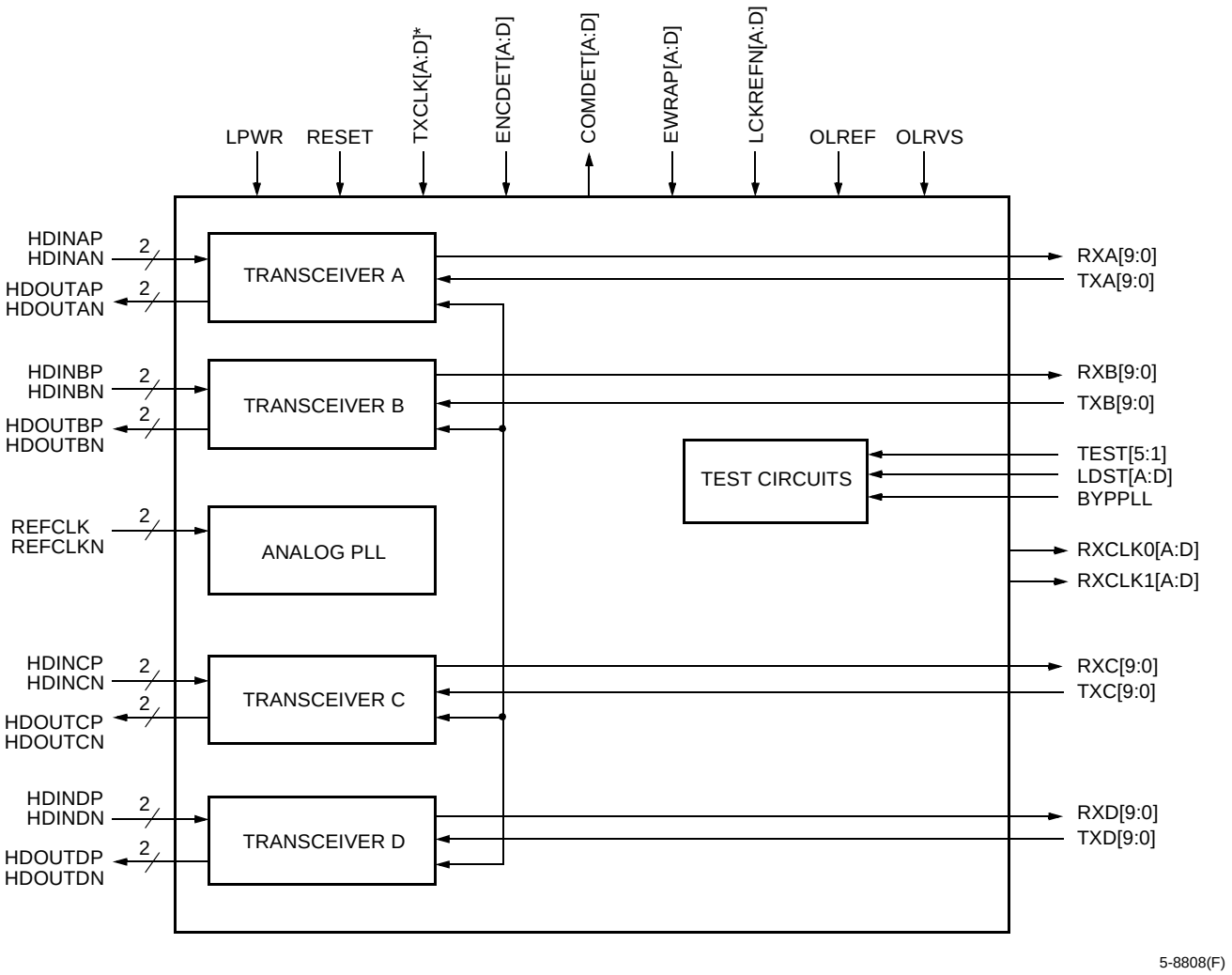
1. The single analog PLL is forced to operate at the minimum frequency possible for its VCO. The PLL will not be locked in this condition.
2. The HDOUTP, HDOUTN outputs are forced to a PECL logic 0.
3. The deserializer clocks, but input data at HDINP, HDINN is ignored and the RX[9:0] signals remain in their previous state.
4. The phase interpolation/selection circuits are deactivated and the selected phase is reset.
5. The receiver digital low-pass filter in the DPLL is reset. Normally, a reset is not necessary for correct operation, although a reset can aid rapid lock-in of the internal PLL circuitry. This active-low pin is internally pulled high.

Sleep Mode

The LU5X34F has a sleep mode that is activated by enabling LPWR. In this mode, a divided-down version of the REFCLK is used to refresh the dynamic circuits within the transceiver. The PLL is powered down in this mode also. LCKREFN can also be activated to reduce the power even further. Note that complete powerdown for $I_{DD}Q$ testing is not supported due to the dynamic logic used in the high-speed sections of the transceiver. The lock-in sequence timing is needed when coming out of sleep mode.

Functional Description (continued)

Block Diagrams



* Synchronous with REFCLK(N).

Figure 1. LU5X34F Quad Gigabit Ethernet Transceiver Block Diagram

Functional Description (continued)

Block Diagrams (continued)

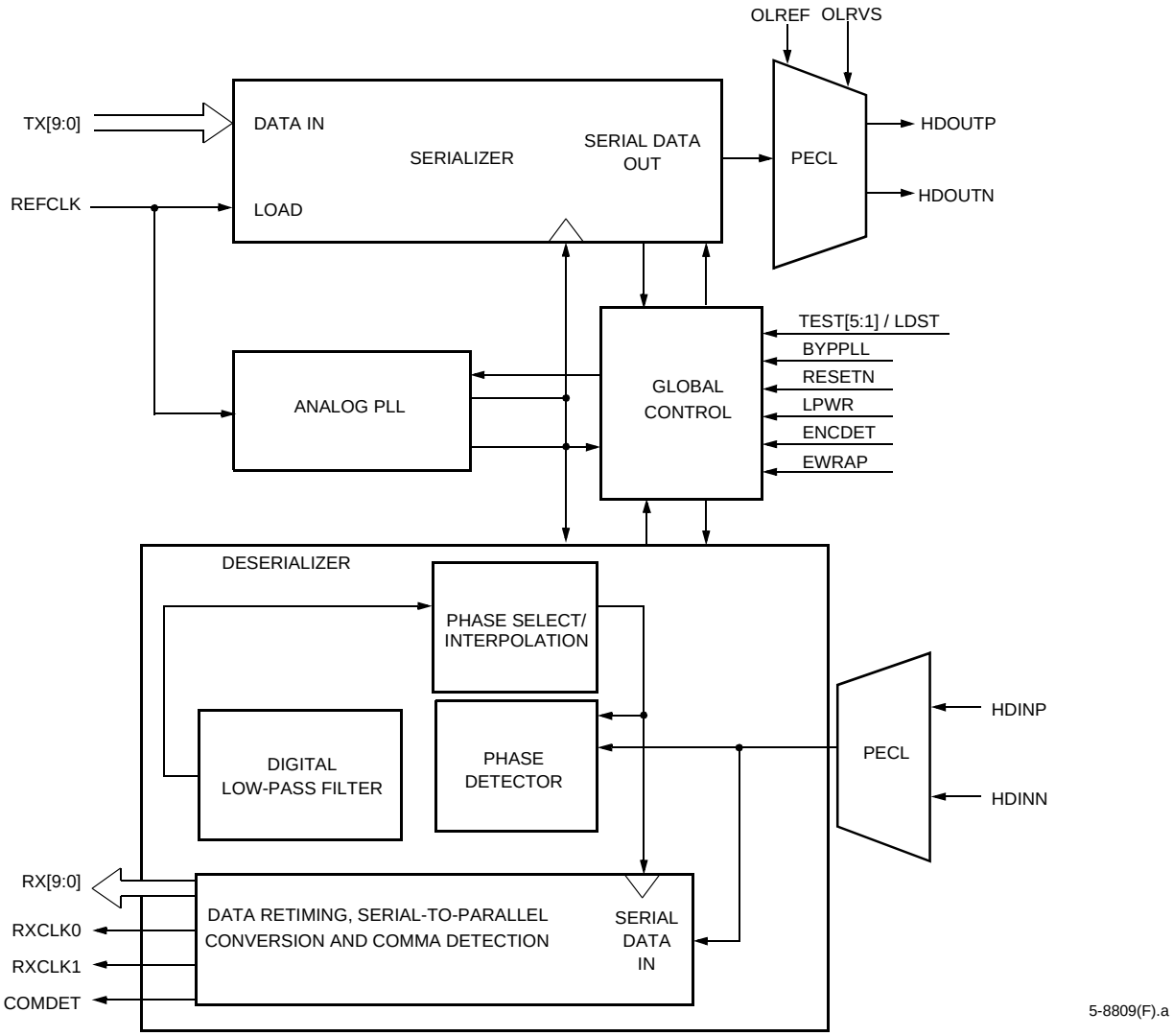


Figure 2. LU5X34F Single-Channel Transceiver Functional Diagram

Input/Output Information

	A	B	C	D	E	F	G	H	J	K	L	M	N	P	R	T	U
1	RXB7	RXB6	RXB2	EWRAPA	LCKREFA	LCKREFB	TEST2	TEST4	BYPPLL	REFCLK	ENCDETC	ENCDETD	LCKREFD	TXC1	TXC5	TXC5	N/C
2	RXB8	VSS	RXB5	RXB1	ENCDETA	EWRAPB	RESETN	TEST3	TEST5	REFCLKN	LDSTC	LDSTD	TXC0	TXC4	TXC8	VSS	TXCLKC
3	RXCLK0B	RXB9	VSS	RXB4	N/C	LDSTA	ENCDETB	TEST1	LPWR	EWRAPC	LPBKD	N/C	TXC3	TXC7	VSS	N/C	N/C
4	TXB9	RXCLK1B	COMDETB	VSS	RXB3	RXB0	LDSTB	VDD	VSS	VDD	LCKREFC	TXC2	TXC6	VSS	RXCLK1C	COMDETC	RXC7
5	TXB6	TXB8	N/C	VDD										RXCLK0C	RXC8	RXC6	RXC4
6	TXB4	TXB5	TXB7	TXCLKB										RXC9	RXC5	RXC3	RXC0
7	TXB0	TXB1	TXB3	TXB2										RXC1	RXC2	N/C	TXD1
8	RXA1	RXA0	N/C	VDD				VSS	VSS	VSS				VDD	TXD0	TXD2	TXD3
9	RXA3	RXA4	RXA2	VSS				VSS	VSS	VSS				VSS	TXD6	TXD4	TXD5
10	RXA5	RXA6	RXA8	VDD				VSS	VSS	VSS				VDD	TXD10	TXD8	TXD7
11	RXA7	RXA9	RXCLK0A	N/C										N/C	RXCLK1D	TXCLKD	N/C
12	COMDETA	RXCLK1A	TXCLKA	TXA7										RXD6	RXD9	N/C	RXCLK0D
13	N/C	VDD	TXA8	TXA4										RXD2	RXD5	RXD8	COMDETD
14	TXA9	TXA6	TXA3	VSST	HDINAN	HDOUTAP	HDOUTBP	VDDR	VSST	VDDR	VSSRC	N/C	VDDTD	VSS	RXD1	RXD4	RXD7
15	TXA5	TXA2	VSST	HDINAP	HDOUTAN	HDINBP	HDOUTBN	VSSP	VREG	VSSRC	VDDTC	HDOUTCP	HDINDP	HDOUTDN	VSS	RXD0	RXD3
16	TXA1	VSST	VSSRA	VDDTA	VSSRB	VSSRB	VDDTB	VDDP	N/C	OLREF	HDINCP	HDOUTCN	VDDTC	HDINDN	HDOUTDP	VSS	N/C
17	TXA0	N/C	VSSRA	VDDTA	HDINBN	VDDTB	VDDP	VSSP	N/C	OLRVS	N/C	HDINCN	N/C	VSSRD	VSSRD	VDDTD	N/C

5-8880(F)

Figure 3. Pin Designations (Top View)

Input/Output Information (continued)

Table 3a. Pinout—Channel A I/O

Name	Pin	I/O	Level	Description
TXA9 TXA8 TXA7 TXA6 TXA5 TXA4 TXA3 TXA2 TXA1 TXA0	A14 C13 D12 B14 A15 D13 C14 B15 A16 A17	Input	TTL/ CMOS	**Channel A, Transmit Data [9:0].** Parallel input bits [9:0], one 10-bit, 8b/10b encoded data byte, clocked-in on the rising edge of TXCLKA. TXA0 is the LSB.
RXA9 RXA8 RXA7 RXA6 RXA5 RXA4 RXA3 RXA2 RXA1 RXA0	B11 C10 A11 B10 A10 B9 A9 C9 A8 B8	Output	TTL/ CMOS	**Channel A, Receive Data [9:0].** Parallel output bits [9:0], one 10-bit data type, clocked-out on the alternate rising edge of RXCLK0A, RXCLK1A. RXA0 is the LSB.
TXCLKA	C12	Input	TTL/ CMOS	**Transmit Clock (100 MHz—125 MHz).** Used to latch TXA[9:0] data into the LU5X34F. Synchronous with REFCLK(N)
RXCLK0A	C11	Output	TTL/ CMOS	**Channel A, Receive Byte-Align Clock 0.**
RXCLK1A	B12	Output	TTL/ CMOS	**Channel A, Receive Byte-Align Clock 1.**
ENCDETA	E2	Input	TTL/ CMOS	**Channel A, Enable Comma Detect A.**
COMDETA	A12	Output	TTL/ CMOS	**Channel A, Byte-Aligned Comma A.**
EWRAPA	D1	Input	TTL/ CMOS	**Channel A, Loopback at Serial I/O A.**
LCKREFNA	E1	Input	TTL/ CMOS	**Channel A, Lock Receiver to Clock.**
HDINAP, HDINAN	D15, E14	Input	PECL	**Channel A, Differential Serial Inputs.**
HDOUTAP, HDOUTAN	F14, E15	Output	PECL	**Channel A, Differential Serial Outputs.**
LDSTA	F3	Input	TTL/ CMOS	**Channel A, Load Test[5:1] Inputs.**

Input/Output Information (continued)

Table 3b. Pinout—Channel B I/O

Name	Pin	I/O	Level	Description
TXB9 TXB8 TXB7 TXB6 TXB5 TXB4 TXB3 TXB2 TXB1 TXB0	A4 B5 C6 A5 B6 A6 C7 D7 B7 A7	Input	TTL/ CMOS	**Channel B**, **Transmit Data [9:0].** Parallel input bits [9:0], one 10-bit, 8b/10b encoded data byte, clocked-in on the rising edge of TXCLKB. TXB0 is the LSB.
RXB9 RXB8 RXB7 RXB6 RXB5 RXB4 RXB3 RXB2 RXB1 RXB0	B3 A2 A1 B1 C2 D3 E4 C1 D2 F4	Output	TTL/ CMOS	**Channel B, Receive Data [9:0].** Parallel output bits [9:0], one 10-bit data type, clocked-out on the alternate rising edge of RXCLK0B, RXCLK1B. RXB0 is the LSB.
TXCLKB	D6	Input	TTL/ CMOS	**Transmit Clock (100 MHz—125 MHz).** Used to latch TXB[9:0] data into the LU5X34F. Synchronous with REFCLK(N)
RXCLK0B	A3	Output	TTL/ CMOS	**Channel B, Byte-Align Clock 0.**
RXCLK1B	B4	Output	TTL/ CMOS	**Channel B, Byte-Align Clock 1.**
ENCDETB	G3	Input	TTL/ CMOS	**Channel B, Enable Comma Detect.**
COMDETB	C4	Output	TTL/ CMOS	**Channel B, Byte-Aligned Comma.**
EWRAPB	F2	Input	TTL/ CMOS	**Channel B, Loopback at Serial I/O.**
LCKREFNB	F1	Input	TTL/ CMOS	**Channel B, Lock Receiver to Clock.**
HDINBP, HDINBN	F15, E17	Input	PECL	**Channel B, Differential Serial Inputs.**
HDOUTBP, HDOUTBN	G14, G15	Output	PECL	**Channel B, Differential Serial Outputs.**
LDSTB	G4	Input	TTL/ CMOS	**Channel B, Load TEST[5:1] inputs.**

Input/Output Information (continued)

Table 3c. Pinout—Channel C I/O

Name	Pin	I/O	Level	Description
TXC9 TXC8 TXC7 TXC6 TXC5 TXC4 TXC3 TXC2 TXC1 TXC0	T1 R2 P3 N4 R1 P2 N3 M4 P1 N2	Input	TTL/ CMOS	**Channel C, Transmit Data [9:0].** Parallel input bits [9:0], one 10-bit, 8b/10b encoded data byte, clocked in on the rising edge of TXCLKC. TXC0 is the LSB.
RXC9 RXC8 RXC7 RXC6 RXC5 RXC4 RXC3 RXC2 RXC1 RXC0	P6 R5 U4 T5 R6 U5 T6 R7 P7 U6	Output	TTL/ CMOS	**Channel C, Receive Data [9:0].** Parallel output bits [9:0], one 10-bit data type, clocked-out on the alternate rising edge of RXCLK0C, RXCLK1C. RXC0 is the LSB.
TXCLKC	U2	Input	TTL/ CMOS	**Transmit Clock (100 MHz—125 MHz).** Used to latch TXC[9:0] data into the LU5X34F. Synchronous with REFCLK(N)
RXCLK0C	P5	Output	TTL/ CMOS	**Channel C, Byte-Align Clock 0.**
RXCLK1C	R4	Output	TTL/ CMOS	**Channel C, Byte-Align Clock 1.**
ENCDETC	L1	Input	TTL/ CMOS	**Channel C, Enable-Comma Detect.**
COMDETC	T4	Output	TTL/ CMOS	**Channel C, Byte-Aligned Comma.**
EWRAPC	K3	Input	TTL/ CMOS	**Channel C, Loopback at Serial I/O.**
LCKREFNC	L4	Input	TTL/ CMOS	**Channel C, Lock Receiver to Clock.**
HDINCP, HDINCN	L16, M17	Input	PECL	**Channel C, Differential Serial Inputs.**
HDOUTCP, HDOUTCN	M15, M16	Output	PECL	**Channel C, Differential Serial Outputs.**
LDSTC	L2	Input	TTL/ CMOS	**Channel C, Load Test[5:1] Inputs.**

Input/Output Information (continued)

Table 3d. Pinout—Channel D I/O

Name	Pin	I/O	Level	Description
TXD9 TXD8 TXD7 TXD6 TXD5 TXD4 TXD3 TXD2 TXD1 TXD0	R10 T10 U10 R10 U9 T9 U8 T8 U7 R8	Input	TTL/ CMOS	**Channel D, Transmit Data [9:0].** Parallel input bits [9:0], one 10-bit, 8b/10b encoded data byte, clocked-in on the rising edge of TXCLKD. TXD0 is the LSB.
RXD9 RXD8 RXD7 RXD6 RXD5 RXD4 RXD3 RXD2 RXD1 RXD0	R12 T13 U14 P12 R13 T14 U15 P13 R14 T15	Output	TTL/ CMOS	**Channel D, Receive Data [9:0].** Parallel output bits [9:0], one 10-bit data type, clocked-out on the alternate rising edge of RXCLK0D, RXCLK1D. RXD0 is the LSB.
TXCLKD	T11	Input	TTL/ CMOS	**Transmit Clock (100 MHz—125 MHz).** Used to latch TXD[9:0] data into the LU5X34F. Synchronous with REFCLK(N)
RXCLK0D	U12	Output	TTL/ CMOS	**Channel D, Byte-Align Clock 0.**
RXCLK1D	R11	Output	TTL/ CMOS	**Channel D, Byte-Align Clock 1.**
ENCDETD	M1	Input	TTL/ CMOS	**Channel D, Enable Comma Detect.**
COMDETD	U13	Output	TTL/ CMOS	**Channel D, Byte-Aligned Comma.**
EWRAPD	L3	Input	TTL/ CMOS	**Channel D, Loopback at Serial I/O.**
LCKREFND	N1	Input	TTL/ CMOS	**Channel D, Lock Receiver to Clock.**
HDINDP, HDINDN	N15, P16	Input	PECL	**Channel D, Differential Serial Inputs.**
HDOUTDP, HDOUTDN	R16, P15	Output	PECL	**Channel D, Differential Serial Outputs.**
LDSTD	M2	Input	TTL/ CMOS	**Channel D, Load Test[5:1] Inputs.**

Input/Output Information (continued)

Table 3e. Pinout—Common I/O

Name	Pin	I/O	Level	Description
OLREF	K16	Input/ Output	Analog	**PECL Level Set Resistor Terminal 1.**
OLRVS	K17	Input/ Output	Analog	**PECL Level Set Resistor Terminal 2.**
LPWR	J3	Input	TTL/ CMOS	**Device Low-Power Mode.**
RESETN	G2	Input	TTL/ CMOS	**Device Reset (Active-Low).**
TEST5*	J2	Input/ Output	TTL/ CMOS	**Global Test Control Input/Output.**
TEST4*	H1	Input	TTL/ CMOS	**Local Test Control Input.**
TEST3*	H2	Input	TTL/ CMOS	**Local Test Control Input.**
TEST2*	G1	Input	TTL/ CMOS	**Local Test Control Input.**
TEST1*	H3	Input	TTL/ CMOS	**Local Test Control Input.**
BYPPLL	J1	Input	TTL/ CMOS	**Test Control, PLL Bypass Mode.**
REFCLK, REFCLKN	K1, K2	Input	PECL or TTL/ CMOS	**Reference Clock Input (100 MHz—125 MHz).** Used by the transmitter PLL to generate the 1.0 Gbits/s— 1.25 Gbits/s serial data; has a $\pm$100 ppm tolerance requirement.

* For related information, see Table 18, Test Modes.

Table 3f. Pinout—Power I/O

Name	Pin	Description
V_{DD}	D5, D8, D10, B13, H4, K4, P8, P10	**Device Digital Power.**
$V_{DD}P$	G17, H16	**PLL Power.**
$V_{DD}T_X$	D16, D17, F17, G16, L15, N16, N14, T17,	**High-Speed Analog Transmitter Power.**
$V_{DD}R$	H14, K14	**High-Speed Analog Receiver Power.**
V_{SS}	B2, C3, D4, D9, H8, H9, H10, J4, J8, J9, J10, K8, K9, K10, P4, P9, P14, R3, R15, T2, T16	**Device Digital Ground.**
$V_{SS}P$	H15, H17	**PLL Ground.**
$V_{SS}T$	B16, C15, D14, J14	**High-Speed Analog Transmitter Ground.**
$V_{SS}R_X$	C16, C17, E16, F16, K15, L14, P17, R17	**High-Speed Analog Receiver Ground.**

Electrical Specifications

Transmitter

Table 4. Reference Clock Specifications (REFCLK and REFCLKN)

Parameter	Min	Max	Unit
Frequency Range	100	125	MHz
Frequency Tolerance	–100	100	ppm
Duty Cycle*	40	60	%
Rise Time (PECL)	—	0.8	ns
Fall Time (PECL)	—	0.8	ns
Rise Time (TTL/CMOS)	—	1.5	ns
Fall Time (TTL/CMOS)	—	1.5	ns
In-band Jitter, 1 Gbit/s—1.25 Gbits/s	—	30	ps_{p-p}
Out-of-Band Jitter	—	50	ps_{p-p}

* Measured at 50% amplitude point.

Table 5. PLL Specifications

Parameter	Min	Typ	Max	Unit
Bandwidth	—	1.5	—	MHz
Jitter Peaking	—	0.5	—	dB
Lock Time	—	—	230	µs

Table 6. Output Jitter at 1.0 Gbit/s—1.25 Gbits/s Data Rate

Parameter	Min	Max	Unit
Deterministic	—	0.08	UI_{p-p}
Random	—	0.12	UI_{p-p}
Total	—	0.2	UI_{p-p}

Receiver

Table 7. Input Data Rate

Parameter	Min	Max	Unit
Frequency Range	1.0	1.25	Gbits/s
Frequency Tolerance with REFCLK	–100	100	ppm

Table 8. Data Lock Characteristics

Parameter	Min	Typ	Max	Unit
Bandwidth*	0.3†	—	1*	MHz
Jitter Peaking*	—	0.5	—	dB
Lock Time*	—	—	2	µs

* Data pattern: 101010 . . . .
† Data pattern: 1111100000 . . . .

Electrical Specifications (continued)

Receiver (continued)

Table 9. Power Dissipation *

Parameter	Min	Typ	Max	Unit
Power	—	—	2.0	W
Package Thermal Resistance	TBD	—	TBD	°C/W
Sleep Mode (LPWR)	—	TBD	—	mW

* Depending on application (PCB layout), etc.

Table 10. dc Electrical Specifications*

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Supply Voltage	V_{DD}, $V_{DD}P$	—	3.135	3.3	3.465	V
Output Low	V_{OL}	—	0	—	0.6	V
Output High	V_{OH}	—	2.4	—	V_{DD}	V
Input Low	V_{IL}	—	0	—	0.8	V
Input High	V_{IH}	—	2.0	—	V_{DD}	V
Diff. PECL Output		Load, as in Figure 9.	800	—	—	mV
Diff. PECL Input		Source configuration, as in Figure 9.	400	—	1600	mV

* Depending on application (PCB layout), etc.

Table 11. Absolute Maximum Ratings

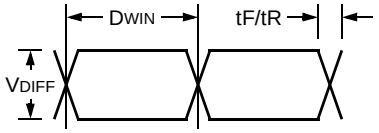
Parameter	Min	Typ	Max	Unit
Supply Voltage	3.135	3.3	3.465	V
TTL High Input Voltage	3.0	—	3.6	V
PECL Output Current	—	—	16	mA
Junction Operating Temperature	0	—	125	°C
Storage Temperature	–65	—	150	°C

Timing Characteristics

Serial Timing

Table 12. Serial Output Timing Levels

Description	Min	Typ	Max	Unit
Rise Time 20%—80%	0.17	0.2	0.22	ns
Fall Time 80%—20%	0.17	0.2	0.22	ns
Common Mode	$V_{DD}/2 - 0.1$	$V_{DD}/2$	$V_{DD}/2 + 0.1$	V
Differential Swing	0.8	—	1.6	V_{p-p}
Load (See Table 16)	50	—	75	Ω



5-8813(F)

Figure 4. Serial Interface Timing

Table 13. Serial Input Interface Timing

Description	Min	Max	Unit
Rise Time (tR)	150	225	ps
Fall Time (tF)	150	225	ps
Differential Swing (V_{DIFF})	0.4	1.6	mV_{p-p}
Source Impedance	50	75	Ω
Data Eye Opening	320	—	ps

Timing Characteristics (continued)

Receiver Section Timing

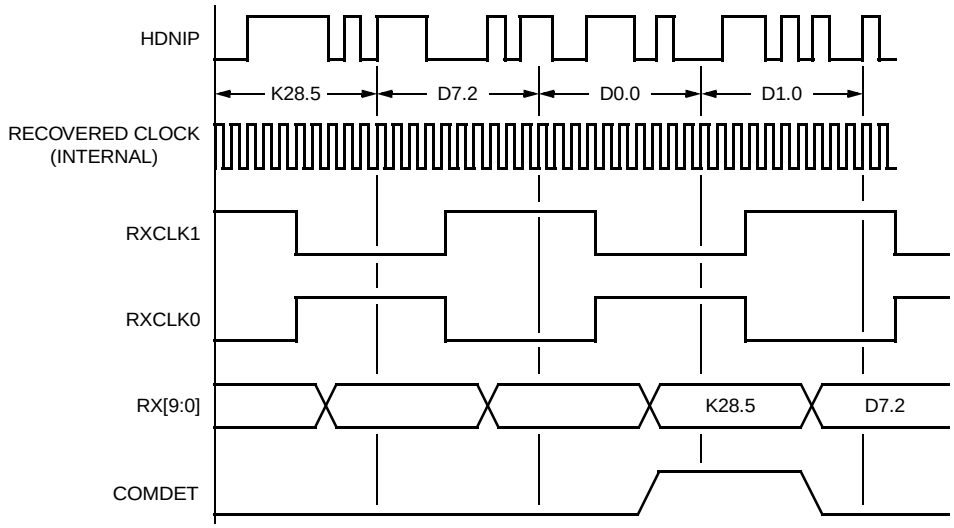
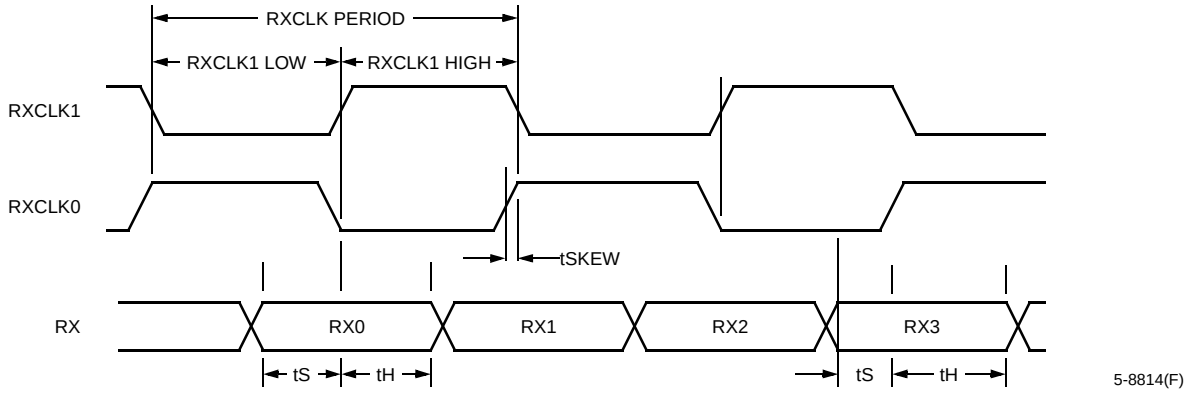


Figure 5. Receiver Section Timing

5-8813 (F)

Receiver Port Timing



5-8814(F)

Figure 6. Receiver Port Timing

Table 14. Receiver Parallel Port Timing

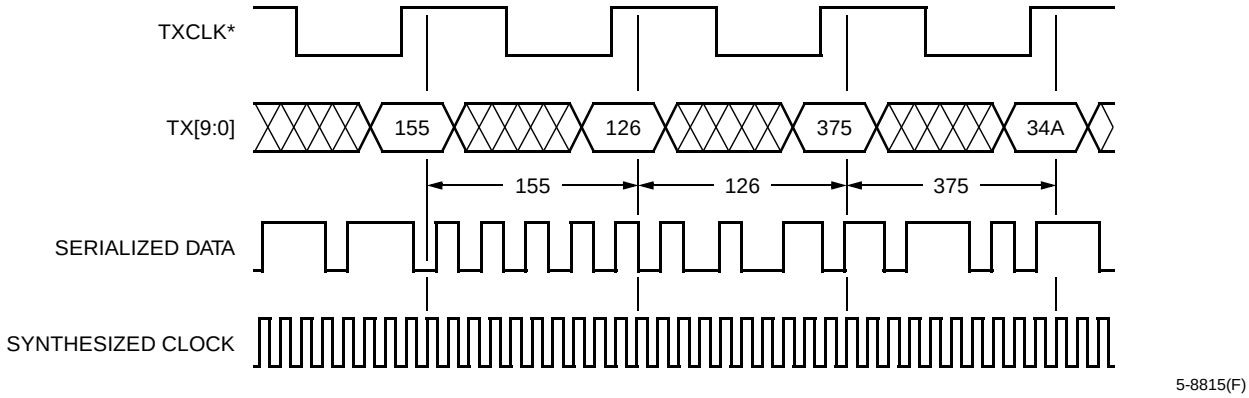
Symbol	Parameter	Min	Max	Units
—	RXCLK[1:0] Frequency*	—	62.5	MHz
—	RXCLK[1:0] Low	7.0	9.0	ns
—	RXCLK[1:0] High	7.0	9.0	ns
tR/F	RXCLK[1:0] (0.4 V to 2.6 V)†	0.2	0.5	ns
tR/F	Data Output (0.4 V to 2.6 V)†	0.2	0.5	ns
tS	Setup Time	3.0	—	ns
tH	Hold Time	2.0	—	ns
tSKEW	Skew	—	1.0	ns

* 1.25 Gbits/s.

† 0.5 pF load.

Timing Characteristics (continued)

Transmitter Section Timing



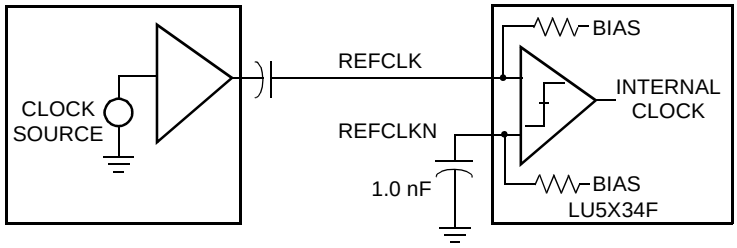
* Synchronous with REFCLK(N).

Figure 7. Parallel Interface Transmit Timing

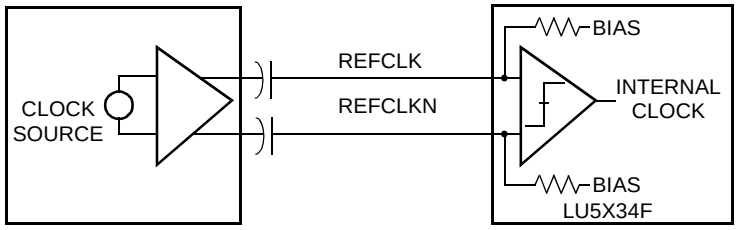
Table 15. Transmitter Timing at Parallel Interface

Description	Min	Max	Unit	Conditions
Data Setup	2	—	ns	With positive edge TXCLK
Data Hold	2	—	ns	With positive edge TXCLK
Rise Time	—	1	ns	—
Fall Time	—	1	ns	—

Application Section



SINGLE-ENDED CLOCK SOURCE

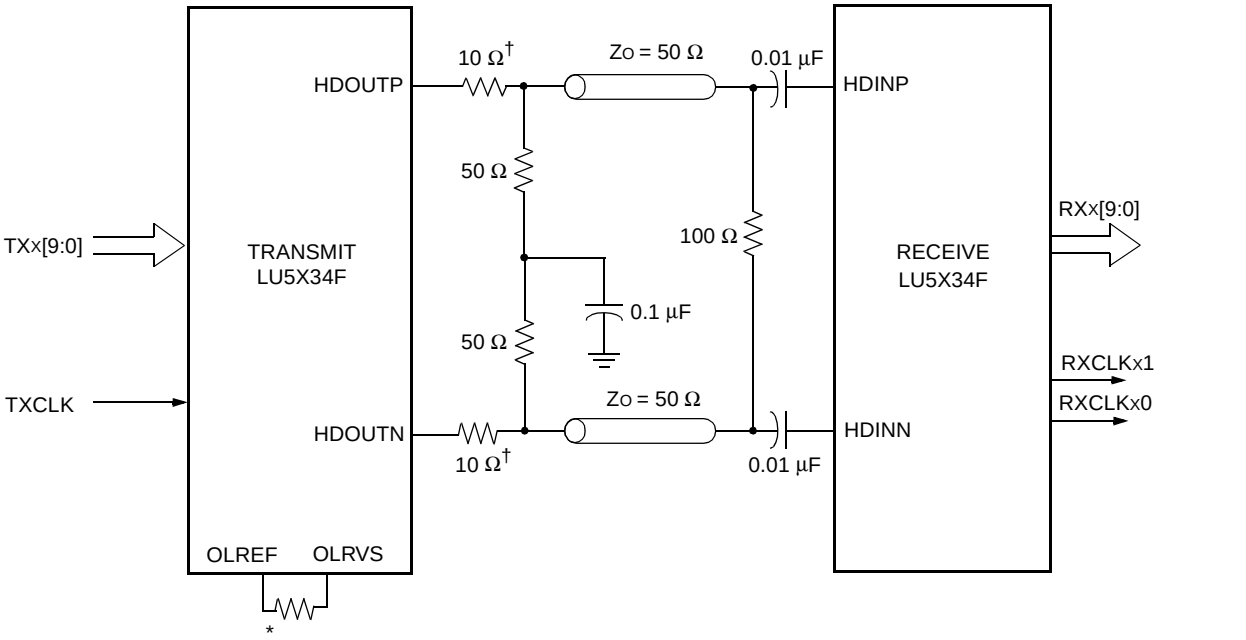


DIFFERENTIAL CLOCK SOURCE

5-8013(F)

Figure 8. Reference Clock Connections with Single-Ended and Differential Sources

Application Section (continued)



5-8811(F).c

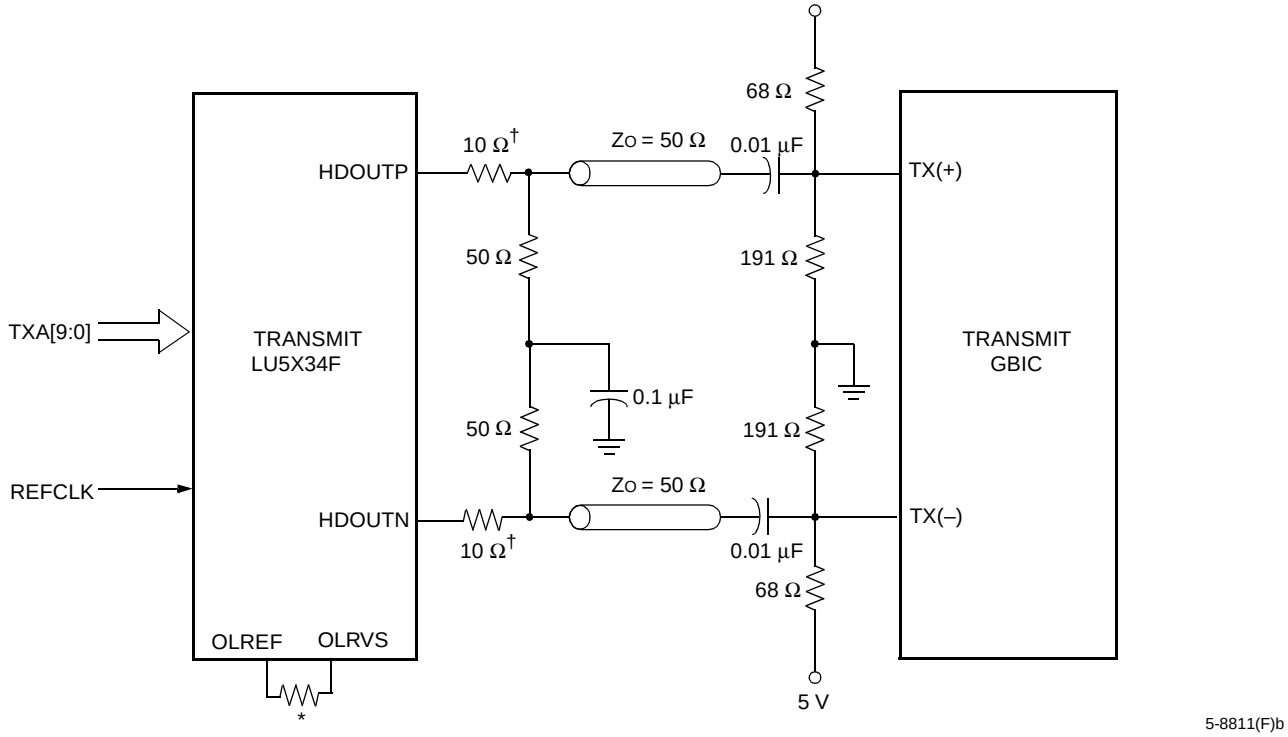
* External resistor connected between OLREF and OLRVS. See Table 16 for external resistor value.
† Damping resistor, maximum = 10 Ω.

Figure 9. Typical Termination for a Single-Channel, High-Speed Serial Transmit-and-Receive Port in a 50 Ω Backplane Application

Table 16. External Resistor Value vs. Differential Output Level Viewing

Resistor Value (Ω)	Termination Impedance (Ω)	Differential Output Voltage (V)
7.5 k/11.25 k	50/75	0.8
5 k/7.5 k		1.2
4 k/6 k		1.6

Application Section (continued)



* External resistor connected between OLREF and OLRVS. See Table 17 for resistor value vs. termination impedance and output swing.
† Damping resistor, maximum = 10 Ω.

Figure 10. Typical Termination for a Single-Channel, High-Speed Serial Transmit Port Interfacing a 5 V GBIC Transceiver

Table 17. External Resistor Value vs. Differential Output Level Viewing

Resistor Value (Ω)	**Termination Impedance** (Ω)	**Differential Output Voltage** (V)
7.5 k/11.25 k	50/75	0.8
5 k/7.5 k		1.2
4 k/6 k		1.6

Test Modes

Note: Test modes are intended for manufacture test only and are not guaranteed to be operational. They may be modified or eliminated without prior notice.

The device has per-channel test modes as well as global test modes. The bypass PLL, BYPPLL, is a global test input because it modifies the operation of the analog PLL. Test bits TEST[4:1] generally operate in the localized mode. The LDST[A:D] inputs are enable signals that permit the TEST[4:1] signals to be injected into a particular channel.

For example, if LDSTA = 1, the TEST[4:1] signals directly control the test modes in the A channel. Once LDSTA = 0, the previous values of TEST[4:1] are held for the A channel. The TEST[4:1] signals control the four channels (A, B, C, D) via level sense latches that are gated with the LDST[A:D] inputs. TEST[5] is a global test pin used for both injection of signals as well as for monitoring points within the device.

Table 18. Test Modes

Global	Local Test Configuration				Global	Operation
BYPPLL	TEST1	TEST2	TEST3	TEST4	TEST5	
0	1	1	1	1	X	Normal operation.
0	1	1	1	0	Output	Analog PLL feedback signal viewed at TEST5 pin.
0	1	1	0	1	X	Transceiver operates normally except RX[9:0] output is from digital filter, not the serial data.
0	1	1	0	0	Output	Transceiver operates normally except RX[9:0] output is from digital filter and the analog PLL feedback signal is viewed at TEST5 pin.
0	1	0	1	P	P	Digital filter forced to count. Pulses applied at TEST4 increment accumulator; pulses at TEST5 decrement accumulator.
0	1	0	0	P	P	RX[9:0] output is from digital filter, not the serial data. Digital filter forced to count. Pulses applied at TEST4 increment accumulator; pulses at TEST5 decrement accumulator.
0	0	1	1	1	X	Parallel loopback. TX[9:0] = RX[9:0]. RX[9:0] remains active.
0	0	1	1	0	Output	Parallel loopback. TX[9:0] = RX[9:0] and analog PLL feedback signal viewed at TEST5 pin. RX[9:0] remains active.
0	0	1	0	1	X	RX[9:0] output is from digital filter, not the serial data. Receive channel is held in reset. BYPPLL overrides this reset.
0	0	1	0	0	Output	RX[9:0] output is from digital filter, not the serial data. Receive channel is held in reset. BYPPLL overrides this reset. Analog PLL feedback signal viewed at TEST5 pin

Test Modes (continued)

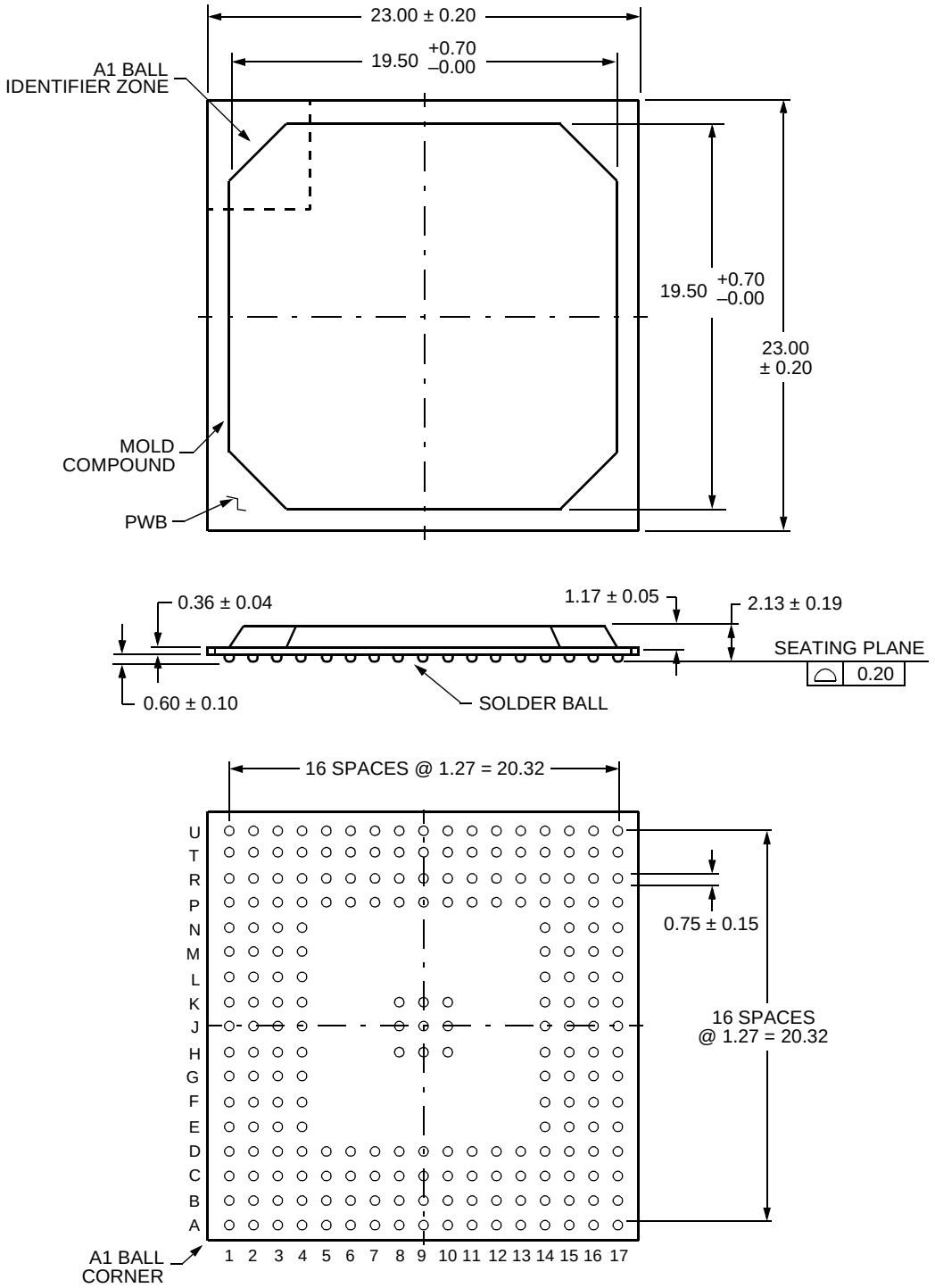
Table 18. Test Modes (continued)

Global	Local Test Configuration				Global	OPERATION
BYPPLL	TEST1	TEST2	TEST3	TEST4	TEST5	
0	0	0	1	0	Output	Transmitter is held in reset. BYPPLL overrides this reset. Analog PLL feedback signal viewed at TEST5 pin.
0	0	0	0	1	X	Transmitter and receiver are held in reset. RX[9:0] output is from digital filter, not the serial data.
0	0	0	0	0	Output	Transmitter and receiver are held in reset. RX[9:0] output is from digital filter, not the serial data. Analog PLL feedback signal viewed at TEST5 pin.
1	X	X	1	C-0	C-90	Analog PLL is bypassed for low speed functional test. A low-speed clock is input to TEST4, and a quadrature clock is applied to TEST5. Frequency of clocks is 5X REFCLK, but here REFCLK is lowered to about 1 MHz.
1	X	X	0	C-0	C-90	Analog PLL is bypassed for low-speed functional test. A low-speed clock is input to TEST4, and a quadrature clock is applied to TEST5. Frequency of clocks is 5X REFCLK, but here REFCLK is lowered to about 1 MHz. RX[9:0] output is from digital filter, not the serial data.

Outline Diagram

217-pin PBGA

Dimensions are in millimeters.



5-6562 (F)

Ordering Information

Device Code	Comcode	Package	Temperature
LU5X34F	108497850	217-pin PBGA	0 °C—70 °C

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