



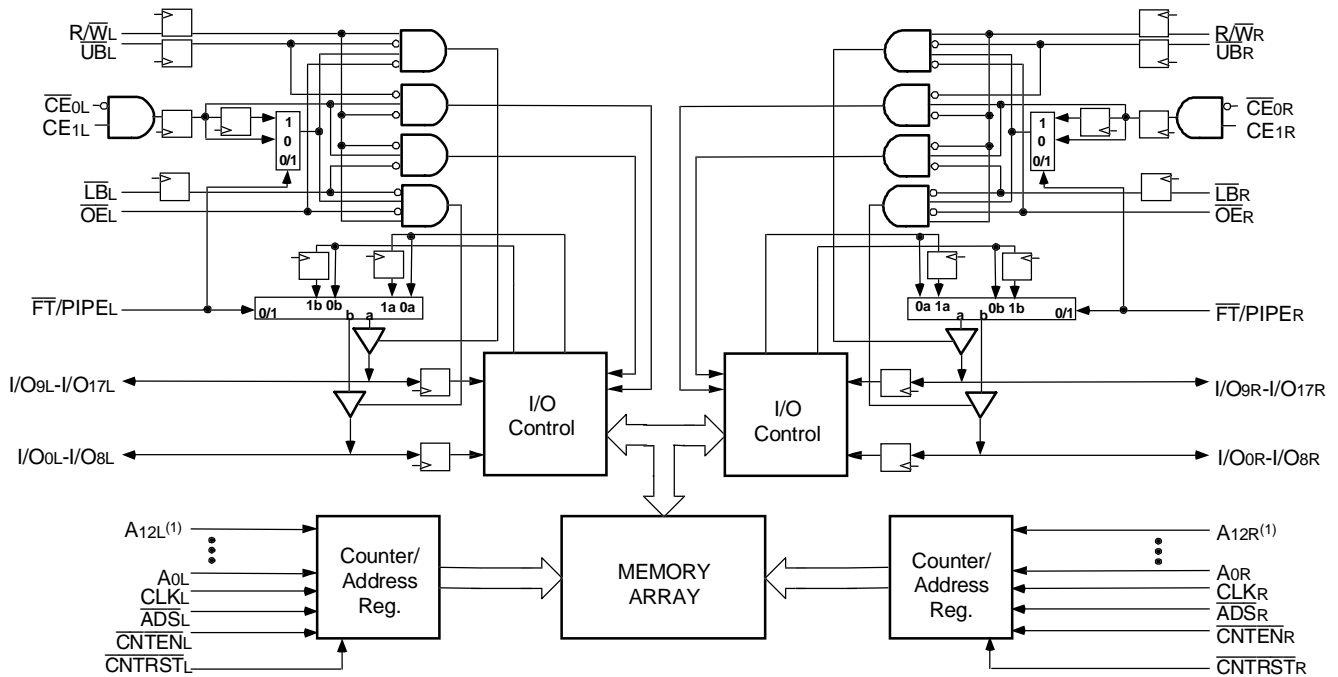
# HIGH-SPEED 2.5V 8/4K x 18 SYNCHRONOUS PIPELINED DUAL-PORT STATIC RAM

**PRELIMINARY  
IDT70T9359/49L**

## Features:

- ◆ True Dual-Ported memory cells which allow simultaneous access of the same memory location
- ◆ High-speed clock to data access
  - Commercial: 7.5/9/12ns (max.)
  - Industrial: 9ns (max.)
- ◆ Low-power operation
  - IDT70T9359/49L
  - Active: 225mW (typ.)
  - Standby: 1.5mW (typ.)
- ◆ Flow-Through or Pipelined output mode on either port via the  $\overline{\text{FT}}/\text{PIPE}$  pins
- ◆ Counter enable and reset features
- ◆ Dual chip enables allow for depth expansion without additional logic
- ◆ Full synchronous operation on both ports
  - 4.0ns setup to clock and 0.5ns hold on all control, data, and address inputs
  - Data input, address, and control registers
  - Fast 7.5ns clock to data out in the Pipelined output mode
  - Self-timed write allows fast cycle time
  - 12ns cycle time, 83MHz operation in Pipelined output mode
- ◆ Separate upper-byte and lower-byte controls for multiplexed bus and bus matching compatibility
- ◆ LVTTTL-compatible, single 2.5V ( $\pm 100\text{mV}$ ) power supply
- ◆ Industrial temperature range ( $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ ) is available for 66MHz
- ◆ Available in a 100-pin Thin Quad Flatpack (TQFP) and 100-pin fine pitch Ball Grid Array (fpBGA) packages.

## Functional Block Diagram



5640 drw 01

### NOTE:

1. A12 is a NC for IDT70T9349.

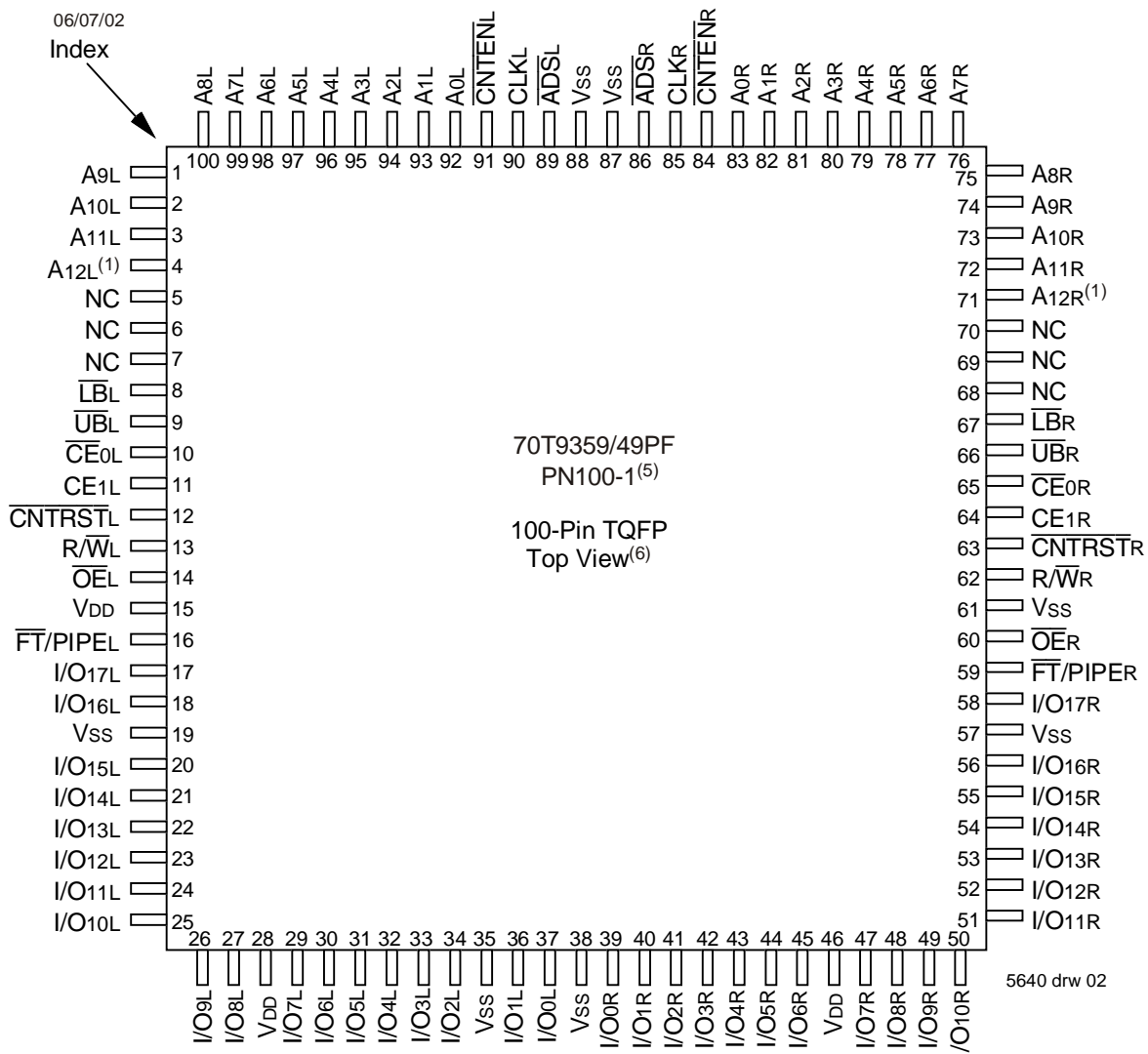
**JULY 2002**

## Description:

The IDT70T9359/49 is a high-speed 8/4K x 18 bit synchronous Dual-Port RAM. The memory array utilizes Dual-Port memory cells to allow simultaneous access of any address from both ports. Registers on control, data, and address inputs provide minimal setup and hold times. The timing latitude provided by this approach allows systems to be designed with very short cycle times.

With an input data register, the IDT70T9359/49 has been optimized for applications having unidirectional or bidirectional data flow in bursts. An automatic power down feature, controlled by  $\overline{CE_0}$  and  $CE_1$ , permits the on-chip circuitry of each port to enter a very low standby power mode. Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 225mW of power.

## Pin Configurations (1,2,3,4)



### NOTES:

1. A12 is a NC for IDT70T9349.
2. All V<sub>DD</sub> pins must be connected to power supply.
3. All V<sub>SS</sub> pins must be connected to ground supply.
4. Package body is approximately 14mm x 14mm x 1.4mm.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

## Pin Configurations (con't.)(1,2,3,4)

70T9359/49BF  
BF100<sup>(5)</sup>

100-Pin fpBGA  
Top View<sup>(6)</sup>

06/07/02

A1 A8R	A2 A11R	A3 $\overline{UBR}$	A4 $\overline{CNTRSTR}$	A5 Vss	A6 Vss	A7 Vss	A8 I/O13R	A9 I/O10R	A10 I/O17R
B1 A6R	B2 A7R	B3 A10R	B4 A12R <sup>(1)</sup>	B5 R/ $\overline{WR}$	B6 $\overline{OER}$	B7 PL/ $\overline{FTR}$	B8 I/O12R	B9 I/O9R	B10 I/O6R
C1 A3R	C2 A4R	C3 A5R	C4 A9R	C5 CE1R	C6 I/O16R	C7 I/O15R	C8 I/O11R	C9 I/O7R	C10 I/O3R
D1 A0R	D2 CLKR	D3 A1R	D4 A2R	D5 $\overline{LBR}$	D6 $\overline{CE0R}$	D7 I/O14R	D8 I/O8R	D9 I/O5R	D10 I/O1R
E1 Vss	E2 $\overline{ADS_R}$	E3 $\overline{CNTEN_R}$	E4 A1L	E5 $\overline{ADS_L}$	E6 Vss	E7 I/O4R	E8 I/O2R	E9 I/O0R	E10 VDD
F1 Vss	F2 CLKL	F3 A0L	F4 A3L	F5 VDD	F6 Vss	F7 VDD	F8 I/O2L	F9 I/O1L	F10 I/O0L
G1 $\overline{CNTEN_L}$	G2 A4L	G3 A7L	G4 $\overline{UBL}$	G5 Vss	G6 I/O13L	G7 NC	G8 I/O4L	G9 Vss	G10 I/O3L
H1 A2L	H2 A6L	H3 A11L	H4 $\overline{CE0L}$	H5 $\overline{CNTRST_L}$	H6 I/O15L	H7 I/O9L	H8 I/O7L	H9 I/O6L	H10 I/O5L
J1 A5L	J2 A9L	J3 A12L <sup>(1)</sup>	J4 R/ $\overline{WL}$	J5 $\overline{OEL}$	J6 PL/ $\overline{FTL}$	J7 I/O12L	J8 I/O10L	J9 Vss	J10 I/O8L
K1 A8L	K2 A10L	K3 $\overline{LBL}$	K4 CE1L	K5 VDD	K6 VDD	K7 I/O16L	K8 I/O14L	K9 I/O11L	K10 I/O17L

5640 drw 03

### NOTES:

1. A12 is a NC for IDT70T9349.
2. All VDD pins must be connected to power supply.
3. All Vss pins must be connected to ground supply.
4. Package body is approximately 10mm x 10mm x 1.4mm with 0.8mm ball pitch.
5. This package code is used to reference the package diagram.
6. This text does not indicate orientation of the actual part-marking.

## Pin Names

Left Port	Right Port	Names
$\overline{CE}_{0L}$ , CE1L	$\overline{CE}_{0R}$ , CE1R	Chip Enables <sup>(3)</sup>
R/ $\overline{WL}$	R/ $\overline{WR}$	Read/Write Enable
$\overline{OE}_L$	$\overline{OE}_R$	Output Enable
A0L - A12L <sup>(1)</sup>	A0R - A12R <sup>(1)</sup>	Address
I/O0L - I/O17L	I/O0R - I/O17R	Data Input/Output
CLKL	CLKR	Clock
$\overline{UB}_L$	$\overline{UB}_R$	Upper Byte Select <sup>(2)</sup>
$\overline{LB}_L$	$\overline{LB}_R$	Lower Byte Select <sup>(2)</sup>
$\overline{ADS}_L$	$\overline{ADS}_R$	Address Strobe Enable
$\overline{CNTEN}_L$	$\overline{CNTEN}_R$	Counter Enable
$\overline{CNRST}_L$	$\overline{CNRST}_R$	Counter Reset
$\overline{FT}/PIPE_L$	$\overline{FT}/PIPE_R$	Flow-Through / Pipeline
V <sub>DD</sub>		Power (2.5V)
V <sub>SS</sub>		Ground (0V)

5640 tbl 01

### NOTES:

1. A<sub>12</sub> is a NC for IDT70T9349.
2.  $\overline{LB}$  and  $\overline{UB}$  are single buffered regardless of state of  $\overline{FT}/PIPE$ .
3.  $\overline{CE}_0$  and CE<sub>1</sub> are single buffered when  $\overline{FT}/PIPE = V_{IL}$ ,  $\overline{CE}_0$  and CE<sub>1</sub> are double buffered when  $\overline{FT}/PIPE = V_{IH}$ , i.e. the signals take two cycles to deselect.

## Truth Table I—Read/Write and Enable Control<sup>(1,2,3)</sup>

$\overline{OE}$	CLK	$\overline{CE}_0$ <sup>(5)</sup>	CE <sub>1</sub> <sup>(5)</sup>	$\overline{UB}$ <sup>(4)</sup>	$\overline{LB}$ <sup>(4)</sup>	R/ $\overline{W}$	Upper Byte I/O <sub>9-17</sub>	Lower Byte I/O <sub>0-8</sub>	MODE
X	↑	H	X	X	X	X	High-Z	High-Z	Deselected—Power Down
X	↑	X	L	X	X	X	High-Z	High-Z	Deselected—Power Down
X	↑	L	H	H	H	X	High-Z	High-Z	Both Bytes Deselected
X	↑	L	H	L	H	L	DATA <sub>IN</sub>	High-Z	Write to Upper Byte Only
X	↑	L	H	H	L	L	High-Z	DATA <sub>IN</sub>	Write to Lower Byte Only
X	↑	L	H	L	L	L	DATA <sub>IN</sub>	DATA <sub>IN</sub>	Write to Both Bytes
L	↑	L	H	L	H	H	DATA <sub>OUT</sub>	High-Z	Read Upper Byte Only
L	↑	L	H	H	L	H	High-Z	DATA <sub>OUT</sub>	Read Lower Byte Only
L	↑	L	H	L	L	H	DATA <sub>OUT</sub>	DATA <sub>OUT</sub>	Read Both Bytes
H	X	L	H	X	X	X	High-Z	High-Z	Outputs Disabled

5640 tbl 02

### NOTES:

1. "H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>, "X" = Don't Care.
2.  $\overline{ADS}$ ,  $\overline{CNTEN}$ ,  $\overline{CNRST}$  = X.
3.  $\overline{OE}$  is an asynchronous input signal.
4.  $\overline{LB}$  and  $\overline{UB}$  are single buffered regardless of state of  $\overline{FT}/PIPE$ .
5.  $\overline{CE}_0$  and CE<sub>1</sub> are single buffered when  $\overline{FT}/PIPE = V_{IL}$ .  $\overline{CE}_0$  and CE<sub>1</sub> are double buffered when  $\overline{FT}/PIPE = V_{IH}$ , i.e. the signals take two cycles to deselect.

**Truth Table II—Address Counter Control<sup>(1,2)</sup>**

External Address	Previous Internal Address	Internal Address Used	CLK	$\overline{ADS}$	$\overline{CNTEN}$	$\overline{CNTRST}$	I/O <sup>(3)</sup>	MODE
An	X	An	↑	L <sup>(4)</sup>	X	H	Dvo (n)	External Address Used
X	An	An + 1	↑	H	L <sup>(5)</sup>	H	Dvo(n+1)	Counter Enabled—Internal Address generation
X	An + 1	An + 1	↑	H	H	H	Dvo(n+1)	External Address Blocked—Counter disabled (An + 1 reused)
X	X	A0	↑	X	X	L <sup>(4)</sup>	Dvo(0)	Counter Reset to Address 0

5640 tbl 03

**NOTES:**

- "H" = V<sub>IH</sub>, "L" = V<sub>IL</sub>, "X" = Don't Care.
- $\overline{CE_0}$ ,  $\overline{LB}$ ,  $\overline{UB}$ , and  $\overline{OE}$  = V<sub>IL</sub>; CE<sub>1</sub> and  $\overline{RW}$  = V<sub>IH</sub>.
- Outputs configured in Flow-Through Output mode: if outputs are in Pipelined mode the data out will be delayed by one cycle.
- $\overline{ADS}$  and  $\overline{CNTRST}$  are independent of all other signals including  $\overline{CE_0}$ , CE<sub>1</sub>,  $\overline{UB}$  and  $\overline{LB}$ .
- The address counter advances if  $\overline{CNTEN}$  = V<sub>IL</sub> on the rising edge of CLK, regardless of all other signals including  $\overline{CE_0}$ , CE<sub>1</sub>,  $\overline{UB}$  and  $\overline{LB}$ .

**Recommended Operating Temperature and Supply Voltage**

Grade	Ambient Temperature <sup>(1)</sup>	GND	V <sub>DD</sub>
Commercial	0°C to +70°C	0V	2.5V ± 100mV
Industrial	-40°C to +85°C	0V	2.5V ± 100mV

5640 tbl 04

**NOTES:**

- This is the parameter T<sub>A</sub>. This is the "instant on" case temperature.

**Recommended DC Operating Conditions**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply Voltage	2.4	2.5	2.6	V
V <sub>SS</sub>	Ground	0	0	0	V
V <sub>IH</sub>	Input High Voltage	1.7	—	V <sub>DD</sub> +0.3V <sup>(2)</sup>	V
V <sub>IL</sub>	Input Low Voltage	-0.3 <sup>(1)</sup>	—	0.7	V

5640 tbl 05

**NOTES:**

- V<sub>IL</sub> ≥ -1.5V for pulse width less than 10 ns.
- V<sub>TERM</sub> must not exceed V<sub>DD</sub> +0.3V.

**Absolute Maximum Ratings<sup>(1)</sup>**

Symbol	Rating	Commercial & Industrial	Unit
V <sub>TERM</sub> <sup>(2)</sup>	Terminal Voltage with Respect to GND	-0.5 to +3.6	V
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	°C
T <sub>STG</sub>	Storage Temperature	-65 to +150	°C
I <sub>OUT</sub>	DC Output Current	50	mA

5640 tbl 06

**NOTES:**

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- V<sub>TERM</sub> must not exceed V<sub>DD</sub> + 0.3V for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of V<sub>TERM</sub> ≥ V<sub>DD</sub> + 0.3V.

**Capacitance<sup>(1)</sup>****(T<sub>A</sub> = +25°C, f = 1.0MHz)**

Symbol	Parameter	Conditions <sup>(2)</sup>	Max.	Unit
C <sub>IN</sub>	Input Capacitance	V <sub>IN</sub> = 3dV	9	pF
C <sub>OUT</sub> <sup>(3)</sup>	Output Capacitance	V <sub>OUT</sub> = 3dV	10	pF

5640 tbl 07

**NOTES:**

- These parameters are determined by device characterization, but are not production tested.
- 3dV references the interpolated capacitance when the input and output switch from 0V to 3V or from 3V to 0V.
- C<sub>OUT</sub> also references C<sub>I/O</sub>.

## DC Electrical Characteristics Over the Operating Temperature and Supply Voltage Range ( $V_{DD} = 2.5V \pm 100mV$ )

Symbol	Parameter	Test Conditions	70T9359/49L		Unit
			Min.	Max.	
I <sub>LI</sub>	Input Leakage Current <sup>(1)</sup>	$V_{DD} = 2.6V, V_{IN} = 0V$ to $V_{DD}$	—	5	μA
I <sub>LO</sub>	Output Leakage Current	$\overline{CE} = V_{IH}$ or $CE1 = V_{IL}, V_{OUT} = 0V$ to $V_{DD}$	—	5	μA
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = +2mA	—	0.4	V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -2mA	2.0	—	V

**NOTE:**

- At  $V_{DD} \leq 2.0V$  input leakages are undefined.

5640 tbl08

## DC Electrical Characteristics Over the Operating Temperature Supply Voltage Range<sup>(3)</sup> ( $V_{DD} = 2.5V \pm 100mV$ )

Symbol	Parameter	Test Condition	Version	70T9359/49L7 Com'l Only		70T9359/49L9 Com'l & Ind		70T9359/49L12 Com'l Only		Unit
				Typ. <sup>(4)</sup>	Max.	Typ. <sup>(4)</sup>	Max.	Typ. <sup>(4)</sup>	Max.	
I <sub>DD</sub>	Dynamic Operating Current (Both Ports Active)	$\overline{CE}_L$ and $\overline{CE}_R = V_{IL}$ , Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L L	80	200	75	175	70	150	mA
			IND L	—	—	75	220	—	—	
I <sub>SB1</sub>	Standby Current (Both Ports - TTL Level Inputs)	$\overline{CE}_L = \overline{CE}_R = V_{IH}$ $f = f_{MAX}^{(1)}$	COM'L L	20	60	20	50	20	40	mA
			IND L	—	—	20	70	—	—	
I <sub>SB2</sub>	Standby Current (One Port - TTL Level Inputs)	$\overline{CE}^*A = V_{IL}$ and $\overline{CE}^*B = V_{IH}^{(5)}$ Active Port Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L L	50	115	47	100	45	85	mA
			IND L	—	—	47	190	—	—	
I <sub>SB3</sub>	Full Standby Current (Both Ports - CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{DD} - 0.2V$ , $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V, f = 0^{(2)}$	COM'L L	0.1	3.0	0.1	3.0	0.1	3.0	mA
			IND L	—	—	0.1	3.0	—	—	
I <sub>SB4</sub>	Full Standby Current (One Port - CMOS Level Inputs)	$\overline{CE}^*A \leq 0.2V$ and $\overline{CE}^*B \geq V_{DD} - 0.2V^{(6)}$ $V_{IN} \geq V_{DD} - 0.2V$ or $V_{IN} \leq 0.2V$ , Active Port, Outputs Disabled, $f = f_{MAX}^{(1)}$	COM'L L	50	115	47	100	45	85	mA
			IND L	—	—	47	190	—	—	

**NOTES:**

- At  $f = f_{MAX}$ , address and control lines (except Output Enable) are cycling at the maximum frequency clock cycle of 1/t<sub>cv</sub>, using "AC TEST CONDITIONS" at input levels of GND to 3V.
- $f = 0$  means no address, clock, or control lines change. Applies only to input at CMOS level standby.
- Port "A" may be either left or right port. Port "B" is the opposite from port "A".
- $V_{DD} = 2.5V, T_A = 25^\circ C$  for Typ, and are not production tested. I<sub>DD DC</sub>(f=0) = 75mA (Typ).
- $\overline{CE}^*X = V_{IL}$  means  $\overline{CE}^*OX = V_{IL}$  and  $CE1X = V_{IH}$   
 $\overline{CE}^*X = V_{IH}$  means  $\overline{CE}^*OX = V_{IH}$  or  $CE1X = V_{IL}$   
 $\overline{CE}^*X \leq 0.2V$  means  $\overline{CE}^*OX \leq 0.2V$  and  $CE1X \geq V_{DD} - 0.2V$   
 $\overline{CE}^*X \geq V_{DD} - 0.2V$  means  $\overline{CE}^*OX \geq V_{DD} - 0.2V$  or  $CE1X \leq 0.2V$   
 "X" represents "L" for left port or "R" for right port.

5640 tbl09

### AC Test Conditions

Input Pulse Levels	GND to 2.5V
Input Rise/Fall Times	2ns Max.
Input Timing Reference Levels	1.25V
Output Reference Levels	1.25V
Output Load	Figure 1 and 2

5640 tbl 10

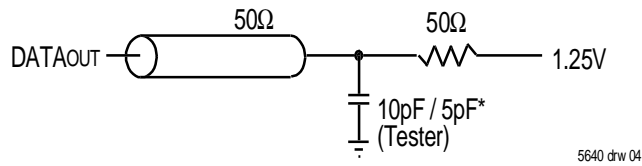


Figure 1. AC Output Test load.  
(For tCKLZ, tCKHZ, tOLZ, and tOHZ).

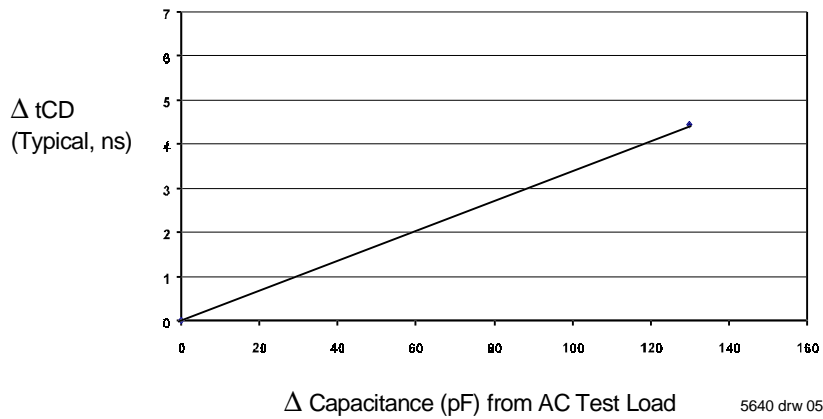


Figure 2. Typical Output Derating (Lumped Capacitive Load).

## AC Electrical Characteristics Over the Operating Temperature Range (Read and Write Cycle Timing)<sup>(3)</sup> ( $V_{DD} = 2.5V \pm 100mV$ , $T_A = 0^\circ C$ to $+70^\circ C$ )

Symbol	Parameter	70T9359/49L7 Com'l Only		70T9359/49L9 Com'l & Ind		70T9359/49L12 Com'l Only		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
t <sub>CYC1</sub>	Clock Cycle Time (Flow-Through) <sup>(2)</sup>	22	—	25	—	30	—	ns
t <sub>CYC2</sub>	Clock Cycle Time (Pipelined) <sup>(2)</sup>	12	—	15	—	20	—	ns
t <sub>CH1</sub>	Clock High Time (Flow-Through) <sup>(2)</sup>	7.5	—	12	—	12	—	ns
t <sub>CL1</sub>	Clock Low Time (Flow-Through) <sup>(2)</sup>	7.5	—	12	—	12	—	ns
t <sub>CH2</sub>	Clock High Time (Pipelined) <sup>(2)</sup>	5	—	6	—	8	—	ns
t <sub>CL2</sub>	Clock Low Time (Pipelined) <sup>(2)</sup>	5	—	6	—	8	—	ns
t <sub>r</sub>	Clock Rise Time	—	3	—	3	—	3	ns
t <sub>f</sub>	Clock Fall Time	—	3	—	3	—	3	ns
t <sub>SA</sub>	Address Setup Time	4	—	4	—	4	—	ns
t <sub>HA</sub>	Address Hold Time	0	—	1	—	1	—	ns
t <sub>SC</sub>	Chip Enable Setup Time	4	—	4	—	4	—	ns
t <sub>HC</sub>	Chip Enable Hold Time	0	—	1	—	1	—	ns
t <sub>SB</sub>	Byte Enable Setup Time	4	—	4	—	4	—	ns
t <sub>HB</sub>	Byte Enable Hold Time	0	—	1	—	1	—	ns
t <sub>SW</sub>	R $\bar{W}$ Setup Time	4	—	4	—	4	—	ns
t <sub>HW</sub>	R $\bar{W}$ Hold Time	0	—	1	—	1	—	ns
t <sub>SD</sub>	Input Data Setup Time	4	—	4	—	4	—	ns
t <sub>HD</sub>	Input Data Hold Time	0	—	1	—	1	—	ns
t <sub>SAD</sub>	$\overline{ADS}$ Setup Time	4	—	4	—	4	—	ns
t <sub>HAD</sub>	$\overline{ADS}$ Hold Time	0	—	1	—	1	—	ns
t <sub>SCN</sub>	$\overline{CNTEN}$ Setup Time	4	—	4	—	4	—	ns
t <sub>HCN</sub>	$\overline{CNTEN}$ Hold Time	0	—	1	—	1	—	ns
t <sub>SRST</sub>	$\overline{CNTRST}$ Setup Time	4	—	4	—	4	—	ns
t <sub>HRST</sub>	$\overline{CNTRST}$ Hold Time	0	—	1	—	1	—	ns
t <sub>OE</sub>	Output Enable to Data Valid	—	7.5	—	9	—	12	ns
t <sub>OLZ</sub>	Output Enable to Output Low-Z <sup>(1)</sup>	2	—	2	—	2	—	ns
t <sub>OHZ</sub>	Output Enable to Output High-Z <sup>(1)</sup>	1	7	1	7	1	7	ns
t <sub>CD1</sub>	Clock to Data Valid (Flow-Through) <sup>(2)</sup>	—	18	—	20	—	25	ns
t <sub>CD2</sub>	Clock to Data Valid (Pipelined) <sup>(2)</sup>	—	7.5	—	9	—	12	ns
t <sub>DC</sub>	Data Output Hold After Clock High	2	—	2	—	2	—	ns
t <sub>CKHZ</sub>	Clock High to Output High-Z <sup>(1)</sup>	2	9	2	9	2	9	ns
t <sub>CKLZ</sub>	Clock High to Output Low-Z <sup>(1)</sup>	2	—	2	—	2	—	ns
<b>Port-to-Port Delay</b>								
t <sub>CWDD</sub>	Write Port Clock High to Read Data Delay	—	28	—	35	—	40	ns
t <sub>CSS</sub>	Clock-to-Clock Setup Time	—	10	—	15	—	15	ns

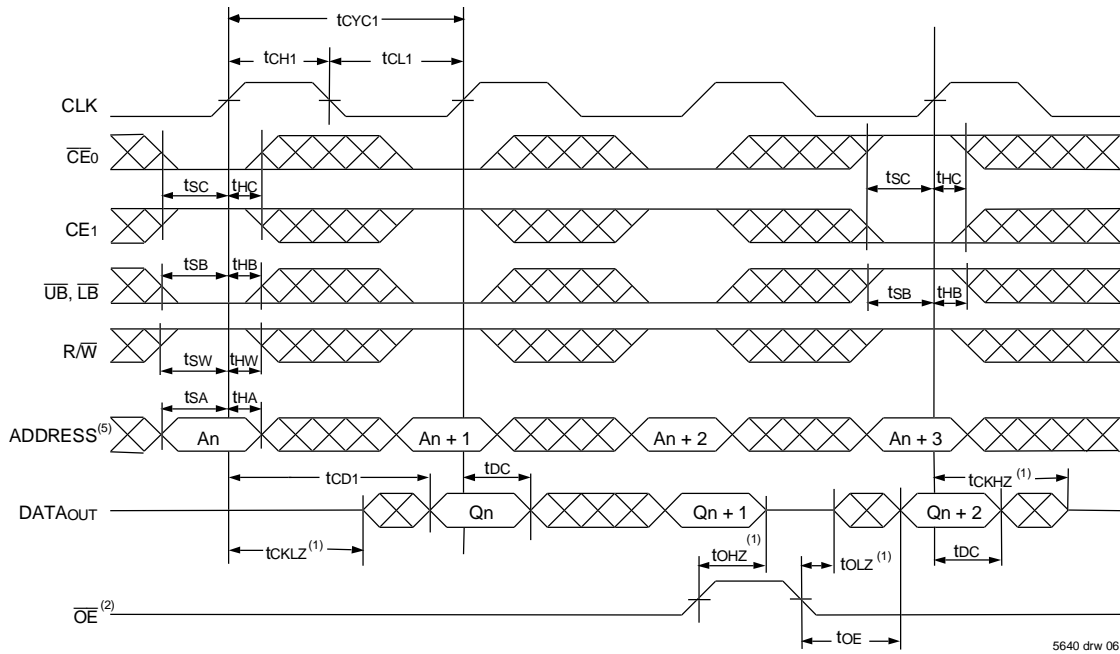
**NOTES:**

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2). This parameter is guaranteed by device characterization, but is not production tested.
2. The Pipelined output parameters (t<sub>CYC2</sub>, t<sub>CD2</sub>) apply to either or both the Left and Right ports when  $\overline{FT}/PIPE = V_{IH}$ . Flow-through parameters (t<sub>CYC1</sub>, t<sub>CD1</sub>) apply when  $\overline{FT}/PIPE = V_{IL}$  for that port.
3. All input signals are synchronous with respect to the clock except for the asynchronous Output Enable ( $\overline{OE}$ ),  $\overline{FT}/PIPE_R$ , and  $\overline{FT}/PIPE_L$ .

5640 tbl 11

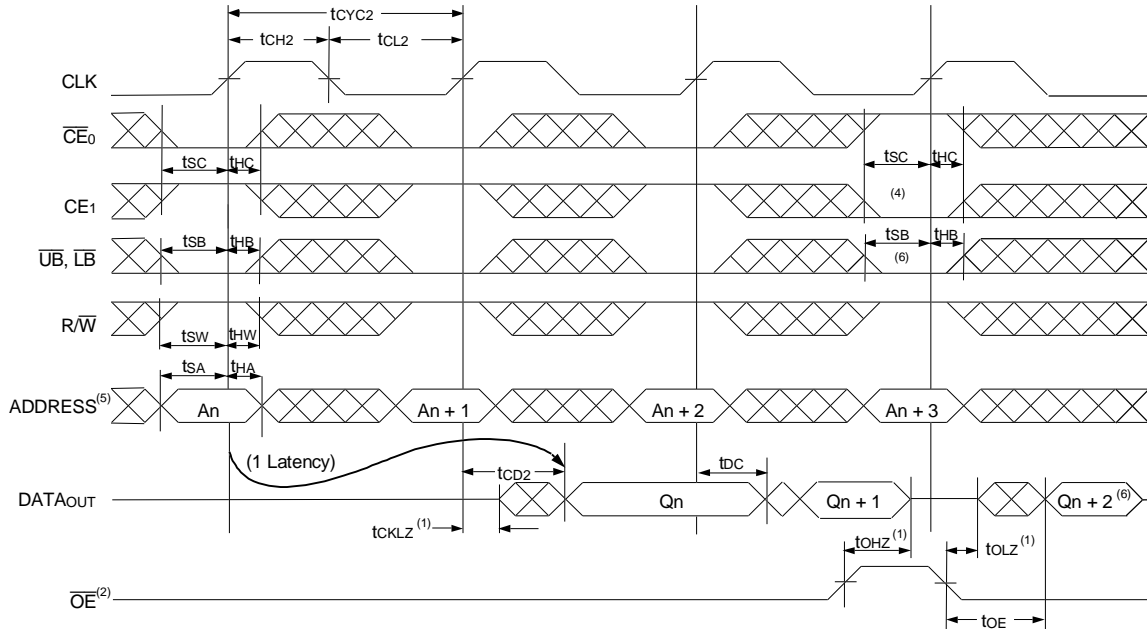


### Timing Waveform of Read Cycle for Flow-Through Output ( $\overline{FT}/PIPE^*X = V_{IL}$ )(3,7)



5640 drw 06

### Timing Waveform of Read Cycle for Pipelined Operation ( $\overline{FT}/PIPE^*X = V_{IH}$ )(3,7)

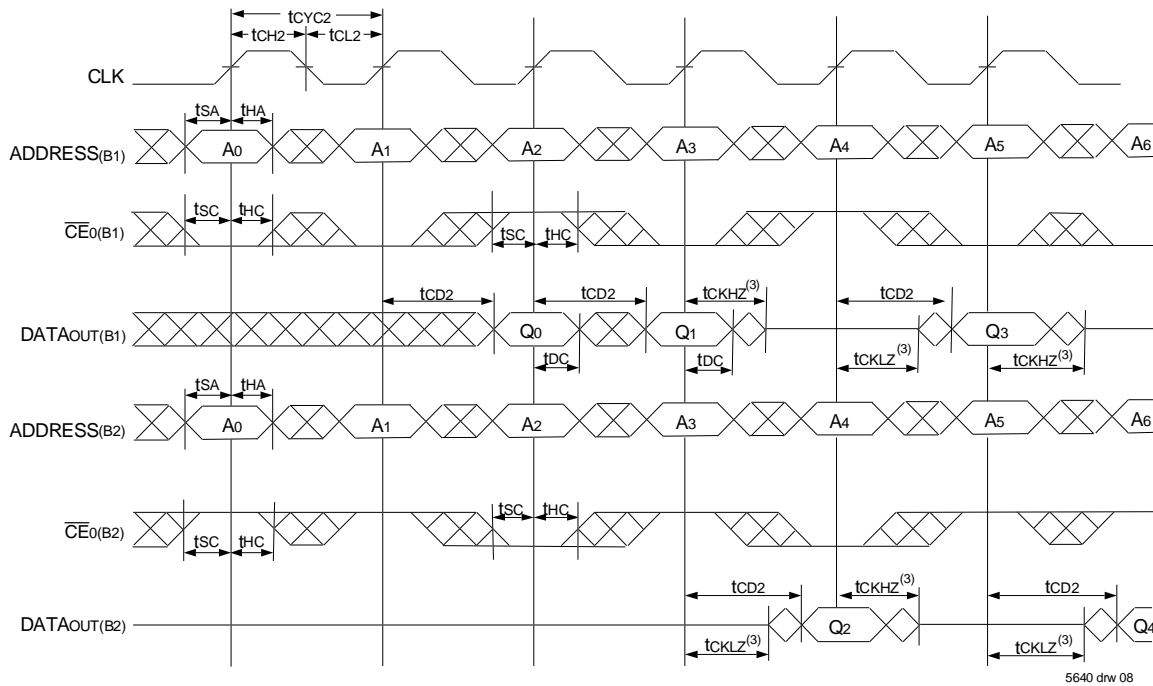


5640 drw 07

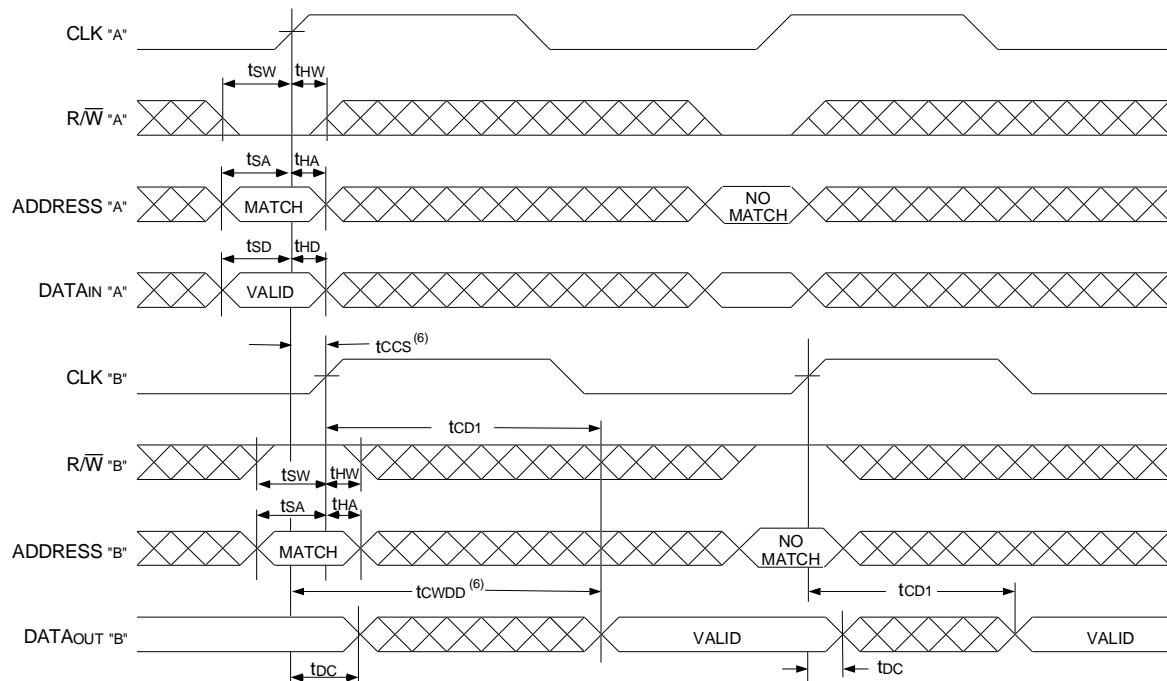
**NOTES:**

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2.  $\overline{OE}$  is asynchronously controlled; all other inputs are synchronous to the rising clock edge.
3.  $\overline{ADS} = V_{IL}$ ,  $\overline{CNTEN}$  and  $\overline{CNRST} = V_{IH}$ .
4. The output is disabled (High-Impedance state) by  $\overline{CE0} = V_{IH}$ ,  $CE1 = V_{IL}$  following the next rising edge of the clock. Refer to Truth Table 1.
5. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
6. If  $\overline{UB}$  or  $\overline{LB}$  was HIGH, then the Upper Byte and/or Lower Byte of  $DATA_{OUT}$  for  $Q_{n+2}$  would be disabled (High-Impedance state).
7. \*X here denotes Left or Right port. The diagram is with respect to that port.

## Timing Waveform of a Bank Select Pipelined Read<sup>(1,2)</sup>



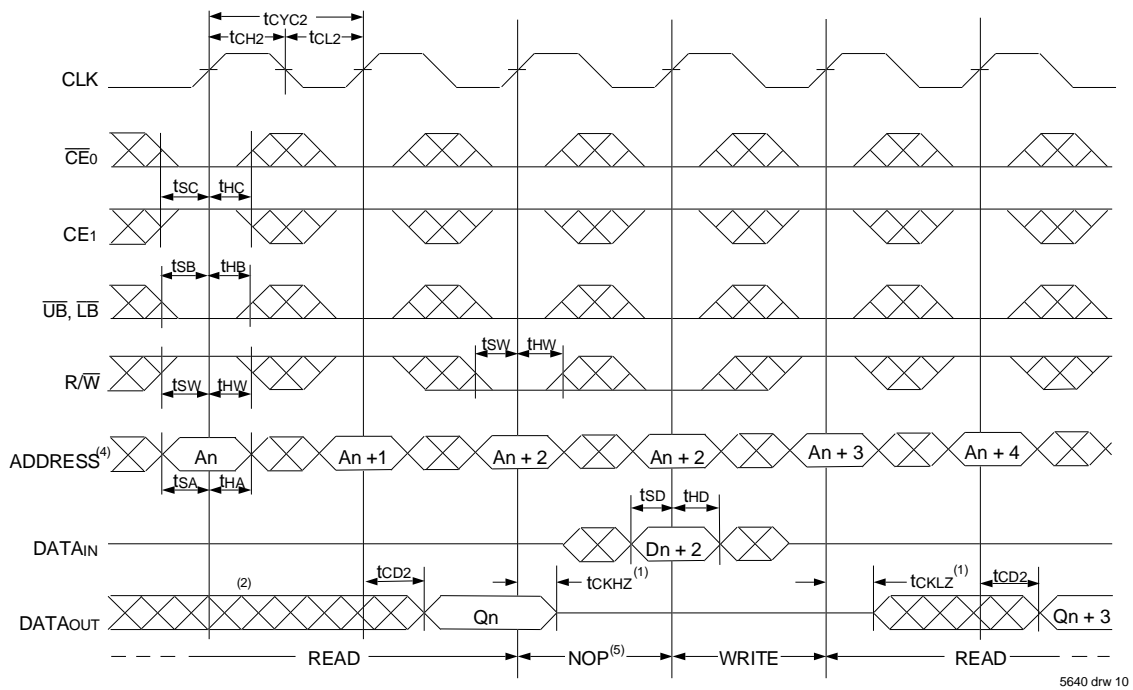
## Timing Waveform with Port-to-Port Flow-Through Read<sup>(4,5,7)</sup>



### NOTES:

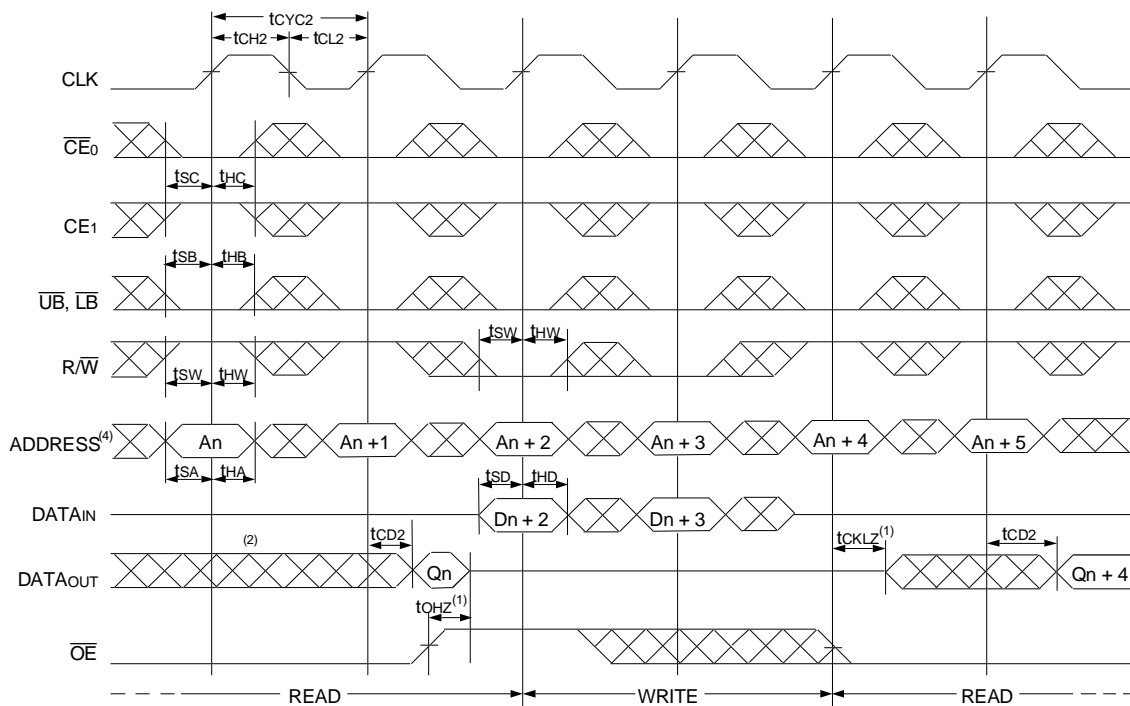
1. B1 Represents Bank #1; B2 Represents Bank #2. Each Bank consists of one IDT70T9359/49 for this waveform, and are setup for depth expansion in this example. ADDRESS<sub>(B1)</sub> = ADDRESS<sub>(B2)</sub> in this situation.
2.  $\overline{UB}$ ,  $\overline{LB}$ ,  $\overline{OE}$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_{1(B1)}$ ,  $CE_{1(B2)}$ ,  $R/\overline{W}$ ,  $\overline{CNTEN}$ , and  $\overline{CNTRST} = V_{IH}$ .
3. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
4.  $\overline{CE}_0$ ,  $\overline{UB}$ ,  $\overline{LB}$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_1$ ,  $\overline{CNTEN}$ , and  $\overline{CNTRST} = V_{IH}$ .
5.  $\overline{OE} = V_{IL}$  for the Right Port, which is being read from.  $\overline{OE} = V_{IH}$  for the Left Port, which is being written to.
6. If  $t_{CCS} \leq$  maximum specified, then data from right port READ is not valid until the maximum specified for  $t_{CWD}$ . If  $t_{CCS} >$  maximum specified, then data from right port READ is not valid until  $t_{CCS} + t_{CD1}$ .  $t_{CWD}$  does not apply in this case.
7. All timing is the same for both Left and Right ports. Port "A" may be either Left or Right port. Port "B" is the opposite from Port "A".

### Timing Waveform of Pipelined Read-to-Write-to-Read ( $\overline{OE} = V_{IL}$ )<sup>(3)</sup>



5640 drw 10

### Timing Waveform of Pipelined Read-to-Write-to-Read ( $\overline{OE}$ Controlled)<sup>(3)</sup>

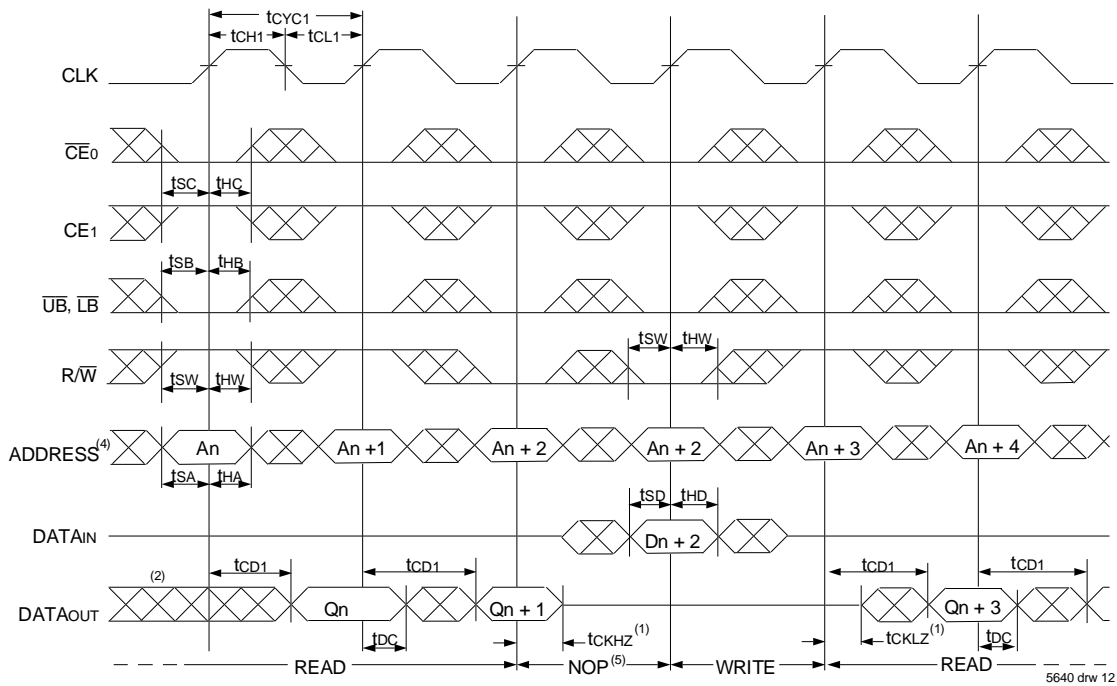


5640 drw 11

**NOTES:**

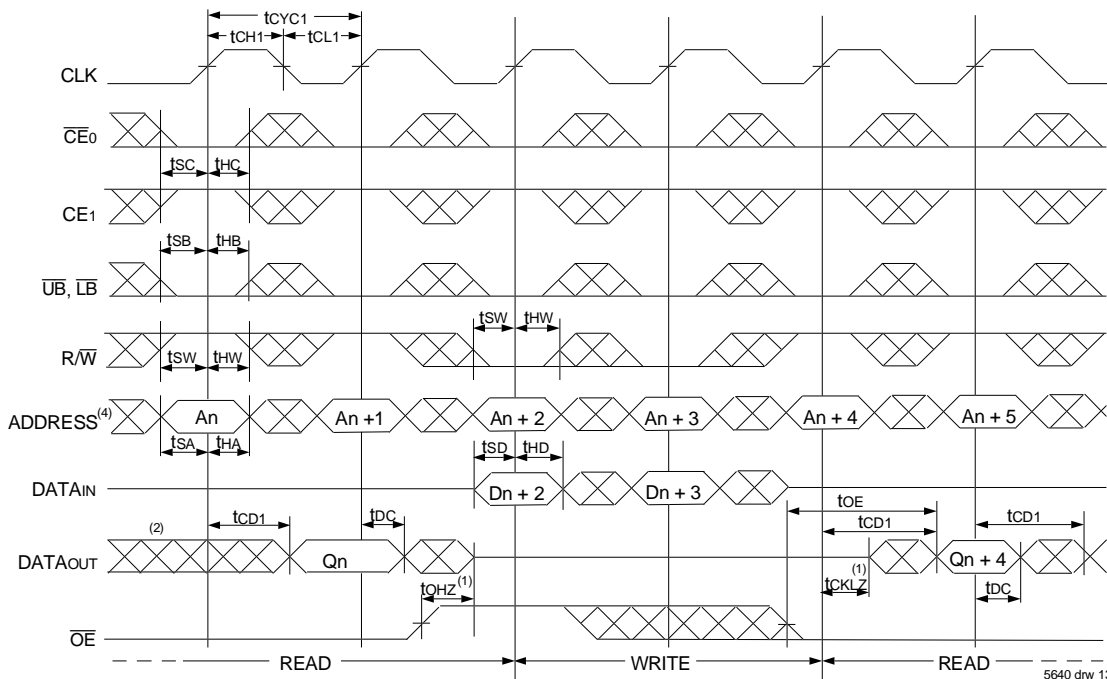
1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3.  $\overline{CE}_0$ ,  $\overline{UB}$ ,  $\overline{LB}$ , and  $\overline{ADS} = V_{IL}$ ;  $CE_1$ ,  $\overline{CNTEN}$ , and  $\overline{CNTRST} = V_{IH}$ . "NOP" is "No Operation".
4. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

### Timing Waveform of Flow-Through Read-to-Write-to-Read ( $\overline{OE} = V_{IL}$ )<sup>(3)</sup>



5640 drw 12

### Timing Waveform of Flow-Through Read-to-Write-to-Read ( $\overline{OE}$ Controlled)<sup>(3)</sup>

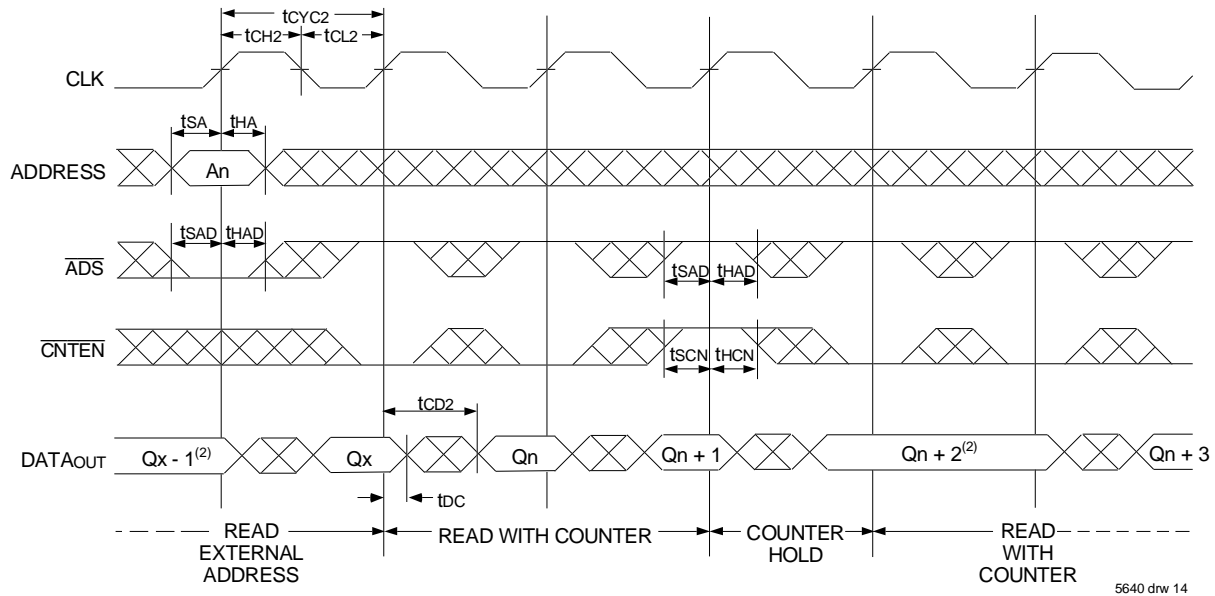


5640 drw 13

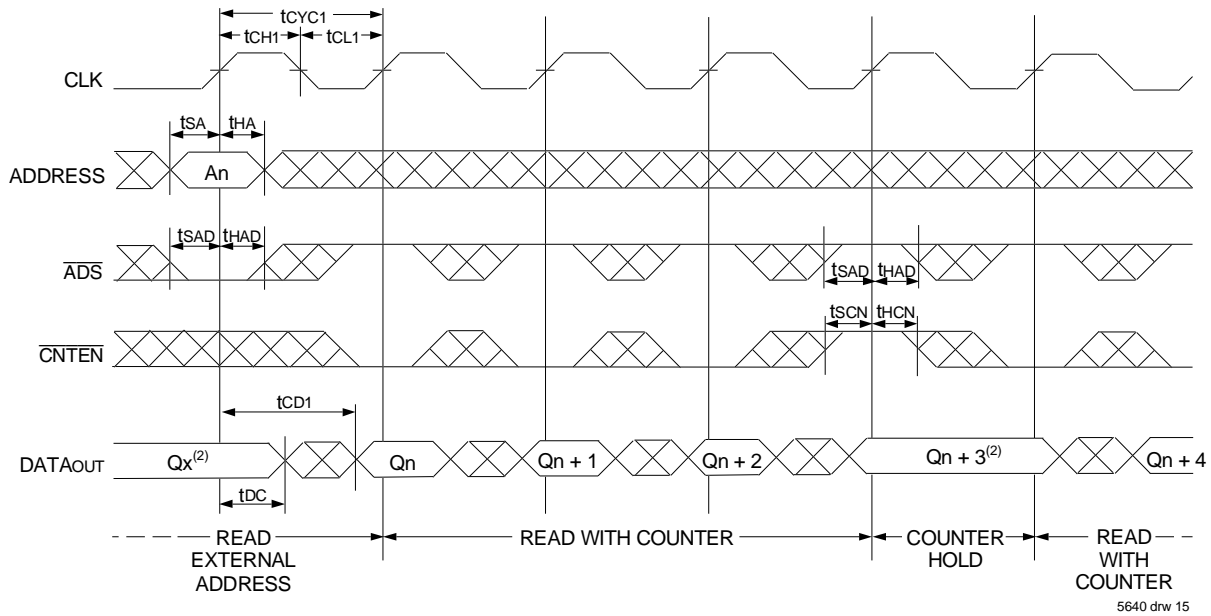
**NOTES:**

1. Transition is measured 0mV from Low or High-impedance voltage with the Output Test Load (Figure 2).
2. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
3.  $\overline{CE0}$ ,  $\overline{UB}$ ,  $\overline{LB}$ , and  $\overline{ADS} = V_{IL}$ ;  $\overline{CE1}$ ,  $\overline{CNTEN}$ , and  $\overline{CNTRST} = V_{IH}$ . "NOP" is "No Operation".
4. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. "NOP" is "No Operation." Data in memory at the selected address may be corrupted and should be re-written to guarantee data integrity.

### Timing Waveform of Pipelined Read with Address Counter Advance<sup>(1)</sup>



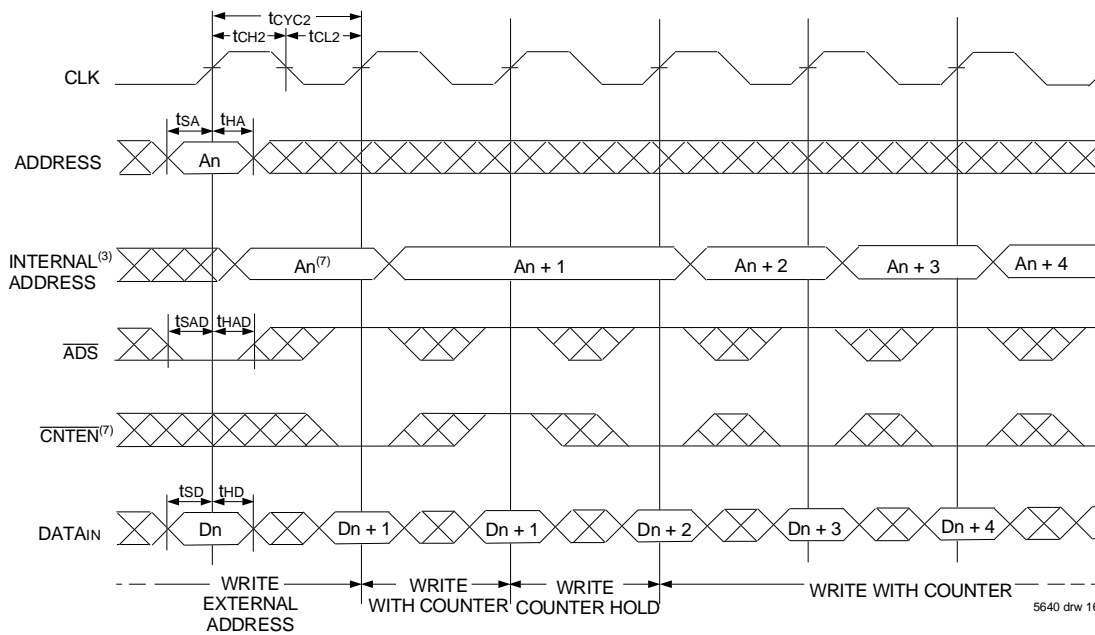
### Timing Waveform of Flow-Through Read with Address Counter Advance<sup>(1)</sup>



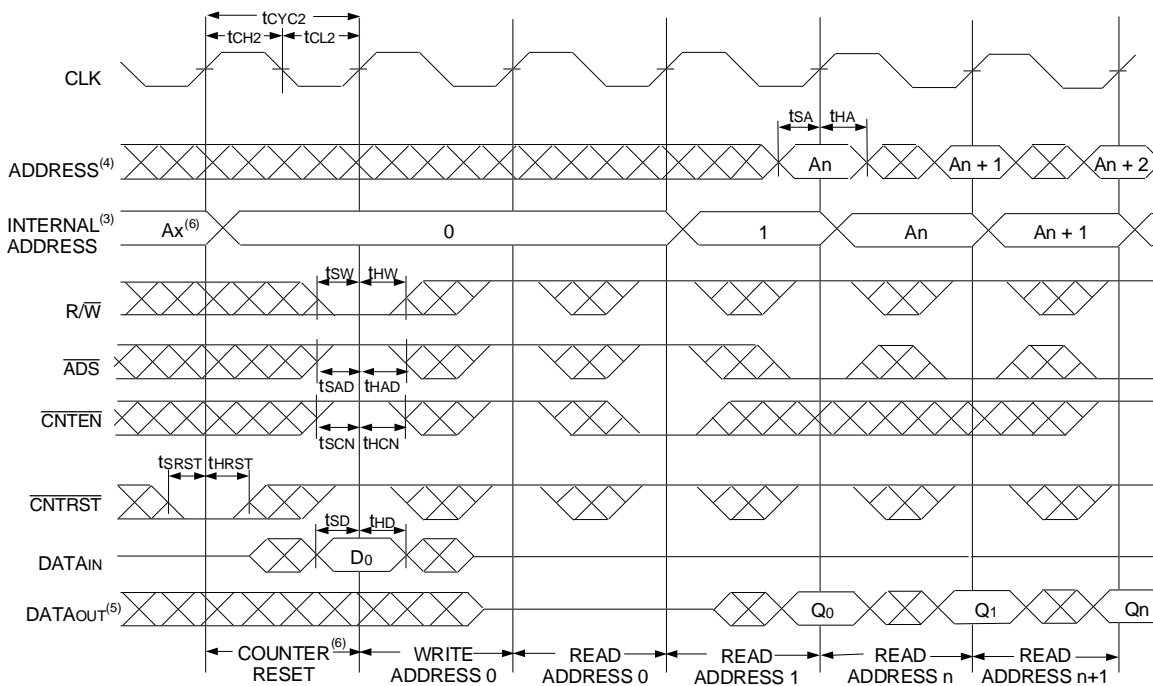
**NOTES:**

1.  $\overline{CE}_0$ ,  $\overline{OE}$ ,  $\overline{UB}$ , and  $\overline{LB} = V_{IL}$ ;  $CE_1$ ,  $R\overline{W}$ , and  $\overline{CNRST} = V_{IH}$ .
2. If there is no address change via  $ADS = V_{IL}$  (loading a new address) or  $\overline{CNTEN} = V_{IL}$  (advancing the address), i.e.  $\overline{ADS} = V_{IH}$  and  $\overline{CNTEN} = V_{IH}$ , then the data output remains constant for subsequent clocks.

## Timing Waveform of Write with Address Counter Advance (Flow-Through or Pipelined Outputs)<sup>(1)</sup>



## Timing Waveform of Counter Reset (Pipelined Outputs)<sup>(2)</sup>



**NOTES:**

1.  $\overline{CE}_0$ ,  $\overline{UB}$ ,  $\overline{LB}$ , and  $R/\overline{W}$  =  $V_{IL}$ ;  $CE_1$  and  $\overline{CNTRST}$  =  $V_{IH}$ .
2.  $\overline{CE}_0$ ,  $\overline{UB}$ ,  $\overline{LB}$  =  $V_{IL}$ ;  $CE_1$  =  $V_{IH}$ .
3. The "Internal Address" is equal to the "External Address" when  $\overline{ADS} = V_{IL}$  and equals the counter output when  $\overline{ADS} = V_{IH}$ .
4. Addresses do not have to be accessed sequentially since  $\overline{ADS} = V_{IL}$  constantly loads the address on the rising edge of the CLK; numbers are for reference use only.
5. Output state (High, Low, or High-impedance) is determined by the previous cycle control signals.
6. No dead cycle exists during counter reset. A READ or WRITE cycle may be coincidental with the counter reset cycle.  $ADDR_0$  will be accessed. Extra cycles are shown here simply for clarification.
7.  $\overline{CNTEN} = V_{IL}$  advances Internal Address from 'An' to 'An + 1'. The transition shown indicates the time required for the counter to advance. The 'An + 1' Address is written to during this cycle.

## Functional Description

The IDT70T9359/49 provides a true synchronous Dual-Port Static RAM interface. Registered inputs provide minimal set-up and hold times on address, data, and all critical control inputs. All internal registers are clocked on the rising edge of the clock signal, however, the self-timed internal write pulse is independent of the LOW to HIGH transition of the clock signal.

An asynchronous output enable is provided to ease asynchronous bus interfacing. Counter enable inputs are also provided to stall the operation of the address counters for fast interleaved memory applications.

$\overline{CE}_0 = V_{IL}$  and  $CE_1 = V_{IH}$  for one clock cycle will power down the internal circuitry to reduce static power consumption. Multiple chip enables allow easier banking of multiple IDT70T9359/49's for depth expansion configurations. When the Pipelined output mode is enabled, two cycles are required with  $\overline{CE}_0 = V_{IL}$  and  $CE_1 = V_{IH}$  to re-activate the outputs.

## Depth and Width Expansion

The IDT70T9359/49 features dual chip enables (refer to Truth Table I) in order to facilitate rapid and simple depth expansion with no requirements for external logic. Figure 4 illustrates how to control the various chip enables in order to expand two devices in depth.

The IDT70T9359/49 can also be used in applications requiring expanded width, as indicated in Figure 4. Since the banks are allocated at the discretion of the user, the external controller can be set up to drive the input signals for the various devices as required to allow for 36-bit or wider applications.

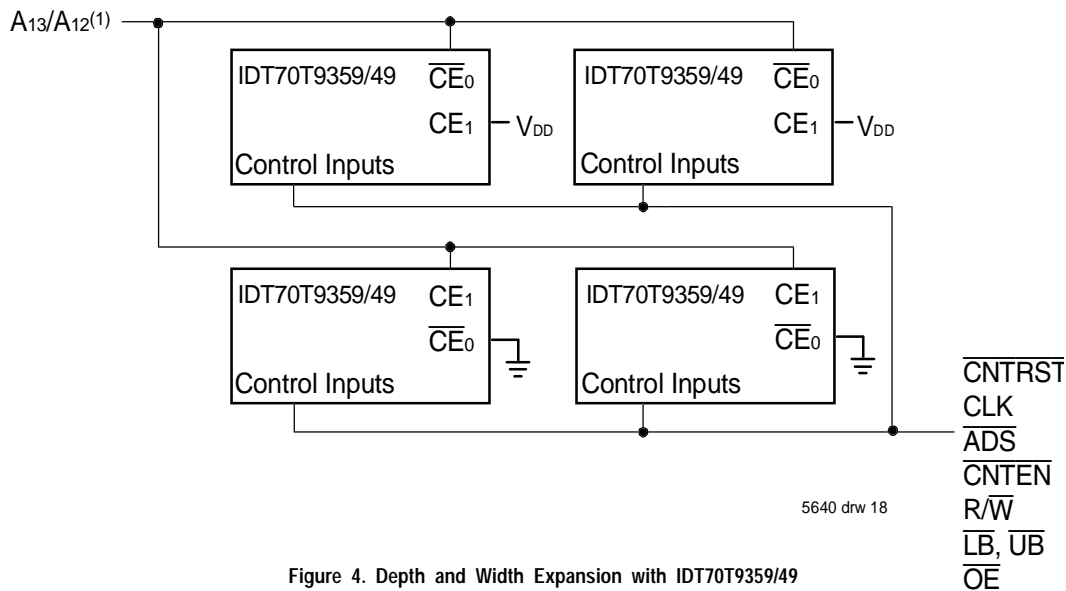
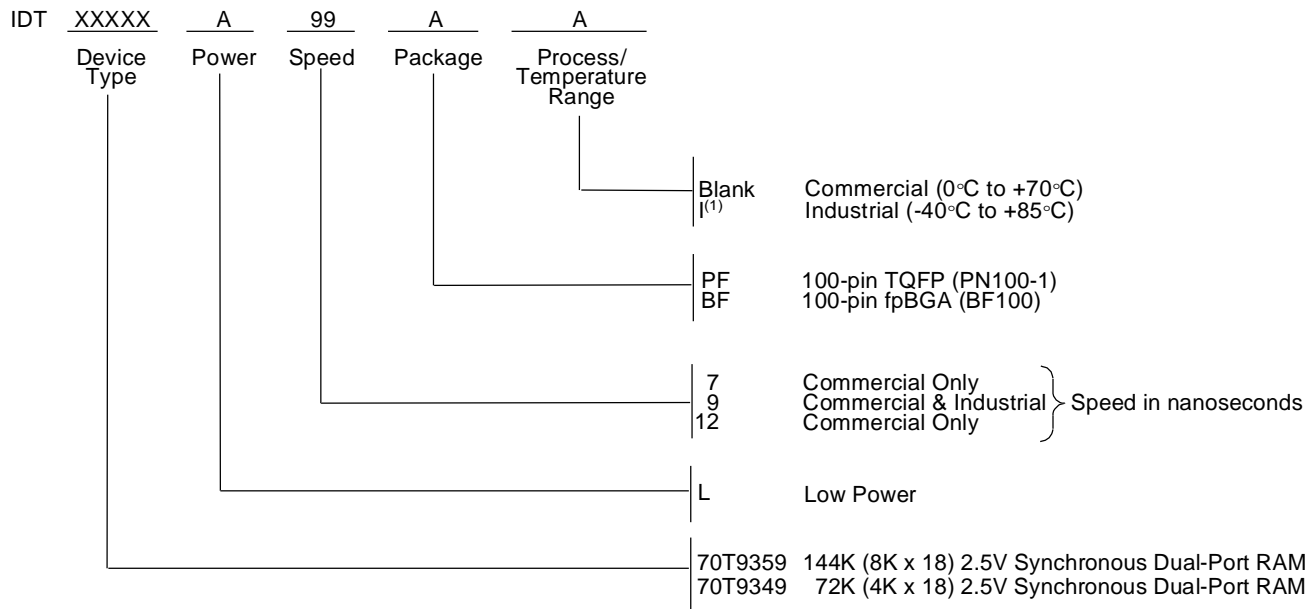


Figure 4. Depth and Width Expansion with IDT70T9359/49

**NOTE:**

1. A13 is for IDT70T9359, A12 is for IDT70T9349.

## Ordering Information



5640 drw 19

**NOTE:**

1. Contact your local sales office for Industrial temp range for other speeds, packages and powers.

## Datasheet Document History

07/08/02: Initial Public Release



**CORPORATE HEADQUARTERS**  
 2975 Stender Way  
 Santa Clara, CA 95054

**for SALES:**  
 800-345-7015 or 408-727-6116  
 fax: 408-492-8674  
 www.idt.com

**for Tech Support:**  
 831-754-4613  
 DualPortHelp@idt.com

The IDT logo is a registered trademark of Integrated Device Technology, Inc.