Dual Fractional-N / Integer-N Frequency Synthesizer

■ Features

- Fully standard CMOS dual frequency synthesizer
  2.5 GHz Fractional-N / 1.0 GHz Integer-N
- 2.7V to 3.6V operation
- Very low current consumption (@ V_{DD} = 3.0V, typ)
  HM6F5201 : 7 mA (for PCS)
- Dual-modulus low prescaler value
  RF prescaler 8/9 or 12/13 for Fractional-N
  IF prescaler 8/9 for Integer-N
- Digital fractional spurious compensation
  Fractional spurious reduction (< 80 dBc)
- Low noise & spur selection
- Fast channel switching time
  < 500 us (@ CDMA)
- Selectable power-save mode(H/W & S/W)
- Selectable charge pump current levels
- Saperate supply for V_{DD} and V_{DDCP}
- Low voltage 3 wire interface (2.0V ~ up to Vcc)
- ESD protection content with JEDEC standard
- Small 24 pin LGA (Leadless Grid Array) package

■ Applications

- Cordless telephone systems
- Portable wireless communications (PDAs)
- Handsets and base stations for mobile communications
  GSM, DCS, PCS, CDMA, WCDMA,
  Dual Mode telephone system
- TDMA systems
- Cable TV tuners(CATV)
- Other wireless communication systems
- Fine frequency resolution application

■ General Description

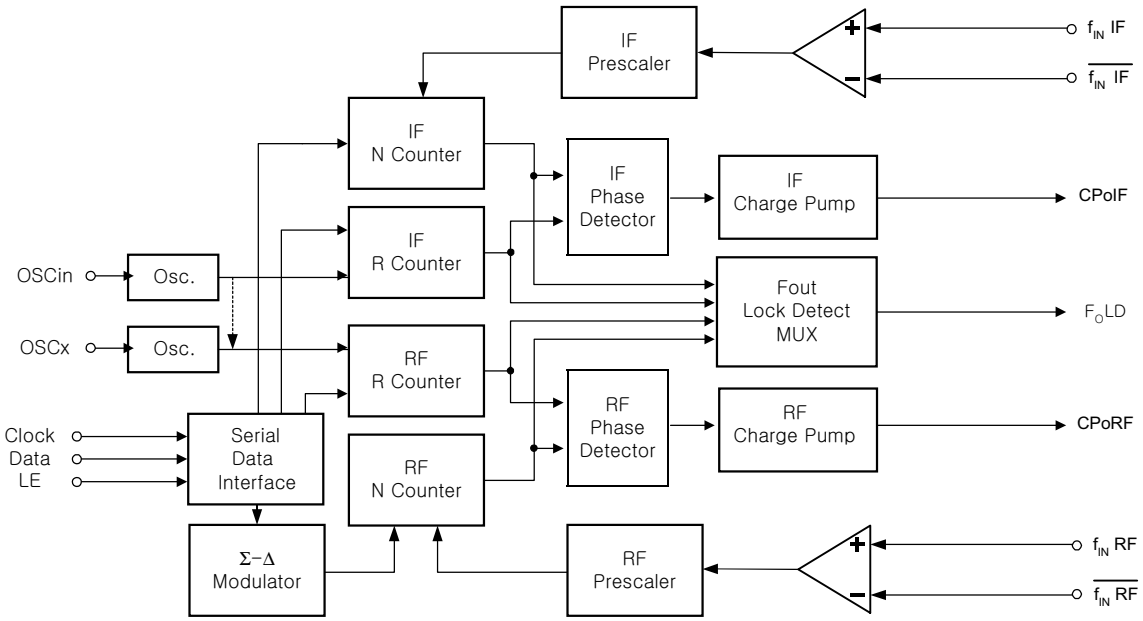
The HM6F5201 integrates programmable dividers, charge pumps and phase comparators to implement dual frequency synthesizer. The synthesizer is to be used as a local oscillator for RF and IF of a dual conversion transceiver. It is fabricated using Hynix semiconductor's standard 0.25um CMOS process.

HM6F5201 has fully programmable main and reference dividers for both RF and IF synthesizer, fractional divider for RF synthesizer. A sigma-delta modulator is used to achieve fractional division and two programmable 11 bits, which are for numerator and denominator, are used for fine fractional resolution.

Using digital phase locked loop technique, HM6F5201 provides the tuning voltage for voltage-controlled oscillators to generate very stable low noise RF & IF local oscillator signals. Serial data is transferred into the HM6F5201 via three-wire serial interface (Data, Enable, and Clock). Supply voltage can range from 2.7V to 3.6V.

HM6F5201 is available in an LGA (Leadless Grid Array) 24-pin surface mount plastic package.

■ Functional Block Diagram



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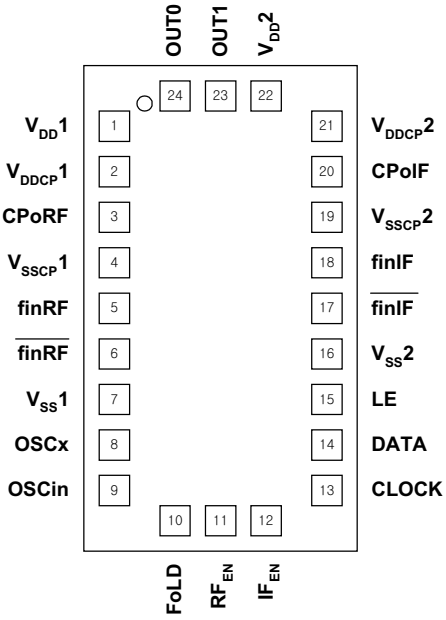
■ Pin Assignment

LGA 24 Pin Package



■ Pin Descriptions

Pin No.	PIN NAME	I/O	Description
1	$V_{DD}1$	-	Power supply voltage input for RF analog and RF digital circuits. Input may range from 2.7V to 3.6V. $V_{DD}1$ must equal to $V_{DD}2$. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
2	$V_{DDCP}1$	-	Power Supply for RF charge pump. Must be ≥ $V_{DD}1$ and $V_{DD}2$.
3	CPoRF	O	Internal RF charge pump output. For connection to a loop filter for driving the input of an external VCO.
4	$V_{SSCP}1$	-	Ground for RF charge pump and phase comparator.
5	finRF	I	RF prescaler input. Small signal input from the VCO.
6	finRF/	I	RF prescaler complementary input. For a single-ended output for RF VCO, a bypass capacitor should be placed as close as possible to this pin and be connected directly to the ground plane
7	$V_{SS}1$	-	Ground for RF analog and digital circuitry with internal seperation.
8	OSCx	I	Dual mode oscillator ouput or RF R counter input – use which can be configured depending on the state of the programming bit, *IF_R[21]* (See Table.20)
9	OSCin	I	Oscillator input to drive both the IF and RF R counter inputs or only the IF R counter, which can be configured depending on the state of the OSC programming bit, *IF_R[21]*. (See Table.20)
10	FoLD	O	Multiplexed output of the RF/IF programmable or reference dividers, and RF/IF lock detect signals. CMOS output. (See Table.11)

■ Pin Descriptions (continued)

Pin No.	PIN NAME	I/O	Description
11	RF_{EN}	I	RF PLL Enable (Enable when HIGH, Power down when LOW). Controls the RF PLL to power down directly, not depending on a program control. Also set the charge pump output to be in TRI-STATE when LOW. Powers up when HIGH depends on the state of RF_PWDN. (See Table.10)
12	IF_{EN}	I	IF PLL Enable (Enable when HIGH, Power down when LOW). Controls the IF PLL to power down directly. The same as **RF_EN** except that power-up depends on the state of IF_PWDN. (See Table.5)
13	CLOCK	I	High impedance CMOS Clock input. Data for the various counters is clocked in on the rising edge, into the 24-bit shift register.
14	DATA	I	Binary serial data input. Data entered MSB first. The last two bits are the control bits. High impedance CMOS input.
15	LE	I	Load enable high impedance CMOS input. When **LE** goes HIGH.
16	$V_{SS}2$	.	Ground for RF analog and digital circuitry with internal seperation.
17	finIF/	I	IF Prescaler complementary input. For a single-ended output IF VCO, a bypass capacitor should be placed as close as possible to this pin.
18	finIF	I	IF prescaler input. Small signal input from the VCO.
19	$V_{SSCP}2$	-	Ground for IF charge pump and phase comparator.
20	CPoIF	O	Internal IF charge pump output. For connection to a loop filter for driving the input of an external VCO.
21	$V_{DDCP}2$	-	Power Supply for IF charge pump. Must be ≥ $V_{DD}2$ and $V_{DD}1$.
22	$V_{DD}2$	-	Power supply voltage input for IF analog, IF digital, data interface, F**oLD** and oscillator circuits. Input may range from 2.7V to 3.6V. $V_{DD}2$ must equal to $V_{DD}1$. Bypass capacitors should be placed as close as possible to this pin and be connected directly to the ground plane.
23	OUT1	O	Programmable CMOS Output. Level of the output is controlled by *RF_N[19]* bit. (See Table.14)
24	OUT0	O	Programmable CMOS Output. Level of the output is controlled by *RF_N[18]* bit. In the SwiftLock mode, the **OUT0** and **OUT1** pins can be utilized as synchronous switches between active low and tri-state. (See Table.14)

■ Absolute Maximum Ratings

Parameter	Symbol	Value			Units
		Min	Typ	Max	
Power Supply Voltage	V_{DD}(1,2)	-0.3		4.2	V
	V_{DDCP}(1,2)	-0.3		4.2	V
Voltage on any pin with GND=0 volts	Vi	-0.3		4.2	V
Operating Temperature	T_A	-40		+85	^{O}C
Storage Temperature Range	T_S	-65		+150	^{O}C
Lead Temperature	T_L			+260	^{O}C

Notes : Stress above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. Other conditions above those indicated in the operational sections of this specification are not implied.

■ Electrostatic Characteristics

Parameter	Pin NO.	ESD Level	Units
Human Body Model	All	2000	V
Machine Model	All	200	V
Charge Device Model	All	500	V

Notes : When handling this device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device is content with JEDEC ESD protection requirements and has circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the level specified above table. So, Handling and assembly of this device should only be done at ESD free workstations.

* This device is immune to latch-up. (Latch-up test is done.)

■ Recommended Operating Conditions

Parameter	Symbol	Value			Units
		Min	Typ	Max	
Power Supply	V_{DD}1	2.7		3.6	V
	V_{DD}2	V_{DD}1		V_{DD}1	V
	V_{DDCP}1	V_{DD}		3.6	V
	V_{DDCP}2	V_{DD}		3.6	V
Operating Temperature	T_A	-40		+85	^{O}C

■ Electrical Characteristics

$V_{DD}1 = V_{DD}2 = V_{DDCP}1 = V_{DDCP}2 = 3.0V$, $-40°C < T_A < 85°C$, Except as Specified

Symbol	Parameter		Conditions	Value			Value
				Min	Typ	Max	
General							
I_{DD}	Power Supply Current	CDMA	RF=On, IF=On		6	8.5	mA
		> PCS	RF=On, IF=On		7	9.5	mA
			IF Only		1	2	mA
$I_{DD-PWRDN}$	Power down Current		RF_{EN}, IF_{EN} = 0		1	10	μA

■ Electrical Characteristics (Continued)

$V_{DD}1 = V_{DD}2 = V_{DDCP}1 = V_{DDCP}2 = 3.0V$, $-40°C < T_A < 85°C$, Except as Specified

Symbol	Parameter		Conditions	Value			Units
				Min	Typ	Max	
Operating Frequency, Input Sensitivity							
$f_{IN}RF$	Operating Frequency	HM6F5201	P = 12/13	1.2	-	2.5	GHz
			P = 8/9	0.5	-	1.2	GHz
$f_{IN}IF$	Operating Frequency		P = 8/9	45	-	1000	MHz
f_{OSC}	Oscillator Frequency.			2	-	40	MHz
f_{Φ}	Maximum Phase Detector Freq.			-	-	20	MHz
$Pf_{IN}RF$	RF Input Sensitivity		V_{DD}=2.7V to 3.6V	- 15	-	0	dBm
$Pf_{IN}IF$	IF Input Sensitivity		V_{DD}=2.7V to 3.6V	-10	-	0	dBm
V_{OSC}	Oscillator Sensitivity		OSC_{IN}	0.5	-	V_{DD}	V_{P-P}
Reference Oscillator Inputs							
I_{IHR}	Oscillator Input Current		V_{IH} =V_{DD}=3.6V	-	-	100	µA
I_{ILR}	Oscillator Input Current		V_{IL} =0V, V_{DD}=3.6V	-100	-	-	µA
Digital Inputs[1]							
V_{IH}	High Level Input Voltage		*	0.8 V_{DD}	-	-	V
V_{IL}	Low Level Input Voltage		*	-	-	0.2 V_{DD}	V
I_{IH}	High Level Input Current		V_{IH} =V_{DD}=3.6V	-1.0	-	1.0	µA
I_{IL}	Low Level Input Current		V_{IL} =0V, V_{DD}=3.6V	-1.0	-	1.0	µA
Digital Outputs[1]							
V_{OH}	High-Level Output Voltage		I_{OH} = -500 µA	V_{DD}-0.4	-	-	V
V_{OL}	Low-Level Output Voltage		I_{OL} = 500 µA	-	-	0.4	V
Serial Data Control[2]							
t_{CK}	Clock Cycle Time		See Data Input Timing	40	-	-	ns
t_r	Clock Rise Time		See Data Input Timing	-	-	50	ns
t_f	Clock Fall Time		See Data Input Timing	-	-	50	ns
t_{CS}	Data Setup Time to Clock		See Data Input Timing	5	-	-	ns
t_{CH}	Data Hold Time to Clock		See Data Input Timing	0	-	-	ns
t_{CWH}	Clock Pulse Width High		See Data Input Timing	10	-	-	ns
t_{CWL}	Clock Pulse Width Low		See Data Input Timing	10	-	-	ns
t_{ES}	Clock to Load Enable Setup Time		See Data Input Timing	10	-	-	ns
t_{EH}	Clock to Load Enable Hold Time		See Data Input Timing	12	-	-	ns
t_{ED}	Load Enable to Clock Delay Time		See Data Input Timing	12	-	-	ns
t_{EW}	Load Enable Pulse Width		See Data Input Timing	50	-	-	ns

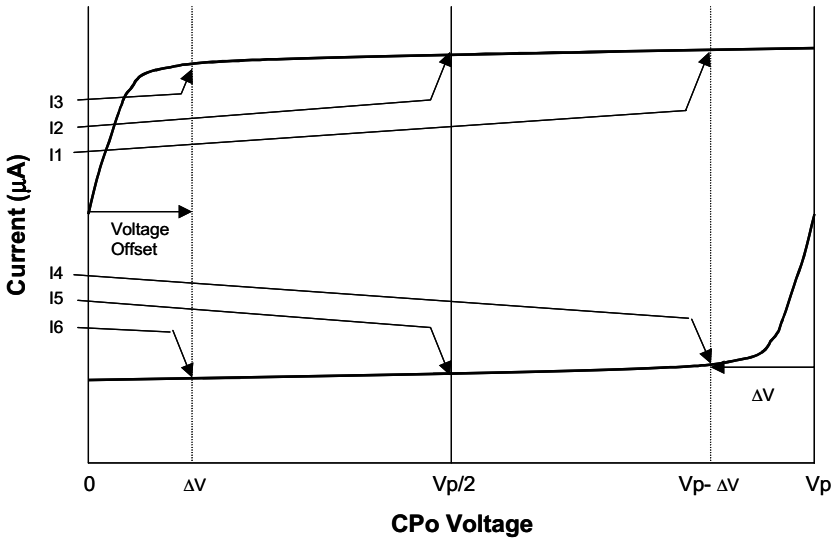
Notes : For signal Clock, Data, LE, RF_{EN}, IF_{EN}, FoLD. Does not include $f_{IN}RF$, $f_{IN}IF$ and OSC_{IN}.
All timing is referenced to the 50% level of the waveform, unless otherwise noted.

■ Electrical Characteristics (Continued)

$V_{DD}1 = V_{DD}2 = V_{DDCP}1 = V_{DDCP}2 = 3.0V$, $-40°C < T_A < 85°C$, Except as Specified

Symbol	Parameter	Conditions	Value			Units
			Min	Typ	Max	
Charge Pump						
$I_{CPo\text{-source RF}}$	RF Charge Pump Output Current (see the Table.9)	$V_{CPo} = V_p/2$, RF_CP = 000	-	-100	-	µA
$I_{CPo\text{-sink RF}}$		$V_{CPo} = V_p/2$, RF_CP = 000	-	100	-	µA
$I_{CPo\text{-source RF}}$		$V_{CPo} = V_p/2$, RF_CP = 111	-	-800	-	µA
$I_{CPo\text{-sink RF}}$		$V_{CPo} = V_p/2$, RF_CP = 111	-	800	-	µA
$I_{CPo\text{-source IF}}$	IF Charge Pump Output Current (see the Table.4)	$V_{CPo} = V_p/2$, IF_CP = 0	-	-100	-	µA
$I_{CPo\text{-sink IF}}$		$V_{CPo} = V_p/2$, IF_CP = 0	-	100	-	µA
$I_{CPo\text{-source IF}}$		$V_{CPo} = V_p/2$, IF_CP = 1	-	-800	-	µA
$I_{CPo\text{-sink IF}}$		$V_{CPo} = V_p/2$, IF_CP = 1		800		µA
$I_{CPo\text{-TRI}}$	Charge Pump TRI_STATE Current	$0.5 \le V_{CPo} \le V_p\text{-}0.5$ $-40°C \le T_A \le +85°C$	-2.5	-	2.5	nA
RF $I_{CPo\text{- sink}}$ vs. $I_{CPo\text{-source}}$	RF CP Sink vs. Source Mismatch	$V_{CPo} = V_p/2$, $T_A = 25°C$ RF I_{CPo}		2	6	%
I_{CPo} vs. V_{CPo}	CP Current vs. Voltage Variation	$0.5 \le T_A \le V_p\text{-}0.5$ $T_A = 25°C$, RF I_{CPo}		2	5	%
I_{CPo} vs. Temp.	CP Current vs. Temperature	$V_{CPo} = V_p/2$, RF I_{CPo} $-40°C \le T_A \le +85°C$		3		%

■ Charge Pump Current Specification Definitions



I1 = CP sink current at $V_{CPo} = V_p - \Delta V$
I2 = CP sink current at $V_{CPo} = V_p/2$
I3 = CP sink current at $V_{CPo} = \Delta V$
I4 = CP source current at $V_{CPo} = V_p - \Delta V$
I5 = CP source current at $V_{CPo} = V_p/2$
I6 = CP source current at $V_{CPo} = \Delta V$

ΔV = Voltage offset from positive and negative rails. Dependent on VCO tuning range relative to VDD and ground. Typical values are between 0.5V and 1.0V

Notes

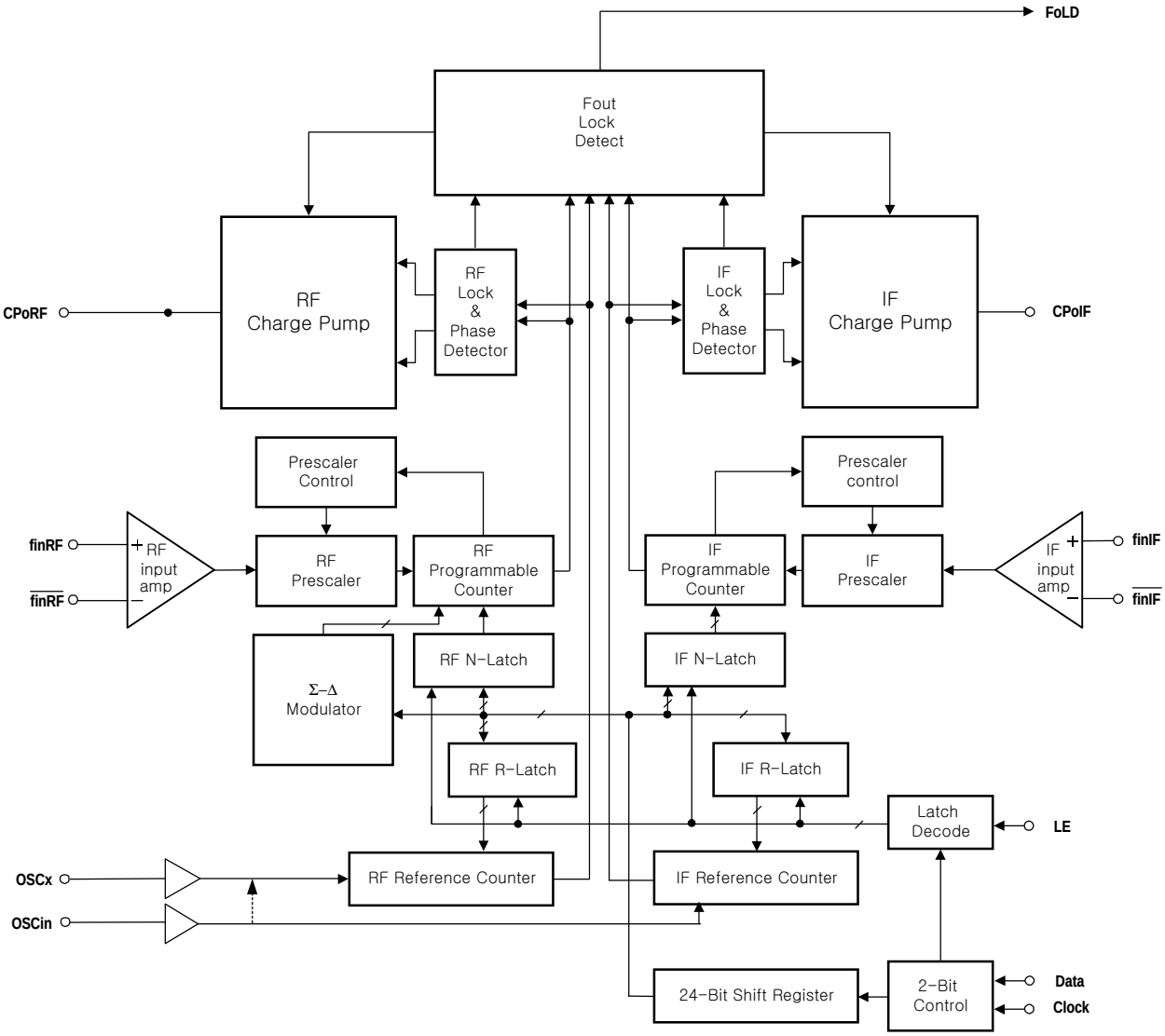
I_{CPo} vs. V_{CPo} = [1/2 * {|I1|-|I3|}] / [1/2 * {|I1|+|I3|}] * 100% and [1/2 * {|I4|-|I6|}] / [1/2 * {|I4|+|I6|}] * 100%

$I_{CPo\text{-sink}}$ vs. $I_{CPo\text{-source}}$ = [|I2|-|I5|] / [1/2 * {|I2| + |I5|}] * 100%

I_{CPo} vs. T_A = [| I2@temp | - | I2@25°C |] / | I2@25°C | * 100% and [| I5@temp | - | I5@25°C |] / | I5@25°C | * 100%

■ Functional Block Diagram

The simplified block diagram below shows the 24bit data register, 15-bit IF R and N counters, two 11-bit fractional counters and 2-bit RF R counter and 9-bit N Counters. The data stream is clocked (on the rising edge of Clock) into the DATA input, MSB first. The last two bits are the Control Bits. The DATA is transferred into the counters as follows:



■ Functional Description

POWER ON RESET

The HM6F5201 generates a power on reset operation at power up.

REFERENCE OSCILLATOR INPUTS

The Reference oscillator frequency for RF and IF PLL is provided by an external reference through the OSCin pin and OSCx pin. OSCif/OSCrf block can operate 40MHz with an input sensitivity 0.5v Vpp. The OSC Bit selects whether the oscillator input pins OSCin and OSCx drive the IF and RF R counters separately or common input signal path. ***(See the Table.20)***

When an external TCXO is connected only at the OSCin input pin and not at OSCrf pin, the TCXO drive both IF R counter and RF R counter. When configured as separate inputs, the OSCin pin drives the IF R counter while OSCx pin drives RF R counter.

REFERENCE DIVIDER

The RF and IF R Counters are clocked through the Oscillator block either separately or in common. The maximum frequency is 40MHz. RF R counter is 2 bits CMOS counters with a divide range from 1 to 3. IF R counter is 15 bits CMOS counter with a divide range from 2 to 32767.

(See the Table.3 for IF and the Table.8 for RF)

PROGRAMMABLE DIVIDER

The RF and IF N Counters are clocked by the small signal fin RF and finIF input pins respectively. The RF N counter consists of 5-bit programmable counter(B counter) and 4-bit swallow counter(A counter). The IF N counter consists of 12-bit programmbable counter(B counter) and 3-bit swallow counter(A counter).

(See the Table.12/13 for IF and the Table.17/18 for RF)

PRESCALER

The fully CMOS RF prescaler consists of a differential input buffer and CML frequency divider, while the fully CMOS IF prescaler consists of a differential input buffer and TSPC frequency divider.

The input buffer amplifies an input signal from an external VCO to the required level set by sensitivity requirements. The output of the RF amplifier delivers a differential signal to the RF divider with the correct DC level, while the IF amplifier a single-ended signal to the IF divider. The buffers may be either single-ended or differentially driven. The single-ended operation is preferred in typical applications due to external VCO. In this case, we recommend that the complementary inputs /fin of the input buffers be AC coupled to ground through external capacitors, even though it is internally coupled to ground via an internal 1pF capacitor. The other input pins fin of the buffers also need external capacitors for decoupling the DC component and controlling the input power level.

The RF prescaler provides 8/9 or 12/13 prescaler ratios to allow the multi-modulus operation, while the IF circuitry contains 8/9 dual-modulus prescaler. The prescaler clocks the subsequent CMOS flip-flop chain comprising the fully programmable A and B counters. ***(See the Table.19)***

FRACTIONAL COMPENSATION

(Σ–Δ modulator)

The RF part of HM6F5201 adopts the Σ–Δ modulator as core of the fractional counter that makes it possible to obtain divide ratio N to be a fractional number between two contiguous integers. The Σ–Δ modulator effectively randomizes the quantization noise generated from digitizing process and results in extreme suppression of in-band noise power by pushing it out to out-of-band as in conventional Σ–Δ data converter. This technique eliminates the need for compensation current injection into the loop filter and improves fractional spurious performance, suitable for high-tier applications.

For proper Σ–Δ modulator operation, the user shouldbe kept in mind that

1. A fractional number should be set in the range from 0 to K-1 in step 1/K
2. The clock frequency (OSCin/R) that is higher than 10 MHz is recommended for better performance. But power consumption can be increase.

Note that the clock frequency much lower than 10 MHz can deteriorate the fractional noise performance.

(See the Table.7 for Denominator and the Table.16 for Numerator as Fractional Divider)

SERIAL INTERFACE

The programmable functions are accessed through the serial interface. The interface is made of 3 functions: clock, data, and latch enable(LE). Serial data for the various counters is clocked in from data on the rising edge of clock, into the 24-bit shift register. Data is entered MSB first. The last two bits decode the internal register address. On the rising edge of LE, data stored in the shift register is loaded into one of the 4 appropriate latches (selected by address bits). A complete programming description is included in the following sections.

POWER CONTROL

Each PLL is individually power controlled by device enable pin or serial interface power down bits. The enable pins override the power down bits. The RF_EN pin controls the RF PLL; IF_EN pin controls the IF PLL. When both pins are high, the power down bits determine the state of power control.

(See the Table.5 and the Table.10 and the Table.20)

Activation of any PLL power down mode results in the disabling of the respective N counter and de-biasing of its respective fin input(to a high impedance state). The R counter functionality also becomes disabled when power down bit is activated. The oscillator input block also powers down. Power down forces the respective charge pump and phase detector logic to a TRI-STATE condition. A power down counter reset function resets both N and R counters. Upon powering up the N counter resumes counting in close alignment with R counter (the maximum error is one prescaler cycle). The serial interface remains active and capable of loading and latching in data during all of power down modes.

PFD and CP

The RF/IF phase detector, composed of PFD and CP, outputs an average proportional to the phase difference of between outputs of N and R counter. This average is converted to the control voltage of VCO by external loop filter. The slope of the PFD is programmable using RF_R[16]*(RF_PFD_POL)* and IF_R[17]*(IF_PFD_POL)* depending on whether RF/IF VCO has positive slope or negative slope.

(See the Table.4 for IF and the Table.9 for RF)

Also, the RF charge pump output current gain is programmable from 100uA to 800 uA in 100uA steps using RF_R[19:17] *(RF_CP_GAIN)* and the IF charge pump output gain is set to either 100uA or 800uA using IF_R[18]*(IF_CP_GAIN)*.

(See the Table.4 for IF and the Table.9 for RF)

■ Programming Description

INPUT DATA REGISTER

The HM6F5201 can be programmed via the serial bus interface. The interface is made of 3 functional signals: **Clock**, **Data**, and load enable(**LE**). Serial data is moved into the 24-bit shift register on the rising edge of the clock. These data enters MSB first. When **LE** goes HIGH, data in the shift register is moved into one of the 4 latches(by the 2-bit control).

MSB ◀—— data flow(MSB first) **LSB**

DATA[23:2]	CTL[1:0]

Table.1 Control Bit Map (CTL[1:0])

CONTROL BITS		DATA LOCATION
C[1]	C[0]	
0	0	IF_R Register
0	1	IF_N Register
1	0	RF_R Register
1	1	RF_N Register

Table.2 Data Bit Map (DATA[23:2])

Register Name	REGISTER BIT LOCATION MSB																						LSB	
	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
IF_R	FoLD		OSC	IF_PWDN		IF_CP		IF_R_DIV (15bit)															0	0
IF_N	*VNT*		FRAC_MODE		CMOS			IF_B_DIV (12bit)												IF_A_DIV(3bit)			0	1
RF_R	FoLD		RF_PWDN		RF_CP			*X*	RF_R_DIV(2bit)		FRAC_K_DIV(11bit)												1	0
RF_N	*VNT*	PRE	RF_B_DIV(5bit)					RF_A_DIV(4bit)			FRAC_F_DIV(11bit)												1	1

Notes: *VNT(vendor test bits*) and *X* (dummy bit) are reserved.
They should be set to be zero (LOW) for normal usage.

■ Programming Description (Continued)

PROGRAMMABLE REFERENCE DIVIDERS

IF_R REGISTER

If the Control Bits(C[1:0]) are 00, data is moved from the 24-bit shift register into the IF_R register which sets the IF reference counter. Serial data format is shown in the table below.

MSB **IF_R[23:0]** **LSB**

FoLD [1:0]		OSC	IF_PWDN [1:0]		IF_CP [1:0]		IF_R_DIV [14:0]		C[1]	C[0]
23	22	21	20	19	18	17	16	2	1	0

Table.3 Binary 15-Bit Programmable IF R Divider Ratio (R Counter) (IF_R[16] –IF_R[2])

Division Ratio	IF_R [16]	IF_R [15]	IF_R [14]	IF_R [13]	IF_R [12]	IF_R [11]	IF_R [10]	IF_R [9]	IF_R [8]	IF_R [7]	IF_R [6]	IF_R [5]	IF_R [4]	IF_R [3]	IF_R [2]
3	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
•	•	•	•	•	•	•	•	•	•	•	•	•	•	•	•
32767	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Notes : Division ratio: 3 to 32767 (The divide ratios less than 3 are prohibited)

Data shifted in MSB first.

Table.4 IF Charge Pump and Phase Frequency Control - (IF_CP) (IF_R[18:17])

IF_CP_GAIN	IF_PFD_POL

Acronym	Data Bits	Low(0)	High(1)	Comments
IF_CP_GAIN	IF_R[18]	1X	8X	IF Charge Pump Current Gain
IF_PFD_POL	IF_R[17]	Negative	Positive	IF Phase Detector Polarity

Table.5 IF Power Down and Power Down Mode - (IF_PWDN) (IF_R[20:19])

PWRDN_IF	PWRDN_MODE_IF

Acronym	Data Bits	Low(0)	High(1)	Comments
PWRDN_IF	IF_R[20]	Power Up	Power Down	IF Power Down
PWRDN_MODE_IF	IF_R[19]	Asynchronous power down	Synchronous power down	IF Power Down Mode Select

■ Programming Description (Continued)

Table.6 Reference Oscillator Input - (OSC) (IF_R[21])

Acronym	Data Bits	Low(0)	High(1)	Comments
OSC	IF_R[21]	Separate Inputs ; OSCin for IF, OSCx for RF	Common Input through OSCin for both RF and IF	Reference Oscillator Input Control

Fout / Lock Detect Programming Bits - (FoLD)

See the RF_R register section for more detail.

RF_R REGISTER

If the Control Bits(C[1:0]) are 10, data is moved from the 24-bit shift register into the RF_R register which sets the RF reference (RF R counter; 2-bit) / fractional counter (K counter; 11-bit). Serial data format is shown below.

MSB **RF_R[23:0]** **LSB**

FoLD [1:0]		RF_PWDN [1:0]		RF_CP [3:0]		*X*	RF_R_DIV [1:0]		FRAC_K_DIV [10:0]		C[1]	C[0]
23	22	21	20	19	16	15	14	13	12	2	1	0

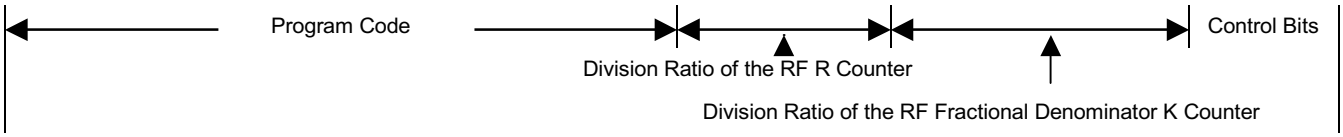


Table.7 Binary 11-Bit Programmable Fractional Denominator K Divider Ratio (K Counter) (RF_R[12:2])

Division Ratio	RF_R [12]	RF_R [11]	RF_R [10]	RF_R [9]	RF_R [8]	RF_R [7]	RF_R [6]	RF_R [5]	RF_R [4]	RF_R [3]	RF_R [2]
1	0	0	0	0	0	0	0	0	0	0	1
2	0	0	0	0	0	0	0	0	0	1	0
3	0	0	0	0	0	0	0	0	0	1	1
•	•	•	•	•	•	•	•	•	•	•	•
2047	1	1	1	1	1	1	1	1	1	1	1

Notes : Division ratio: 1 to 2047

Data shifted in MSB first.

■ Programming Description (Continued)

Table.8 Binary 2-Bit Programmable RF R Divider Ratio (RF R Counter) (RF_R[14:13])

Division Ratio	RF_R [14]	RF_R [13]
1	0	1
2	1	0
3	1	1

Notice : We recommend that RF R divider ratio is 2. In this ratio, HM6F5201 have best optimized performance in power, fractional compensation and lock time.

Table.9 RF Charge Pump and Phase Frequency Detector Control - (RF_CP) (RF_R[19:16])

RF_CP_8X	RF_CP_4X	RF_CP_1X	RF_PFD_POL

Acronym	Data Bits	Low(0)	High(1)	Comments
RF_PFD_POL	RF_R[16]	Negative	Positive	RF Phase Detector Polarity

RF ICPo μA (typ)	RF_CP_8X RF_R[19]	RF_CP_4X RF_R[18]	RF_CP_1X RF_R[17]
100	0	0	0
200	0	0	1
300	0	1	0
400	0	1	1
500	1	0	0
600	1	0	1
700	1	1	0
800	1	1	1

Table.10 RF Power Down and Power Down Mode - (RF_PWDN) (RF_R[21:20])

PWRDN_RF	PWRDN_MODE_RF

Acronym	Data Bits	Low(0)	High(1)	Comments
PWRDN_RF	RF_R[21]	Power Up	Power Down	RF Power Down
PWRDN_MODE_RF	RF_R[20]	Asynchronous power down	Synchronous power down	RF Power Down Mode Select

■ Programming Description (Continued)

Table.11 Fout / Lock Detect Programming Truth Table - (FoLD) (IF_R[23:22] / RF_R[23:22])

RF_R[22] (RF LD)	IF_R[22] (IF LD)	RF_R[23] (RF Fo)	IF_R[23] (IF Fo)	FoLD Output State
0	0	0	0	Disabled
0	1	0	0	IF Lock Detect
1	0	0	0	RF Lock Detect
1	1	0	0	RF/IF Lock Detect
X	0	0	1	IF Reference Divider Output
X	0	1	0	RF Reference Divider Output
X	1	0	1	IF Programmable Divider Output
X	1	1	0	RF Programmable Divider Output
0	0	1	1	Vendor Test mode
0	1	1	1	IF Counter Reset
1	0	1	1	RF Counter Reset
1	1	1	1	RF and IF Counter Reset

X = Don't care condition

Notes :

When FoLD output is disabled, it is actively pulled to low logic state.

Lock detect output provided to indicate when the VCO frequency is in "LOCK". When the loop is locked and a lock detect mode is selected, the pins output is high with narrow pulses LOW. In RF/IF detect mode a locked condition is indicated when RF and IF are both locked.

■ Programming Description (Continued)

PROGRAMMABLE DIVIDER

IF_N REGISTERS

If the Control Bits(C[1:0]) are 01, data is transferred from the 24-bit shift register into the IF_N register which sets the IF programmable counter. IF N counter consists of swallow counter(A counter: 3-bit), main counter(B counter; 12-bit). Serial data format is shown below.

MSB **IF_N[23:0]** **LSB**

VNT [1:0]		FRAC_MODE [1:0]		CMOS [2:0]		IF_B_DIV [11:0]		IF_A_DIV [2:0]		C[0]	C[1]
23	22	21	20	19	17	16	5	4	2	1	0

Program Code — Division Ratio of the IF N Counter — Control Bits

Table.12 Binary 3-Bit Programmable Swallow Counter Division Ratio (IF A Counter) (IF_N[4:2])

Division Ratio	IF_N [4]	IF_N [3]	IF_N [2]
0	0	0	0
1	0	0	1
•	•	•	•
7	1	1	1

Division ratio : 0 to 7 B > A

Table.13 Binary 12-Bit Programmable IF Main Counter Division Ratio (IF B Counter) (IF_N[16:5])

Division Ratio	IF_N [15]	IF_N [15]	IF_N [14]	IF_N [13]	IF_N [12]	IF_N [11]	IF_N [10]	IF_N [9]	IF_N [8]	IF_N [7]	IF_N [6]	IF_N [5]
3	0	0	0	0	0	0	0	0	0	0	1	1
4	0	0	0	0	0	0	0	0	0	1	0	0
5	0	0	0	0	0	0	0	0	0	1	0	1
•	•	•	•	•	•	•	•	•	•	•	•	•
4095	1	1	1	1	1	1	1	1	1	1	1	1

Notes : Division ratio: 3 to 4095 (The division ratio less than 3 are prohibited)

■ Programming Description (Continued)

Table.14 Programmable CMOS Output - (CMOS) (IF_N[19:17])

SwiftLock	OUT1	OUT0

Acronym	Data Bits	Low(0)	High(1)	Comments
SwifLock	IF_N[19]	CMOS Output	Swift Lock Mode	Fast Lock
OUT1	IF_N[18]	Voltage LOW	Voltage HIGH	Pin #23
OUT0	IF_N[17]	Voltage LOW	Voltage HIGH	Pin #24

When the SwiftLock bit is set to 1, the **OUT0** and **OUT1** are don't care bits. In the SwiftLock mode, OUT0 and OUT1 pins can be utilized as synchronous switches between active low and tri-state. The SwiftLock mode activates the **OUT0** and **OUT1** pins to be connected to GROUND with a low impedance (< 150 Ω) while a high charge pump gain (8X) is selected and otherwise to the TRISTATE.

For using a programmable CMOS output, the CMOS output bit(*IF_N[20]* =L) should be activated and then the desired logic level should be programmed with the control bits *IF_N[18]* for **OUT1** and *IF_N[17]* for **OUT0**.

Table.15 Fractional Spur Compensation Mode (IF_N[21:20])

Data Bits	Low(0)	High(1)	Comments
IF_N[20]	Dithering On	Dithering Off	Selection of Fractional Spur Reduction
IF_N[21]	Fractional On	Fractional Off	Selection of Fractional Spur Compensation

With IF_N[21:20] set to [0,0], this mode enable the dithering so that the most fractional spurious is reduced. The dithering randomizes the fractional quantization noise so that it looks more like white noise rather than spurious noise. This mode would normally be used when PLL closed loop bandwidth is wide. We recommended this mode.
When this bit set to [0,1], the HM6F5201 operates with more reduced phase noise level but fractional spur is not reduced due to disable the dithering. So, this mode should be used when PLL closed loop bandwidth is narrow.
In IF_N[21] is high, IF_N[20] don't care. This mode is such as Integer-N PLL.

Vendor Test Bits - (VNT) (IF_N[23:22])

Vendor test bits are for verification of some functions and characteristics. In normal usage, they should be set to LOW.

■ Programming Description (Continued)

RF_N REGISTER

If the Control Bits(C[1:0]) are 11, data is moved from the 24-bit shift register into the RF_N register, which sets the RF programmable counter. RF N counter consists of swallow counter(A counter: 4-bit), main counter(B counter; 5-bit) and RF fractional counter (F counter; 11-bit). Serial data format is shown below.

MSB **RF_N[23:0]** **LSB**

VNT	PRE	RF_B_DIV [4:0]	RF_A_DIV [3:0]	FRAC_F_DIV [10:0]	C[1]	C[0]
23	22	21 17	16 13	12 2	1	0

Division Ratio of the RF N Counter

Control Bits

Division Ratio of the RF Fractional Numerator F Counter

Table.16 Binary 11-Bit Programmable Fractional Numerator Value (F Counter) (RF_N[12:2])

Division Ratio	RF_N [12]	RF_N [11]	RF_N [10]	RF_N [9]	RF_N [8]	RF_N [7]	RF_N [6]	RF_N [5]	RF_N [4]	RF_N [3]	RF_N [2]
1023	0	1	1	1	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•
1	0	0	0	0	0	0	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0
-1	1	1	1	1	1	1	1	1	1	1	1
•	•	•	•	•	•	•	•	•	•	•	•
-1024	1	0	0	0	0	0	0	0	0	0	0

Notes : F counter value: -1024 (2's complementary) to 1023

For a negative integer, the F counter value should be entered as the corresponding 2's complementary binary code.

For example, the 2's complemetary binary code of -2 is 1 1111 1111 1111 1110.

Table.17 Binary 4-Bit Programmable Swallow Counter Division Ratio (RF A Counter) (RF_N[16:13])

When RF prescaler has 12/13 divide ratio

Division Ratio	RF_N [16]	RF_N [15]	RF_N [14]	RF_N [13]
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
•	•	•	•	•
11	1	1	1	1

When RF prescaler has 8/9 divide ratio

Division Ratio	RF_N [16]	RF_N [15]	RF_N [14]	RF_N [13]
0	X	0	0	0
1	X	0	0	1
•	•	•	•	•
7	X	1	1	1
X	X	X	X	X

Notes : Division ratio : 0 to 11 B > A

■ Programming Description (Continued)

Table.18 Binary 5-Bit Programmable RF Main Counter Division Ratio (RF B Counter) (RF_N[21:17])

Division Ratio	RF_N [21]	RF_N [20]	RF_N [19]	RF_N [18]	RF_N [17]
3	0	0	0	1	1
4	0	0	1	0	0
5	0	0	1	0	1
•	•	•	•	•	•
31	1	1	1	1	1

Notes : Division ratio: 3 to 31 (The division ratio less than 3 are prohibited)

Table.19 RF Prescaler Select - (PRE) (RF_N[22])

Acronym	Data Bits	Low(0)	High(1)	Comments
PRE	RF_N[22]	8/9	12/13	RF Prescaler Modulus Select

Notes : PRE (prescaler select) is used to set RF prescaler. The HM6F5201 contains two dual modulus prescaler. It uses the 8/9 or 12/13 dual modulus prescaler mode to operate at 500 MHz ~ 2.5 GHz.

In 8/9 dual modulus prescaler mode, the HM6F5201 can operate up to 2.3 GHz. But we recommend that you select RF prescaler mode following rule.

8/9 prescaler mode to operate 500 MHz ~ 1.2 GHz

12/13 prescaler mode to operate 1.2 GHz ~ 2.5 GHz

■ Program Mode Control

REFERENCE OSCILLATOR INPUT and POWER DOWN CONTROL

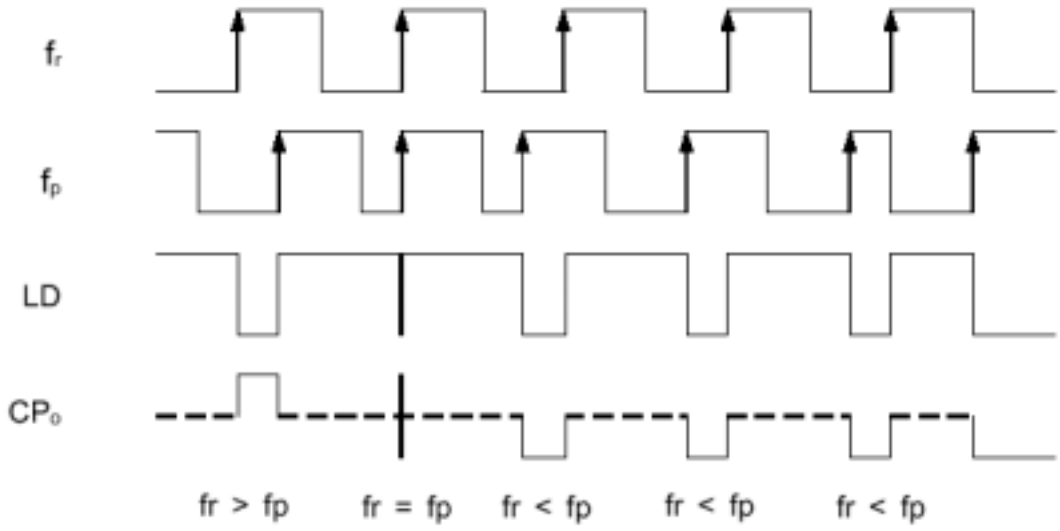
Table.20 Reference Oscillator Input and Power Down Control

OSC	PWRDN_IF	PWRDN_RF	IF	RF
IF_R[21]	IF_R[18]	RF_R[21]		
LOW	0	0	OSCin	OSCx
	0	1	OSCin	LOW (Power down)
	1	0	LOW (Power down)	OSCx
	1	1	LOW (Power down)	LOW (Power down)
HIGH	0	0	OSCin	OSCin
	0	1	OSCin	LOW (Power down)
	1	0	LOW (Power down)	OSCin
	1	1	LOW (Power down)	LOW (Power down)

■ Phase Detector and Charge Pump Characteristics

Phase difference detection Range : -2π ~ +2π

When the positive-slope polarity of PFD is selected, IF_R[17]=HIGH or RF_R[16]=HIGH;



■ Application Example

Pulse Swallow Function

The RF VCO's frequency fvco becomes N_{INT} + N_{FRAC} N times the comparison frequency (fosc / R) where N_{INT} is the integer divide ratio and N_{FRAC}(=F/K) is the fractional component;.

fvco = (N + F / K) * Fosc / R

where N = (P * B) + A,

RF PLL : N_{FRAC} = F/K, 0 < K < 2048, -1024 ≤ F≤ 1023, -0.5 ≤ F/K ≤ 0.5

IF PLL : N_{FRAC} = 0, B > A, and 3 ≤ R ≤ 32767

fvco : External VCO output frequency

fosc : External reference frequency(From external oscillator)

R : Preset divide ratio of programmable R counter(RF :1 ~ 2 IF : 3 ~ 32767)

P : Preset modulus of Dual modulus prescaler (RF : 8 or 12 IF : 8)

B : Preset value of main counter (RF : 3 ~ 31 IF : 3 ~ 2047)

A : Preset value of swallow counter division ratio (RF : 0 ~ 11 IF : 0 ~ 8 A < B)

F : Preset value of fractional counter (RF : 0 ~ K-1)

K : Preset value of fractional reference (RF : 1 ~ 2047)

For examples in fractional mode for cellular (fosc=19.68MHz, R=2, P=8)

1) for fvco = 955.02MHz : N = 97, B = 12, A = 1, K = 1968, F = 108

2) for fvco = 955.03MHz : N = 97, B = 12, A = 1, K = 1968, F = 110

3) for fvco = 956.25MHz : N = 97, B = 12, A = 1, K = 1968, F = 354

4) for fvco = 970.35MHz : N = 99, B = 12, A = 3, K = 1968, F = -762

For examples in fractional mode for PCS (fosc=19.68MHz, R=2, P=12)

1) for fvco = 1620.87MHz : N = 165, B = 13, A = 9, K = 1968, F = -546

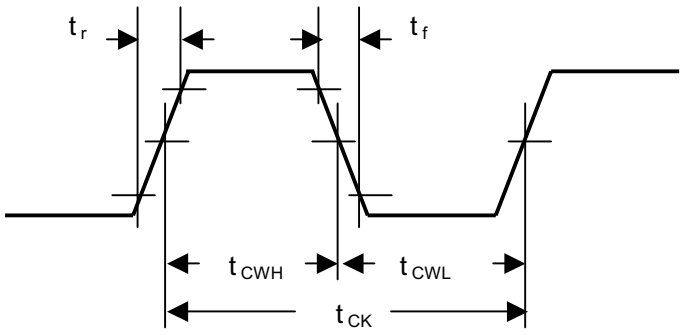
2) for fvco = 1620.88MHz : N = 165, B = 13, A = 9, K = 1968, F = -544

3) for fvco = 1622.12MHz : N = 165, B = 13, A = 9, K = 1968, F = -296

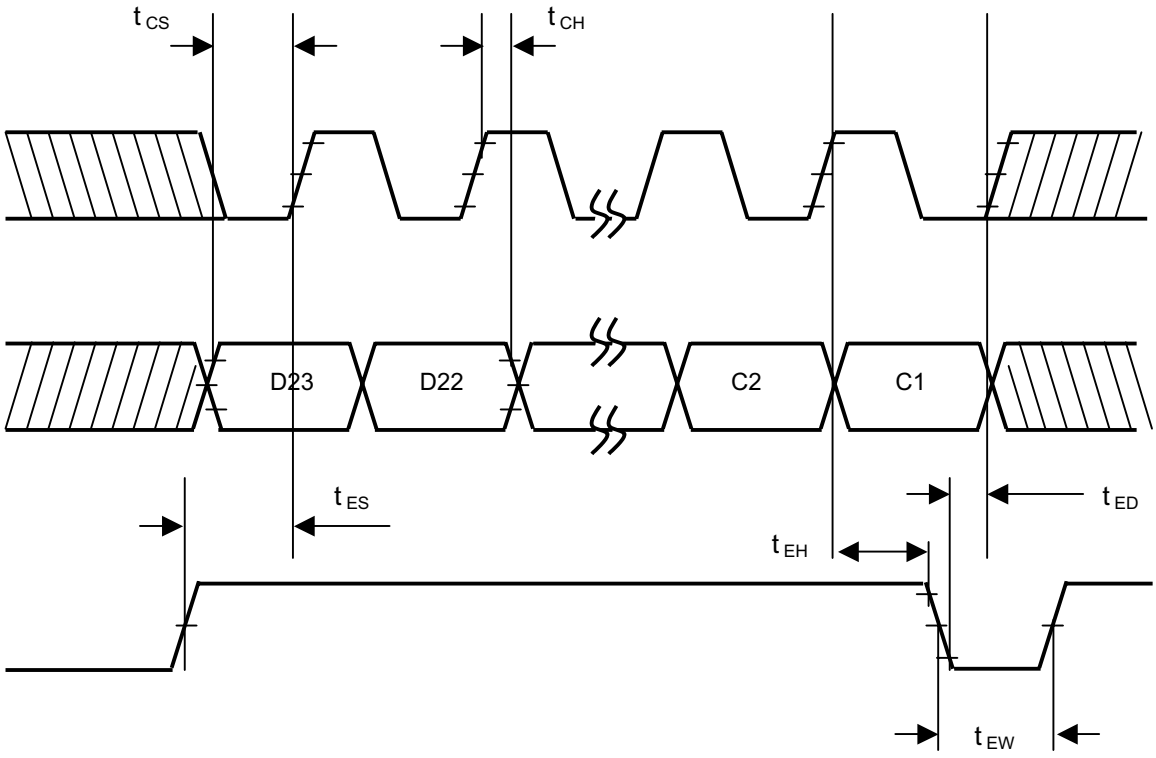
4) for fvco = 1632.12MHz : N = 166, B = 13, A = 10, K = 1968, F = -264

4) for fvco = 1648.37MHz : N = 168, B = 14, A = 0, K = 1968, F = -950

■ Serial Data Input Timing



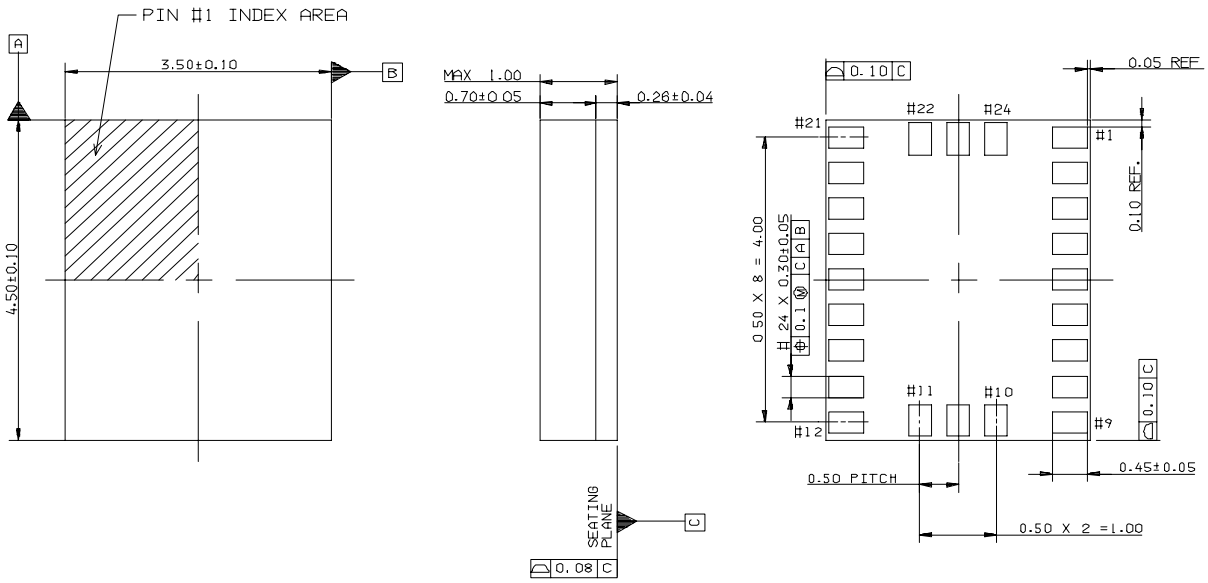
CLOCK Timing Diagram



Serial Data Timing Diagram

■ Package Outline

Physical Dimensions (unit : ㎜)



Leadless Grid Array Package

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