S75NS-N

S29NS-N: MirrorBit™ 1.8 Volt-only Simultaneous Read/ Write, Burst-mode Multiplexed Flash (NOR Interface) S30MS-P: ORNAND™ Flash (NAND interface) Multiplexed Synchronous pSRAM

Data Sheet *(Advance Information)*

Notice to Readers: This document states the current technical specifications regarding the Spansion product(s) described herein. Each product described herein may be designated as Advance Information, Preliminary, or Full Production. See *Notice On Data Sheet Designations* for definitions.

Publication Number S75NS-N_00 **Revision** 01E **Issue Date** May 3, 2006

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The Preliminary designation indicates that the product development has progressed such that a commitment to production has taken place. This designation covers several aspects of the product life cycle, including product qualification, initial production, and the subsequent phases in the manufacturing process that occur before full production is achieved. Changes to the technical specifications presented in a Preliminary document should be expected while keeping these aspects of production under consideration. Spansion places the following conditions upon Preliminary content:

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Combination

Some data sheets contain a combination of products with different designations (Advance Information, Preliminary, or Full Production). This type of document distinguishes these products and their designations wherever necessary, typically on the first page, the ordering information page, and pages with the DC Characteristics table and the AC Erase and Program table (in the table notes). The disclaimer on the first page refers the reader to the notice on this page.

Full Production (No Designation on Document)

When a product has been in production for a period of time such that no changes or only nominal changes are expected, the Preliminary designation is removed from the data sheet. Nominal changes may include those affecting the number of ordering part numbers available, such as the addition or deletion of a speed option, temperature range, package type, or V_{IO} range. Changes may also include those needed to clarify a description or to correct a typographical error or incorrect specification. Spansion LLC applies the following conditions to documents in this category:

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Questions regarding these document designations may be directed to your local AMD or Fujitsu sales office.

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Data Sheet *(Advance Information)*

Features

- **Power supply voltage of 1.7 V to 1.95 V**
- **Burst Speed: 66 MHz**
- **Package - MCP BGA: 0.5 mm ball pitch**
  - 11 x 13 x 1.4 mm, 112 ball
- **Operating Temperature**
  - Wireless, –25°C to +85°C

General Description

The S75NS-N Series is a product line of stacked Multi-Chip Product (MCP) packages and consists of the following items:

- S29NS-N
- S30MS-P
- Mux pSRAM

The products covered by this document are listed in the tables below.

	pSRAM
S29NS128 +	**32 Mb**
S30MS512P	S75NS128NBF
S30MS01GP	S75NS128NBG

Product Selector Guide

Device	pSRAM Density	pSRAM Type
S75NS128NBF	32 Mb	Multiplexed pSRAM Type 3
S75NS128NBG	32 Mb	Multiplexed pSRAM Type 3

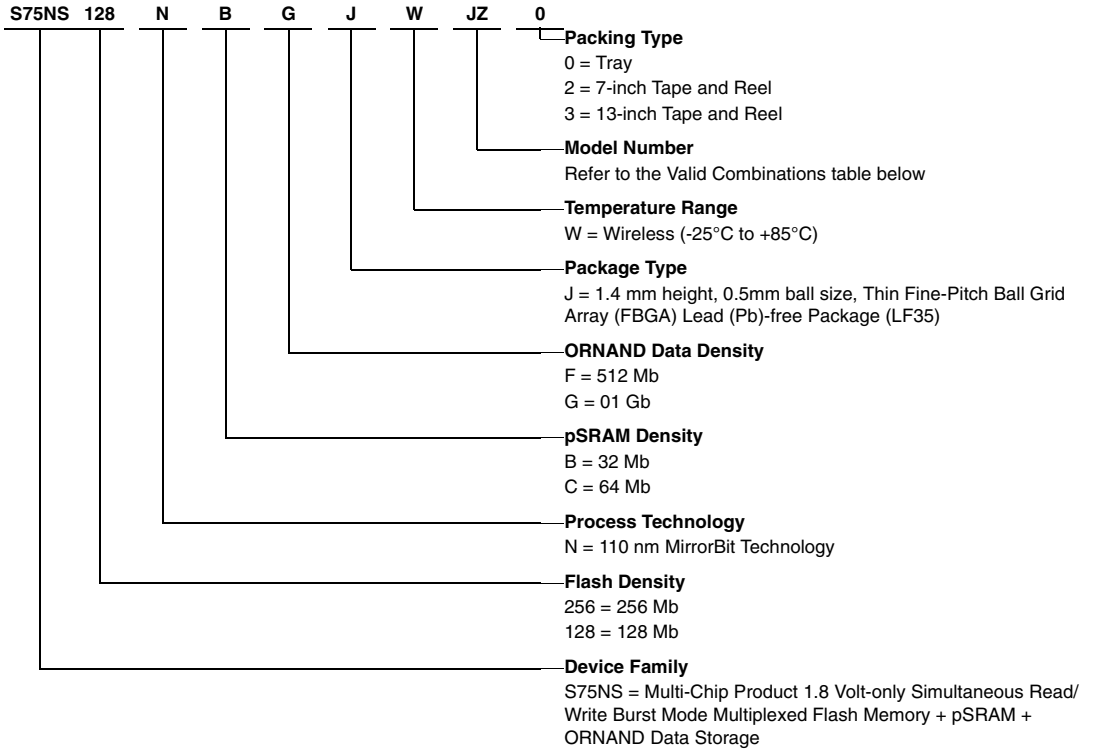
For detailed specifications, please refer to the individual data sheets:

Document	Publication Identification Number
S29NS-N	S29NS-N_00
S30MS-P	S30MS-P_00
32 Mb Multiplexed pSRAM Type 3	muxpsram_04

Publication Number S75NS-N_00 **Revision 01E** **Issue Date** May 3, 2006

1. Ordering Information

The ordering part number is formed by a valid combination of the following:



1.1 Valid Combinations

Valid Combinations list configurations planned to be supported in volume for this device. Consult your local sales office to confirm availability of specific valid combinations and to check on newly released combinations.

Table 1.1 MCP Configurations and Valid Combinations

Base Ordering Part Number (Note 2)	Package & Temperature	Model Number	Packing Type	pSRAM Type	Flash Speed Options	pSRAM Speed Options
S75NS128NBF	UJW	JZ	0, 2, 3	pSRAM Type 3	66 MHz	66 MHz
S75NS128NBG		JZ		pSRAM Type 3	66 MHz	66 MHz

Notes:

1. *Type 0 is standard. Specify other options as required.*
2. *The package marking omits the leading* S *and packing type designator from the ordering part number.*
3. *Contact factory for availability of any of the OPNs listed because RAM type availability may vary over time.*

2. Input/Output Descriptions

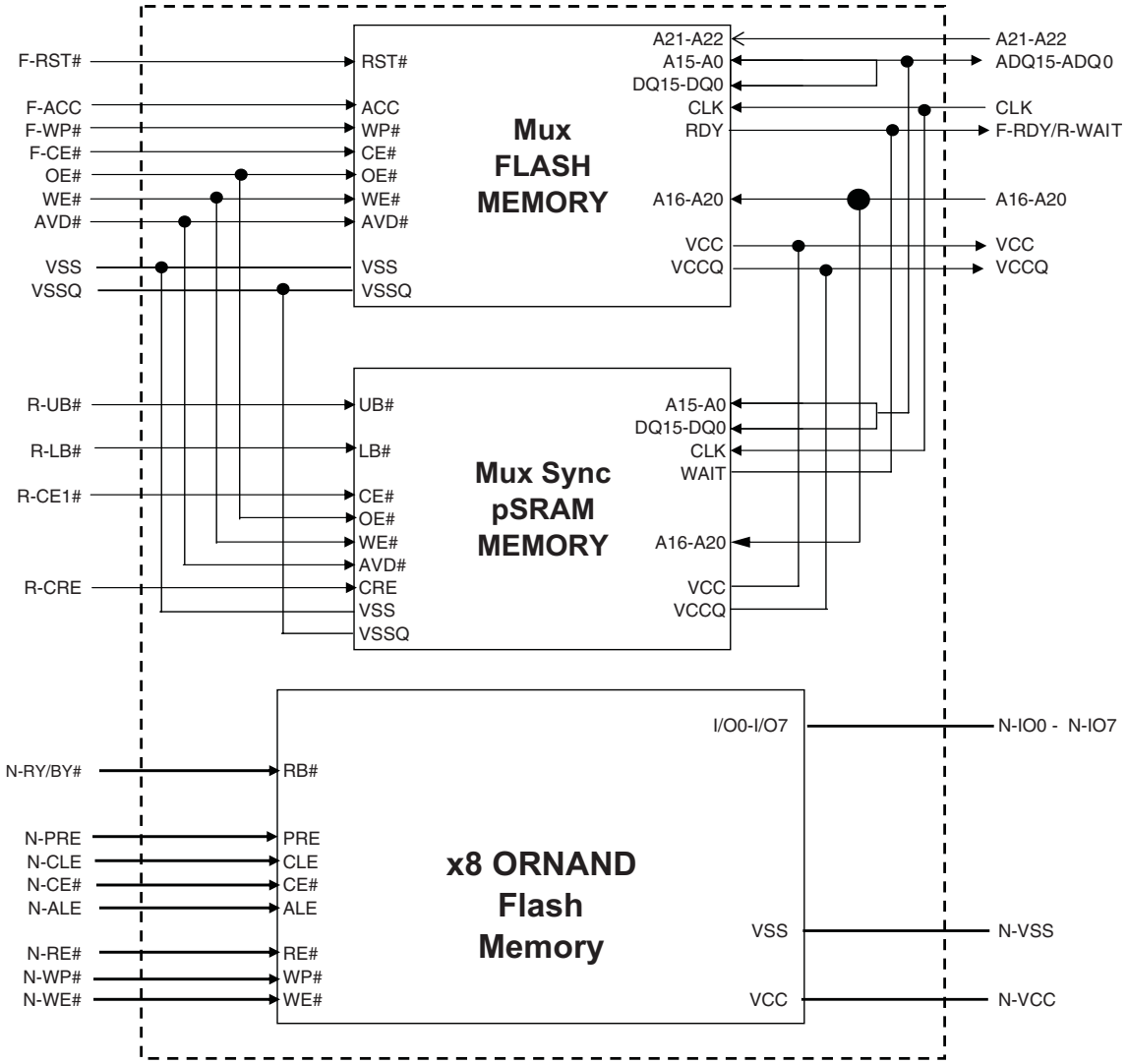
Table 2.1 identifies the input and output package connections provided on the device.

Table 2.1 Input/Output Descriptions

Symbol	Signal Type	Description	NS (NOR)	pSRAM	MS (ORNAND)
AMAX – A16	Input	Address inputs	X	X	
ADQ15 – ADQ0	I/O	Multiplexed Address/Data	X	X	
OE#	Input	Output Enable input. Asynchronous relative to CLK for the Burst mode.	X	X	
WE#	Input	Write Enable input.	X	X	
V_{SS}	Ground	Ground	X	X	
F-RDY / R-WAIT	Output	Ready output. Indicates the status of the Burst read. The WAIT# pin of the pSRAM is tied to RDY.	X	X	
CLK	Input	Clock input. In burst mode, after the initial word is output, subsequent active edges of CLK increment the internal address counter. Should be at V_{IL} or V_{IH} while in asynchronous mode	X	X	
AVD#	Input	Address Valid input. Indicates to device that the valid address is present on the address inputs. Low = for asynchronous mode, indicates valid address; for burst mode, causes starting address to be latched. High = device ignores address inputs	X	X	
F-RST#	Input	Hardware reset input. Low = device resets and returns to reading array data	X		
F-WP#	Input	Hardware write protect input. At V_{IL}, disables program and erase functions in the four outermost sectors. Should be at V_{IH} for all other conditions.	X		
F-ACC	Input	Accelerated input. At V_{HH}, accelerates programming; automatically places device in unlock bypass mode. At V_{IL}, disables all program and erase functions. Should be at V_{IH} for all other conditions.	X		
F-CE#	Input	Chip-enable input for Flash. Asynchronous relative to CLK for Burst Mode.	X		
V_{CC}	Power	Flash 1.8 Volt-only single power supply	X	X	
R-CE1#	Input	Chip-enable input for pSRAM		X	
R-CRE	Input	Control Register Enable (pSRAM)		X	
R-V_{CC}	Power	pSRAM Power Supply		X	
R-UB#	Input	Upper Byte Control (pSRAM)		X	
R-LB#	Input	Lower Byte Control (pSRAM)		X	
N-CLE	Input	Command Latch Enable			X
N-ALE	Input	Address Latch Enable			X
N-CE#	Input	Chip Enable input for ORNAND			X
N-WE#	Input	Write Enable input			X
N-RE#	Input	Read Enable input			X
N-IO0 - N-IO7	I/O	Data Input/Output			X
N-WP#	Input	Hardware write protect input. At V_{IL}, disables program and erase functions in the four outermost sectors. Should be at V_{IH} for all other conditions.			X
N-RY/BY#	Input	Ready/Busy output			X
N-PRE	Input	Power-On Read Enable			X
N-V_{SS}	Ground	Ground			X
N-V_{CC}	Power	ORNAND 1.8 Volt-only single power supply.			X
DNU	—	Do Not Use			
NC	—	No Connect; not connected internally			

3. MCP Block Diagram

Figure 3.1 MCP Block Diagram



4. Connection Diagrams/Physical Dimensions

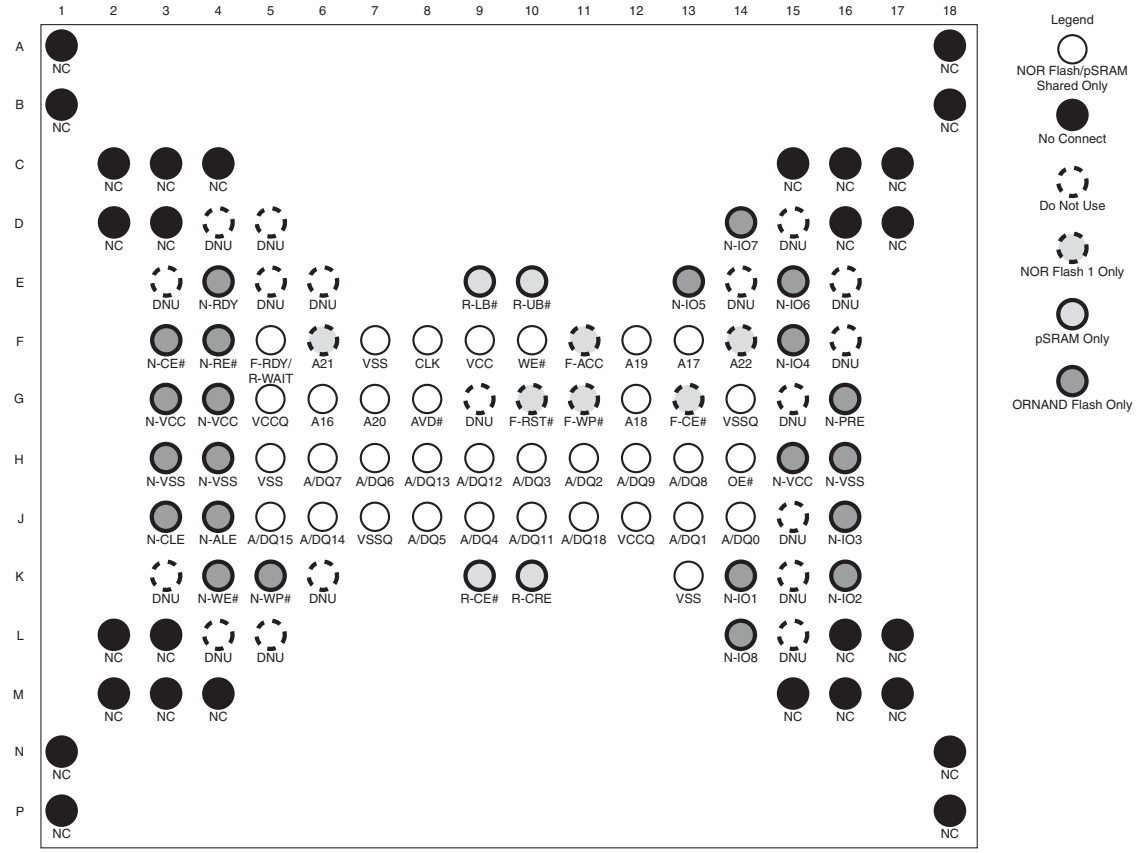
This section contains the I/O designations and package specifications for the S71NS-N.

4.1 Special Handling Instructions for FBGA Packages

Special handling is required for Flash Memory products in FBGA packages.

Flash memory devices in FBGA packages may be damaged if exposed to ultrasonic cleaning methods. The package and/or data integrity may be compromised if the package body is exposed to temperatures above 150°C for prolonged periods of time.

4.2 Connection Diagrams

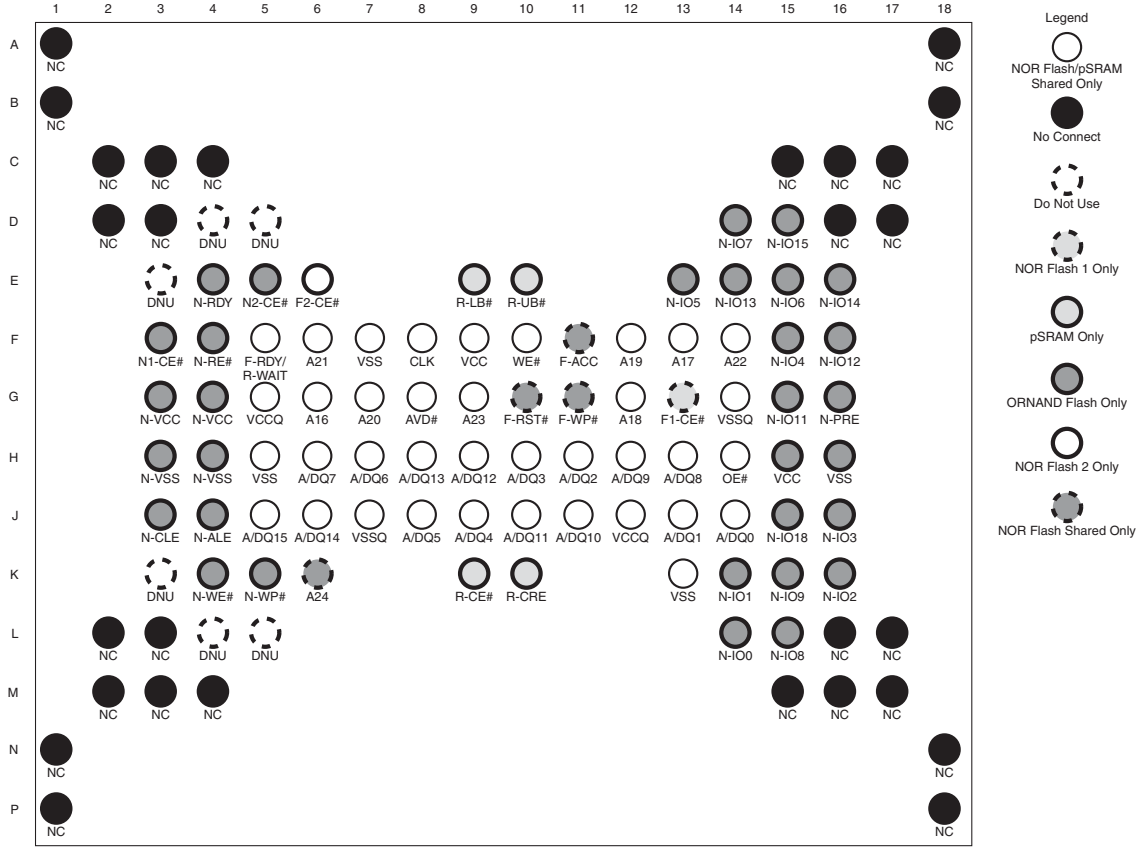


Note:
Addresses are shared between Flash and RAM depending on the density of the pSRAM.

MCP	Flash-Only Addresses	Shared Addresses	Shared ADQ Pins
S75NS128NBG	A22-A21	A20-A16	ADQ15 – ADQ0
S75NS128NBF	A22-A21	A20-A16	ADQ15 – ADQ0

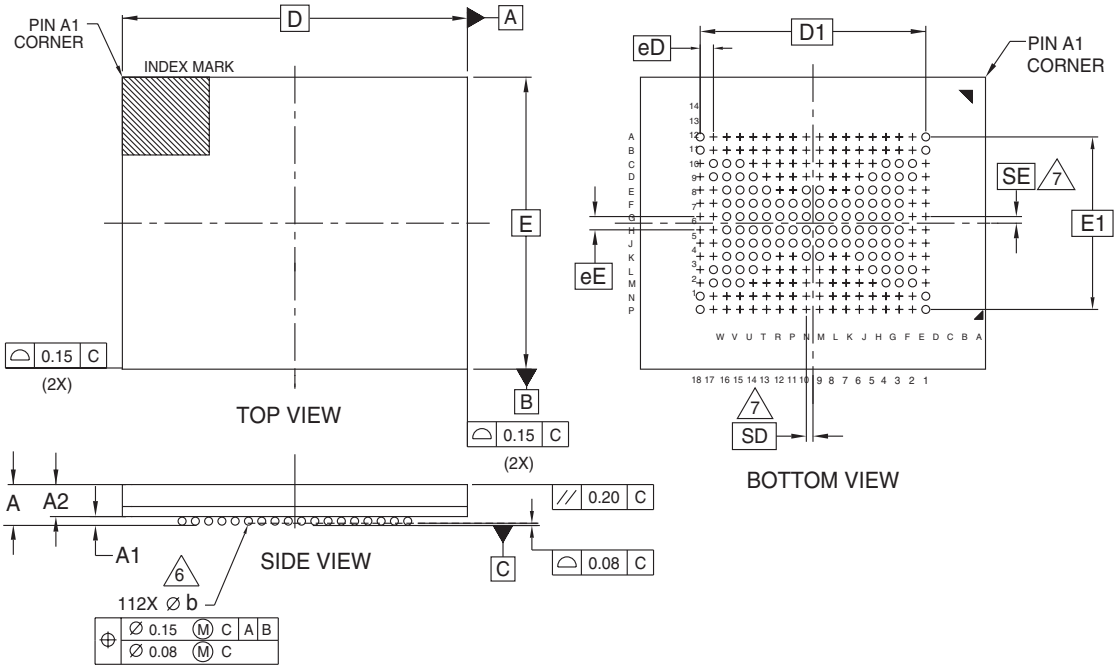
4.2.1 Lookahead Connection Diagram

Figure 4.1 112-ball x16 MUX NOR FLASH (Bus 1) + x16 MUX pSRAM (Bus 1) + x8/x16 ORNAND (Bus2)



4.3 Physical Dimensions

Figure 4.2 MMB112—11 x 13 mm, 112-ball VFBGA



PACKAGE	MMB 112			
JEDEC	N/A			
D x E	13.00 mm x 11.00 mm PACKAGE			
SYMBOL	MIN	NOM	MAX	NOTE
A	---	---	1.40	PROFILE
A1	0.20	---	---	BALL HEIGHT
A2	0.94	---	1.11	BODY THICKNESS
D	13.00 BSC			BODY SIZE
E	11.00 BSC			BODY SIZE
D1	8.50 BSC			MATRIX FOOTPRINT
E1	6.50 BSC			MATRIX FOOTPRINT
MD	18			MATRIX SIZE D DIRECTION
ME	14			MATRIX SIZE E DIRECTION
n	112			BALL COUNT
Øb	0.25	0.30	0.35	BALL DIAMETER
eE	0.50 BSC			BALL PITCH
eD	0.50 BSC			BALL PITCH
SD / SE	0.25 BSC			SOLDER BALL PLACEMENT
	1C~1M,2A,2B,2E~2K,3A,3B,3N,3P,4A,4B,4N, 4P,5A,5B, 5C,5M,5N,5P,6A~6D,6L~6P,7A~7E, 8A~8E,8K~8P,9A~9D,9L~9P,10A~10D, 10L~10P,11A~11E,11K~11P,12A~12E, 12K~12P,13A~13D,13L~13P,14A~14C, 14M~14P,15A,15B,15N,15P,16A,16B, 16N,16P,17A,17B,17N,17P,18C~18M			DEPOPULATED SOLDER BALLS

NOTES:

1. DIMENSIONING AND TOLERANCING METHODS PER ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. BALL POSITION DESIGNATION PER JEP95, SECTION 4.3, SPP-010.
4. e REPRESENTS THE SOLDER BALL GRID PITCH.
5. SYMBOL "MD" IS THE BALL MATRIX SIZE IN THE "D" DIRECTION.

   SYMBOL "ME" IS THE BALL MATRIX SIZE IN THE "E" DIRECTION.

   n IS THE NUMBER OF POPULTED SOLDER BALL POSITIONS FOR MATRIX SIZE MD X ME.

6. DIMENSION "b" IS MEASURED AT THE MAXIMUM BALL DIAMETER IN A PLANE PARALLEL TO DATUM C.
7. SD AND SE ARE MEASURED WITH RESPECT TO DATUMS A AND B AND DEFINE THE POSITION OF THE CENTER SOLDER BALL IN THE OUTER ROW.

   WHEN THERE IS AN ODD NUMBER OF SOLDER BALLS IN THE OUTER ROW SD OR SE = 0.000.

   WHEN THERE IS AN EVEN NUMBER OF SOLDER BALLS IN THE OUTER ROW, SD OR SE = e/2
8. "+" INDICATES THE THEORETICAL CENTER OF DEPOPULATED BALLS.
9. A1 CORNER TO BE IDENTIFIED BY CHAMFER, LASER OR INK MARK, METALLIZED MARK INDENTATION OR OTHER MEANS.

3558 \ 16-038.29 \ 4.27.6

5. Revision History

5.1 Revision A (May 3, 2006)

Initial release.

Colophon

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