MC74LVX541

Octal Bus Buffer

The MC74LVX541 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining CMOS low power dissipation.

The MC74LVX541 is a noninverting type. When either $\overline{OE1}$ or $\overline{OE2}$ are high, the terminal outputs are in the high impedance state.

The internal circuit is composed of three stages, including a buffer output which provides high noise immunity and stable output. The inputs tolerate voltages up to 7 V, allowing the interface of 5 V systems to 3 V systems.
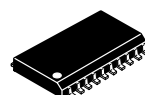
- High Speed: t_{PD} = 5.0 ns (Typ) at V_{CC} = 3.3V
- Low Power Dissipation: I_{CC} = 4 μA (Max) at T_A = 25°C
- High Noise Immunity: V_{NIH} = V_{NIL} = 28% V_{CC}
- Power Down Protection Provided on Inputs
- Balanced Propagation Delays
- Designed for 2 V to 3.6 V Operating Range
- Low Noise: V_{OLP} = 1.2 V (Max)
- Pin and Function Compatible with Other Standard Logic Families
- Latchup Performance Exceeds 300 mA
- ESD Performance: HBM > 2000 V; Machine Model > 200 V
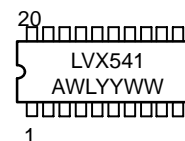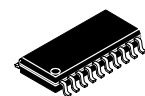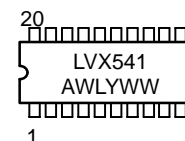- Chip Complexity: 134 FETs or 33.5 Equivalent Gates

MARKING DIAGRAMS

SOIC–20
DW SUFFIX
CASE 751D

```
20
LVX541
AWLYYWW
1
```

TSSOP–20
DT SUFFIX
CASE 948E

```
20
LVX541
AWLYWW
1
```

SOIC EIAJ–20
M SUFFIX
CASE 967

```
20
LVX541
ALYW
1
```
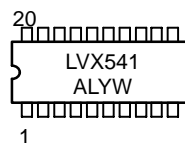
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

A = Assembly Location
WL = Wafer Lot
Y   = Year
WW = Work Week

A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week

ORDERING INFORMATION

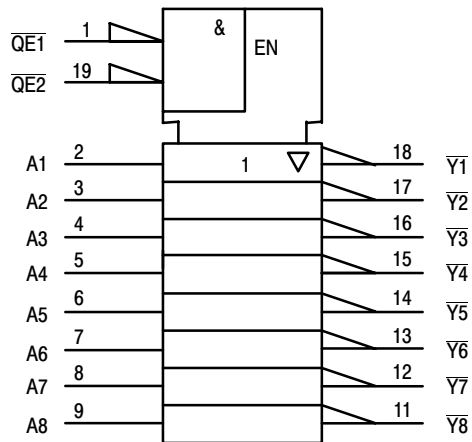| Device	Package	Shipping
MC74LVX541DW	SOIC–20	38 Units/Rail
MC74LVX541DT	TSSOP–20	75 Units/Rail
MC74LVX541DTR2	TSSOP–20	2500 Units/Reel
MC74LVX541M	SOIC EIAJ–20	40 Units/Rail
MC74LVX541MEL	SOIC EIAJ–20	2000 Units/Reel

MC74LVX541

LOGIC DIAGRAM

DATA INPUTS	A1	2		18	Y1	NONINVERTING OUTPUTS
	A2	3		17	Y2	
	A3	4		16	Y3	
	A4	5		15	Y4	
	A5	6		14	Y5	
	A6	7		13	Y6	
	A7	8		12	Y7	
	A8	9		11	Y8	

OUTPUT ENABLES $\overline{OE1}$ 1
$\overline{OE2}$ 19
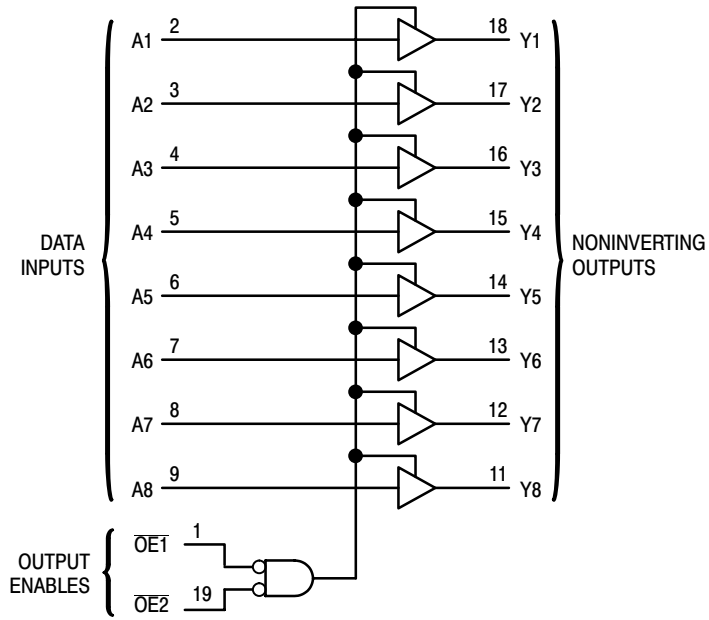
PIN ASSIGNMENT

$\overline{OE1}$	1●		20	V_{CC}
A1	2		19	$\overline{OE2}$
A2	3		18	Y1
A3	4		17	Y2
A4	5		16	Y3
A5	6		15	Y4
A6	7		14	Y5
A7	8		13	Y6
A8	9		12	Y7
GND	10		11	Y8

FUNCTION TABLE

Inputs			Output Y
$\overline{OE1}$	$\overline{OE2}$	A	
L	L	L	L
L	L	H	H
H	X	X	Z
X	H	X	Z

IEC LOGIC DIAGRAM

$\overline{QE1}$ 1
$\overline{QE2}$ 19

& EN

A1	2	1 ▽	18	$\overline{Y1}$
A2	3		17	$\overline{Y2}$
A3	4		16	$\overline{Y3}$
A4	5		15	$\overline{Y4}$
A5	6		14	$\overline{Y5}$
A6	7		13	$\overline{Y6}$
A7	8		12	$\overline{Y7}$
A8	9		11	$\overline{Y8}$

MC74LVX541

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
V_{CC}	DC Supply Voltage	− 0.5 to + 7.0	V
V_{in}	DC Input Voltage	− 0.5 to + 7.0	V
V_{out}	DC Output Voltage	− 0.5 to V_{CC} + 0.5	V
I_{IK}	Input Diode Current	− 20	mA
I_{OK}	Output Diode Current	± 20	mA
I_{out}	DC Output Current, per Pin	± 25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins	± 50	mA
P_D	Power Dissipation in Still Air, SOIC Packages† TSSOP Package†	500 450	mW
T_{stg}	Storage Temperature	− 65 to + 150	°C

* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute–maximum–rated conditions is not implied.

†Derating — SOIC Packages: − 7 mW/°C from 65° to 125°C
                    TSSOP Package: − 6.1 mW/°C from 65° to 125°C

> This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND ≤ (V_{in} or V_{out}) ≤ V_{CC}.
>
> Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	3.6	V
V_{in}	DC Input Voltage		0	5.5	V
V_{out}	DC Output Voltage		0	V_{CC}	V
T_A	Operating Temperature, All Package Types		−40	+ 85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 3.3V ±0.3V	0	100	ns/V

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V_{CC} V	T_A = 25°C Min	T_A = 25°C Typ	T_A = 25°C Max	T_A = − 40 to 85°C Min	T_A = − 40 to 85°C Max	Unit
V_{IH}	Minimum High–Level Input Voltage		2.0 3.0 3.6	1.50 2.0 2.4			1.50 2.0 2.4		V
V_{IL}	Maximum Low–Level Input Voltage		2.0 3.0 3.6			0.50 0.80 0.80		0.50 0.80 0.80	V
V_{OH}	Minimum High–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OH} = − 50 μA I_{OH} = − 50 μA I_{OH} = − 4 mA	2.0 3.0 3.0	1.9 2.9 2.58	2.0 3.0		1.9 2.9 2.48		V
V_{OL}	Maximum Low–Level Output Voltage V_{in} = V_{IH} or V_{IL}	I_{OL} = 50 μA I_{OL} = 50 μA I_{OL} = 4 mA	2.0 3.0 3.0		0.0 0.0	0.1 0.1 0.36		0.1 0.1 0.44	V

MC74LVX541

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Test Conditions	V$_{CC}$ V	T$_A$ = 25°C			T$_A$ = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
I$_{in}$	Maximum Input Leakage Current	V$_{in}$ = 5.5 V or GND	0 to 3.6			±0.1		±1.0	µA
I$_{OZ}$	Maximum Three–State Leakage Current	V$_{in}$ = V$_{IL}$ or V$_{IH}$ V$_{out}$ = V$_{CC}$ or GND	3.6			±0.25		±2.5	µA
I$_{CC}$	Maximum Quiescent Supply Current	V$_{in}$ = V$_{CC}$ or GND	3.6			4.0		40.0	µA

AC ELECTRICAL CHARACTERISTICS (Input t$_r$ = t$_f$ = 3.0 ns)

Symbol	Parameter	Test Conditions		T$_A$ = 25°C			T$_A$ = – 40 to 85°C		Unit
				Min	Typ	Max	Min	Max	
t$_{PLH}$, t$_{PHL}$	Maximum Propagation Delay, A to Y	V$_{CC}$ = 2.7 V	C$_L$ = 15 pF C$_L$ = 50 pF		5.0 7.5	7.0 10.5	1.0 1.0	8.5 12.0	ns
		V$_{CC}$ = 3.3 ± 0.3 V	C$_L$ = 15 pF C$_L$ = 50 pF		3.5 5.0	5.0 7.0	1.0 1.0	6.0 8.0	
t$_{PZL}$, t$_{PZH}$	Output Enable TIme, $\overline{OE}$ to Y	V$_{CC}$ = 2.7 V R$_L$ = 1 kΩ	C$_L$ = 15 pF C$_L$ = 50 pF		6.8 9.3	10.5 14.0	1.0 1.0	12.5 16.0	ns
		V$_{CC}$ = 3.3 ± 0.3 V R$_L$ = 1 kΩ	C$_L$ = 15 pF C$_L$ = 50 pF		4.7 6.2	7.2 9.2	1.0 1.0	8.5 10.5	
t$_{PLZ}$, t$_{PHZ}$	Output Disable Time, $\overline{OE}$ to Y	V$_{CC}$ = 2.7 V R$_L$ = 1 kΩ	C$_L$ = 50 pF		11.2	15.4	1.0	17.5	ns
		V$_{CC}$ = 3.3 ± 0.3 V R$_L$ = 1 kΩ	C$_L$ = 50 pF		6.0	8.8	1.0	10.0	
t$_{OSLH}$, t$_{OSHL}$	Output to Output Skew	V$_{CC}$ = 2.7 V (Note 1)	C$_L$ = 50 pF			1.5		1.5	ns
		V$_{CC}$ = 3.3 ± 0.3 V (Note 1)	C$_L$ = 50 pF			1.0		1.0	ns
C$_{in}$	Maximum Input Capacitance				4.0	10		10	pF
C$_{out}$	Maximum Three–State Output Capacitance (Output in High Impedance State)				6.0				pF

		Typical @ 25°C, V$_{CC}$ = 5.0V	
C$_{PD}$	Power Dissipation Capacitance (Note 2)	18	pF

1. Parameter guaranteed by design. t$_{OSLH}$ = |t$_{PLHm}$ − t$_{PLHn}$|, t$_{OSHL}$ = |t$_{PHLm}$ − t$_{PHLn}$|.
2. C$_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I$_{CC(OPR)}$ = C$_{PD}$ • V$_{CC}$ • f$_{in}$ + I$_{CC}$/8 (per bit). C$_{PD}$ is used to determine the no–load dynamic power consumption; P$_D$ = C$_{PD}$ • V$_{CC}^2$ • f$_{in}$ + I$_{CC}$ • V$_{CC}$.

NOISE CHARACTERISTICS (Input t$_r$ = t$_f$ = 3.0 ns, C$_L$ = 50 pF, V$_{CC}$ = 3.3 V)

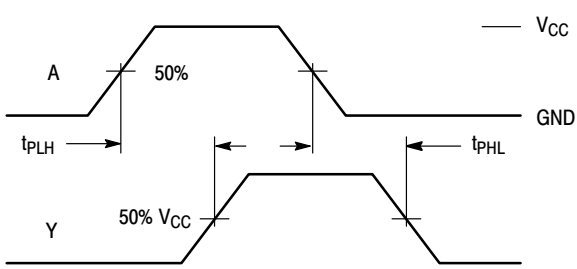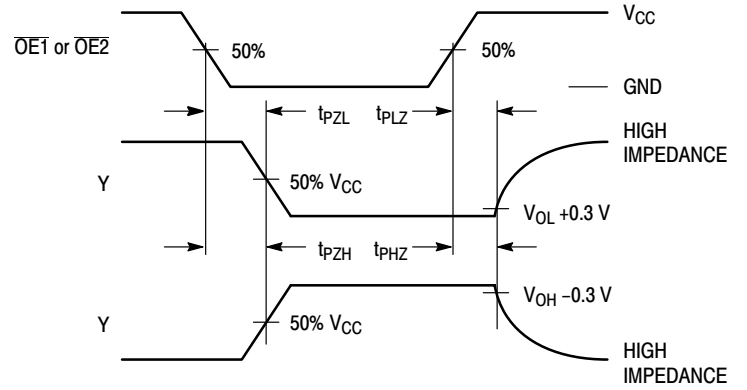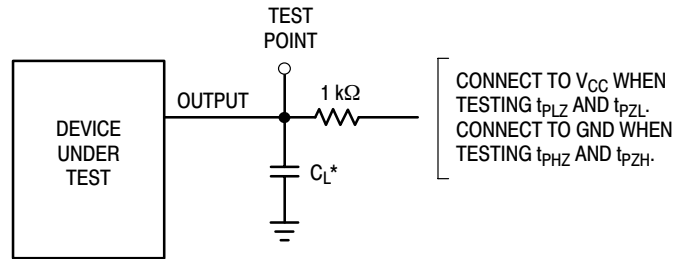| Symbol	Parameter	T$_A$ = 25°C		Unit
		Typ	Max	
V$_{OLP}$	Quiet Output Maximum Dynamic V$_{OL}$	0.5	0.8	V
V$_{OLV}$	Quiet Output Minimum Dynamic V$_{OL}$	−0.5	−0.8	V
V$_{IHD}$	Minimum High Level Dynamic Input Voltage		2.0	V
V$_{ILD}$	Maximum Low Level Dynamic Input Voltage		0.8	V

MC74LVX541

SWITCHING WAVEFORMS

Figure 1.

Figure 2.

TEST CIRCUITS
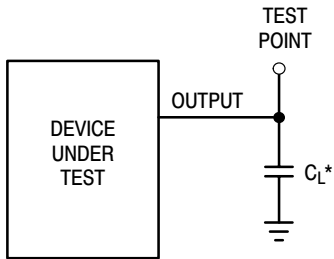
*Includes all probe and jig capacitance

Figure 3.

CONNECT TO V_{CC} WHEN TESTING t_{PLZ} AND t_{PZL}. CONNECT TO GND WHEN TESTING t_{PHZ} AND t_{PZH}.
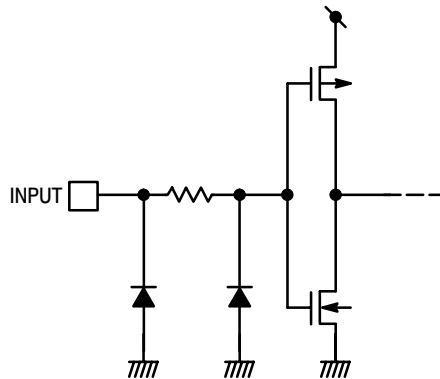
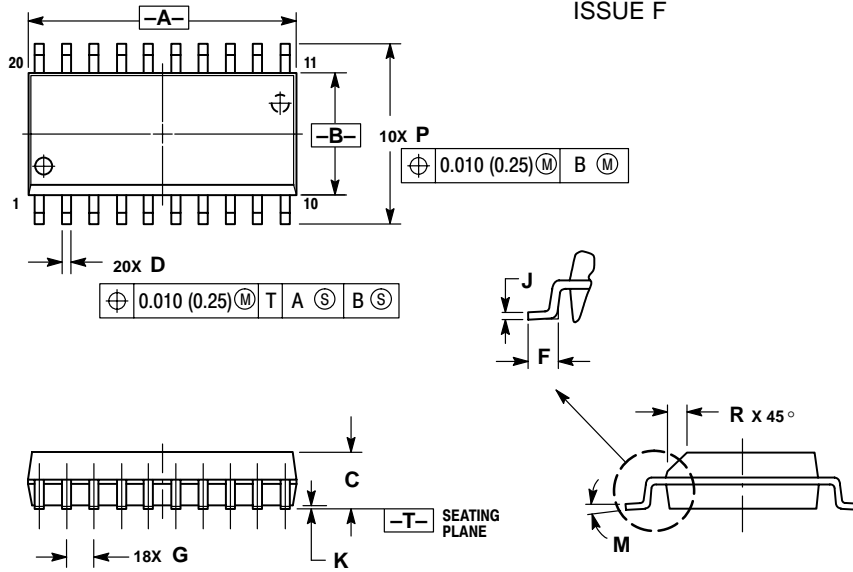*Includes all probe and jig capacitance

Figure 4.

INPUT EQUIVALENT CIRCUIT

MC74LVX541

PACKAGE DIMENSIONS

SOIC–20
DW SUFFIX
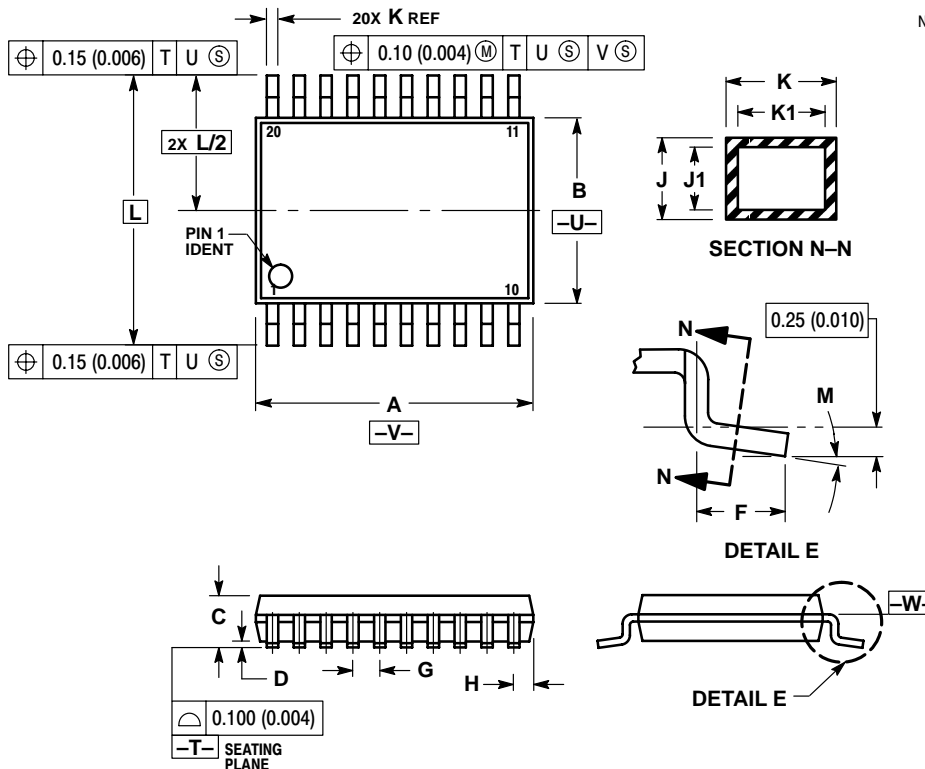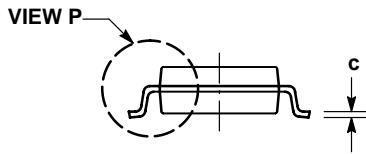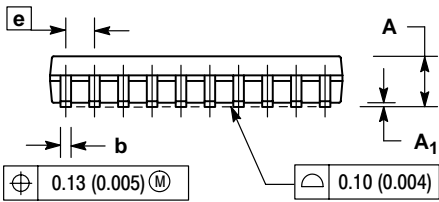PLASTIC SOIC WIDE PACKAGE
CASE 751D–05
ISSUE F

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.150 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	12.65	12.95	0.499	0.510
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
J	0.25	0.32	0.010	0.012
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

TSSOP–20
DT SUFFIX
PLASTIC TSSOP PACKAGE
CASE 948E–02
ISSUE A

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE –W–.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	6.40	6.60	0.252	0.260
B	4.30	4.50	0.169	0.177
C	–––	1.20	–––	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.27	0.37	0.011	0.015
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

SECTION N–N

DETAIL E

PACKAGE DIMENSIONS

SOIC EIAJ–20
M SUFFIX
PLASTIC SOIC EIAJ PACKAGE
CASE 967–01
ISSUE O
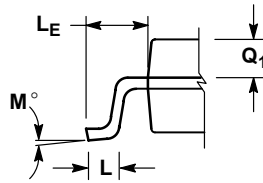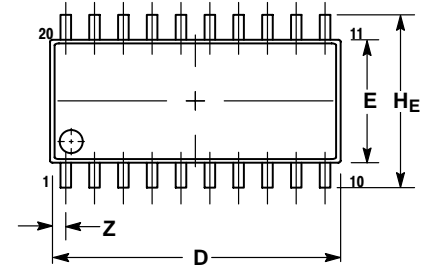
NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DETAIL P

VIEW P

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A_1	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.18	0.27	0.007	0.011
D	12.35	12.80	0.486	0.504
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H_E	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
L_E	1.10	1.50	0.043	0.059
M	0 °	10 °	0 °	10 °
Q_1	0.70	0.90	0.028	0.035
Z	---	0.81	---	0.032

⊕ 0.13 (0.005) Ⓜ

⌓ 0.10 (0.004)

MC74LVX541

PUBLICATION ORDERING INFORMATION