

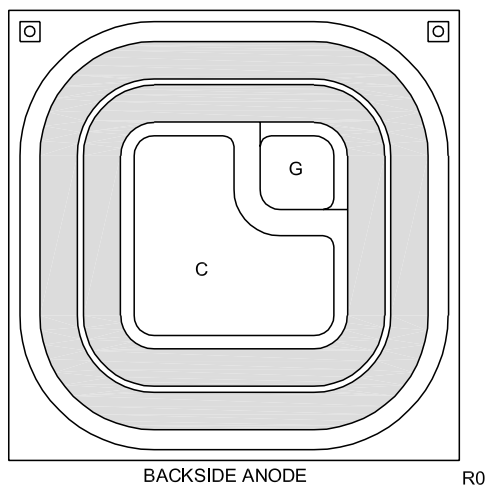
PROCESS CPS041
Silicon Controlled Rectifier
Sensitive Gate SCR Chip

CentralTM
Semiconductor Corp.

PROCESS DETAILS

Process	GLASS PASSIVATED MESA
Die Size	41 x 41 MILS
Die Thickness	8.7 MILS $\pm$ 0.6 MILS
Cathode Bonding Pad Area	18 x 8 MILS
Gate Bonding Pad Area	7.1 x 7.1 MILS
Top Side Metalization	Al - 45,000Å
Back Side Metalization	Au - 10,000Å

GEOMETRY



GROSS DIE PER 4 INCH WAFER

6,474

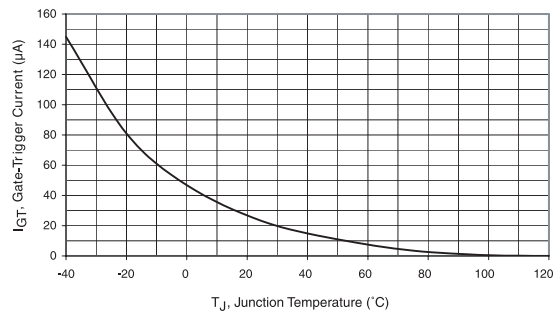
PRINCIPAL DEVICE TYPES

CS18D
BRX49
CS92D
CS89M

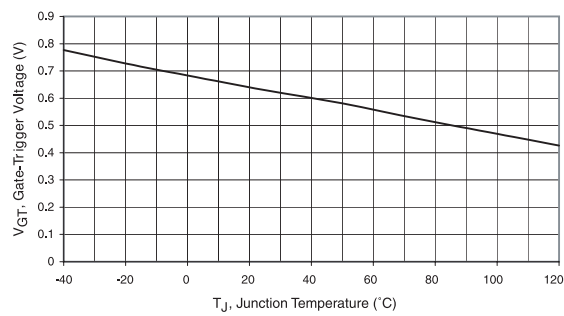
145 Adams Avenue
Hauppauge, NY 11788 USA
Tel: (631) 435-1110
Fax: (631) 435-1824
www.centralsemi.com

R1 (19 -May 2005)

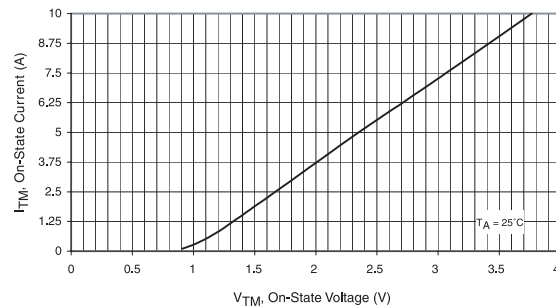
Typical Gate-Trigger Current



Typical Gate-Trigger Voltage



Typical On-State Voltage



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