

**CMLDM7002A
CMLDM7002AJ
SURFACE MOUNT PICOmini™
DUAL N-CHANNEL
ENHANCEMENT-MODE
SILICON MOSFET**

PICOmini™



SOT-563 CASE

**Central™
Semiconductor Corp.**

DESCRIPTION:

The CENTRAL SEMICONDUCTOR CMLDM7002A and CMLDM7002AJ are special dual versions of the 2N7002 Enhancement-mode N-Channel Field Effect Transistor, manufactured by the N-Channel DMOS Process, designed for high speed pulsed amplifier and driver applications. The CMLDM7002A utilizes the USA pinout configuration, while the CMLDM7002AJ utilizes the Japanese pinout configuration. These special Dual Transistor devices offer low $r_{DS(ON)}$ and low $V_{DS(ON)}$.

**MARKING CODE: CMLDM7002A: L02
CMLDM7002AJ: 02J**

MAXIMUM RATINGS ($T_A=25^\circ\text{C}$)

	SYMBOL		UNITS
Drain-Source Voltage	V_{DS}	60	V
Drain-Gate Voltage	V_{DG}	60	V
Gate-Source Voltage	V_{GS}	40	V
Continuous Drain Current	I_D	280	mA
Continuous Source Current (Body Diode)	I_S	280	mA
Maximum Pulsed Drain Current	I_{DM}	1.5	A
Maximum Pulsed Source Current	I_{SM}	1.5	A
Power Dissipation	P_D	350	mW (Note 1)
Power Dissipation	P_D	300	mW (Note 2)
Power Dissipation	P_D	150	mW (Note 3)
Operating and Storage			
Junction Temperature	T_J, T_{stg}	-65 to +150	$^\circ\text{C}$
Thermal Resistance	θ_{JA}	357	$^\circ\text{C/W}$

ELECTRICAL CHARACTERISTICS PER TRANSISTOR ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
I_{GSSF}	$V_{GS}=20\text{V}, V_{DS}=0\text{V}$		100	nA
I_{GSSR}	$V_{GS}=20\text{V}, V_{DS}=0\text{V}$		100	nA
I_{DSS}	$V_{DS}=60\text{V}, V_{GS}=0\text{V}$		1.0	μA
I_{DSS}	$V_{DS}=60\text{V}, V_{GS}=0\text{V}, T_J=125^\circ\text{C}$		500	μA
$I_{D(ON)}$	$V_{GS}=10\text{V}, V_{DS} \geq 2V_{DS(ON)}$	500		mA
BV_{DSS}	$V_{GS}=0\text{V}, I_D=10\mu\text{A}$	60		V
$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu\text{A}$	1.0	2.5	V
$V_{DS(ON)}$	$V_{GS}=10\text{V}, I_D=500\text{mA}$		1.0	V
$V_{DS(ON)}$	$V_{GS}=5.0\text{V}, I_D=50\text{mA}$		0.15	V
$r_{DS(ON)}$	$V_{GS}=10\text{V}, I_D=500\text{mA}$		2.0	Ω
$r_{DS(ON)}$	$V_{GS}=10\text{V}, I_D=500\text{mA}, T_J=125^\circ\text{C}$		3.5	Ω
$r_{DS(ON)}$	$V_{GS}=5.0\text{V}, I_D=50\text{mA}$		3.0	Ω
$r_{DS(ON)}$	$V_{GS}=5.0\text{V}, I_D=50\text{mA}, T_J=125^\circ\text{C}$		5.0	Ω
gFS	$V_{DS} \geq 2V_{DS(ON)}, I_D=200\text{mA}$	80		mmhos

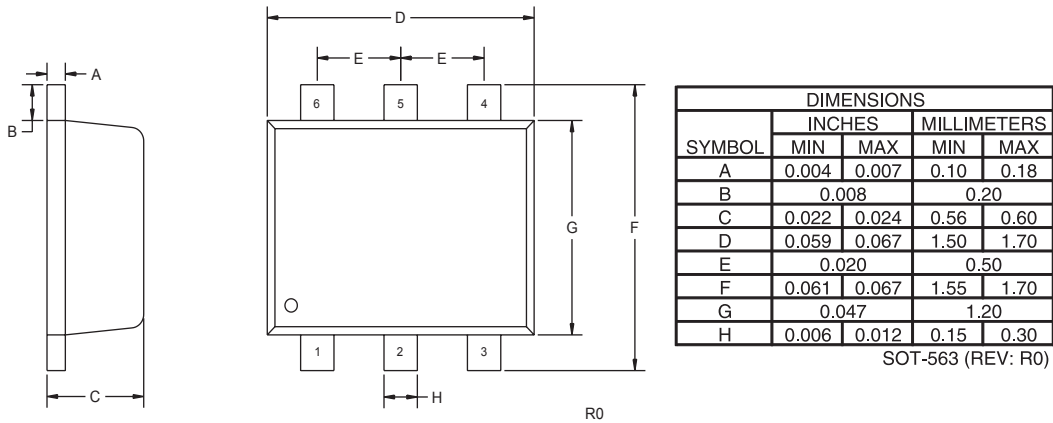
Notes: (1) Ceramic or aluminum core PC Board with copper mounting pad area of 4.0 mm²
 (2) FR-4 Epoxy PC Board with copper mounting pad area of 4.0 mm²
 (3) FR-4 Epoxy PC Board with copper mounting pad area of 1.4 mm²

R3 (19-December 2003)

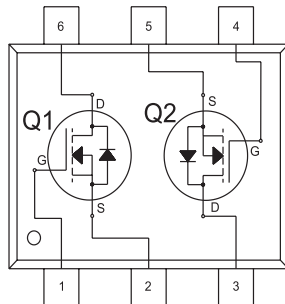
ELECTRICAL CHARACTERISTICS PER TRANSISTOR - Continued ($T_A=25^\circ\text{C}$ unless otherwise noted)

SYMBOL	TEST CONDITIONS	MIN	MAX	UNITS
C_{rss}	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$		5.0	pF
C_{iss}	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$		50	pF
C_{oss}	$V_{DS}=25\text{V}, V_{GS}=0, f=1.0\text{MHz}$		25	pF
t_{on}	$V_{DD}=30\text{V}, V_{GS}=10\text{V}, I_D=200\text{mA}$		20	ns
t_{off}	$R_G=25\Omega, R_L=150\Omega$		20	ns
V_{SD}	$V_{GS}=0\text{V}, I_S=400\text{mA}$		1.2	V

SOT-563 CASE - MECHANICAL OUTLINE



CMLDM7002A (USA Pinout)

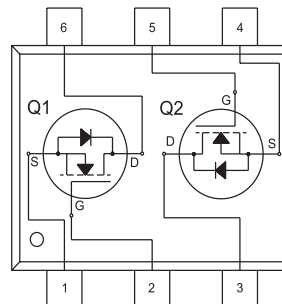


LEAD CODE:

- 1) GATE Q1
- 2) SOURCE Q1
- 3) DRAIN Q2
- 4) GATE Q2
- 5) SOURCE Q2
- 6) DRAIN Q1

MARKING CODE: L02

CMLDM7002AJ (Japanese Pinout)



LEAD CODE:

- 1) SOURCE Q1
- 2) GATE Q1
- 3) DRAIN Q2
- 4) SOURCE Q2
- 5) GATE Q2
- 6) DRAIN Q1

MARKING CODE: 02J