GENERAL DESCRIPTION

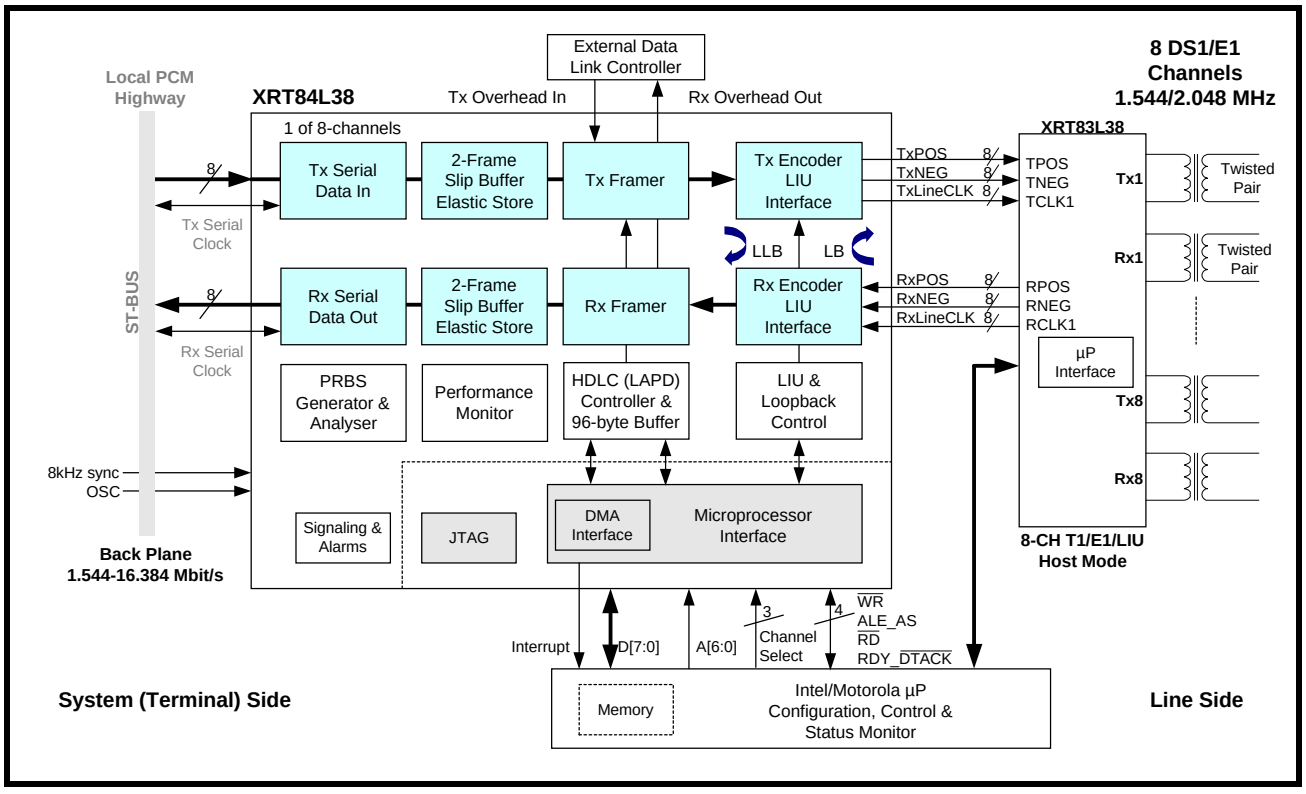
The XRT84L38 is an eight-channel 1.544 Mbit/s or 2.048 Mbit/s DS1/E1/J1 framing controller. The XRT84L38 contains an integrated DS1/E1/J1 framer which provides DS1/E1/J1 framing and error accumulation in accordance with ANSI/ITU_T specifications. Each framer has its own framing synchronizer and transmit-receive slip buffers, and can be independently enabled or disabled as required and can be configured to frame to the common DS1/E1/J1 signal formats

Each Framer block contains its own Transmit and Receive T1/E1/J1 Framing function including 3 HDLC controllers to support V5.2. Each Transmit HDLC controller encapsulates contents of the Transmit HDLC buffers into LAPD Message frames. Each Receive HDLC controller extracts payload content of Receive LAPD Message frames from the incoming T1/E1/J1 data stream and writes it into the Receive HDLC buffer. Each framer also contains a Transmit and Overhead Data Input port, which permits Data Link Terminal Equipment direct access to the outbound T1/E1/J1 frames Likewise, a Receive Overhead output data port permits Data Link Terminal Equipment direct access to the Data Link bits of the inbound T1/E1/J1 frames.

The XRT84L38 fully meets all of the latest T1/E1/J1 specifications: ANSI T1/E1.107-1988, ANSI T1/E1.403-1995, ANSI T1/E1.231-1993, ANSI T1/E1.408-1990, AT&T TR 62411 (12-90) TR54016, and ITU G-703, G.704, G706 and G.733, AT&T Pub. 43801, and ETS 300 011, 300 233, JT G.703, JT G.704, JT G706, I.431. Extensive test and diagnostic functions include Loop-backs, Boundary scan, Pseudo Random bit sequence (PRBS) test pattern generation, Performance Monitor, Bit Error Rate (BER) meter, forced error insertion, and LAPD unchannelized data payload processing according to ITU-T standard Q.921.

Applications and Features (next page)

FIGURE 1. XRT84L38 8-CHANNEL DS1 (T1/E1/J1) FRAMER



APPLICATIONS

- High-Density T1/E1/J1 interfaces for Multiplexers, Switches, LAN Routers and Digital Modems
- SONET/SDH terminal or Add/Drop multiplexers (ADMs)
- T1/E1/J1 add/drop multiplexers (MUX)
- Channel Service Units (CSUs): T1/E1/J1 and Fractional T1/E1/J1
- Digital Access Cross-connect System (DACs)
- Digital Cross-connect Systems (DCS)
- Frame Relay Switches and Access Devices (FRADS)
- ISDN Primary Rate Interfaces (PRA)
- PBXs and PCM channel bank
- T3 channelized access concentrators and M13 MUX
- Wireless base stations
- ATM equipment with integrated DS1 interfaces
- Multichannel DS1 Test Equipment
- T1/E1/J1 Performance Monitoring
- Voice over packet gateways
- Routers

FEATURES

- Eight independent, full duplex DS1 Tx and Rx Framers
- Two 512-bit (two-frame) elastic store, PCM frame slip buffers (FIFO) on TX and Rx provide up to 8.192 MHz asynchronous back plane connections with jitter and wander attenuation
- Supports input PCM and signaling data at 1.544, 2.048, 4.096 and 8.192 Mbits. Also supports 4-channel multiplexed 12.352/16.384 (HMVIP/H.100) Mbit/s on the back plane bus
- Programmable output clocks for Fractional T1/E1/J1
- Supports Channel Associated Signaling (CAS)
- Supports Common Channel Signalling (CCS)
- Supports ISDN Primary Rate Interface (ISDN PRI) signaling
- Extracts and inserts robbed bit signaling (RBS)
- 3 independent HDLC Controllers for Receive and Transmit on a per channel basis
- Each HDLC controller contains two 96-BYTE buffers
- Timeslot assignable HDLC
- V5.1 and V5.2 Interface
- 8-bit Intel/Motorola µP and MIPS Power PC interfaces for configuration, control and status monitoring
- Parallel search algorithm for fast frame synchronization
- Wide choice of T1 framing structures: D4, ESF, SLC®96, TIDM and N-Frame (non-framing)
- Direct access to D and E channels for fast transmission of data link information
- PRBS and QRSS generation and detection
- Programmable Interrupt output pin
- Supports programmed I/O, Burst and DMA modes of Read-Write access
- Each framer block encodes and decodes the T1/E1/J1 Frame serial data into and from the Single-rail or Dual-rail (B8ZS) format
- Dual or single rail line side digital PCM inputs
- Detects and forces Red (SAI), Yellow (RAI) and Blue (AIS) Alarms
- Detects OOF, LOF, LOS errors and COFA conditions
- Loopbacks: Local (LLB) and Line remote (LB)
- Facilitates Inverse Multiplexing for ATM
- Performance monitor with one second polling
- Boundary scan (IEEE 1149.1) JTAG test port
- Accepts external 8kHz Sync reference
- 3.3V CMOS operation with 5V tolerant inputs
- 388-pin BGA package with –40°C to +85°C operation
- Direct Interface to Exar's XRT83L38 (Octal) LIU

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT84L38IB	388 Pin Plastic Ball Grid Array	-40°C to +85°C

FIGURE 2. PIN OUT OF THE XRT84L38 TOP VIEW (SEE PIN LIST FOR NAMES AND FUNCTION)

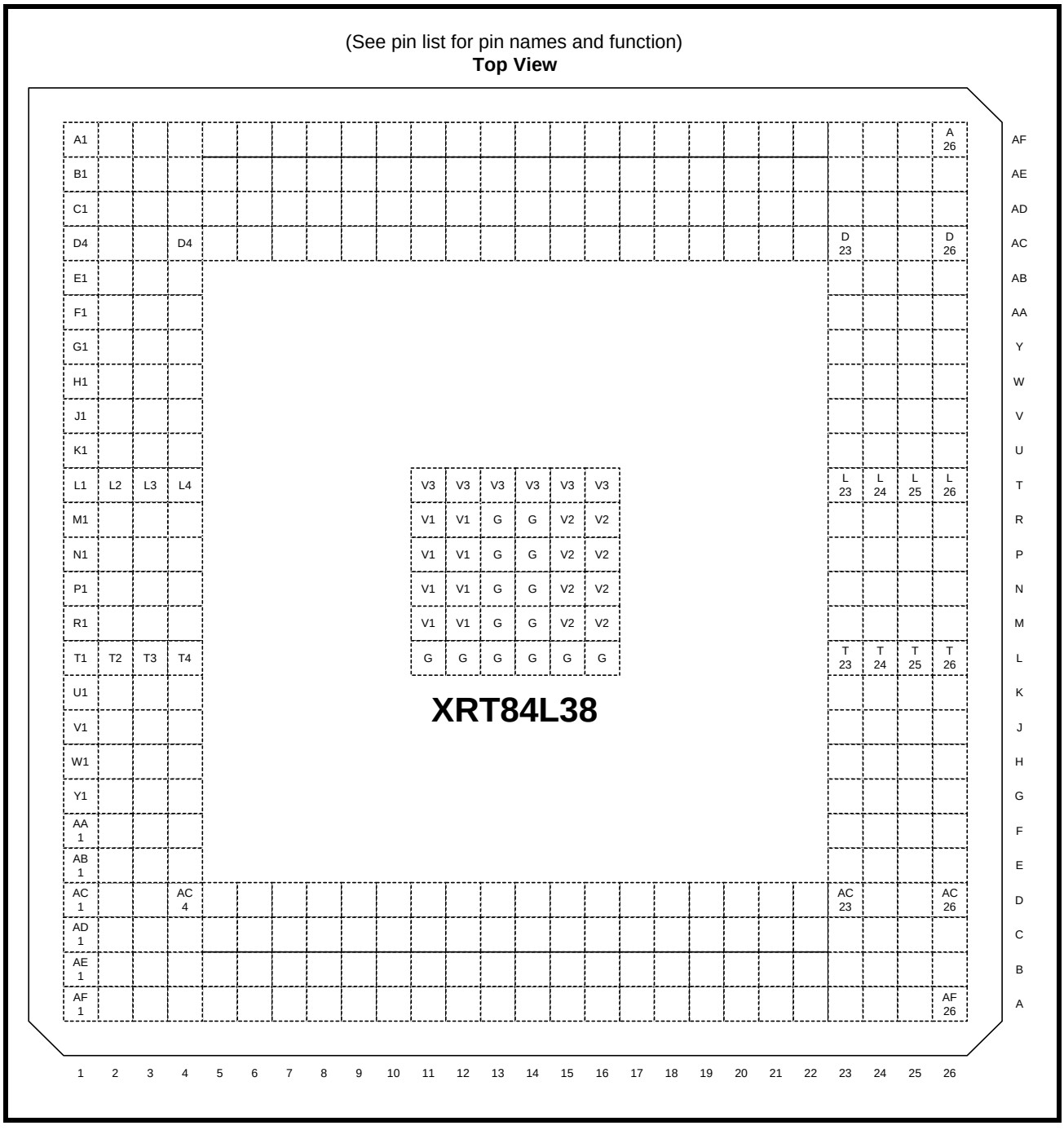


TABLE OF CONTENTS

TABLE 1: LIST BY PIN NUMBER

PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME
A1	TCK	B1	TDI	C1	RxNEG_0	D1	RxLineClk_0
A2	RxTSb0_0 RxSig_0	B2	RxSerClk_0	C2	TMS	D2	RxLOS_0
A3	RxSync_0	B3	RxMSync_0 RxCRCMSync_0	C3	TRST	D3	TDO
A4	RxCASMSync_0	B4	RxTSb2_0 RxTSChn_0	C4	RxTSClk_0	D4	RxSer_0
A5	TxOHClk_0	B5	RxTSb3_0 Rx8kHz_0	C5	RxOHClk_0	D5	RxTSb1_0 RxFrTD_0
A6	NC	B6	TxSer_0	C6	TxMSync_0 TxInClk_0	D6	TxSync_0
A7	TxOH_0	B7	NC	C7	RxOH_0	D7	RxTSb4_0
A8	TxTSb2_0 Tx12.352MHz_0	B8	TxTSb3_0 TxOHSync_0	C8	TxTSb0_0 TxSig_0	D8	TxSerClk_0
A9	RxSer_1	B9	RxSerClk_1	C9	RxMSync_1 RxCRCMSync_1	D9	TxTSb1_0 TxFrTD_0
A10	RxTSb1_1 RxFrTD_1	B10	RxOH_1	C10	TxTSb4_0	D10	TxTSClk_0
A11	RxCASMSync_1	B11	RxSync_1	C11	RxTSb2_1 RxTSChn_1	D11	RxTSClk_1
A12	TxSync_1	B12	RxOHClk_1	C12	NC	D12	RxTSb0_1 RxSig_1
A13	RxTSb4_1	B13	TxMSync_1 TxInClk_1	C13	NC	D13	RxTSb3_1 Rx8kHz_1
A14	TxSer_1	B14	TxTSClk_1	C14	TxOH_1	D14	NC
A15	TxTSb2_1 Tx12.352MHz_1	B15	TxTSb1_1 TxFrTD_1	C15	TxOHClk_1	D15	TxTSb0_1 TxSig_1
A16	TxSerClk_1	B16	RxSync_2	C16	NC	D16	TxTSb3_1 TxOHSync_1
A17	RxSerClk_2	B17	NC	C17	TxTSb4_1	D17	NC
A18	RxTSb0_2 RxSig_2	B18	RxCASMSync_2	C18	RxSer_2	D18	RxTSClk_2
A19	RxMSync_2 RxCRCMSync_2	B19	RxTSb1_2 RxFrTD_2	C19	RxOH_2	D19	RxOHClk_2
A20	NC	B20	RxTSb2_2 RxTSChn_2	C20	RxTSb3_2 Rx8kHz_2	D20	TxSerClk_2
A21	TxSync_2	B21	RxTSb4_2	C21	TxTSClk_2	D21	TxOHClk_2
A22	TxMSync_2 TxInClk_2	B22	TxSer_2	C22	TxTSb1_2 TxFrTD_2	D22	TxTSb4_2
A23	TxTSb0_2 TxSig_2	B23	TxTSb2_2 Tx12.352MHz_2	C23	NC	D23	TxOH_2
A24	TxTSb3_2 TxOHSync_2	B24	RxSer_3	C24	RxSync_3	D24	RxCASMSync_3
A25	RxTSClk_3	B25	RxOHClk_3	C25	RxTSb0_3 RxSig_3	D25	TxTSClk_3
A26	RxMSync_3 RxCRCMSync_3	B26	RxOH_3	C26	RxTSb1_3 RxFrTD_3	D26	RxTSb3_3 Rx8kHz_3

PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME
E1	NC	F1	RxNEG_1	G1	RxLineClk_1	H1	RxPOS_2
E2	NC	F2	TxLineClk_0	G2	TxLineClk_1	H2	TxNEG_1 TxMX_1
E3	TxPOS_0 TxNRZ_0	F3	TxNEG_0 TxMX_0	G3	RxPOS_1	H3	TxPOS_1 TxNRZ_1
E4	RxPOS_0	F4	NC	G4	LOS_0	H4	RxLOS_1
E23	RxSerClk_3	F23	TxOH_3	G23	TxSerClk_3	H23	TxTSb1_3 TxFrTD_3
E24	RxTSb2_3 RxTSChn_3	F24	TxOHClk_3	G24	TxTSb0_3 TxSig_3	H24	TxTSb3_3 TxOHSync_3
E25	TxSync_3	F25	TxSer_3	G25	$\overline{CS}$	H25	NC
E26	RxTSb4_3	F26	TxMSync_3 TxInClk_3	G26	$\overline{WR}$	H26	NC

PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME
J1	RxLOS_2	K1	LOS_2	L1	TxPOS_3 TxNRZ_3	M1	GPO3 $\overline{CS}$0
J2	TxLineClk_2	K2	TxNEG_2 TxMX_2	L2	RxPOS_3	M2	LOS_3
J3	RxNEG_2	K3	TxPOS_2 TxNRZ_2	L3	RxNEG_3	M3	TxNEG_3 TxMX_3
J4	LOS_1	K4	RxLineClk_2	L4	RxLOS_3	M4	RxLineClk_3
				L11	VDD	M11	VDD
				L12	VDD	M12	VDD
				L13	VDD	M13	VSS
				L14	VDD	M14	VSS
				L15	VDD	M15	VDD
				L16	VDD	M16	VDD
J23	TxTSb2_3 Tx12.352MHz_3	K23	A6	L23	A4	M23	NC
J24	Data7	K24	Data6	L24	Data4	M24	$\overline{INT}$
J25	TxTSb4_3	K25	Data5	L25	$\overline{Blast}$	M25	µPType2
J26	A5	K26	NC	L26	A3	M26	A2

PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME
N1	GPO0 SDO0	P1	GPO7 $\overline{CS1}$	R1	GPO4 SDO1	T1	OSCClk
N2	GPO2 SClk0	P2	GPO6 SClk1	R2	RxPOS_4	T2	RxNEG_4
N3	GPO1 SDI0	P3	Test Mode	R3	$\overline{Reset}$	T3	RxLineClk_4
N4	TxLineClk_3	P4	GPO5 SDI1	R4	LOP	T4	TxPOS_4 TxNRZ_4
N11	VDD			R11	VDD	T11	VSS
N12	VDD			R12	VDD	T12	VSS
N13	VSS	P13	VSS	R13	VSS	T13	VSS
N14	VSS	P14	VSS	R14	VSS	T14	VSS
N15	VDD			R15	VDD	T15	VSS
N16	VDD			R16	VDD	T16	VSS
N23	A1	P23	RDY_$\overline{DTACK}$	R23	µPClk	T23	$\overline{ACK1}$
N24	ALE_AS	P24	µPType1	R24	Data0	T24	Indirect
N25	Data3	P25	$\overline{DBEn}$	R25	Data1	T25	µPType0
N26	Data2	P26	A0	R26	$\overline{RD}$	T26	$\overline{Req0}$

PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME
U1	RxLOS_4	V1	TxNEG_4 TxMX_4	W1	RxNEG_5	Y1	RxLOS_5
U2	8kHzRef	V2	LOS_4	W2	RxPOS_5	Y2	TxNEG_5 TxMX_5
U3	NC	V3	NC	W3	TxPOS_5 TxNRZ_5	Y3	TxLineClk_5
U4	NC	V4	TxLineClk_4	W4	RxLineClk_5	Y4	NC
U23	$\overline{Req1}$	V23	RxOHClk_4	W23	RxTSb3_4 Rx8kHz_4	Y23	TxSerClk_4
U24	RxSerClk_4	V24	RxTSClk_4	W24	RxTSb0_4 RxSig_4	Y24	RxCASMSync_4
U25	NC	V25	RxMSync_4 RxCRCMSync_4	W25	RxOH_4	Y25	RxTSb2_4 RxTSChn_4
U26	$\overline{ACK0}$	V26	RxSync_4	W26	RxSer_4	Y26	RxTSb1_4 RxFrTD_4

PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME	PIN	PIN NAME
AA1	LOS_5	AB1	RxNEG_6	AC1	TxNEG_6 TxMX_6	AD1	RxNEG_7
AA2	RxPOS_6	AB2	TxPOS_6 TxNRZ_6	AC2	RxPOS_7	AD2	TxPOS_7 TxNRZ_7
AA3	RxLOS_6	AB3	LOS_6	AC3	TxLineClk_6		
AA4	RxLineClk_6	AB4	RxLOS_7	AC4	TxLineClk_7		
				AC5	TxTSClk_7	AD5	TxOH_7
				AC6	TxSerClk_7	AD6	TxTSb1_7 TxFrTD_7
				AC7	TxTSb0_7 TxSig_7	AD7	RxSerClk_7
				AC8	RxMSync_7 RxCRCMSync_7	AD8	RxSer_7
				AC9	RxTSClk_7	AD9	TxSerClk_6
				AC10	RxCASMSync_7	AD10	RxOHClk_7
				AC11	RxOH_7	AD11	TxTSb4_6
				AC12	TxTSb3_6 TxOHSync_6	AD12	RxCASMSync_6
				AC13	TxTSb0_6 TxSig_6	AD13	TxOHClk_6
				AC14	TxOH_6	AD14	RxSync_6
				AC15	RxTSb4_6	AD15	RxSerClk_6
				AC16	RxTSb0_6 RxSig_6	AD16	RxTSb2_6 RxTSChn_6
				AC17	TxOH_5	AD17	RxOHClk_6
				AC18	TxSerClk_5	AD18	TxTSb3_5 TxOHSync_5
				AC19	TxSync_5	AD19	TxSer_5
				AC20	RxOH_5	AD20	TxOHClk_5
				AC21	RxTSb1_5 RxFrTD_5	AD21	RxTSb4_5
				AC22	RxSync_5	AD22	RxTSb0_5 RxSig_5
AA23	TxSync_4			AC23	NC	AD23	RxCASMSync_5
AA24	TxOH_4	AB24	TxTSB0_4 TxSig_4	AC24	TxTSb1_4 TxFrTD_4	AD24	RxMSync_5 RxCRCMSync_5
AA25	NC	AB25	TxTSClk_4	AC25	TxOHClk_4	AD25	RxTSClk_5
AA26	RxTSb4_4	AB26	TxSer_4	AC26	TxMSync_4 TxInClk_4	AD26	NC

PIN	PIN NAME	PIN	PIN NAME
AE1	TxNEG_7 TxMX_7	AF1	LOS_7
AE2	RxLineClk_7	AF2	NC
AE3	NC	AF3	TxOHClk_7
AE4	TxTSb4_7	AF4	TxTSb3_7 TxOHSync_7
AE5	TxTSb2_7 Tx12.352MHz_7	AF5	TxSer_7
AE6	TxMSync_7 TxInClk_7	AF6	TxSync_7
AE7	RxSync_7	AF7	RxTSb4_7
AE8	RxTSb3_7 Rx8kHz_7	AF8	RxTSb2_7 RxTSChn_7
AE9	RxTSb1_7 RxFrTD_7	AF9	RxTSb0_7 RxSig_7
AE10	TxSync_6	AF10	TxMSync_6 TxInClk_6
AE11	TxSer_6	AF11	NC
AE12	TxTSb2_6 Tx12.352MHz_6	AF12	TxTSb1_6 TxFrTD_6
AE13	TxTSClk_6	AF13	RxMSync_6 RxCRCMSync_6
AE14	NC	AF14	NC
AE15	NC	AF15	RxTSClk_6
AE16	RxSer_6	AF16	RxTSb3_6 Rx8kHz_6
AE17	NC	AF17	RxTSb1_6 RxFrTD_6
AE18	TxTSb4_5	AF18	RxOH_6
AE19	TxTSb2_5 Tx12.352MHz_5	AF19	TxTSb1_5 TxFrTD_5
AE20	TxTSClk_5	AF20	TxTSb0_5 TxSig_5
AE21	RxOHClk_5	AF21	TxMSync_5 TxInClk_5
AE22	RxTSb3_5 Rx8kHz_5	AF22	NC
AE23	RxSer_5	AF23	RxTSb2_5 RxTSChn_5
AE24	TxTSb4_4	AF24	NC
AE25	NC	AF25	RxSerClk_5
AE26	TxTSb2_4 Tx12.352MHz_4	AF26	TxTSb3_4 TxOHSync_4

PIN DESCRIPTIONS

TRANSMIT SERIAL DATA INPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxSer_0 TxSer_1 TxSer_2 TxSer_3 TxSer_4 TxSer_5 TxSer_6 TxSer_7	B6 A14 B22 F25 AB26 AD19 AE11 AF5	I	**Transmit Serial Data Input—Transmit Framer_n:** This input pin along with TxSerClk_n functions as the Transmit Serial input port for Framer_n. **DS1 Mode:** Any payload data applied to this pin would be inserted into a DS1 frame and output onto the T1 line via the TxPOS_n and TxNEG_n output pins. If Framer_n is configured accordingly, the framing alignment bits, the facility data link bits and the CRC-6 bits can also be inserted to input pin.The signal applied to this input pin can be latched to the Transmit Payload Data Input Interface on either the rising edge or the falling edge of TxSerClk_n according to configurations of Framer_n. **E1 Mode:** Any payload data applied to this pin would be inserted into an E1 frame and output onto the E1 line via the TxPOS_n and TxNEG_n output pins. All data intended to be transported via Time Slots 1 through 15 and Time slots 17 through 31, within each E1 frame, must be applied to this input pin. If Framer_n is configured accordingly, data intended for Time Slots 0 and 16 can also be applied to this input pin.

TRANSMIT SERIAL DATA INPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxSerClk_0 TxSerClk_1 TxSerClk_2 TxSerClk_3 TxSerClk_4 TxSerClk_5 TxSerClk_6 TxSerClk_7	D8 A16 D20 G23 Y23 AC18 AD9 AC6	I or O	**Transmit Serial Clock Signal --Transmit Framer_n:** This clock signal is used by the Transmit payload data Input Interface, to latch the contents of the TxSer_n signal into the Octal T1/E1/J1 Framer IC. Data that is applied at the TxSer_n input is latched into the Transmit payload data Input Interface (for Framer_n) on either the rising edge or the falling edge of TxSerClk_n depending on configurations of Framer_n. TxSerClk_n can either be an input or an output. **DS1 Mode:** **Transmit Back-plane Interface-1.544 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 00 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 1.544 Mbit/s. If the Transmit Section of Framer_n has been configured to use the TxSerClk_n signal as the timing source, then this signal will be an **Input**. If the Transmit Section of Framer_n has been configured to use either the RxLineClk_n signal or the OSCClk signal as the timing source, then TxSerClk_n will be an **Output**. **Transmit Back-plane Interface-High Speed Clock Mode** If TxMUXEN ≠ 0 and TxIMODE[1:0] ≠ 00 in Transmit interface control register, Transmit back-plane interface of Framer_n is operating at a high-speed mode and is taking data at rates of 2.048 Mbit/s, 4.096 Mbit/s, 8.192 Mbit/s, 12.352 Mbit/s or 16.384 Mbit/s. The TxSerClk_n signal will be an Input clock signal running at 1.544 MHz. **E1 Mode:** **Transmit Back-plane Interface-2.048 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 00 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 2.048 Mbit/s. If the Transmit Section of Framer_n has been configured to use the TxSerClk_n signal as the timing source, then this signal will be an **Input**. If the Transmit Section of Framer_n has been configured to use either the RxLineClk_n signal or the OSCClk signal as the timing source, then TxSerClk_n will be an **Output**. **Transmit Back-plane Interface-High Speed Clock Mode** If TxMUXEN ≠ 0 or TxIMODE[1:0] ≠ 00 in Transmit interface control register, Transmit back-plane interface of Framer_n is operating at a high-speed mode. The TxSerClk_n signal will be an Input clock signal running at 2.048 MHz.

TRANSMIT SERIAL DATA INPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxSync_0 TxSync_1 TxSync_2 TxSync_3 TxSync_4 TxSync_5 TxSync_6 TxSync_7	D6 A12 A21 E25 AA23 AC19 AE10 AF6	I or O	**Single Frame Sync Pulse Input/Output—Transmit Framer_n:** This pin is configured to be an **input** if the TxSerClk_n input pin is configured to be the timing reference for the Transmit Portion of Framer_n. This pin is configured as an **output** if the RxLineClk_n input pin or the OSCClk input pins are configured to be the timing reference for the Transmit portion of Framer_n. **DS1 Mode:** **When pin is configured to be an Input** If this pin is configured to be an **input**, then the user must pulse this pin "High" for one period of TxSerClk_n, when the Transmit payload data Input Interface (of Framer_n) is processing the first bit (F-bit) of an outbound DS1 frame. ***NOTE:*** *It is imperative that the TxSync_n input signal be synchronized with the TxSerClk_n input signal.* **When pin is configured to be an Output** If this pin is configured to be an **output**, then it will pulse "High", for one period of TxSerClk_n, when the Transmit payload data Input Interface (of Framer_n) is processing the last payload bit within an outbound DS1 frame. **E1 Mode:** **When pin is configured to be an Input** If this pin is configured to be an **input**, then the user must pulse this pin "High" for one period of TxSerClk_n, when the Transmit payload data Input Interface (of Framer_n) is processing the International Bit (Si) of an outbound E1 frame. ***NOTE:*** *It is imperative that the TxSync_n input signal be synchronized with the TxSerClk_n input signal.* **When pin is configured to be an Output** If this pin is configured to be an **output**, then it will pulse "High", for one period of TxSerClk_n, when the Transmit payload data Input Interface (of Framer_n) is processing the last bit within a given outbound E1 frame.

TRANSMIT SERIAL DATA INPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxMSync_0 TxMSync_1 TxMSync_2 TxMSync_3 TxMSync_4 TxMSync_5 TxMSync_6 TxMSync_7	C6 B13 A22 F26 AC26 AF21 AF10 AE6	I or O	**Multiframe Sync Pulse Input/Output—Framer_n:** This signal indicates the boundary of an outbound multi-frame. **DS1 Mode:** **Transmit Back-plane Interface-1.544 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 00 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 1.544 Mbit/s. This pin is configured to be an **Input** if the TxSerClk_n input pin is configured to be the timing reference for the Transmit section of Framer_n. Conversely, this pin will be configured as an **Output** if the RxLineClk input pin or the OSCClk input pins are configured to be the timing reference for the Transmit section of Framer_n.The roles of these pins when configured as input or output, is described below. **When pin is configured to be an Input** If this pin is configured to be an **input**, this pin must be pulsed "High" for one period of TxSerClk_n, the instant that the Transmit payload data Interface (of Framer_n) is processing the first bit of a DS1 Multi-frame. ***NOTE:*** *It is imperative that the TxMSync_n input signal be synchronized with the TxSerClk_n input signal.* **When pin is configured to be an Output** If this pin is configured to be an **output**, then it will pulse "High", for one period of TxSerClk_n, when the Transmit payload data Input Interface (of Framer_n) is processing the last bit of a DS1 Multi-frame. **E1 Mode:** **Transmit Back-plane Interface-2.048 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 00 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 2.048 Mbit/s. This pin is configured to be an **Input** if the TxSerClk_n input pin is configured to be the timing reference for the Transmit section of Framer_n. Conversely, this pin will be configured as an **Output** if the RxLineClk input pin or the OSCClk input pins are configured to be the timing reference for the Transmit section of Framer_n. **When pin is configured to be an Input** If this pin is configured to be an input, this pin must be pulsed "High" for one period of TxSerClk_n, the instant that the Transmit payload data Interface (of Framer_n) is processing the first International Bit (Si) of an "outbound" CRC payload data Multiframe. ***NOTES:*** *1. This pin is ignored if CRC Multiframe Alignment has been disabled.* *2. It is imperative that the TxMSync_n input signal be synchronized with the TxSerClk_n input signal.* **When pin is configured to be an Output** If this pin is configured to be an output, then it will pulse "High", for one period of TxSerClk_n, when the Transmit payload data Input Interface (of Framer_n) is processing the last bit, within an "outbound" CRC Multi-frame. ***NOTES:*** *1. This pin is inactive if CRC Multi-frame Alignment has been disabled.* *2. The purpose of this output pin is to permit the Terminal Equipment to maintain alignment with the "outbound" CRC-Multi-frame structure.*

TRANSMIT SERIAL DATA INPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxInClk_0 TxInClk_1 TxInClk_2 TxInClk_3 TxInClk_4 TxInClk_5 TxInClk_6 TxInClk_7	C6 B13 A22 F26 AC26 AF21 AF10 AE6	I	**Transmit Input Clock Signal -- Transmit Framer _n** If TxMUXEN ≠ 0 or TxIMODE[1:0] ≠ 00 in Transmit interface control register, Transmit back-plane interface of Framer_n is operating at a high-speed mode. This pin will function as an input clock signal for the high-speed Transmit back-plane interface. **DS1 Mode:** **Transmit Back-plane Interface-MVIP, 2.048 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 01 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 2.048 Mbit/s. The TxInClk_n signal will be an Input clock signal running at 2.048 MHz. **Transmit Back-plane Interface-4.096 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 10 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 4.096 Mbit/s. The TxInClk_n signal will be an Input clock signal running at 4.096 MHz. **Transmit Back-plane Interface-8.192 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 11 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 8.192 Mbit/s. The TxInClk_n signal will be an Input clock signal running at 8.192 MHz. **Transmit Back-plane Interface-Multiplexed at 12.352 MHz Clock Mode** If TxMUXEN = 1 and TxIMODE[1:0] = 00 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking multiplexed data at a rate of 12.352 Mbit/s. TxInClk_0 and TxInClk_4 signals will be Input clock signals running at 12.352 MHz. TxInClk_1, 2, 3 and TxInClk_5, 6, 7 signals are not required. Transmit Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_0 via TxSer_0 input pin. Transmit Payload data of Channel 4, 5, 6 and 7 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_4 via TxSer_4 input pin. Inside the Octal Framer, data will be de-multiplexed into 8 channels from the serial inputs of Channel 0 and 4. **Transmit Back-plane Interface-Multiplexed at 16.384 MHz Clock Mode** If TxMUXEN = 1 and TxIMODE[1:0] = 01 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking multiplexed data at a rate of 16.384 Mbit/s. TxInClk_0 and TxInClk_4 signals will be Input clock signals running at 16.384 MHz. TxInClk_1, 2, 3 and TxInClk_5, 6, 7 signals are not required. Transmit Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_0 via TxSer_0 input pin. Transmit Payload data of Channel 4, 5, 6 and 7 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_4 via TxSer_4 input pin. Inside the Octal Framer, data will be de-multiplexed into 8 channels from the serial inputs of Channel 0 and 4. **Transmit Back-plane Interface-HMVIP, 16.384 MHz Clock Mode** If TxMUXEN = 1 and TxIMODE[1:0] = 10 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking multiplexed data at a rate of 16.384 Mbit/s. TxInClk_0 and TxInClk_4 signals will be Input clock signals running at 16.384 MHz. TxInClk_1, 2, 3 and TxInClk_5, 6, 7 signals are not required. Transmit Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_0 via TxSer_0 input pin. Transmit Payload data of Channel 4, 5, 6 and 7 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_4 via TxSer_4 input pin. Inside the Octal Framer, data will be de-multiplexed into 8 channels from the serial inputs of Channel 0 and 4.

TRANSMIT SERIAL DATA INPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxInClk_0 TxInClk_1 TxInClk_2 TxInClk_3 TxInClk_4 TxInClk_5 TxInClk_6 TxInClk_7	C6 B13 A22 F26 AC26 AF21 AF10 AE6	I	**Transmit Input Clock Signal -- Transmit Framer _n (continued)** **Transmit Back-plane Interface-H.100, 16.384 MHz Clock Mode** If TxMUXEN = 1 and TxIMODE[1:0] = 11 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking multiplexed data at a rate of 16.384 Mbit/s. TxInClk_0 and TxInClk_4 signals will be Input clock signals running at 16.384 MHz. TxInClk_1, 2, 3 and TxInClk_5, 6, 7 signals are not required. Transmit Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_0 via TxSer_0 input pin. Transmit Payload data of Channel 4, 5, 6 and 7 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_4 via TxSer_4 input pin. Inside the Octal Framer, data will be de-multiplexed into 8 channels from the serial inputs of Channel 0 and 4. **E1 Mode:** **Transmit Back-plane Interface-2.048 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 01 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 2.048 Mbit/s. The TxInClk_n signal will be an Input clock signal running at 2.048 MHz. **Transmit Back-plane Interface-4.096 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 10 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 4.096 Mbit/s. The TxInClk_n signal will be an Input clock signal running at 4.096 MHz. **Transmit Back-plane Interface-8.192 MHz Clock Mode** If TxMUXEN = 0 and TxIMODE[1:0] = 11 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking data at a rate of 8.192 Mbit/s. The TxInClk_n signal will be an Input clock signal running at 8.192 MHz. **Transmit Back-plane Interface-Multiplexed at 16.384 MHz Clock Mode** If TxMUXEN = 1 and TxIMODE[1:0] = 01 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking multiplexed data at a rate of 16.384 Mbit/s. TxInClk_0 and TxInClk_4 signals will be Input clock signals running at 16.384 MHz. TxInClk_1, 2, 3 and TxInClk_5, 6, 7 signals are not required. Transmit Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_0 via TxSer_0 input pin. Transmit Payload data of Channel 4, 5, 6 and 7 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_4 via TxSer_4 input pin. Inside the Octal Framer, data will be de-multiplexed into 8 channels from the serial inputs of Channel 0 and 4. **Transmit Back-plane Interface-HMVIP, 16.384 MHz Clock Mode** If TxMUXEN = 1 and TxIMODE[1:0] = 10 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking multiplexed data at a rate of 16.384 Mbit/s. TxInClk_0 and TxInClk_4 signals will be Input clock signals running at 16.384 MHz. TxInClk_1, 2, 3 and TxInClk_5, 6, 7 signals are not required. Transmit Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_0 via TxSer_0 input pin. Transmit Payload data of Channel 4, 5, 6 and 7 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_4 via TxSer_4 input pin. Inside the Octal Framer, data will be de-multiplexed into 8 channels from the serial inputs of Channel 0 and 4.

TRANSMIT SERIAL DATA INPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxInClk_0 TxInClk_1 TxInClk_2 TxInClk_3 TxInClk_4 TxInClk_5 TxInClk_6 TxInClk_7	C6 B13 A22 F26 AC26 AF21 AF10 AE6	I	**Transmit Input Clock Signal -- Transmit Framer _n (continued)** **Transmit Back-plane Interface-H.100, 16.384 MHz Clock Mode** If TxMUXEN = 1 and TxIMODE[1:0] = 11 in Transmit interface control register, Transmit back-plane interface of Framer_n is taking multiplexed data at a rate of 16.384 Mbit/s. TxInClk_0 and TxInClk_4 signals will be Input clock signals running at 16.384 MHz. TxInClk_1, 2, 3 and TxInClk_5, 6, 7 signals are not required. Transmit Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_0 via TxSer_0 input pin. Transmit Payload data of Channel 4, 5, 6 and 7 are multiplexed and latched into Transmit back-plane interface using clock edge of TxInClk_4 via TxSer_4 input pin. Inside the Octal Framer, data will be de-multiplexed into 8 channels from the serial inputs of Channel 0 and 4.
TxTSb0_0 TxTSb0_1 TxTSb0_2 TxTSb0_3 TxTSb0_4 TxTSb0_5 TxTSb0_6 TxTSb0_7	C8 D15 A23 G24 AB24 AF20 AC13 AC7	O	**Transmit Framer_n--Time Slot Octet Identifier Output-Bit [0:4]:** These output signals (TxTSb4_n through TxTSb0_n) reflects the five-bit binary value of the number of Time Slot (in the incoming DS1 frame), being accepted and processed by the Transmit Payload Data Input Interface block associated with Framer_n. Terminal Equipment should use the TxTSClk_n clock signal to sample the five output pins of each channel in order to identify the time-slot being processed by the Transmit Payload Data Input Interface block of Framer_n.
TxSig_0 TxSig_1 TxSig_2 TxSig_3 TxSig_4 TxSig_5 TxSig_6 TxSig_7	C8 D15 A23 G24 AB24 AF20 AC13 AC7	I	**Transmit Serial Signaling Input--Transmit Framer_n** These pins can be used to input robbed-bit signaling data within an outbound DS1 frame or to input Channel Associated Signaling (CAS) bits within an outbound E1 frame, if Framer_n is configured accordingly.
TxTSb1_0 TxTSb1_1 TxTSb1_2 TxTSb1_3 TxTSb1_4 TxTSb1_5 TxTSb1_6 TxTSb1_7	D9 B15 C22 H23 AC24 AF19 AF12 AD6	O	**Transmit Framer_n--Time Slot Octet Identifier Output-Bit 1:** These output signals (TxTSb4_n through TxTSb0_n) reflects the five-bit binary value of the number of Time Slot (in the incoming DS1 frame), being accepted and processed by the Transmit Payload Data Input Interface block associated with Framer_n. Terminal Equipment should use the TxTSClk_n clock signal to sample the five output pins of each channel in order to identify the time-slot being processed by the Transmit Payload Data Input Interface block of Framer_n.
TxFrTD_0 TxFrTD_1 TxFrTD_2 TxFrTD_3 TxFrTD_4 TxFrTD_5 TxFrTD_6 TxFrTD_7	D9 B15 C22 H23 AC24 AF19 AF12 AD6	I	**Transmit Serial Fractional T1/E1 Input--Transmit Framer_n** These pins can be used to input fractional DS1/E1 payload data within an outbound DS1/E1 frame, if Framer_n is configured accordingly. In this mode, terminal equipment will use either TxTSClk_n or TxSerClk_n output pins to clock out fractional DS1/E1 payload data. Framer_n will then use TxTSClk_n or TxSerClk_n to clock in fractional DS1/E1 payload data. Please see pin description of TxTSClk_n for details.

TRANSMIT SERIAL DATA INPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxTSb2_0 TxTSb2_1 TxTSb2_2 TxTSb2_3 TxTSb2_4 TxTSb2_5 TxTSb2_6 TxTSb2_7	A8 A15 B23 J23 AE26 AE19 AE12 AE5	O	**Transmit Framer_n--Time Slot Octet Identifier Output-Bit 2:** These output signals (TxTSb4_n through TxTSb0_n) reflects the five-bit binary value of the number of Time Slot (in the incoming DS1 frame) being accepted and processed by the Transmit Payload Data Input Interface block associated with Framer_n. Terminal Equipment should use the TxTSClk_n clock signal to sample the five output pins of each channel in order to identify the time-slot being processed by the Transmit Payload Data Input Interface block of Framer_n. If TxTSb1_n pin is configured as TxFrTD_n to input fractional DS1 payload data into Framer_n, the TxTSb2_n pin will serially output the five-bit binary value of the number of the Time Slot being accepted and processed by the Transmit Payload Data Input Interface block associated with Framer_n.
Tx12.352MHz_0 Tx12.352MHz_1 Tx12.352MHz_2 Tx12.352MHz_3 Tx12.352MHz_4 Tx12.352MHz_5 Tx12.352MHz_6 Tx12.352MHz_7	A8 A15 B23 J23 AE26 AE19 AE12 AE5	O	**Transmit 12.352MHz Clock Output-Transmit Framer_n:** These pins can be used to output 12.352MHz clock derived from OSCClk, if Framer_n is configured accordingly.
TxTSb3_0 TxTSb3_1 TxTSb3_2 TxTSb3_3 TxTSb3_4 TxTSb3_5 TxTSb3_6 TxTSb3_7	B8 D16 A24 H24 AF26 AD18 AC12 AF4	O	**Transmit Framer_n-Time Slot Octet Identifier Output-Bit 3:** These output signals (TxTSb4_n through TxTSb0_n) reflects the five-bit binary value of the number of Time Slot (in the incoming DS1 frame) being accepted and processed by the Transmit Payload Data Input Interface block associated with Framer_n. Terminal Equipment should use the TxTSClk_n clock signal to sample the five output pins of each channel in order to identify the time-slot being processed by the Transmit Payload Data Input Interface block of Framer_n.
TxOHSync_0 TxOHSync_1 TxOHSync_2 TxOHSync_3 TxOHSync_4 TxOHSync_5 TxOHSync_6 TxOHSync_7	B8 D16 A24 H24 AF26 AD18 AC12 AF4	O	**Transmit Overhead Synchronization Pulse--Transmit Framer_n:** These pins can be used to output Overhead Synchronization Pulse that indicate the first bit of each multi-frame, if Framer_n is configured accordingly.
TxTSb4_0 TxTSb4_1 TxTSb4_2 TxTSb4_3 TxTSb4_4 TxTSb4_5 TxTSb4_6 TxTSb4_7	C10 C17 D22 J25 AE24 AE18 AD11 AE4	O	**Transmit Framer_n--Time Slot Octet Identifier Output-Bit 4:** These output signals (TxTSb4_n through TxTSb0_n) reflects the five-bit binary value of the number of Time Slot (in the incoming DS1 frame) being accepted and processed by the Transmit Payload Data Input Interface block associated with Framer_n. Terminal Equipment should use the TxTSClk_n clock signal to sample the five output pins of each channel in order to identify the time-slot being processed by the Transmit Payload Data Input Interface block of Framer_n.

TRANSMIT SERIAL DATA INPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxTSClk_0 TxTSClk_1 TxTSClk_2 TxTSClk_3 TxTSClk_4 TxTSClk_5 TxTSClk_6 TxTSClk_7	D10 B14 C21 D25 AB25 AE20 AE13 AC5	O	**Transmit Channel Clock Output Signal—Framer_n:** This pin indicates the boundary of each time slot of an outbound DS1/E1 frame. **DS1 Mode:** Each of these output pins are a 192kHz clock output which pulses "High" whenever the Transmit Payload Data Input Interface block accepts the LSB of each of the 24 time slots, within the DS1 data stream, being processed via Framer _n. The Terminal Equipment should use this clock signal to sample the TxTSb0_n through TxTSb4_n output signals and identify the time-slot being processed via the "Transmit Section" of each Framer_n. If TxTSb1_n pin is configured as TxFrTD_n to input fractional DS1 payload data into Framer_n, the TxTSClk_n pin can be configured to function as one of the following: The pin will output gaped fractional DS1 clock that can be used by terminal equipment to clock out fractional DS1 payload data at rising edge of the clock. Framer_n will then input fractional DS1 payload data using falling edge of the clock.Otherwise, this pin will be a clock enable signal to Transmit fractional DS1 Input (TxFrTD_n) if Framer_n is configured accordingly. In this mode, fractional DS1 payload data is clocked into the chip using un-gaped TxSerClk_n. **E1 Mode:** Each of these output pins are a 256kHz clock output which pulses "High" whenever the Transmit Payload Data Input Interface block accepts the LSB of each of the 32 time slots, within the E1 data stream, being processed via Framer _n. The Terminal Equipment should use this clock signal to sample the TxTSb0_n through TxTSb4_n output signals, and identify the time-slot being processed via the "Transmit Section" of each Framer_n. If TxTSb1_n pin is configured as TxFrTD_n to input fractional E1 payload data into Framer_n, the TxTSClk_n pin can be configured to function as one of the following: The pin will output gaped fractional E1 clock that can be used by terminal equipment to clock out fractional E1 payload data at rising edge of the clock. Framer_n will then input fractional E1 payload data using falling edge of the clock.Otherwise, this pin will be a clock enable signal to Transmit fractional E1 Input (TxFrTD_n) if Framer_n is configured accordingly. In this mode, fractional E1 payload data is clocked into the chip using un-gaped TxSerClk_n.

OVERHEAD INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxOH_0 TxOH_1 TxOH_2 TxOH_3 TxOH_4 TxOH_5 TxOH_6 TxOH_7	A7 C14 D23 F23 AA24 AC17 AC14 AD5	I	**Transmit Overhead Input—Framer_n:** This input pin, along with TxOHClk_n functions as the Transmit Overhead input port for Framer_n. **DS1 Mode:** This input pin will become active if the Transmit Section of Framer_n has been configured to use this input as the source of Facility Data Link bits in ESF framing mode, Fs bits in the SLC96 and N framing mode, and R bit in T1DM mode. The data that is input into this pin will be inserted into the Data Link Bits within the outbound DS1 frames at the falling edge of TxOHClk_n. ***NOTE:*** *This input pin will be disabled if Framer_n is using the Transmit HDLC Controller, or the TxSer_n input as the source for the Data Link Bits.* **E1 Mode:** This input pin will become active if the Transmit Section of Framer_n has been configured to use this input as the source of Data Link bits. The data that is input into this pin will be inserted into the Sa4 through Sa8 bits (the National Bits) within the outbound non-FAS E1 frames. ***NOTE:*** *This input pin will be disabled if Framer_n is using the Transmit HDLC Controller, or the TxSer_n input as the source for the Data Link Bits.*
TxOHClk_0 TxOHClk_1 TxOHClk_2 TxOHClk_3 TxOHClk_4 TxOHClk_5 TxOHClk_6 TxOHClk_7	A5 C15 D21 F24 AC25 AD20 AD13 AF3	O	**Transmit OH Serial Clock Output Signal—Framer_n:** This output clock signal functions as a demand clock signal for the "Transmit Overhead Data Input Interface" block associated with Framer_n. **DS1 Mode:** If the "Transmit Overhead Data Input Interface" has been configured to be the source of Facility Data Link bits in ESF framing mode, Fs bits in the SLC96 and N framing mode, and R bit in T1DM framing mode, then the Transmit Overhead data Input Interface block will provide a clock edge for each Data Link Bit. Data Link Equipment, which is interfaced to this pin, should update its data (on the TxOH_n line) on the rising edge of this clock signal. The Transmit Overhead Data Input Interface will latch the data (on the TxOH_n line) on the falling edge of this clock signal. ***NOTES:*** 1. *If the "Transmit Overhead Data Input Interface" has not been configured to be the source of the Data Link information, then this output signal will be inactive.* 2. *Depending on the configurations of Framer_n, the clock frequency in ESF framing mode can be 2KHz or 4KHz in ESF.* **E1 mode:** If the "Transmit Overhead data Input Interface" has been configured to be the source of Data Link information, then the Transmit Overhead data Input Interface block will provide a clock edge for each "Sa" bit that is carrying data link information. Data Link Equipment, which is interfaced to this pin, should update its data (on the TxOH_n line) on the rising edge of this clock signal. The Transmit Overhead Data Input Interface will latch the data (on the TxOH_n line) on the falling edge of this clock signal. ***NOTE:*** *If the "Transmit Overhead Data Input Interface" has not been configured to be the source of the Data Link information, then this output signal will be inactive.*

OVERHEAD INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxOH_0 RxOH_1 RxOH_2 RxOH_3 RxOH_4 RxOH_5 RxOH_6 RxOH_7	C7 B10 C19 B26 W25 AC20 AF18 AC11	O	**Receive Overhead Output—Framer_n:** This pin, along with RxOHClk_n functions as the Receive Overhead Output Interface for Framer_n. **DS1 Mode:** This pin unconditionally outputs the contents of the Facility Data Link Bit in ESF framing mode, Fs bit in the SLC96 and N framing mode, and R bit in T1DM framing mode. ***NOTE:*** *This output pin is active even if the Receive HDLC Controller (within Framer_n) is active.* **E1 mode:** This pin unconditionally outputs the contents of the National Bits (the "Sa4" through the "Sa8" bits). If Framer_n has been configured to interpret the National bits of the incoming E1 frames as carrying "Data Link" information; then the Receive Overhead Output Interface will provide a clock pulse (via the RxOHClk_n output pin) for each "Sa" bit carrying Data Link information. ***NOTE:*** *This output pin is active even if the Receive HDLC Controller (within Framer_n) is active.*
RxOHClk_0 RxOHClk_1 RxOHClk_2 RxOHClk_3 RxOHClk_4 RxOHClk_5 RxOHClk_6 RxOHClk_7	C5 B12 D19 B25 V23 AE21 AD17 AD10	O	**Receive OH Serial Clock Output Signal—Framer_n:** This pin, along with RxOH_n functions as the Receive Overhead Output Interface for Framer_n. **DS1 Mode:** This pin outputs a clock edge corresponding to each Facility Data Link Bit in ESF framing mode, Fs bit in the SLC96 and N framing mode, and R bit in T1DM framing mode, which carries Data Link information. ***NOTES:*** 1. *Depending on the configurations of Framer_n, the clock frequency in ESF framing mode can be 2KHz or 4KHz.* 2. *This output pin is inactive if the Receive HDLC Controller (within Framer_n) has been enabled.* **E1 mode:** This pin outputs a clock edge corresponding to each National Bit that is carrying "Data Link" information. ***NOTE:*** *This output pin is inactive if the Receive HDLC Controller (within Framer_n) has been enabled.*

RECEIVE SERIAL DATA OUTPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxSync_0 RxSync_1 RxSync_2 RxSync_3 RxSync_4 RxSync_5 RxSync_6 RxSync_7	A3 B11 B16 C24 V26 AC22 AD14 AE7	I or O	**Single Frame Sync Pulse Input/Output pin—Receive Framer_n:** This pin is configured to be an **Input** if the Slip Buffer associated with Framer_n is enabled. Conversely, this pin will be configured to be an **Output** if the Slip-Buffer is by-passed. **DS1 Mode:** **When pin is configured to be an Input** If this pin is configured to be an input, then the user must pulse this pin "High" for one period of RxSerClk_n, when the Receive payload data output Interface (of Framer_n) is processing the first bit (F-bit) of an inbound DS1 frame. ***NOTE:*** *It is imperative that the RxSync_n input signal be synchronized with the RxSerClk_n input signal.* **When pin is configured to be an Output** If this pin is configured to be an output, then it will pulse "High", for one period of RxSerClk_n, when the Receive payload data output Interface (of Framer_n) is processing the first bit (F-bit) of an inbound DS1 frame. **E1 Mode:** **When pin is configured to be an Input** If this pin is configured to be an input, then this pin must be pulsed "High" for one period of RxSerClk_n, when the Receive E1 Serial (or Overhead) Output Interface, outputs the International bit (Si) of an inbound E1 frame. ***NOTE:*** *It is imperative that the RxSync_n input signal be synchronized with the RxSerClk_n input signal.* **When pin is configured to be an Output** If this pin is configured to be an output, then it will pulse "High" for one period of RxSerClk_n, when the Receive E1 Serial (or Overhead) output Interface outputs the last bit, in an inbound E1 frame.
RxMSync_0 RxMSync_1 RxMSync_2 RxMSync_3 RxMSync_4 RxMSync_5 RxMSync_6 RxMSync_7	B3 C9 A19 A26 V25 AD24 AF13 AC8	O	**Multiframe Sync Pulse Output--Receive Framer_n:** This DS1-only signal will pulse "High" for one period of RxSerClk_n, the instant that the Receive payload data Interface (of Framer_n) is processing the first bit of a DS1 Multi-frame.
RxCRCMSync_0 RxCRCMSync_1 RxCRCMSync_2 RxCRCMSync_3 RxCRCMSync_4 RxCRCMSync_5 RxCRCMSync_6 RxCRCMSync_7	B3 C9 A19 A26 V25 AD24 AF13 AC8	O	**Receive "CRC Multiframe" Sync Output signal-Framer_n:** This E1-only signal pulses "High" for one period of RxSerClk_n whenever the Receive E1 Output Interface of Framer_n outputs the first bit, within a given "CRC Multiframe". ***NOTE:*** *This output pin is inactive if CRC Multiframe Alignment is disabled.*

RECEIVE SERIAL DATA OUTPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxSerClk_0 RxSerClk_1 RxSerClk_2 RxSerClk_3 RxSerClk_4 RxSerClk_5 RxSerClk_6 RxSerClk_7	B2 B9 A17 E23 U24 AF25 AD15 AD7	I or O	**Receive Serial Clock Signal—Receive Framer_n:** This signal is used by the Receive payload data output Interface, to latch the contents of the RxSer_n signal out from the Octal T1/E1/J1 Framer IC. Framer_n can use either the rising edge or the falling edge of RxSerClk_n signal to latch the received DS1 payload data out. Depending on configurations of Framer_n. RxSerClk_n can either be an input or an output. **DS1 Mode:** **Receive Back-plane Interface-1.544 MHz Clock Mode** If RxMUXEN = 0 and RxIMODE[1:0] = 00 in Receive interface control register, Receive back-plane interface of Framer_n is presenting data at a rate of 1.544 Mbit/s. This pin is configured to be an Input if the Slip Buffer associated with Framer_n is enabled. Conversely, this pin will be configured to be an Output if the "Slip-Buffer" is "by-passed". **Receive Back-plane Interface-MVIP, 2.048 MHz Clock Mode** If RxMUXEN = 0 and RxIMODE[1:0] = 01 in Receive interface control register, Receive back-plane interface of Framer_n is presenting data at a rate of 2.048 Mbit/s. The RxSerClk_n signal will be an Input clock signal running at 2.048 MHz. **Receive Back-plane Interface-4.096 MHz Clock Mode** If RxMUXEN = 0 and RxIMODE[1:0] = 10 in Receive interface control register, Receive back-plane interface of Framer_n is presenting data at a rate of 4.096 Mbit/s. The RxSerClk_n signal will be an Input clock signal running at 4.096 MHz. **Receive Back-plane Interface-8.192 MHz Clock Mode** If RxMUXEN = 0 and RxIMODE[1:0] = 11 in Receive interface control register, Receive back-plane interface of Framer_n is presenting data at a rate of 8.192 Mbit/s. The RxSerClk_n signal will be an Input clock signal running at 8.192 MHz. **Receive Back-plane Interface-Multiplexed at 12.352 MHz Clock Mode** If RxMUXEN = 1 and RxIMODE[1:0] = 00 in Receive interface control register, Receive back-plane interface of Framer_n is presenting multiplexed data at a rate of 12.352 Mbit/s. RxSerClk_0 and RxSerClk_4 signals will be Input clock signals running at 12.352 MHz. RxSerClk_1, 2, 3 and RxSerClk_5, 6, 7 signals are not required. Received DS1 Payload data of Channel 0, 1, 2 and 3 are multi-plexed and latched out from Receive back-plane interface using clock edge of RxSerClk_0 via RxSer_0 output pin. Receive DS1 Payload data of Channel 4, 5, 6 and 7 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_4 via RxSer_4 output pin.

RECEIVE SERIAL DATA OUTPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxSerClk_0 RxSerClk_1 RxSerClk_2 RxSerClk_3 RxSerClk_4 RxSerClk_5 RxSerClk_6 RxSerClk_7	B2 B9 A17 E23 U24 AF25 AD15 AD7	I or O	**Receive Serial Clock Signal—Receive Framer_n: (Continued)** **Receive Back-plane Interface-Multiplexed at 16.384 MHz Clock Mode** If RxMUXEN = 1 and RxIMODE[1:0] = 01 in Receive interface control register, Receive back-plane interface of Framer_n is presenting multiplexed data at a rate of 16.384 Mbit/s. RxSerClk_0 and RxSerClk_4 signals will be Input clock signals running at 16.384 MHz. RxSerClk_1, 2, 3 and RxSerClk_5, 6, 7 signals are not required. Received DS1 Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_0 via RxSer_0 output pin. Receive DS1 Payload data of Channel 4, 5, 6 and 7 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_4 via RxSer_4 output pin. **Receive Back-plane Interface-HMVIP, 16.384 MHz Clock Mode** If RxMUXEN = 1 and RxIMODE[1:0] = 10 in Receive interface control register, Receive back-plane interface of Framer_n is presenting multiplexed data at a rate of 16.384 Mbit/s. RxSerClk_0 and RxSerClk_4 signals will be Input clock signals running at 16.384 MHz. RxSerClk_1, 2, 3 and RxSerClk_5, 6, 7 signals are not required. Received DS1 Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_0 via RxSer_0 output pin. Receive DS1 Payload data of Channel 4, 5, 6 and 7 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_4 via RxSer_4 output pin. **Receive Back-plane Interface-H.100, 16.384 MHz Clock Mode** If RxMUXEN = 1 and RxIMODE[1:0] = 11 in Receive interface control register, Receive back-plane interface of Framer_n is presenting multiplexed data at a rate of 16.384 Mbit/s. RxSerClk_0 and RxSerClk_4 signals will be Input clock signals running at 16.384 MHz. RxSerClk_1, 2, 3 and RxSerClk_5, 6, 7 signals are not required. Received DS1 Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_0 via RxSer_0 output pin. Receive DS1 Payload data of Channel 4, 5, 6 and 7 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_4 via RxSer_4 output pin. **E1 Mode:** **Receive Back-plane Interface-2.048 MHz (XRT84V24 Compatible) Clock Mode** If RxMUXEN = 0 and RxIMODE[1:0] = 00 in Receive interface control register, Receive back-plane interface of Framer_n is presenting data at a XRT84V24 compatible rate of 2.048 Mbit/s. This pin is configured to be an Input if the Slip Buffer associated with Framer_n is enabled. Conversely, this pin will be configured to be an Output if the "Slip-Buffer" is "by-passed". **Receive Back-plane Interface-2.048 MHz Clock Mode** If RxMUXEN = 0 and RxIMODE[1:0] = 01 in Receive interface control register, Receive back-plane interface of Framer_n is presenting data at a rate of 2.048 Mbit/s. The RxSerClk_n signal will be an Input clock signal running at 2.048 MHz. **Receive Back-plane Interface-4.096 MHz Clock Mode** If RxMUXEN = 0 and RxIMODE[1:0] = 10 in Receive interface control register, Receive back-plane interface of Framer_n is presenting data at a rate of 4.096 Mbit/s. The RxSerClk_n signal will be an Input clock signal running at 4.096 MHz. **Receive Back-plane Interface-8.192 MHz Clock Mode** If RxMUXEN = 0 and RxIMODE[1:0] = 11 in Receive interface control register, Receive back-plane interface of Framer_n is presenting data at a rate of 8.192 Mbit/s. The RxSerClk_n signal will be an Input clock signal running at 8.192 MHz.

RECEIVE SERIAL DATA OUTPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxSerClk_0 RxSerClk_1 RxSerClk_2 RxSerClk_3 RxSerClk_4 RxSerClk_5 RxSerClk_6 RxSerClk_7	B2 B9 A17 E23 U24 AF25 AD15 AD7	I or O	**Receive Serial Clock Signal—Receive Framer_n: (Continued)** **Receive Back-plane Interface-Multiplexed at 16.384 MHz Clock Mode** If RxMUXEN = 1 and RxIMODE[1:0] = 01 in Receive interface control register, Receive back-plane interface of Framer_n is presenting bit-multiplexed data at a rate of 16.384 Mbit/s. RxSerClk_0 and RxSerClk_4 signals will be Input clock signals running at 16.384 MHz. RxSerClk_1, 2, 3 and RxSerClk_5, 6, 7 signals are not required. Received DS1 Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_0 via RxSer_0 output pin. Receive DS1 Payload data of Channel 4, 5, 6 and 7 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_4 via RxSer_4 output pin. **Receive Back-plane Interface-HMVIP, 16.384 MHz Clock Mode** If RxMUXEN = 1 and RxIMODE[1:0] = 10 in Receive interface control register, Receive back-plane interface of Framer_n is presenting multiplexed data at a rate of 16.384 Mbit/s. RxSerClk_0 and RxSerClk_4 signals will be Input clock signals running at 16.384 MHz. RxSerClk_1, 2, 3 and RxSerClk_5, 6, 7 signals are not required. Received DS1 Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_0 via RxSer_0 output pin. Receive DS1 Payload data of Channel 4, 5, 6 and 7 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_4 via RxSer_4 output pin. **Receive Back-plane Interface-H.100, 16.384 MHz Clock Mode** If RxMUXEN = 1 and RxIMODE[1:0] = 11 in Receive interface control register, Receive back-plane interface of Framer_n is presenting multiplexed data at a rate of 16.384 Mbit/s. RxSerClk_0 and RxSerClk_4 signals will be Input clock signals running at 16.384 MHz. RxSerClk_1, 2, 3 and RxSerClk_5, 6, 7 signals are not required. Received DS1 Payload data of Channel 0, 1, 2 and 3 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_0 via RxSer_0 output pin. Receive DS1 Payload data of Channel 4, 5, 6 and 7 are multiplexed and latched out from Receive back-plane interface using clock edge of RxSerClk_4 via RxSer_4 output pin.
RxSer_0 RxSer_1 RxSer_2 RxSer_3 RxSer_4 RxSer_5 RxSer_6 RxSer_7	D4 A9 C18 B24 W26 AE23 AE16 AD8	O	**Receive Serial Data Output—Receive Framer_n:** This output pin along with RxSerClk_n functions as the Receive Serial Output port for Framer_n. **T1 mode:** Any incoming **T1** line data that is received from the RxPOS_n and RxNEG_n input pins, will be decoded and output via this pin.Framer_n can use either the rising edge or the falling edge of RxSerClk_n input pin to latch the received **T1** payload data out according to configurations of Framer_n. **E1 mode:** Much of the data that is received from the line via the RxPOS_n and RxNEG_n input pins, will be decoded and output via this pin, in a binary format.All data that is transported via Time Slots 1 through 15 and Time Slots 17 through 31, within each incoming **E1** frame, will be output via this pin. If Framer_n is configured accordingly, the data for Time Slots 0 and 16 will also be output via this pin. Framer_n can use either the rising edge or the falling edge of RxSerClk_n input pin to latch the received DS1/E1 payload data out according to configurations of Framer_n.

RECEIVE SERIAL DATA OUTPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxTSb0_0 RxTSb0_1 RxTSb0_2 RxTSb0_3 RxTSb0_4 RxTSb0_5 RxTSb0_6 RxTSb0_7	A2 D12 A18 C25 W24 AD22 AC16 AF9	O	**Receive Framer_n--Time Slot Octet Identifier Output-Bit 0:** These output signals (RxTSb4_n through RxTSb0_n) reflect the five-bit binary value of the number of Time Slot (in the incoming DS1 frame) being received and output to the Terminal Equipment via the Receive Payload Data Output Interface block associated with Framer_n. The Terminal Equipment should use the RxTSClk_n clock to sample these five output pins in order to identify the time-slot being processed by the Receive Section of Framer_n.
RxSig_0 RxSig_1 RxSig_2 RxSig_3 RxSig_4 RxSig_5 RxSig_6 RxSig_7	A2 D12 A18 C25 W24 AD22 AC16 AF9	O	**Receive Serial Signaling Output--Receive Framer_n:** These pins can be used to output robbed-bit signaling data extracted from an incoming DS1 frame, if Framer_n is configured accordingly.
RxTSb1_0 RxTSb1_1 RxTSb1_2 RxTSb1_3 RxTSb1_4 RxTSb1_5 RxTSb1_6 RxTSb1_7	D5 A10 B19 C26 Y26 AC21 AF17 AE9	O	**Receive Framer_n--Time Slot Octet Identifier Output-Bit 1:** These output signals (RxTSb4_n through RxTSb0_n) reflect the five-bit binary value of the number of Time Slot (in the incoming DS1 frame) being received and output to the Terminal Equipment via the Receive Payload Data Output Interface block associated with Framer_n. The Terminal Equipment should use the RxTSClk_n clock to sample these five output pins in order to identify the time-slot being processed by the Receive Section of Framer_n.
RxFrTD_0 RxFrTD_1 RxFrTD_2 RxFrTD_3 RxFrTD_4 RxFrTD_5 RxFrTD_6 RxFrTD_7	D5 A10 B19 C26 Y26 AC21 AF17 AE9	O	**Receive Serial Fractional T1/E1 Input--Receive Framer_n:** These pins can be used to output fractional DS1/E1 payload data extracted from an inbound DS1/E1 frame, if Framer_n is configured accordingly. In this mode, terminal equipment will use either rising edge of RxTSClk_n or RxSerClk_n to clock in fractional DS1/E1 payload data. Please see pin description of RxTSClk_n for details.
RxTSb2_0 RxTSb2_1 RxTSb2_2 RxTSb2_3 RxTSb2_4 RxTSb2_5 RxTSb2_6 RxTSb2_7	B4 C11 B20 E24 Y25 AF23 AD16 AF8	O	**Receive Framer_n--Time Slot Octet Identifier Output-Bit 2:** These output signals (RxTSb4_n through RxTSb0_n) reflect the five-bit binary value of the number of Time Slot (in the incoming DS1 frame) being received and output to the Terminal Equipment via the Receive Payload Data Output Interface block associated with Framer_n. The Terminal Equipment should use the RxTSClk_n clock to sample these five output pins in order to identify the time-slot being processed by the Receive Section of Framer_n.
RxTSChn_0 RxTSChn_1 RxTSChn_2 RxTSChn_3 RxTSChn_4 RxTSChn_5 RxTSChn_6 RxTSChn_7	B4 C11 B20 E24 Y25 AF23 AD16 AF8	O	**Receive Framer_n -- Time Slot Identifier Serial Output** If RxTSb1_n pin is configured as RxFrTD_n to output fractional DS1 payload data from Framer_n, then these pins serially output the five-bit binary value of the number of the Time Slot being accepted and processed by the Transmit Payload Data Input Interface block associated with Framer_n.

RECEIVE SERIAL DATA OUTPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxTSb3_0 RxTSb3_1 RxTSb3_2 RxTSb3_3 RxTSb3_4 RxTSb3_5 RxTSb3_6 RxTSb3_7	B5 D13 C20 D26 W23 AE22 AF16 AE8	O	**Receive Framer_n-Time Slot Octet Identifier Output-Bit 3:** These output signals (RxTSb4_n through RxTSb0_n) reflect the five-bit binary value of the number of Time Slot (in the incoming DS1 frame) being received and output to the Terminal Equipment via the Receive Payload Data Output Interface block associated with Framer_n. The Terminal Equipment should use the RxTSClk_n clock to sample these five output pins in order to identify the time-slot being processed by the Receive Section of Framer_n.
Rx8kHz_0 Rx8kHz_1 Rx8kHz_2 Rx8kHz_3 Rx8kHz_4 Rx8kHz_5 Rx8kHz_6 Rx8kHz_7	B5 D13 C20 D26 W23 AE22 AF16 AE8	O	**Receive 8KHz Clock-Receive Framer_n:** These pins output a reference 8KHz signal clock as if Framer_n is configured accordingly.
RxTSb4_0 RxTSb4_1 RxTSb4_2 RxTSb4_3 RxTSb4_4 RxTSb4_5 RxTSb4_6 RxTSb4_7	D7 A13 B21 E26 AA26 AD21 AC15 AF7	O	**Receive Framer_n--Time Slot Octet Identifier Output-Bit 4:** These output signals (RxTSb4_n through RxTSb0_n) reflect the five-bit binary value of the number of Time Slot (in the incoming DS1 frame) being received and output to the Terminal Equipment via the Receive Payload Data Output Interface block associated with Framer_n. The Terminal Equipment should use the RxTSClk_n clock to sample these five output pins in order to identify the time-slot being processed by the Receive Section of Framer_n.

RECEIVE SERIAL DATA OUTPUT

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxTSClk_0 RxTSClk_1 RxTSClk_2 RxTSClk_3 RxTSClk_4 RxTSClk_5 RxTSClk_6 RxTSClk_7	C4 D11 D18 A25 V24 AD25 AF15 AC9	O	**Receive Channel Clock Output Signal—Framer_n:** This pin indicates the boundary of each time slot of an inbound DS1/E1 frame. **DS1 Mode:** Each of these output pins are a 192kHz clock output which pulses "High" whenever the Receive Payload Data Output Interface block outputs the LSB of each of the 24 time slots (within the inbound DS1 data stream) on the RxSer_n pin. The Terminal Equipment should use this clock signal to sample the RxTSb0_n through RxTSb4_n output signals, and identify the time-slot being processed via the "Receive Section" of each Framer_n. If RxTSb1_n pin is configured as RxFrTD_n to output fractional DS1 payload data from Framer_n, the RxTSClk_n pin can be configured to function as one of the following: The pin will output gaped fractional DS1 clock that can be used by terminal equipment to clock out fractional DS1 payload data at rising edge of the clock. Otherwise, this pin will be a clock enable signal to Receive fractional DS1 Output (RxFrTD_n) if Framer_n is configured accordingly. In this mode, fractional DS1 payload data is clocked into the terminal equipment using un-gapped RxSerClk_n. **E1 Mode:** Each of these output pins are a 256kHz clock output which pulses "High" whenever the Receive Payload Data Output Interface block outputs the LSB of each of the 32 time slots (within the inbound E1 data stream) on the RxSer_n pin. The Terminal Equipment should use this clock signal to sample the RxTSb0_n through RxTSb4_n output signals, and identify the time-slot being processed via the "Receive Section" of each Framer_n. If RxTSb1_n pin is configured as RxFrTD_n to output fractional E1 payload data from Framer_n, the RxTSClk_n pin can be configured to function as one of the following: The pin will output gaped fractional E1 clock that can be used by terminal equipment to clock out fractional E1 payload data at rising edge of the clock. Otherwise, this pin will be a clock enable signal to Receive fractional E1 Output (RxFrTD_n) if Framer_n is configured accordingly. In this mode, fractional E1 payload data is clocked into the terminal equipment using un-gaped RxSerClk_n.
RxLOS_0 RxLOS_1 RxLOS_2 RxLOS_3 RxLOS_4 RxLOS_5 RxLOS_6 RxLOS_7	D2 H4 J1 L4 U1 Y1 AA3 AB4	O	**Receive Loss of Signal Output Indicator—Framer_n:** This output pin will toggle “High” (declare LOS) if the Receive block associated with Framer_n determines that neither the RxPOS_n or the RxNEG_n inputs have received a High level pulse in the last 32 bit periods. This output pin will toggle “Low” if the Receive block, associated with Framer_n, detects a string of 32 consecutive bits, that does not contain a string of 4 consecutive “0’s”. ***NOTE:*** *This output pin will also toggle "High" if the LOS_0 input pin is asserted (e.g., toggled “High” by the LIU LOS output pin).*
RxCASMSync_0 RxCASMSync_1 RxCASMSync_2 RxCASMSync_3 RxCASMSync_4 RxCASMSync_5 RxCASMSync_6 RxCASMSync_7	A4 A11 B18 D24 Y24 AD23 AD12 AC10	O	**Receive “CAS Multiframe” Sync Output Signal--Framer_n:** This E1-only signal pulses "High" for one period of RxSerClk_n whenever the Receive E1 Output Interface of Framer_n outputs the first bit, within a given "CAS Multiframe". ***NOTE:*** *This output pin is inactive if Common Channel Signaling is enabled.*

RECEIVE DECODER LIU INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
RxPOS_0 RxPOS_1 RxPOS_2 RxPOS_3 RxPOS_4 RxPOS_5 RxPOS_6 RxPOS_7	E4 G3 H1 L2 R2 W2 AA2 AC2	I	**Receive Positive Polarity Pulse—Framer_n:** This input pin is intended to be connected to the RxPOS or RPDATA output of the LIU (Line Interface Unit) IC associated with Framer_n. The LIU will assert this input signal (pulse it "High"), when it is receiving a positive-polarity pulse from the line. This input signal is sampled and latched into the Framer, on the user-selectable edge (rising or falling) of the RxLineClk_n signal.
RxNEG_0 RxNEG_1 RxNEG_2 RxNEG_3 RxNEG_4 RxNEG_5 RxNEG_6 RxNEG_7	C1 F1 J3 L3 T2 W1 AB1 AD1	I	**Receive Negative Polarity Pulse—Framer_n:** This input pin is intended to be connected to the RxNEG or RNDATA output of the LIU (Line Interface Unit) associated with Framer_n. The LIU will assert this input signal (pulse it "High"), when it is receiving a negative-polarity pulse from the line. This input signal is sampled and latched into the Framer, on the user-selectable edge (rising or falling) of the RxLineClk_n signal.
RxLineCLK_0 RxLineCLK_1 RxLineCLK_2 RxLineCLK_3 RxLineCLK_4 RxLineCLK_5 RxLineCLK_6 RxLineCLK_7	D1 G1 K4 M4 T3 W4 AA4 AE2	I	**Receive Line Clock Input—Framer_n:** This input pin is intended to be connected to the RxClk output of the LIU (Line Interface Unit) associated with Framer_n. Framer_n uses the user-selectable edge of this signal to sample and latch the signals at the RxPOS_n and RxNEG_n input pins.

TRANSMIT ENCODER LIU INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxPOS_0 TxPOS_1 TxPOS_2 TxPOS_3 TxPOS_4 TxPOS_5 TxPOS_6 TxPOS_7	E3 H3 K3 L1 T4 W3 AB2 AD2	O	**Transmit Positive Polarity Pulse—Framer_n:** This output pin is intended to be connected to the TxPOS or TPDATA input of the LIU (Line Interface Unit) associated with Framer_n. Framer_n will assert this signal when it wishes for the Line Interface Unit (LIU) associated with Framer_n, to transmit a positive polarity pulse on the line.
TxNRZ_0 TxNRZ_1 TxNRZ_2 TxNRZ_3 TxNRZ_4 TxNRZ_5 TxNRZ_6 TxNRZ_7	E3 H3 K3 L1 T4 W3 AB2 AD2	O	**Transmit Non Return to Zero:** Unipolar output for transmitted data. TxNRZ_n includes the results of bit 7 stuffing, but does not include HDB3 encoding.

TRANSMIT ENCODER LIU INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TxNEG_0 TxNEG_1 TxNEG_2 TxNEG_3 TxNEG_4 TxNEG_5 TxNEG_6 TxNEG_7	F3 H2 K2 M3 V1 Y2 AC1 AE1	O	**Transmit Negative Polarity Pulse—Framer_n:** This output pin is intended to be connected to the TxNEG or TNDATA input of the LIU (Line Interface Unit) associated with Framer_n. Framer_n will assert this signal when it wishes for the Line Interface Unit (LIU) associated with Framer_n, to transmit a negative polarity pulse on the line.
TxMX_0 TxMX_1 TxMX_2 TxMX_3 TxMX_4 TxMX_5 TxMX_6 TxMX_7	F3 H2 K2 M3 V1 Y2 AC1 AE1	O	**Transmit Max** Output pulses “High” for one bit time and is coincident with the sampling of the least serial bit of a multiframe.
TxLineCLK_0 TxLineCLK_1 TxLineCLK_2 TxLineCLK_3 TxLineCLK_4 TxLineCLK_5 TxLineCLK_6 TxLineCLK_7	F2 G2 J2 N4 V4 Y3 AC3 AC4	O	**Transmit Line Clock Output—Framer_n:** This output pin is intended to be connected to the TxClk input of the LIU (Line Interface Unit) associated with Framer_n. The LIU uses this pin to sample and latch the signals at its TPDATA and TNDATA input pins.

TIMING

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
OSCClk	T1	I	**Oscillator Clock:** This is a programmable operation clock input. This clock input can be one of six frequencies: E1 Mode: 16.384, 32.768 or 65.536 MHz T1 Mode: 12.352, 24.704 or 49.408 MHz
8kHz_Ref	U2	I	**8 kHz External Reference Clock Input:**
LOP	R4	I	**Loss of Power / Input Pin for Messaging**

LIU CONTROL

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
LOS_0 LOS_1 LOS_2 LOS_3 LOS_4 LOS_5 LOS_6 LOS_7	G4 J4 K1 M2 V2 AA1 AB3 AF1	I	**Loss of Signal Input—LIU Interface-Framer_n:** This input pin is intended to be connected to the RxLOS output pin of the LIU associated with Framer_n. If the LIU IC detects an LOS condition and asserts (toggles "High") this input pin, then the Receive Framer associated with Channel_n will declare a LOS condition. Asserting this input pin "High" will result in Framer_n asserting the RxLOS_n output pin.
GPO7 $\overline{CS1}$	P1	O	**General Purpose Output pin/Chip Select Output pin:** The exact role of this output pin depends upon whether the LIU Controller block is operating in the Hardware or HOST Mode. **Hardware Mode: GPO7** This pin is a general purpose output pin that is controlled by the contents of bit-field 7, within the Line Control Register (Address = 00h, 02h). **HOST Mode:$\overline{CS1}$** This pin is a chip select output pin that is asserted (toggles “Low”) following a write operation to the LIU Access Register 1, associated with framer 4, 5, 6 and 7. This output pin is intended to be tied to the chip select input of an LIU (or other peripheral device) that is configurable via a Microprocessor Serial Interface. Once the HOST Mode serial port has completed its read or write operation, then it will negate (toggle "High") this output pin.
GPO6 SClk1	P2	O	**General Purpose Output pin/Serial Clock Output:** The exact role of this output pin depends upon whether the LIU Controller block is operating in the Hardware or HOST Mode. **Hardware Mode: GPO6** This pin is a general purpose output pin that is controlled by the contents of bit-field 6, within the Line Control Register (Address = 00h, 02h). **HOST Mode:SClk1** This pin functions as the Serial Clock output signal (SCLK), when the LIU Controller Block is configured to operate in the HOST Mode
GPO5 SDI1	P4	O	**General Purpose Output pin/Serial Data Input bit 1:** The exact role of this output pin depends upon whether the LIU Controller block is operating in the Hardware or HOST Mode. **Hardware Mode: GPO5** This pin is a general purpose output pin that is controlled by the contents of bit-field 5, within the Line Control Register (Address = 00h, 02h). **HOST Mode:SDI1** This pin functions as the Serial Data Input (SDI) output pin (to the Microprocessor Serial Interface).
GPO4 SDO1	R1	O	**General Purpose Output pin/Serial Data Output bit 0:** The exact role of this output pin depends upon whether the LIU Controller block is operating in the Hardware or HOST Mode. **Hardware Mode:** GPO4 This pin is a general purpose output pin that is controlled by the contents of bit-field 4, within the Line Control Register (Address = 00h, 02h). **HOST Mode:SDO1** This pin functions as the Serial Data Output (SDO) input pin (into the LIU Controller Block).

LIU CONTROL

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
GPO3 $\overline{CS0}$	M1	O	**General Purpose Output pin/Chip Select Output pin:** The exact role of this output pin depends upon whether the LIU Controller block is operating in the Hardware or HOST Mode. **Hardware Mode: GPO3** This pin is a general purpose output pin that is controlled by the contents of bit-field 3, within the Line Control Register (Address = 0x00, 0x02). **HOST Mode: $\overline{CS0}$** This pin is a chip select output pin that is asserted (toggles “Low”) following a write operation to the LIU Access Register 1, associated with framer 0,1, 2 and 3. This output pin is intended to be tied to the chip select input of an LIU (or other peripheral device) that is configurable via a Microprocessor Serial Interface. Once the HOST Mode serial port has completed its read or write operation, then it will negate (toggle "High") this output pin.
GPO2 SClk0	N2	O	**General Purpose Output/Serial Clock Output:** The exact role of this output pin depends upon whether the LIU Controller block is operating in the Hardware or HOST Mode. **Hardware Mode: GPO2** This pin is a general purpose output pin that is controlled by the contents of bit-field 2, within the Line Control Register (Address = 00h, 02h). **HOST Mode: SClk0** This pin functions as the Serial Clock output signal (SCLK), when the LIU Controller Block is configured to operate in the HOST Mode.
GPO1 SDI0	N3	O	**General Purpose Output pin/Serial Data In Output pin:** The exact role of this output pin depends upon whether the LIU Controller block is operating in the Hardware or HOST Mode. **Hardware Mode: GPO1** This pin is a general purpose output pin that is controlled by the contents of bit field 1, within the Line Control Register (Address = 00h, 02h) **HOST Mode: SDI** This pin functions as the Serial Data Input (SDI) output pin (to the Microprocessor Serial Interface).
GPO0 SDO0	N1	I or O	**General Purpose Output pin/Serial Data Out Input pin:** The exact role of this pin depends upon whether the LIU Controller block is operating in the Hardware or HOST Mode. **Hardware Mode: GPO0** This pin is a general purpose output pin that is controlled by the contents of bit-field 0, within the Line Control Register (Address = 00h, 02h). **HOST Mode: SDO0** This Input pin functions as the Serial Data Output (SDO) input pin (into the LIU Controller Block).

JTAG

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TCK	A1	I	**Test clock:** Boundary Scan clock input. ***Note**: This input pin should be pulled “Low” for normal operation*
TMS	C2	I	**Test Mode Select:** Boundary Scan Mode Select input. ***Note**: This input pin should be pulled “Low” for normal operation*

JTAG

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
TDI	B1	I	**Test Data In:** Boundary Scan Test data input ***Note**: This input pin should be pulled "Low" for normal operation*
TDO	D3	O	**Test Data Out:** Boundary Scan Test data output
TRST	C3	I	**JTAG Test Reset Input**
Test Mode	P3	I	**Factory Test Mode Pin** ***Note:** User should tie this pin to ground*

MICROPROCESSOR INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
Data0 Data1 Data2 Data3 Data4 Data5 Data6 Data7	R24 R25 N26 N25 L24 K25 K24 J24	I/O	**Bidirectional Microprocessor Data Bus Bit 0--LSB** **Bidirectional Microprocessor Data Bus Bit 1** **Bidirectional Microprocessor Data Bus Bit 2** **Bidirectional Microprocessor Data Bus Bit 3** **Bidirectional Microprocessor Data Bus Bit 4** **Bidirectional Microprocessor Data Bus Bit 5** **Bidirectional Microprocessor Data Bus Bit 6** **Bidirectional Microprocessor Data Bus Bit 7--MSB**
$\overline{\text{Req0}}$	T26	O	**DMA Cycle Request Output—DMA Controller 0 (Write)**: The Framer asserts this output pin (toggles it "Low") when at least one of the Transmit HDLC buffers are empty and can receive one more HDLC message. The Framer negates this output pin (toggles it "High") when the HDLC buffer can no longer receive another HDLC message.
$\overline{\text{Req1}}$	U23		**DMA Cycle Request Output—DMA Controller 1 (Read):** The Framer asserts this output pin (toggles it "Low") when one of the Receive HDLC buffer contains a complete HDLC message that needs to be read by the µC/µP. The Framer negates this output pin (toggles it High) when the Receive HDLC buffers are depleted.
$\overline{\text{INT}}$	M24	O	**Interrupt Request Output:** The Framer will assert this active "Low" output (toggles it "Low"), to the local µP, anytime it requires interrupt service.
µPClk	R23	I	**Microprocessor Clock Input:** This clock signal is the Microprocessor Interface System clock. This clock signal is used for synchronous/burst/DMA data transfer. The maximum frequency of this clock signal is 33MHz.

MICROPROCESSOR INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
µPType0	T25	I	**Microprocessor Type Input: Bit 0 (LSB):** This input pin, along with µPTYPE1 and µPTYPE2 permit the user to specify which type of Microprocessor/Microcontroller to be interfaced the Framer.
µPType1 µPType2	P24 M25		**Microprocessor Type Input: Bit 1** **Microprocessor Type Input: Bit 2**

µPType2	µPType1	µPType0	MICROPROCESSOR TYPE
0	0	0	68HC11, 8051, 80C188
0	0	1	MOTOROLA 68K
0	1	0	INTEL X86
0	1	1	INTEL I960
1	0	0	IDT3051/52
1	0	1	IBM POWER PC 403

RDY_$\overline{DTACK}$	P23	O	**Ready/Data Transfer Acknowledge Output:** The exact behavior of this pin depends upon which Microprocessor the Framer is configured to interface to: **Intel Type Microprocessors** This output pin toggles "Low" when the Framer is ready to respond to the current PIO (Programmed I/O) or Burst Transaction. **Motorola Type Microprocessors** This output pin toggles "Low" when the Framer has completed the current bus cycle.
A0 A1 A2 A3 A4 A5 A6	P26 N23 M26 L26 L23 J26 K23	I	**Microprocessor Interface Address Bus Input Bit 0 -- (LSB)** **Microprocessor Interface Address Bus Input Bit 1** **Microprocessor Interface Address Bus Input Bit 2** **Microprocessor Interface Address Bus Input Bit 3** **Microprocessor Interface Address Bus Input Bit 4** **Microprocessor Interface Address Bus Input Bit 5** **Microprocessor Interface Address Bus Input Bit 6 -- (MSB)**
$\overline{DBEn}$	P25	I	**Data Bus Enable Input pin**.
ALE_AS	N24	I	**Address Latch Enable Input_Address Strobe**
$\overline{CS}$	G25	I	**Microprocessor Interface—Chip Select Input:** The Microprocessor/Microcontroller must assert this input pin (toggle it "Low") in order to exchange data with the Framer. ***Note:*** *For the 68K MPU, this signal is generated by address decode and address strobe.*
$\overline{RD}$	R26	I	**Microprocessor Interface—Read Strobe Input:** The exact behavior of this pin depends upon the type of Microprocessor/Microcontroller the Framer has been configured to interface to, as defined by the µPTYPE[2:0] pins. ***Note:*** *See pin T25 (µPType0) for the µP selection table.*

MICROPROCESSOR INTERFACE

(Framer Channel Number indicated by _n)

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
$\overline{WR}$	G26	I	**Microprocessor Interface—Write Strobe Input** **"Low" :** Indicates current bus cycle is a write cycle: Intel 51, 188, MIPS350x **"High" :** Indicates present bus cycle is a write cycle: Intel x86, i960 **"Low" :** Indicates current bus cycle is a read cycle: Intel x86, i960 **"High" :** Indicates present bus cycle is a read cycle: Motorola, Power PC 403 **"Low" :** Also used as write strobe in DMA transfer
$\overline{ACK0}$	U26	I	**DMA Cycle Acknowledge Input—DMA Controller 0 (Write):** The external DMA Controller will assert this input pin "Low" when the following two conditions are met: a. After the DMA Controller, within the Framer has asserted (toggled "Low"), the Req_0 output signal. b. When the external DMA Controller is ready to transfer data from external memory to the selected Transmit HDLC buffer. At this point, the DMA transfer between the external memory and the selected Transmit HDLC buffer may begin. After completion of the DMA cycle, the external DMA Controller will negate this input pin after the DMA Controller within the Framer has negated the $\overline{Req\_0}$ output pin. The external DMA Controller must do this in order to acknowledge the end of the DMA cycle.
$\overline{ACK1}$	T23	I	**DMA Cycle Acknowledge Input—DMA Controller 1 (Read):** The external DMA Controller asserts this input pin "Low" when the following two conditions are met: a. After the DMA Controller, within the Framer has asserted (toggled "Low"), the Req_1 output signal. b. When the external DMA Controller is ready to transfer data from the selected Receive HDLC buffer to external memory. At this point, the DMA transfer between the selected Receive HDLC buffer and the external memory may begin. After completion of the DMA cycle, the external DMA Controller will negate this input pin after the DMA Controller within the Framer has negated the $\overline{Req\_1}$ output pin. The external DMA Controller will do this in order to acknowledge the end of the DMA cycle.
$\overline{Blast}$	L25	I	**Last Cycle of Burst Indicator Input:** The Microprocessor asserts this pin "Low"when it is performing its last read or write cycle, within a burst operation.
$\overline{Reset}$	R3	I	**Reset Input:** Active "Low"

GROUND PINS

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
VDD	L11 L12 L13 L14 L15 L16 M11 M12 M15 M16 N11 N12 N15 N16 R11 R12 R15 R16	****	**Power Supply Pins**

POWER SUPPLY PINS

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
GND	M13 M14 N13 N14 P13 P14 R13 R14 T11 T12 T13 T14 T15 T16	****	**Ground Pins**

NO CONNECT PINS

SIGNAL NAME	PIN #	TYPE	DESCRIPTION
NC	A6 A20 B7 B17 C12 C13 C16 C23 D14 D17 E1 E2 F4 H25 H26 K26 M23 U3 U4 U25 V3 Y4 AA25 AC23 AD26 AE3 AE14 AE15 AE17 AE25 AF2 AF11 AF14 AF22 AF24		**Not Connected**

ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUMS

Power Supply..... -0.5V to +3.465V		Power Dissipation PBGA Package..... 2W
Storage Temperature .....-65°C to 150°C		Input Logic Signal Voltage (Any Pin) .....-0.5V to + 5.5V
Operating Temperature Range.....-40°C to 85°C		ESD Protection.....>2000V
Supply Voltage ..... GND-0.5V to +VDD + 0.5V		Input Current (Any Pin) ..... ± 100mA

DC ELECTRICAL CHARACTERISTICS

Test Conditions: TA = 25°C, VDD = 3.3V ± 5% unless otherwise specified

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNITS	CONDITIONS
I_{DD}	Power Supply Current		450		mA	All Channels on
I_{LL}	Data Bus Tri-State Bus Leakage Current	-10		+10	µA	
V_{IL}	Input Low voltage			0.6	V	PDATA[0:7]
				0.8	V	All Others
V_{IH}	Input High Voltage	2.7		VDD	V	PDATA[0:7]
		2.0		VDD	V	All Others
V_{OL}	Output Low Voltage	0.0		0.4	V	I_{OL} = 2mA
V_{OH}	Output High Voltage	2.4		VDD	V	I_{OH} = 2mA
I_{OC}	Open Drain Output Leakage Current	-10		10	µA	
I_{IH}	Input High Voltage Current	-10		10	µA	V_{IH} = VDD
	Input High Voltage Current (with pull-down resistor)	100		400		
I_{IL}	Input Low Voltage Current	-10		10	µA	V_{IL} = GND
	Input Low Voltage Current (with pull-up resistor)	-150		-30		

TABLE 2: XRT84L38 POWER CONSUMPTION

(Vdd=3.3V±5%, T_A=25°C unless otherwise specified)

MODE	SUPPLYVOLTAGE	MIN	TYP	MAX	UNIT
T1	3.3V	-	1.8	2.0	W
E1	3.3V	-	1.5	1.8	W

1.0 MICROPROCESSOR INTERFACE BLOCK

The Microprocessor Interface section supports communication between the local microprocessor (µP) and the Framer. The Microprocessor Interface supports the following features:

- Communicates through a 7 bit address bus (4 bit for one framer) and an 8 bit data bus.
- Supports DMA read/write data interface
- Supports burst transfers
- Supports Programmed I/O read and write, wait cycle extended with READY/$\overline{\text{DTACK}}$

The Microprocessor Interface section supports the following operations:

- Channel Selection
- Writing configuration data into the Framer on-chip (addressable) registers
- Writing outbound PMDL (Path Maintenance Data Link) messages into the Transmit LAPD Message buffer of the Framer
- Generation of Interrupt Requests to the µP
- Servicing Interrupt Requests from the Framer
- Monitoring the system's health by periodically reading the on-chip Performance Monitor registers
- Reading inbound PMDL Messages from the Receive LAPD Message Buffer of the Framer

Each of these operations (between the local microprocessor and the Framer IC) is discussed in detail, throughout this data sheet.

The Framer supports the following microprocessors/microcontrollers with a minimum amount of glue logic.

- Intel 8051, 80C188, x86, i960
- Motorola 68HC11, 68K
- MIPS 3051/52
- PowerPC 403

The type of microprocessor/microcontroller to interface to the Framer is specified by tying the µPTYPE[2:0] pins to the appropriate level. Table 1, lists the values for µPTYPE[2:0] and the corresponding µP/µC types.

TABLE 3: µC/µP SELECTION TABLE

µPTYPE[2:0] INPUT LEVELS	CORRESPONDING µC/µP
000	68HC11, 8051, 80C188
001	Motorola 68000 Family
010	Intel x86 Family
011	Intel I960
100	IDT3051/52 (MIPS)
101	IBM PowerPC 403

The behavior of some of the pins, associated with the Microprocessor Interface, depends upon the value that the user has applied to the PType[2:0] input pins. The next sections present a detailed discussion on the role of each of these pins, and how to configure the Framer to interface to each of these types of Microprocessors.

The Framer connects to the Microcontroller as if it were external memory. The microcontroller can read or write to two different storage elements in the Framer:

- Flip-flop types of registers
- RAMs

The configuration of the Framer, including the enabling/disabling of interrupts, is selected by setting values in various control registers. The registers can be read as well as written. The Framer can be designed into both

polled and interrupt-driven systems. All detection of change of state of alarm conditions, data link events, error events, or counter overflows can be programmed to cause interrupts.

The Microcontroller Interface Block within the Framer supports three types of data transfer schemes:

- Programmable Input/Output (PIO)
- Burst Transfer
- DMA (Direct Memory Access)

Each of these data transfer methods are also discussed in the next sections.

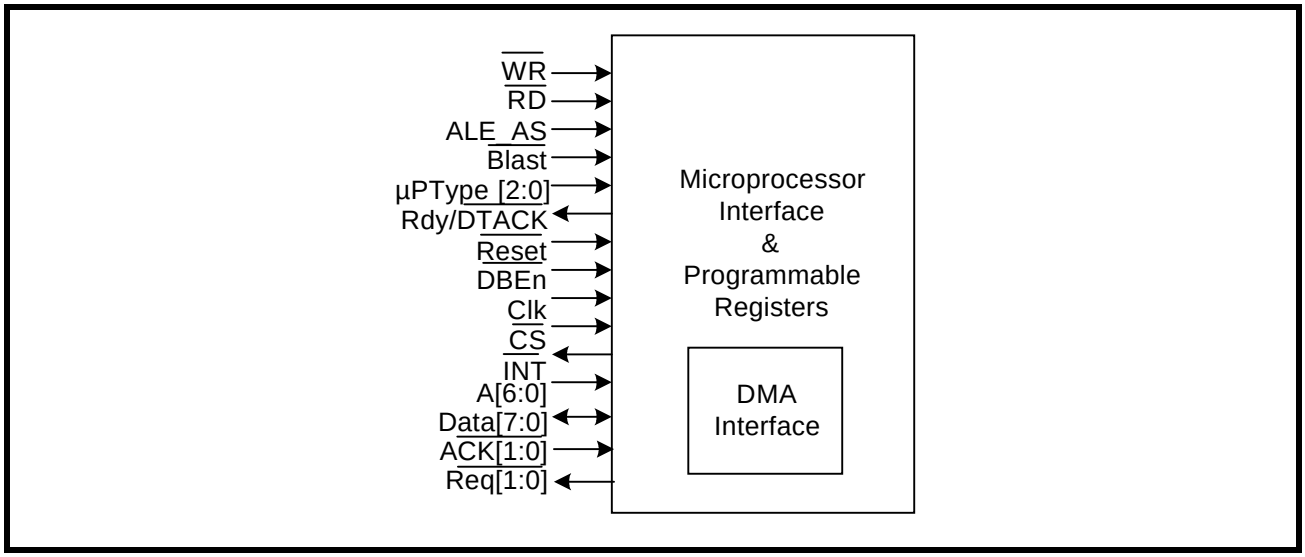
1.1 Channel Selection within the Framer

The XRT84L38 Framer consists of eight independent banks of configuration registers. Each of these banks are identical and correspond to each of the eight channels within the XRT84L38. The XRT84L38 permits selection of and access to, any one of these Configuration Register Banks, via the Three (3) Most Significant Address Pins, A4, A5 and A6. The relationship between the states of A4, A5 and A6, and the corresponding Configuration Register bank, is shown below.

Table 4: Channel Selection

A6	A5	A4	Configuration Register Bank
0	0	0	Channel 0
0	0	1	Channel 1
0	1	0	Channel 2
0	1	1	Channel 3
1	0	0	Channel 4
1	0	1	Channel 5
1	1	0	Channel 6
1	1	1	Channel 7

Figure 3. Simplified Block Diagram of the Microprocessor Interface Block



1.2 The Microprocessor Interface Block Signal

The Framer may be configured into different operating modes and have its performance monitored by software through a standard microprocessor, using data, address and control signals.

The local µP configures the Framer (into a desired operating mode) by writing data into specific addressable, on-chip Read/Write registers, or on-chip RAM. The microprocessor interface provides the signals which are required for a general purpose microprocessor to read or write data into these registers. The Microprocessor Interface also supports polled and interrupt driven environments. These interface signals are described below in Table 5, Table 6, and Table 7. The microprocessor interface can be configured to operate in the Motorola Mode, the Intel mode, as well as other modes. When the Microprocessor Interface is operating in the Motorola mode, some of the control signals function in a manner required by the Motorola 68000 family of microprocessors. Likewise, when the Microprocessor Interface is operating in the Intel Mode, then these Control Signals function in a manner as required by the Intel 80xx family of microprocessors.

Table 5 lists and describes those Microprocessor Interface signals whose role is constant across the two modes. Table 6 describes the role of some of these signals when the Microprocessor Interface is operating in the **Intel Mode**. Likewise, Table 7 describes the role of these signals when the Microprocessor Interface is operating in the **Motorola Mode**.

TABLE 5: XRT84L38 MICROPROCESSOR INTERFACE SIGNALS THAT EXHIBIT CONSTANT ROLES IN BOTH THE INTEL AND MOTOROLA MODES

PIN NAME	TYPE	DESCRIPTION
µPTYPE[2:0]	I	**Microprocessor Interface Mode Select Input pins** These three pins are used to specify the Microprocessor Mode that the Microprocessor Interface will operate in. The relationship between the state of these three input pins, and the corresponding Microprocessor Mode is presented in Table 1.
D[7:0]	I/O	**Bi-Directional Data Bus for register Read or Write Operations.**
A[6:0]	I	**Seven-Bit Address Bus Inputs** The XRT84L38 Framer Microprocessor Interface uses a Multiplexed Address bus. This address bus is provided to permit the user to select an on-chip register or buffer location for Read/Write access.
$\overline{CS}$	I	**Chip Select Input** This active-low signal selects the Microprocessor Interface of the XRT84L38 Framer and enables Read/Write operations with the on-chip registers/buffer locations.

TABLE 6: INTEL MODE: MICROPROCESSOR INTERFACE SIGNALS

XRT84L38 PIN NAME	INTEL EQUIVALENT PIN	TYPE	DESCRIPTION
ALE_AS	ALE	I	**Address-Latch Enable:** This active-high signal is used to latch the contents on the address bus, A[6:0]. The contents of the Address Bus are latched into the A[6:0] inputs on the falling edge of ALE_AS. Additionally, this signal can be used to indicate the start of a burst cycle.
$\overline{RD}$	RD*	I	**Read Signal:** This active-low input functions as the read signal from the local µP. When this signal goes "Low", the Framer Microprocessor Interface places the contents of the addressed register on the Data Bus pins, D[7:0]. The Data Bus is tri-stated once this input signal returns "High".
$\overline{WR}$	WR*	I	**Write Signal:** This active-low input functions as the write signal from the local µP. The contents of the Data Bus (D[7:0]) is written into the addressed register via A[6:0], on the rising edge of this signal.
RDY_$\overline{DTACK}$	READY*	O	**Ready Output:** This active-low signal is provided by the Framer and indicates that the current read or write cycle is to be extended until this signal is asserted. The local µP typically inserts WAIT states until this signal is asserted. This output toggles "Low" when the device is ready for the next Read or Write cycle.

TABLE 7: MOTOROLA MODE: MICROPROCESSOR INTERFACE SIGNALS

XRT84L38 PIN NAME	MOTOROLA EQUIVALENT PIN	TYPE	DESCRIPTION
ALE_AS	AS*	I	**Address Strobe:** This active-low signal is used to latch the contents on the address bus input pins, A[6:0], into the Microprocessor Interface circuitry. The contents of the Address Bus are latched into the Framer on the rising edge of the ALE_AS signal. This signal can also be used to indicate the start of a burst cycle.
$\overline{RD}$	DS*	I	**Data Strobe:** This signal latches the contents of the bi-directional data bus pins into the Addressed Register within the Framer during a Write Cycle.
$\overline{WR}$	R/W*	I	**Read/Write Input:** When this pin is "High", it indicates a Read Cycle. When this pin is "Low", it indicates a Write cycle.
RDY_$\overline{DTACK}$	DTACK*	O	**Data Transfer Acknowledge:** The Framer asserts $\overline{DTACK}$ in order to inform the CPU that the present READ or WRITE cycle is nearly complete. The 68000 family of CPUs requires this signal from its peripheral devices in order to quickly and properly complete a READ or WRITE cycle.

1.3 INTERFACING THE XRT84L38 TO THE LOCAL µC/µP VIA THE MICROPROCESSOR INTERFACE BLOCK

The Microprocessor Interface block within the Framer is very flexible and provides the following options:

- Interface the Framer to a µC/µP over an 8-bit wide bi-directional data bus.
- Interface the Framer to an Intel-type or Motorola-type µC/µP.
- Transfer data (between the Framer IC and the µC/µP) via the Programmed I/O or Burst Mode

1.3.1 Interfacing the Framer to the Microprocessor over an 8 bit wide bi-directional Data Bus

The Framer Microprocessor Interface permits the user to interface it to a µC/µP over an 8-bit wide bi-directional data bus. In general, interfacing the Framer to an 8-bit µC/µP is quite straight-forward. This is because most of the registers, within the Framer, are 8-bits wide. In this mode, the µC/µP can read or write data into both even and odd numbered addresses within the Framer address space.

Example:

Consider that an 8-bit µC/µP needs to read in the PMON LCV Event Count Register. In order to accomplish this task, the 8-bit µC/µP needs to read in the contents of PMON LCV Event Count Register - MSB (located at Address = 0x50) and the contents of the PMON LCV Event Count Register - LSB (located at Address = 0x51). These two eight-bit registers when concatenated together make up the PMON LCV Event Count Register.

If the 8-bit µC/µP reads in the PMON LCV Event Count-LSB register first, then the entire PMON LCV Event Count register will be reset to 0x0000. As a consequence, if the 8-bit µC/µP attempts to read in the PMON LCV Event Count-MSB register in the very next read cycle, it will read in the value 0x00.

1.3.2 Data Access Modes

The Microprocessor Interface block supports data transfer between the Framer and the µC/µP (e.g., Read and Write operations) via the Programmed I/O and the Burst Modes.

1.3.2.1 Programmed I/O

Programmed I/O is basically a handshaking type of asynchronous bus access, which provides relatively slow single read and write data transfers. The Microprocessor must supply an address value to the Address Bus input pins A[6:0] with each read and write cycle. Because of the Indirect Addressing scheme each PIO reads and write access requires two accesses, as illustrated below.

In the first access, the Microprocessor is specifying two things:

1. Which of the four framer register sets it intends to access.
2. Which group of registers within the selected framer's register sets, the Microprocessor wants to access.

As a slave, the E1 is the target of access generated by a bus master, the CPU. Slave accesses are accepted by the slave control state machine, then passed to related functional logic. Address is buffered and decoded to address relevant destination. Data is also latch in both write and read directions. PIO operations are enabled by the Chip Select (CS) input signal. Framer PIO interface supports pipelined (buffered) writes to increase bus throughput. All internal registers and accessible memory are addressable through 6 bits of address bus.

1.3.2.2 Data Access using Programmed I/O

Programmed I/O is the conventional manner in which a microprocessor exchanges data with a peripheral device. However, it is also the slowest method of data exchange between the Framer and the µC/µP.

1.3.2.2.1 Intel Mode Programmed I/O Access

If the Framer is interfaced to an Intel-type µC/µP (e.g., the 80x86 family, etc.), then it should be configured to operate in the Intel mode.

1.3.2.2.1.1 Intel Mode Read Cycle

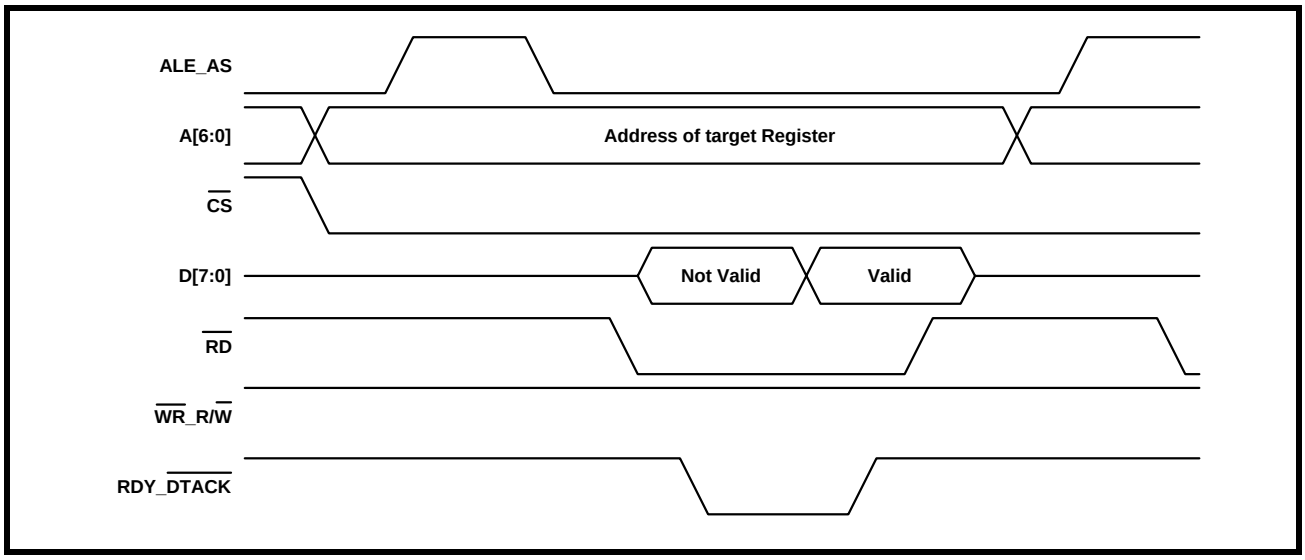
Whenever an Intel-type µC/µP wishes to read the contents of a register or some location within the Receive LAPD Message buffer or the Receive OAM Cell Buffer, within the Framer, it should do the following.

1. Place the address of the target register or buffer location, within the Framer, on the Address Bus input pins A[6:0].
2. While the µC/µP is placing this address value on the Address Bus, the Address Decoding circuitry within the user's system should assert the $\overline{CS}$ (Chip Select) pin of the Framer, by toggling it "Low". This action enables further communication between the µC/µP and the Framer Microprocessor Interface block.
3. Toggle the ALE_AS (Address Latch Enable) input pin "High". This step enables the Address Bus input drivers, within the Microprocessor Interface block of the Framer.
4. After allowing the data on the Address Bus pins to settle, by waiting the appropriate Address Data Setup time, the µC/µP should toggle the ALE_AS pin "Low". This step causes the Framer to latch the contents of the Address Bus into its internal circuitry. At this point, the address of the register or buffer locations, within the Framer, has been selected.
5. Next, the µC/µP should indicate that this current bus cycle is a Read Operation by toggling the $\overline{RD}$_DS (Read Strobe) input pin "Low". This action also enables the bi-directional data bus output drivers of the Framer. At this point, the bi-directional data bus output drivers proceeds to drive the contents of the latched addressed register, or buffer location, onto the bi-directional data bus, D[7:0].
6. Immediately after the µC/µP toggles the Read Strobe signal "Low", the Framer toggles the RDY_$\overline{DTACK}$ output pin "Low". The Framer does this in order to inform the µC/µP that the data to be read from the data bus is NOT READY to be latched into the µC/µP.

7. After some settling time, the data on the bi-directional data bus stabilizes and can be read by the µC/µP. The Framer indicates that this data can be read by toggling the RDY_$\overline{\text{DTACK}}$ (READY) signal "High".
8. After the µC/µP detects the RDY_$\overline{\text{DTACK}}$ signal, from the Framer, it can terminate the Read Cycle by toggling the $\overline{\text{RD}}$_DS (Read Strobe) input pin "High".

Figure 4 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals during an Intel-type Programmed I/O Read Operation.

FIGURE 4. INTEL µP INTERFACE SIGNALS DURING PROGRAMMED I/O READ OPERATION



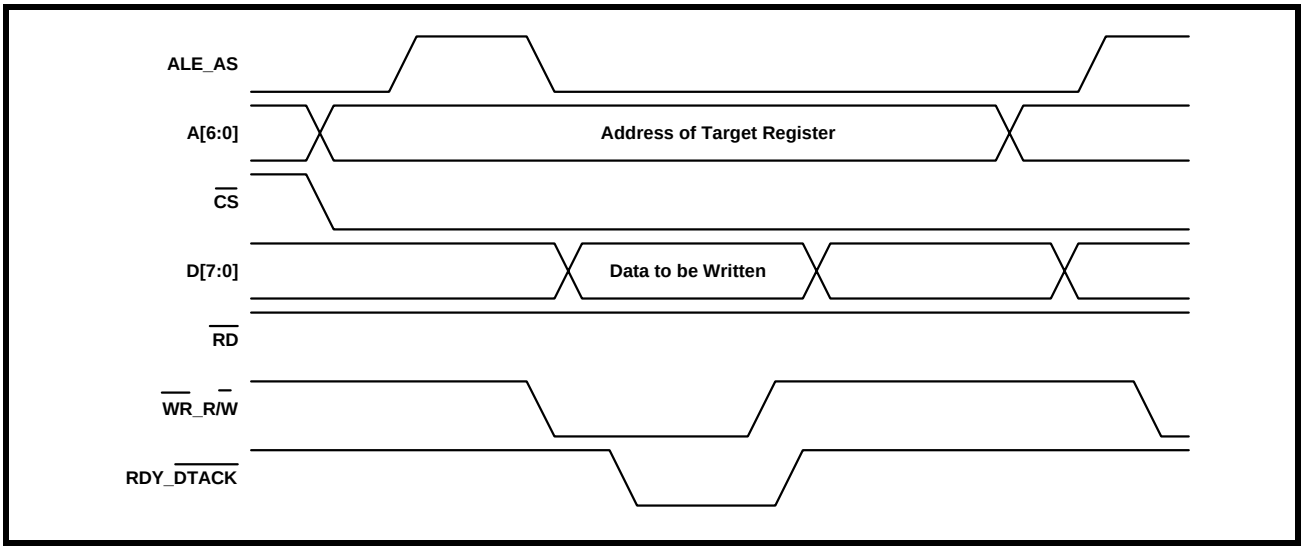
1.3.2.2.1.2 The Intel Mode Write Cycle

Whenever an Intel-type µC/µP wishes to write a byte or word of data into a register or buffer location, within the Framer, it should do the following.

1. Assert the ALE_AS (Address Latch Enable) input pin by toggling it "High". When the µC/µP asserts the ALE_AS input pin, it enables the Address Bus Input Drivers within the Framer chip.
2. Place the address of the target register or buffer location, within the Framer, on the Address Bus input pins, A[6:0].
3. While the µC/µP is placing this address value onto the Address Bus, the Address Decoding circuitry within the user's system should assert the $\overline{\text{CS}}$ input pin of the Framer by toggling it "Low". This step enables further communication between the µC/µP and the Framer Microprocessor Interface block.
4. After allowing the data on the Address Bus pins to settle, by waiting the appropriate Address Setup time, the µC/µP should toggle the ALE_AS input pin "Low". This step causes the Framer to latch the contents of the Address Bus into its internal circuitry. At this point, the address of the register or buffer location within the Framer, has been selected.
5. Next, the µC/µP should indicate that this current bus cycle is a Write Operation by toggling the $\overline{\text{WR}}$_R/$\overline{\text{W}}$ (Write Strobe) input pin "Low". This action also enables the bi-directional data bus input drivers of the Framer.
6. The µC/µP should then place the byte or word that it intends to write into the target register on the bi-directional data bus, D[7:0].
7. After waiting the appropriate amount of time for the data on the bi-directional data bus to settle, the µC/µP should toggle the $\overline{\text{WR}}$_R/$\overline{\text{W}}$ (Write Strobe) input pin "High". This action accomplishes two things:
   a. It latches the contents of the bi-directional data bus into the Framer Microprocessor Interface block.
   b. It terminates the write cycle.

Figure 5 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals, during an Intel-type Programmed I/O Write Operation.

FIGURE 5. INTEL µP INTERFACE SIGNALS DURING PROGRAMMED I/O WRITE OPERATION



1.3.2.2.2 Motorola Mode Programmed I/O Access

If the Framer is interfaced to a Motorola-type µC/µP (e.g., the MC680X0 family, etc.), it should be configured to operate in the Motorola mode.

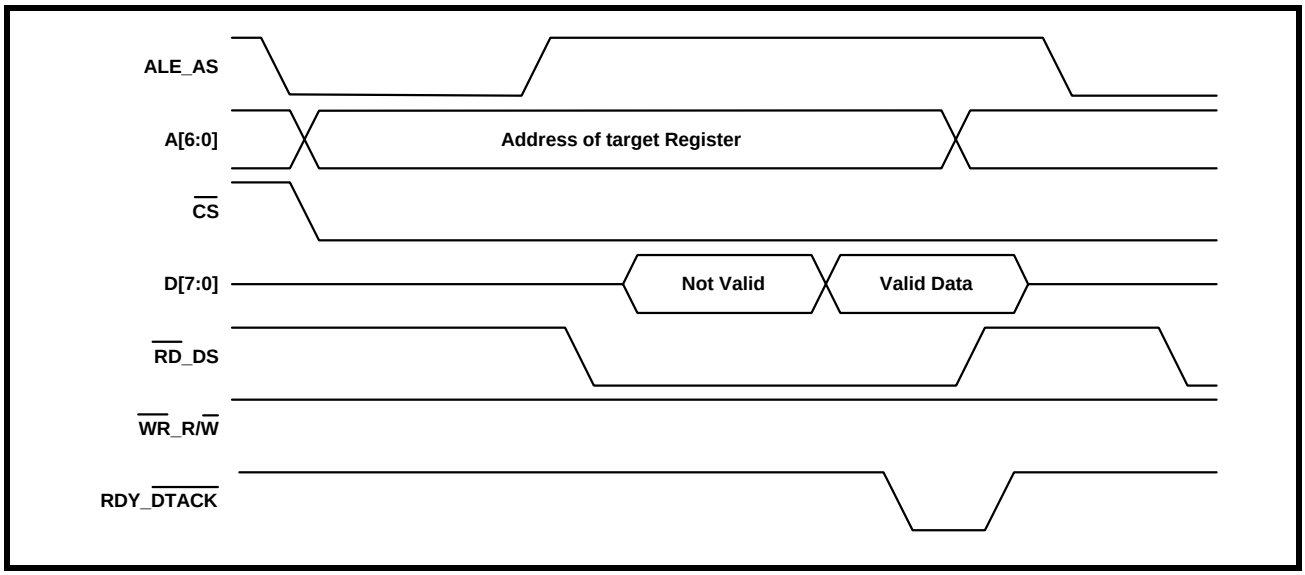
1.3.2.2.2.1 Motorola Mode Read Cycle

Whenever a Motorola-type µC/µP wishes to read the contents of a register or some location within the Receive LAPD Message or Receive OAM Cell Buffer, within the Framer, it should do the following.

1. Assert the ALE_AS (Address-Strobe) input pin by toggling it “Low”. This step enables the Address Bus input drivers within the Microprocessor Interface Block of the Framer.
2. Place the address of the target register or buffer location within the Framer, on the Address Bus input pins, A[6:0].
3. At the same time, the Address Decoding circuitry within the user's system should assert the $\overline{CS}$ (Chip Select) input pin of the Framer, by toggling it "Low". This action enables further communication between the µC/µP and the Framer Microprocessor Interface block.
4. After allowing the data on the Address Bus pins to settle, by waiting the appropriate Address Setup time, the µC/µP should toggle the ALE_AS input pin "High". This step causes the Framer to latch the contents of the Address Bus into its internal circuitry. At this point, the address of the register or buffer location within the Framer has been selected.
5. Further, the µC/µP should indicate that this cycle is a Read cycle by setting the $\overline{WR}$_R/$\overline{W}$ (R/W*) input pin "High".
6. Next the µC/µP should initiate the current bus cycle by toggling the $\overline{RD}$_DS (Data Strobe) input pin "Low". This step enables the bi-directional data bus output drivers, within the Framer. At this point, the bi-directional data bus output drivers will proceed to drive the contents of the Address register onto the bi-directional data bus, D[7:0].
7. After some settling time, the data on the bi-directional data bus will stabilize and can be read by the µC/µP. The Framer will indicate that this data can be read by asserting the RDY_$\overline{DTACK}$ (DTACK) signal “Low”.
8. After the µC/µP detects the RDY_$\overline{DTACK}$ signal (from the Framer) it will terminate the Read Cycle by toggling the $\overline{RD}$_DS (Data Strobe) input pin "High".

Figure 6 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals during a Motorola-type Programmed I/O Read Operation.

FIGURE 6. MOTOROLA µP INTERFACE SIGNALS DURING A PROGRAMMED I/O READ OPERATION



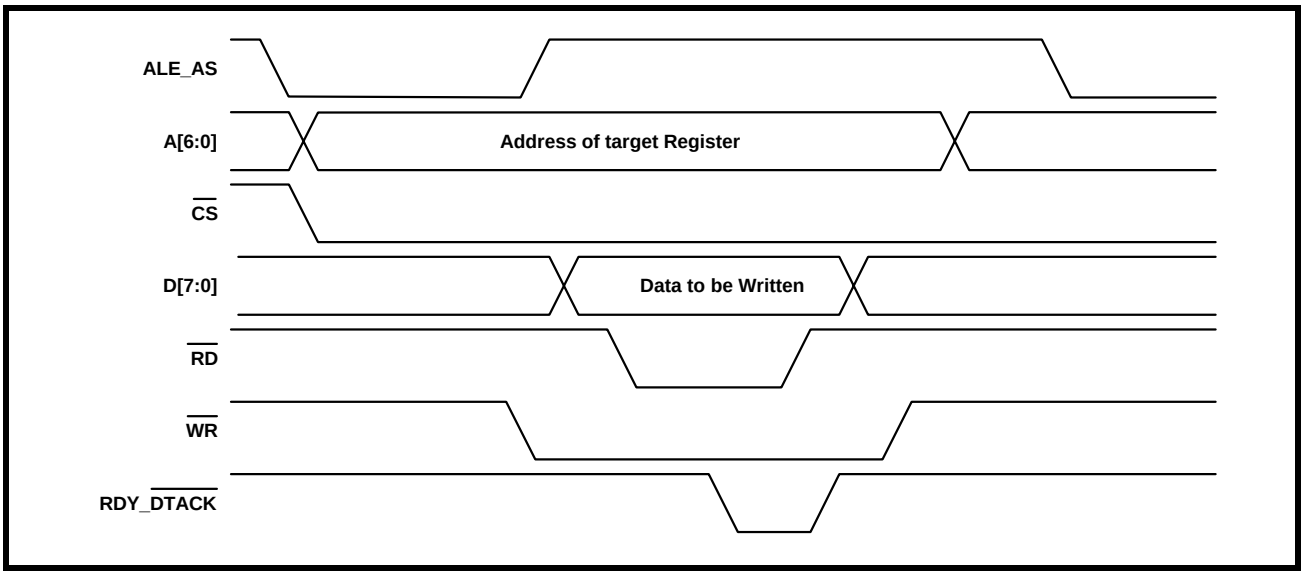
1.3.2.2.2.2 Motorola Mode Write Cycle

Whenever a Motorola-type µC/µP wishes to write a byte or word of data into a register or buffer location, within the Framer, it should do the following.

1. Assert the ALE_AS (Address Select) input pin by toggling it "Low". This step enables the Address Bus input drivers (within the Framer chip).
2. Place the address of the target register or buffer location (within the Framer), on the Address Bus input pins, A[6:0].
3. While the µC/µP is placing this address value onto the Address Bus, the Address-Decoding circuitry (within the user's system) should assert the $\overline{CS}$ (Chip Select) input pins of the Framer by toggling it "Low". This step enables further communication between the µC/µP and the Framer Microprocessor Interface block.
4. After allowing the data on the Address Bus pins to settle (by waiting the appropriate Address Setup time), the µC/µP should toggle the ALE_AS input pin "High". This step causes the Framer to latch the contents of the Address Bus into its own circuitry. At this point, the Address of the register or buffer location (within the Framer), has now been selected.
5. Further, the µC/µP should indicate that this current bus cycle is a Write operation by toggling the $\overline{WR}$_R/$\overline{W}$ (R/W*) input pin "Low".
6. The µC/µP should then place the byte or word that it intends to write into the target register, on the bi-directional data bus, D[7:0].
7. Next, the µC/µP should initiate the bus cycle by toggling the $\overline{RD}$_DS (Data Strobe) input pin "Low". When the Framer senses that the $\overline{WR}$_R/$\overline{W}$ (R/W*) input pin is "High" and that the $\overline{RD}$_DS (Data Strobe) input pin has toggled "Low", it will enable the input drivers of the bi-directional data bus, D[7:0].
8. After waiting the appropriate time, for this newly placed data to settle on the bi-directional data bus (e.g., the Data Setup time) the Framer will assert the RDY_$\overline{DTACK}$ output signal “Low”.
9. After the µC/µP detects the RDY_$\overline{DTACK}$ signal (from the Framer), the µC/µP should toggle the $\overline{RD}$_DS input pin "High". This action accomplishes two things.
   a. It latches the contents of the bi-directional data bus into the Microprocessor Interface block.
   b. It terminates the Write cycle.

Figure 7 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals, during a Motorola-type Programmed I/O Write Operation.

FIGURE 7. MOTOROLA µP INTERFACE SIGNAL DURING PROGRAMMED I/O WRITE OPERATION



1.3.2.3 Burst Mode I/O for Data Access

Burst Mode I/O access is a much faster way to transfer data between the µC/µP and the Microprocessor Interface (of the Framer), than Programmed I/O. The reason why Burst Mode I/O is faster is explained below.

Data is placed upon the Address Bus input pins A[6:0] only for the very first access, within a given burst access. The remaining read or write operations (within this burst access) do not require the placement of the Address Data on the Address Data Bus. As a consequence, the user does not have to wait through the Address Setup and Hold times for each of these Read/Write operation, within the Burst Access.

It is important to note that there are some limitations associated with Burst Mode I/O Operations.

1. All cycles within the Burst Access, must be either all Read or all Write cycles. No mixing of Read and Write cycles is permitted.
2. A Burst Access can only be used when Read or Write operations are to be employed over a contiguous range of address locations, within the Framer.
3. The very first Read or Write cycle, within a burst access, must start at the lowest address value, of the range of addresses to be accessed. Subsequent operations will automatically be incremented to the very next higher address value.

Examples of Burst Mode I/O operations are presented below for read and write operations, with both Intel-type and Motorola-type µC/µP.

1.3.2.3.1 Burst I/O Access: Intel Mode

If the XRT84L38 Framer is interfaced to an Intel-type µC/µP (e.g., the 80x86 family, etc.), then it should be configured to operate in the Intel mode (by tying the MOTO pin to ground). Intel-type Read and Write Burst I/O Access operations are described below.

1.3.2.3.1.1 Intel-Mode Read Burst Access

When an Intel-type µC/µP wants to read the contents of numerous registers or buffer locations over a contiguous range of addresses, then it should do the following.

a. Perform the initial read operation of the burst access.

b. Perform the remaining read operations of the burst access.

c. Terminate the burst access operation.

Each of these operations within the burst access are described below.

1.3.2.3.1.1.1 Initial Read Operation: Intel mode

The initial read operation of an Intel-type read burst access is accomplished by executing a Programmed I/O Read Cycle as summarized below.

A.0 Execute a Single Ordinary (Programmed I/O) Read Cycle, as described in steps A.1 through A.7 below.

A.1 Place the address of the initial-target register or buffer location (within the Framer) on the Address Bus input pins A[6:0].

A.2 While the µC/µP is placing this address value onto the Address Bus, the Address Decoding circuitry (within the user's system) should assert the $\overline{CS}$ input pin of the Framer, by toggling it "Low". This step enables further communication between the µC/µP and the Framer Microprocessor Interface block.

A.3 Assert the ALE_AS (Address Latch Enable) pin by toggling it "High". This step enables the Address Bus input drivers, within the Microprocessor Interface block of the Framer.

A.4 After allowing the data on the Address Bus pins to settle (by waiting the appropriate Address Data Setup time), the µC/µP should then toggle the ALE_AS pin "Low". This step latches the contents, on the Address Bus pins, A[6:0], into the Framer Microprocessor Interface block. At this point, the initial address of the burst access has now been selected.

NOTE: *The ALE_AS input pin should remain "Low" for the remainder of this Burst Access operation.*

A.5 Next, the µC/µP should indicate that this current bus cycle is a Read Operation by toggling the $\overline{RD}$_DS (Read Strobe) input pin "Low". This action also enables the bi-directional data bus output drivers of the Framer. At this point, the bi-directional data bus output drivers will proceed to drive the contents of the addressed register onto the bi-directional data bus, D[7:0].

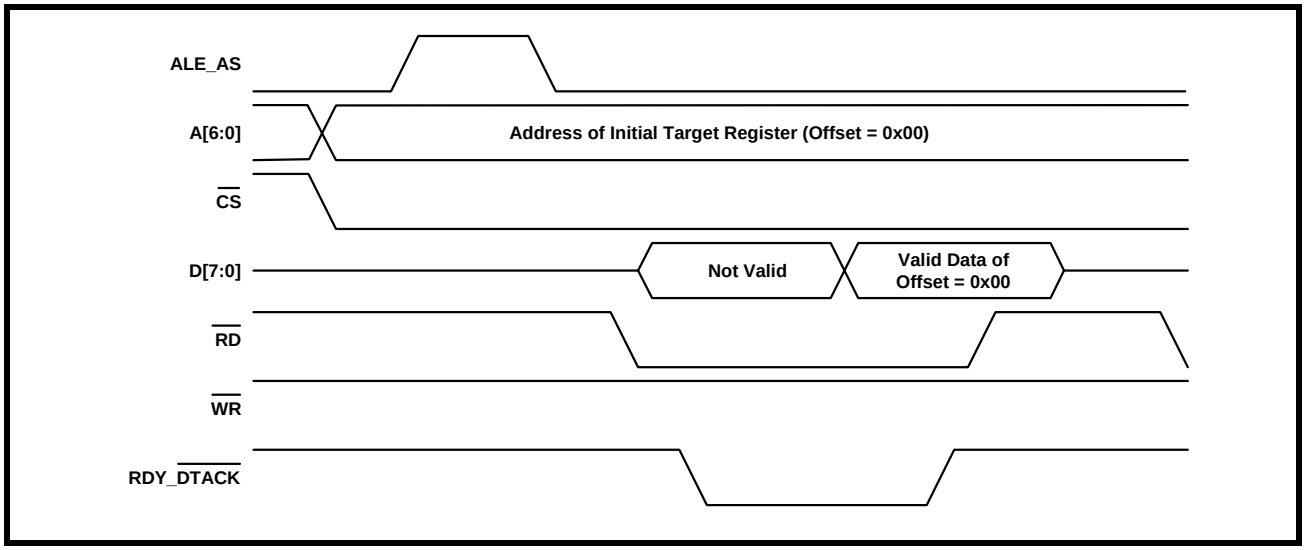
A.6 Immediately after the µC/µP toggles the Read Strobe signal "Low", the Framer will toggle the RDY_$\overline{DTACK}$ (READY) output pin "Low". The Framer does this in order to inform the µC/µP that the data (to be read from the data bus) is NOT READY to be latched into the µC/µP.

A.7 After some settling time, the data on the bi-directional data bus will stabilize and can be read by the µC/µP. The Framer will indicate that this data is ready to be read, by toggling the RDY_$\overline{DTACK}$ (Ready) signal "High".

A.8 After the µC/µP detects the RDY_$\overline{DTACK}$ signal (from the Framer), it can then will terminate the Read cycle by toggling the $\overline{RD}$_DS (Read Strobe) input pin "High".

Figure 8 presents an illustration of the behavior of the Microprocessor Interface Signals, during the initial Read Operation, within a Burst I/O Cycle for an Intel-type µC/µP.

FIGURE 8. INTEL µP INTERFACE SIGNALS, DURING THE INITIAL READ OPERATION OF A BURST CYCLE



At the completion of this initial read cycle, the µC/µP has read in the contents of the first register or buffer location (within the Framer) for this particular burst I/O access operation. In order to illustrate how this burst access

operation works, the byte (or word) of data, that is being read in Figure 8, has been labeled Valid Data at Offset = 0x00. This label indicates that the µC/µP is reading the very first register (or buffer location) in this burst access operation.

1.3.2.3.1.1.2 Subsequent Read Operations

The procedure that the µC/µP must use to perform the remaining read cycles, within this Burst Access operation, is presented below.

B.0 Execute each subsequent Read Cycles, as described in steps 1 through 3 below.

B.1 Without toggling the ALE_AS input pin (e.g., keeping it "Low"), toggle the $\overline{RD}$_DS input pin "Low". This step accomplishes the following.

- **a.** The Framer will internally increments the latched address value (within the Microprocessor Interface circuitry).
- **b.** The output drivers of the bi-directional data bus, D[7:0] are enabled. At some time later, the register or buffer location corresponding to the incremented latched address value will be driven onto the bi-directional data bus.

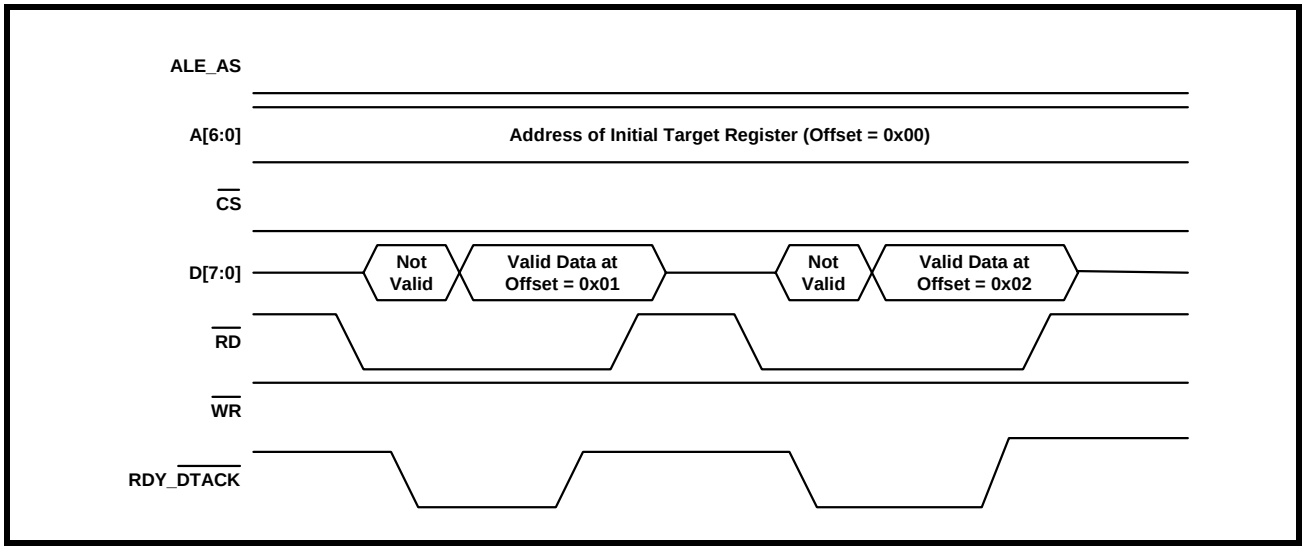
B.2 Immediately after the Read Strobe pin toggles "Low" the Framer will toggle the RDY_$\overline{DTACK}$ (READY) output pin "Low" to indicate its NOT READY status.

B.3 After some settling time, the data on the bi-directional data bus will stabilize and can be read by the µC/µP. The Framer will indicate that this data is ready to be read by toggling the RDY_$\overline{DTACK}$ (READY) signal "High".

B.4 After the µC/µP detects the RDY_$\overline{DTACK}$ signal (from the Framer), it can terminate the Read cycle by toggling the $\overline{RD}$_DS (Read Strobe) input pin "High".

For subsequent read operations, within this burst cycle, the µC/µP simply repeats steps 1 through 3, as illustrated in Figure 9.

FIGURE 9. INTEL µP INTERFACE SIGNALS, DURING SUBSEQUENT READ OPERATIONS OF A BURST I/O CYCLE



In addition to the behavior of the Microprocessor Interface signals, Figure 9 also illustrates other points regarding the Burst Access Operation.

- **a.** The Framer internally increments the address value, from the original latched value shown in Figure 8. This is illustrated by the data, appearing on the data bus, (for the first read access) being labeled Valid Data at Offset = 0x01 and that for the second read access being labeled Valid Data at Offset = 0x02.
- **b.** The Framer performs this address incrementing process even though there are no changes in the Address Bus Data, A[6:0].

1.3.2.3.1.1.3 Terminating the Burst Access Operation

The Burst Access Operation will be terminated upon the rising edge of the ALE_AS input signal. At this point the Framer will cease to internally increment the latched address value. Further, the µC/µP is now free to execute either a Programmed I/O access or to start another Burst Access Operation with the Framer.

1.3.2.3.1.2 Write Burst Access: Intel-Mode

When an Intel-type µC/µP wishes to write data into a contiguous range of addresses, then it should do the following.

a. Perform the initial write operation of the burst access.

b. Perform the remaining write operations, of the burst access.

c. Terminate the burst access operation.

Each of these operations within the burst access are described below.

1.3.2.3.1.2.1 Initial Write Operation

The initial write operation of an Intel-type Write Burst Access is accomplished by executing a Programmed I/O write cycle as summarized below.

A.0 Execute a Single Ordinary (Programmed I/O) Write cycle, as described in Steps A.1 through A.7 below.

A.1 Place the address of the initial target register (or buffer location) within the Framer, on the Address Bus pins, A[6:0].

A.2 At the same time, the Address-Decoding circuitry (within the user's system) should assert the $\overline{CS}$ (Chip Select) input pin of the Framer, by toggling it "Low". This step enables further communication between the µC/µP and the Framer Microprocessor Interface block.

A.3 Assert the ALE_AS (Address Latch Enable) input pin "High". This step enables the Address Bus input drivers, within the Microprocessor Interface Block of the Framer.

A.4 After allowing the data on the Address Bus pins to settle (by waiting the appropriate Address Setup time), the µC/µP should then toggle the ALE_AS input pin "Low". This step latches the contents, on the Address Bus pins, A[6:0], into the XRT84L38 Framer Microprocessor Interface block. At this point, the initial address of the burst access has now been selected.

NOTE: *The ALE_AS input pin should remain "Low" for the remainder of this Burst I/O Access operation.*

A.5 Next, the µC/µP should indicate that this current bus cycle is a Write operation by keeping the $\overline{RD}$_DS pin "High" and toggling the $\overline{WR}$_R/$\overline{W}$ (Write Strobe) pin "Low". This action also enables the bi-directional data bus input drivers of the Framer.

A.6 The µC/µP places the byte (or word) that it intends to write into the target register on the bi-directional data bus, D[7:0].

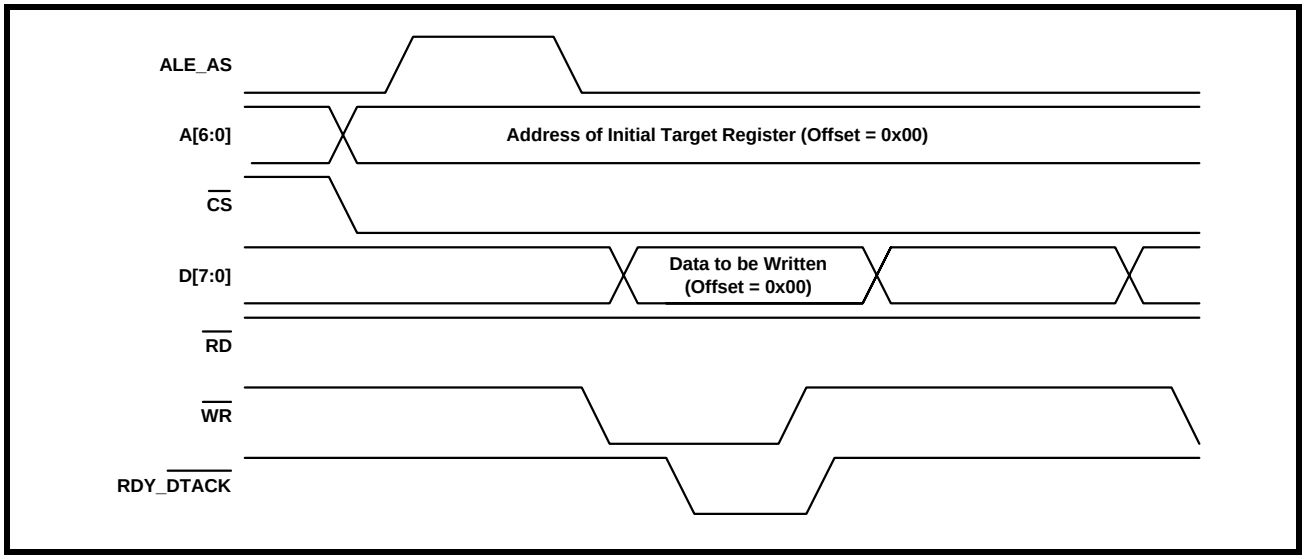
A.7 After waiting the appropriate amount of time, for the data (on the bi-directional data bus) to settle, the µC/µP should toggle the $\overline{WR}$_R/$\overline{W}$ (Write Strobe) input pin "High". This action accomplishes two things.

a. It latches the contents of the bi-directional data bus into the Framer Microprocessor Interface Block.

b. It terminates the write cycle.

Figure 10 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals, during the initial write operation within a Burst Access, for an Intel-type µC/µP.

FIGURE 10. INTEL µP INTERFACE SIGNALS, DURING THE INITIAL WRITE OPERATION OF A BURST CYCLE



At the completion of this initial write cycle, the µC/µP has written a byte or word into the first register or buffer location (within the Framer) for this particular burst access operation. In order to illustrate this point, the byte (or word) of data, that is being written in Figure 10 has been labeled Data to be Written (Offset = 0x00).

1.3.2.3.1.2.2 The Subsequent Write Operations

The procedure that the µC/µP must use to perform the remaining write cycles, within this burst access operation, is presented below.

B.0 Execute each subsequent write cycle, as described in steps B.1 through B.3.

B.1 Without toggling the ALE_AS input pin (e.g., keeping it "Low"), apply the value of the next byte or word (to be written into the Framer) to the bi-directional data bus pins, D[7:0].

B.2 Toggle the $\overline{WR}$_R/$\overline{W}$ (Write Strobe) input pin "Low". This step accomplishes two things.

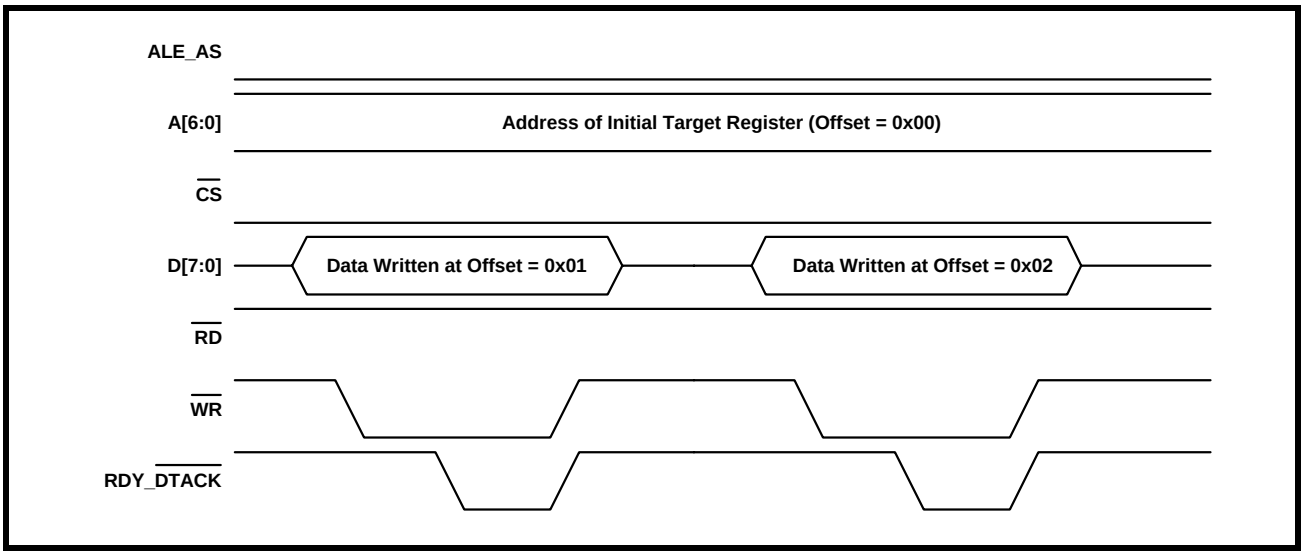
a. It enables the input drivers of the bi-directional data bus.

b. It causes the Framer to internally increment the value of the latched address.

B.3 After waiting the appropriate amount of settling time the data, in the internal data bus, will stabilize and is ready to be latched into the Framer Microprocessor Interface block. At this point, the µC/µP should latch the data into the Framer by toggling the $\overline{WR}$_R/$\overline{W}$ input pin "High".

For subsequent write operations, within this burst I/O access, the µC/µP simply repeats steps B.1 through B.3, as illustrated in Figure 11.

FIGURE 11. µP INTERFACE SIGNALS, DURING SUBSEQUENT WRITE OPERATIONS OF A BURST I/O CYCLE



1.3.2.3.1.2.3 Terminating the Burst I/O Access

Burst Access Operation will be terminated upon the rising edge of the ALE_AS input signal. At this point the Framer will cease to internally increment the latched address value. Further, the µC/µP is now free to execute either a Programmed I/O access or to start another Burst Access Operation with the XRT84L38 Framer.

1.3.2.3.2 Burst I/O Access: Motorola Mode

If the XRT84L38 Framer is interfaced to a Motorola-type µC/µP (e.g., the MC680x0 family, etc.), then it should be configured to operate in the Motorola mode (by tying the MOTO pin to VCC). Motorola-type Read and Write Burst I/O Access operations are described below.

1.3.2.3.2.1 Read Burst I/O Access Operation: Motorola-Mode

Whenever a Motorola-type µC/µP wishes to read the contents of numerous registers or buffer locations over a contiguous range of addresses, then it should do the following.

a. Perform the initial Read operation of the burst access.

b. Perform the remaining read operations in the burst access.

c. Terminate the burst access operation.

Each of these operations, within the Burst Access are discussed below.

1.3.2.3.2.1.1 Initial Read Operation: Motorola Mode

The initial read operation of a Motorola-type read burst access is accomplished by executing a Programmed I/O Read cycle, as summarized below.

A.0 Execute a Single Ordinary (Programmed I/O) Read Cycle, as described in steps A.1 through A.8 below.

A.1 Assert the ALE_AS ($\overline{AS}$) input pin by toggling it "Low". This step enables the Address Bus input drivers (within the Framer) within the Framer Microprocessor Interface Block.

A.2 Place the address of the initial target register or buffer location (within the Framer), on the Address Bus input pins, A[6:0].

A.3 At the same time, the Address-Decoding circuitry (within the user's system) should assert the $\overline{CS}$ (Chip Select) input pins of the Framer by toggling it "Low". This action enables further communication between the µC/µP and the Framer Microprocessor Interface block.

A.4 After allowing the data on the Address Bus pins to settle (by waiting the appropriate Address Setup time), the µC/µP should toggle the ALE_AS input pin "High". This step causes the Framer to latch the contents of the Address Bus into its internal circuitry. At this point, the initial address of the burst access has now been selected.

A.5 Further, the µC/µP should indicate that this cycle is a Read cycle by setting the $\overline{WR}$_R/$\overline{W}$ (R/$\overline{W}$) input pin "High".

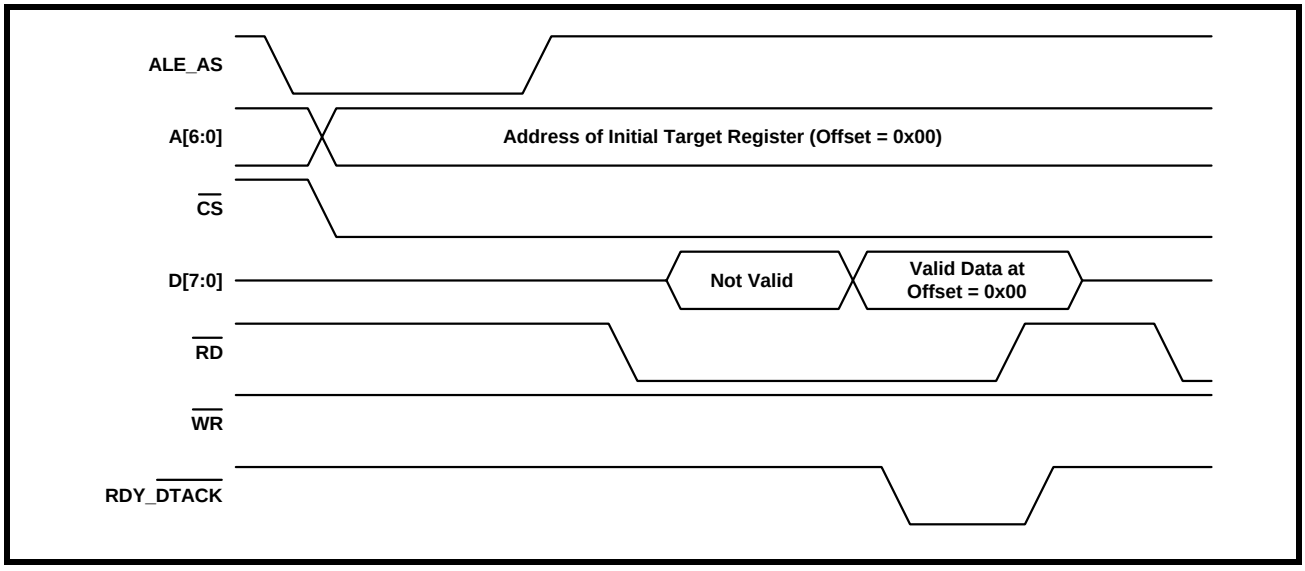
A.6 Next the µC/µP should initiate the current bus cycle by toggling the $\overline{RD}$_DS (Data Strobe) input pin "Low". This step will enable the bi-directional data bus output drivers, within the Framer. At this point, the bi-directional data bus output drivers will proceed to driver the contents of the Address register onto the bi-directional data bus.

A.7 After some settling time, the data on the bi-directional data bus will stabilize and can be read by the µC/µP. The Framer will indicate that this data can be read by asserting the RDY_$\overline{DTACK}$ (DTACK) signal “Low”.

A.8 After the µC/µP detects the RDY_$\overline{DTACK}$ signal (from the Framer) it will terminate the Read Cycle by toggling the $\overline{RD}$_DS (Data Strobe) input pin "High".

Figure 12 presents an illustration of the behavior of the Microprocessor Interface Signals during the initial Read Operation, within a Burst I/O Cycle, for a Motorola-type µC/µP.

FIGURE 12. MOTOROLA µP INTERFACE SIGNALS DURING THE INITIAL READ OPERATION OF A BURST CYCLE



At the completion of this initial read cycle, the µC/µP has read in the contents of the first register or buffer location (within the Framer) for this particular burst access operation. In order to illustrate how this burst I/O cycle

works, the byte (or word) of data, that is being read in Figure 12 has been labeled Valid Data at Offset = 0x00. This indicates that the µC/µP is reading the very first register (or buffer location) in this burst access.

1.3.2.3.2.1.2 Subsequent Read Operations

The procedure that the µC/µP must use to perform the remaining read cycles, within this Burst Access operation, is presented below.

B.0 Execute each subsequent Read Cycle, as described in steps B.1 through B.3, below.

B.1 Without toggling the ALE_AS input pin (e.g., keeping it "High"), toggle the $\overline{RD}$_DS (Data Strobe) input pin "Low". This step accomplishes the following.

a. The Framer internally increments the latched address value (within the Microprocessor Interface circuitry).

b. The output drivers of the bi-directional data bus (D[7:0]) are enabled. At some time later, the register or buffer location corresponding to the incremented latched address value will be driven onto the bi-directional data bus.

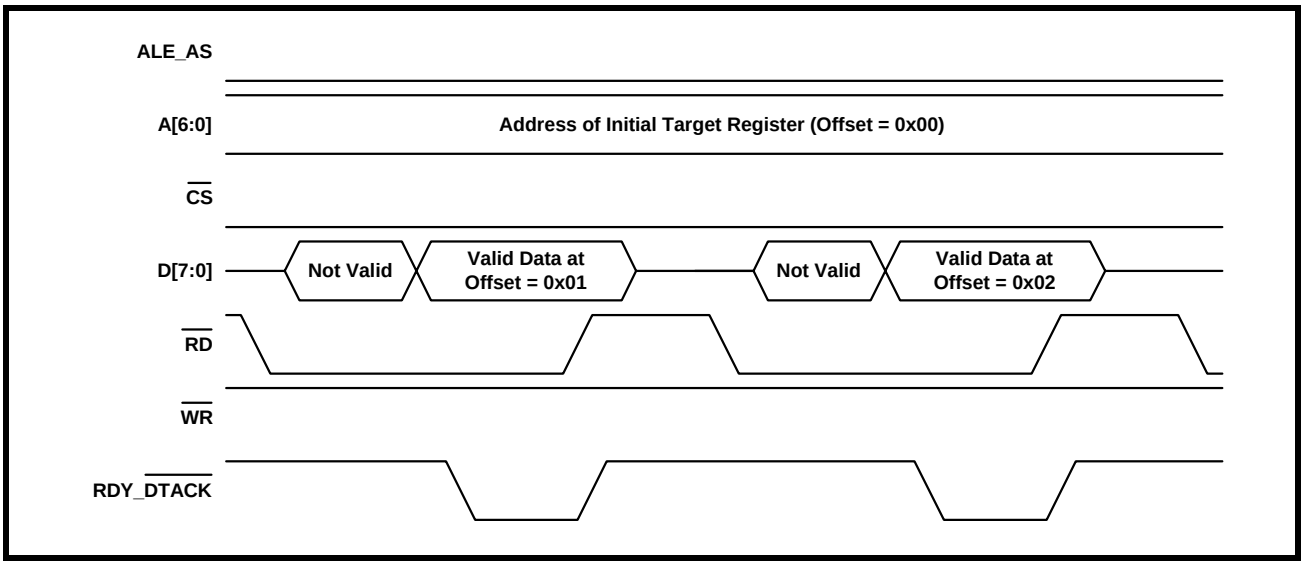
NOTE: *In order to insure that the Framer will interpret this signal as being a Read signal, the* µC/µP *should keep the* $\overline{WR}$_R/$\overline{W}$ *input pin "High".*

B.2 After some settling time, the data on the bi-directional data bus will stabilize and can be read by the µC/µP. The Framer will indicate that this data is ready to be read by asserting the RDY_$\overline{DTACK}$ (DTACK) signal “Low”.

B.3 After the µC/µP detects the RDY_$\overline{DTACK}$ signal (from the Framer), it terminates the Read cycle by toggling the $\overline{RD}$_DS (Data Strobe) input pin "High".

For subsequent read operations, within this burst cycle, the µC/µP simply repeats steps B.1 through B.3, as illustrated in Figure 13.

FIGURE 13. MOTOROLA µP INTERFACE SIGNALS, DURING SUBSEQUENT READ OPERATIONS OF A BURST I/O CYCLE



1.3.2.3.2.1.3 Terminating Burst Access Operation

The Burst I/O Access will be terminated upon the falling edge of the ALE_AS input signal. At this point the Framer will cease to internally increment the latched address value. Further, the µC/µP is now free to execute either a Programmed I/O access or to start another Burst Access Operation with the Framer.

1.3.2.3.2.2 Write Burst Access: Motorola-Mode

Whenever a Motorola-type µC/µP wishes to write the contents of numerous registers or buffer locations over a contiguous range of addresses, then it should do the following.

a. Perform the initial write operation of the burst access.

b. Perform the remaining write operations, of the burst access.

c. Terminate the burst access operation.

1.3.2.3.2.2.1 Initial Write Operation

The initial write operation of a Motorola-type Write Burst Access is accomplished by executing a Programmed I/O Write Cycle as summarized below.

A.0 Execute a Single Ordinary (Programmed I/O) Write cycle, as described in Steps A.1 through A.7 below.

A.1 Assert the ALE_AS (Address Strobe) input pin by toggling it "Low". This step enables the Address Bus input drivers (within the Framer).

A.2 Place the address of the initial target register or buffer location (within the Framer), on the Address Bus input pins, A[6:0].

A.3 At the same time, the Address-Decoding circuitry (within the user's system) should assert the $\overline{CS}$ input pin of the Framer by toggling it "Low". This step enables further communication between the µC/µP and the Framer Microprocessor Interface block.

A.4 After allowing the data on the Address Bus pins to settle (by waiting the appropriate Address Setup time), the µC/µP should toggle the ALE_AS input pin "High". This step causes the Framer to latch the contents of the Address Bus into its own circuitry. At this point, the initial address of the burst access has now been selected.

A.5 Further, the µC/µP should indicate that this current bus cycle is a Write operation by toggling the $\overline{WR}$_R/$\overline{W}$ (R/$\overline{W}$) input pin "Low".

A.6 The µC/µP should then place the byte or word that it intends to write into the target register, on the bi-directional data bus, D[7:0].

A.7 Next, the µC/µP should initiate the bus cycle by toggling the $\overline{RD}$_DS (Data Strobe) input pin "Low". When the XRT84L38 Framer senses that the $\overline{WR}$_R/$\overline{W}$ input pin is "Low", and that the $\overline{RD}$_DS input pin has toggled "Low" it will enable the input drivers of the bi-directional data bus, D[7:0].

A.8 After waiting the appropriate amount of time, for this newly placed data to settle on the bi-directional data bus (e.g., the Data Setup time) the Framer will assert the RDY_$\overline{DTACK}$ (DTACK) output signal.

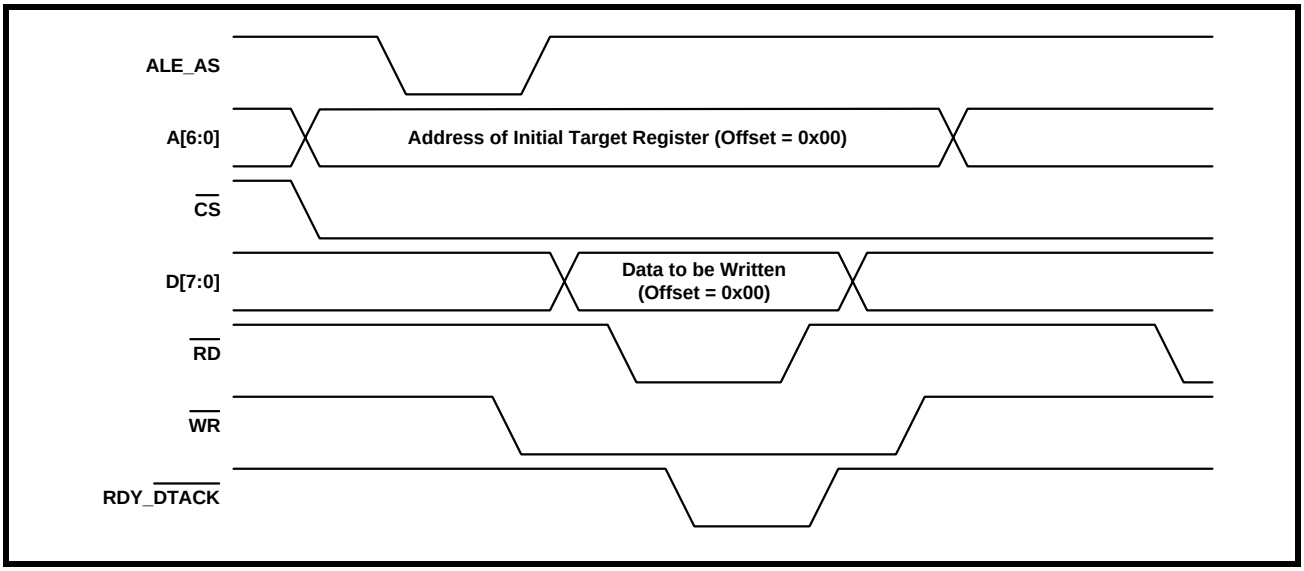
A.9 After the µP/µC detects the RDY_$\overline{DTACK}$ signal (from the Framer) it should toggle the $\overline{RD}$_DS input pin "High". This action accomplishes two things:

a. It latches the contents of the bi-directional data bus into the Framer Microprocessor Interface block.

b. It terminates the Write cycle.

Figure 14 presents a timing diagram which illustrates the behavior of the Microprocessor Interface signals, during the Initial write operation within a Burst Access, for a Motorola-type µC/µP.

FIGURE 14. MOTOROLA µP INTERFACE SIGNALS, DURING THE INITIAL WRITE OPERATION OF A BURST CYCLE



At the completion of this initial write cycle, the µC/µP has written a byte or word into the first register or buffer location (within the Framer) for this particular burst I/O access. In order to illustrate how this burst I/O cycle works, the byte (or word) of data, that is being written in Figure 14 has been labeled Data to be Written (Offset = 0x00).

1.3.2.3.2.2.2 The Subsequent Write Operations

The procedure that the µC/µP must use to perform the remaining write cycles, within this burst access operation, is presented below.

B.0 Execute each subsequent write cycle, as described in steps B.1 through B.3.

B.1 Without toggling the ALE_AS input pin (e.g., keeping it "Low"), apply the value of the next byte or word (to be written into the Framer) to the bi-directional data bus pins, D[7:0].

B.2 Toggle the $\overline{WR}$_R/$\overline{W}$ (Write Strobe) input pin "Low". This step accomplishes two things.

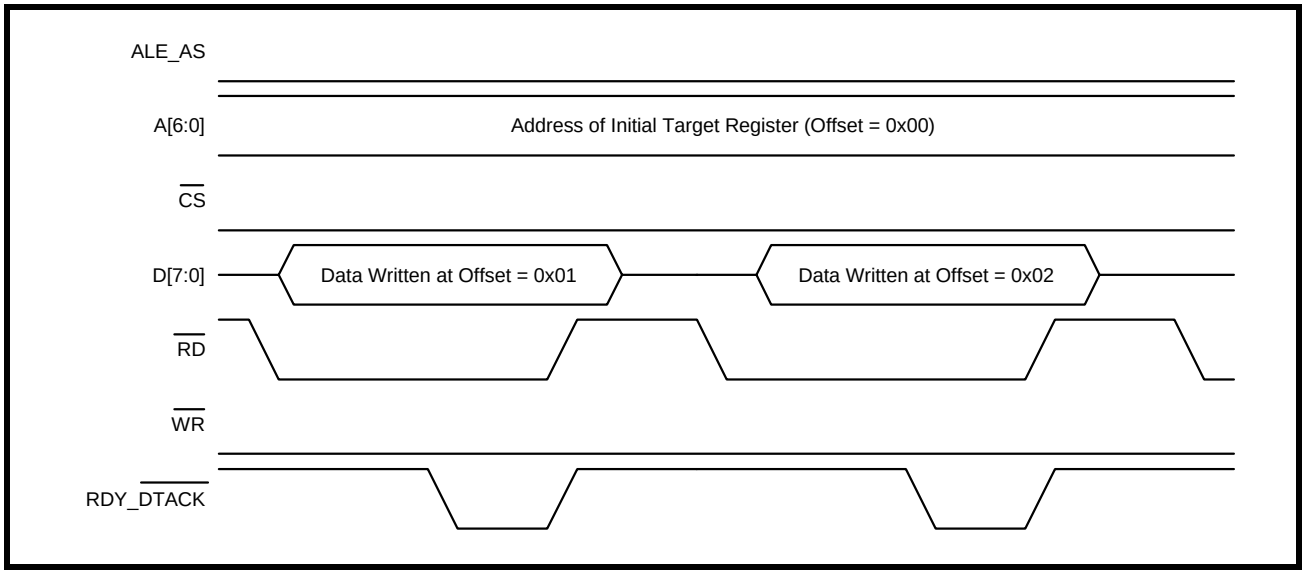
a. It enables the input drivers of the bi-directional data bus.

b. It causes the Framer to internally increment the value of the latched address.

B.3 After waiting the appropriate amount of settling time the data, in the internal data bus, will stabilize and is ready to be latched into the Framer Microprocessor Interface block. At this point, the µC/µP should latch the data into the Framer by toggling the $\overline{WR}$_R/$\overline{W}$ input pin "High".

For subsequent write operations, within this burst I/O access, the µC/µP simply repeats steps B.1 through B.3, as illustrated in Figure 15.

FIGURE 15. MOTOROLA µP INTERFACE SIGNALS DURING SUBSEQUENT WRITE OPERATIONS OF A BURST I/O CYCLE



1.3.2.3.2.2.3 Terminating the Burst I/O Access

The Burst I/O Access will be terminated upon the falling edge of the ALE_AS input signal. At this point the Framer will cease to internally increment the latched address value. Further, the µC/µP is now free to execute either a Programmed I/O access or to start another Burst I/O Access with the Framer.

1.4 DMA READ/WRITE OPERATIONS

The XRT84L38 Framer contains two DMA Controller Interfaces which provide support for all eight framers within the chip. The purpose of the two DMA Controllers is to facilitate the rapid block transfer of data between an external memory location and the on-chip HDLC buffers via the Microprocessor Interface.

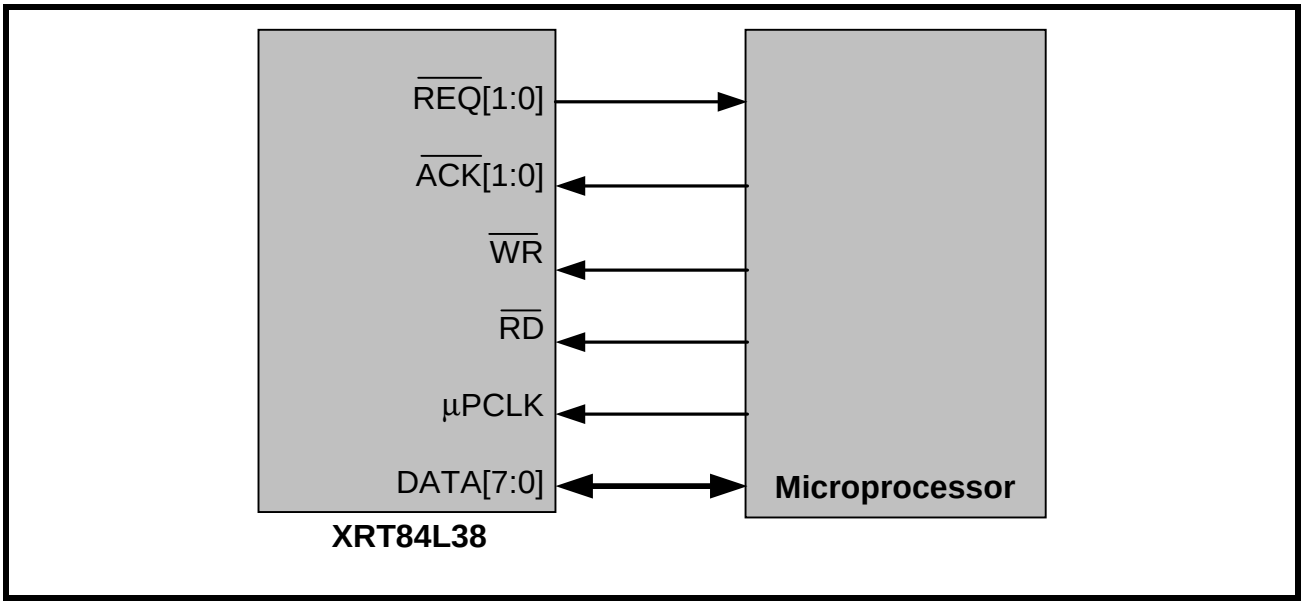
DMA-0 WRITE DMA INTERFACE

DMA 0 Controller Interface handles data transfer between external memory and the selected Transmit HDLC Buffer.

The DMA cycle starts when the XRT84L38 asserts the $\overline{REQ}$0 output pin. The external DMA Controller then responds by asserting the $\overline{ACK0}$ input pin. The contents of the Microprocessor Interface bi-directional data bus are latched into the XRT84L38 each time the pWRL (Write Strobe) input pin is strobed “Low”.

The XRT84L38 ends the DMA cycle by negating the DMA request input ($\overline{REQ0}$) while $\overline{WR}$ is still active. The external DMA Controller acknowledges the end of DMA Transfer by driving the $\overline{ACK0}$ input pin “High”.

FIGURE 16. DMA MODE FOR THE XRT84L38 AND A MICROPROCESSOR



1.5 MEMORY AND REGISTER MAP

This section presents a complete list of the Framer external memory address map and the internal memory map. In addition, the allocations of the three internal storage spaces is depicted.

1.5.1 Memory Mapped I/O Indirect Addressing

The XRT84L38 employs a complete indirect addressing approach for the Microprocessor Interface; in order to support multiple channel implementations, maintaining rich user-controlled features, minimizing the total pin count and providing future scalability without sacrificing performance for microcontroller access. Eight address bits are used with the 4 MSB (most significant bits) identifying each of the eight framers channels and the 4 LSBs to address the indirect mapping registers.

The XRT84L38 framer has approximately 5,800 addressable spaces internally. If each of these addresses has to be accessed directly, it would require a 13-bit address bus. In order to control total pin count as well as to provide future scalability, the XRT84L38 employs an Indirect Addressing Scheme. Using this technique, only 7 address input pins on the XRT84L38 are needed.

The addressable spaces within the XRT84L38 are divided into groups of registers. Each register group consists of a specific number of indirect address registers and a same number of indirect data registers with the exception of LAPD Buffer 0 and 1. Of the 7 total address input bits, the 3 MSB pins are used to identify each of eight T1/E1 framer channels. The remaining 4 LSB bits are used to address the register groups. Table 8 indicates the address mapping of all the register groups within the XRT84L38. Please note that the indirect address registers are with even addresses and the corresponding indirect data registers are with odd addresses with the exception of, again, the LAPD Buffer 0 and 1. The n corresponds to the channel number.

TABLE 8: ADDRESS MAP

ADDRESS	CONTENTS
n_0H	Channel_n - Control Register Indirect Address Register
n_1H	Channel_n - Control Register Indirect Data Register
n_2H	Channel_n - Channel Control Indirect Address Register
n_3H	Channel_n - Channel Control Indirect Data Register
n_4H	Channel_n - Receive Signaling Array Indirect Address Register
n_5H	Channel_n - Receive Signaling Array Indirect Data Register
n_6H	Channel_n - LAPD Buffer 0 Indirect Data Register
n_7H	Channel_n - LAPD Buffer 1 Indirect Data Register
n_8H	Channel_n - Performance Monitor Indirect Address register
n_9H	Channel_n - Performance Monitor Indirect Data register
n_AH	Channel_n - Interrupt Indirect Address register
n_BH	Channel_n - Interrupt Indirect Data register
n_CH - n_FH	Reserved

To access each individual register inside each group, a two-step access by the micro-controller to the XRT84L38 is required. In the first step, a micro-controller WRITE access specifying the indirect address for that register within the register group should be done to the indirect address register of that group. In the second step, a micro-controller READ or WRITE should access the indirect data register of that group. For example, in order to write 0DH into the Framing Select Register of Channel 5 (address 0x50H>07H), one needs to do the following:

WR 0x50 0x07

Write 0x07Hex into the indirect address register (0x50Hex) to specify address of the Framing Select Register within the Control Register group.

WR 0x51 0x0D

Actually WRITE value 0x0DHex into the indirect data register (0x51Hex) of the Control Register group.

The value of the indirect address register will increment after each access of the corresponding indirect data register. Using the above example for illustration, after WRITE to the indirect data register (0x51Hex), the value stored inside the indirect address register (0x50Hex) would become 0x08Hex. This feature can greatly enhance the users' ability to access consecutive locations within a certain register group.

For LAPD Buffer 0 and 1 with addresses 0x06Hex and 0x07Hex respectively, there is no indirect address register. A micro-controller WRITE access to these data registers will access the LAPD Transmit Buffers and a micro-controller READ will access the LAPD Receive Buffers. The very first access of the LAPD buffers will always to location 0. After each access, the pointer within the LAPD buffer will automatically increment by one, making further access to the next location within the buffer. User should keep track of the current location inside the buffer the READ or WRITE is associated with.

1.6 DESCRIPTION OF THE CONTROL REGISTERS

Clock Select Register (CSR) - T1 Mode(Indirect Address = 0xn0H, 0x00H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Bipolar Violation Insertion	T1, E1 Select	8KHz Synchroniza-tion Enable	Clock Loss Detection Enable	OSCCLK Frequency Select Bit 1	OSCCLK Frequency Select Bit 0	Transmit Timing Source Select Bit 1	Transmit Timing Source Select Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	1	0	0	0	1

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Bipolar Violation Insertion	R/W	**Bipolar Violation Insertion:** This READ/WRITE bit-field permits the user to insert Bipolar Violation to the transmit encoder. The line coding for the DS1 signal should be bipolar. This signaling technique consists of transmitting a binary "0" as zero volts, while a binary "1" is transmitted as either a positive or negative pulse, opposite in polarity to the previous pulse. A Bipolar Violation occurs when the alternate polarity rule is violated. A zero-to-one transition of the bit will cause one Bipolar Violation to be inserted into the outgoing data stream.
6	T1/E1 Select	R/W	**T1/E1 Select:** This READ/WRITE bit-field permits the user to select which mode the framer will be operating. When this bit is set to one: The framer is in T1 mode. When this bit is set to zero: The framer is in E1 mode.
5	8KHz Synchronization Enable	R/W	**8KHz Synchronization Enable:** This READ/WRITE bit-field permits the user to activate and deactivate the 8KHz synchronization of the framer. An 8KHz external reference clock can be provided to the framer. When this bit is set to one: If the Transmit Clock Source Select bits are set to two, the transmit clocks of all eight channels will be synchronized to the external applied 8KHz reference clock and thus have the same frequency and the same phase.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Clock Loss Detection Enable	R/W	**Clock Loss Detection Enable:** This READ/WRITE bit-field permits the user to enable the Clock Loss Detection logic for the framer when the Recovered Receive Line Clock is used as transmit timing source of the framer. When this bit is set to zero: The framer disables the Clock Loss Detection logic. When this bit is set to one: The framer enables the Clock Loss Detection logic. If the Recovered Receive Line Clock is used as transmit timing source of the framer, and if clock recovered from the LIU is lost, the framer can detect loss of the Recovered Receive Line Clock. Upon detecting of this occurrence, the framer will automatically begin to use the OSCCLK Driven Divided clock as transmit timing source until the LIU is able to regain clock recovery. ***NOTE:*** *This bit-field is ignored if the TxSerClk or the OSCCLK Driven Divided clock is chosen to be the timing source of Transmit Section of the framer.*
3-2	OSCCLK Frequency Select	R/W	**OSCCLK Frequency Select:** These two READ/WRITE bit-fields permit the user to select internal clock dividing logic of the framer depending on the frequency of incoming oscillator clock (OSCCLK). The frequency of internal clock used by the framer should be 12.352MHz. When these bits are set to 00: The framer will internally divide the incoming OSCCLK by one. Therefore, the external oscillator clock applied to the OSCCLK pin should be 12.352MHz. When these bits are set to 01: The framer will internally divide the incoming OSCCLK by two. Therefore, the external oscillator clock applied to the OSCCLK pin should be 24.704MHz. When these bits are set to 10: The framer will internally divide the incoming OSCCLK by four. Therefore, the external oscillator clock applied to the OSCCLK pin should be 49.408MHz.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Timing Source Select	R/W	**Transmit Timing Source Select:** These two READ/WRITE bit-fields permit the user to select the timing source of Transmit section of the framer. When the framer is operating at non-multiplexed mode, that is, the Transmit Back-plane interface is operating at a clock rate of 1.544MHz for T1, these two READ/WRITE bit-fields also determine the direction of Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk). When the framer is operating at other Back-plane mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all inputs. When these bits are set to 00: The Recovered Receive Line Clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 1.544MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all outputs. Upon losing of the Recovered Receiver Line Clock, the OSCCLK Driven Divided clock is automatically chosen to be the timing source of the Transmit section of the framer. When these bits are set to 01: The Transmit Serial Clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 1.544MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all inputs. When these bits are set to 10: The OSCCLK Driven Divided clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 1.544MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all outputs. Upon losing of the Recovered Receiver Line Clock, the OSCCLK Driven Divided clock is automatically chosen to be the timing source of the Transmit section of the framer. When these bits are set to 11: The Recovered Receive Line Clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 1.544MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all outputs. Upon losing of the Recovered Receiver Line Clock, the OSCCLK Driven Divided clock is automatically chosen to be the timing source of the Transmit section of the framer.

Clock Select Register (CSR) - E1 Mode (Indirect Address = 0xn0H, 0x00H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Bipolar Violation Insertion	T1, E1 Select	8KHz Synchroniza-tion Enable	Clock Loss Detection Enable	OSCCLK Frequency Select Bit 1	OSCCLK Frequency Select Bit 0	Transmit Timing Source Select Bit1	Transmit Timing Source Select Bit0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	1	0	0	0	1

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Bipolar Violation Insertion	R/W	**Bipolar Violation Insertion:** This READ/WRITE bit-field permits the user to insert Bipolar Violation to the transmit encoder. The line coding for the DS1 signal should be bipolar. This signaling technique consists of transmitting a binary "0" as zero volts, while a binary "1" is transmitted as either a positive or negative pulse, opposite in polarity to the previous pulse. A Bipolar Violation occurs when the alternate polarity rule is violated. A zero-to-one transition of the bit will cause one Bipolar Violation to be inserted into the outgoing data stream.
6	T1/E1 Select	R/W	**T1/E1 Select:** This READ/WRITE bit-field permits the user to select which mode the framer will be operating. When this bit is set to one: The framer is in T1 mode. When this bit is set to zero: The framer is in E1 mode.
5	8KHz Synchronization Enable	R/W	**8KHz Synchronization Enable:** This READ/WRITE bit-field permits the user to activate and deactivate the 8KHz synchronization of the framer. An 8KHz external reference clock can be provided to the framer. When this bit is set to one: If the Transmit Clock Source Select bits are set to two, the transmit clocks of all eight channels will be synchronized to the external applied 8KHz reference clock and thus have the same frequency and the same phase.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Clock Loss Detection Enable	R/W	**Clock Loss Detection Enable:** This READ/WRITE bit-field permits the user to enable the Clock Loss Detection logic for the framer when the Recovered Receive Line Clock is used as transmit timing source of the framer. When this bit is set to zero: The framer disables the Clock Loss Detection logic. When this bit is set to one: The framer enables the Clock Loss Detection logic. If the Recovered Receive Line Clock is used as transmit timing source of the framer, and if clock recovered from the LIU is lost, the framer can detect loss of the Recovered Receive Line Clock. Upon detecting of this occurrence, the framer will automatically begin to use the OSCCLK Driven Divided clock as transmit timing source until the LIU is able to regain clock recovery. ***NOTE:*** *This bit-field is ignored if the TxSerClk or the OSCCLK Driven Divided clock is chosen to be the timing source of Transmit Section of the framer.*
3-2	OSCCLK Frequency Select	R/W	**OSCCLK Frequency Select:** These two READ/WRITE bit-fields permit the user to select internal clock dividing logic of the framer depending on the frequency of incoming oscillator clock (OSCCLK). The frequency of internal clock used by the framer should be 16.384MHz. When these bits are set to 00: The framer will internally divide the incoming OSCCLK by one. Therefore, the external oscillator clock applied to the OSCCLK pin should be 16.384MHz. When these bits are set to 01: The framer will internally divide the incoming OSCCLK by two. Therefore, the external oscillator clock applied to the OSCCLK pin should be 32.768MHz. When these bits are set to 10: The framer will internally divide the incoming OSCCLK by four. Therefore, the external oscillator clock applied to the OSCCLK pin should be 65.536MHz.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Timing Source Select	R/W	**Transmit Timing Source Select:** These two READ/WRITE bit-fields permit the user to select the timing source of Transmit section of the framer. When the framer is operating at non-multiplexed mode, that is, the Transmit Back-plane interface is operating at a clock rate of 2.048MHz for T1, these two READ/WRITE bit-fields also determine the direction of Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk). When the framer is operating at other Back-plane mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all inputs. When these bits are set to 00: The Recovered Receive Line Clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 2.048MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all outputs. Upon losing of the Recovered Receiver Line Clock, the OSCCLK Driven Divided clock is automatically chosen to be the timing source of the Transmit section of the framer. When these bits are set to 01: The Transmit Serial Clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 2.048MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all inputs. When these bits are set to 10: The OSCCLK Driven Divided clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 2.048MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all outputs. Upon losing of the Recovered Receiver Line Clock, the OSCCLK Driven Divided clock is automatically chosen to be the timing source of the Transmit section of the framer. When these bits are set to 11: The Recovered Receive Line Clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 2.048MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all outputs. Upon losing of the Recovered Receiver Line Clock, the OSCCLK Driven Divided clock is automatically chosen to be the timing source of the Transmit section of the framer.

Line Interface Control Register (LICR) - T1 Mode (Indirect Address = 0xn0H, 0x01H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Force Transmit LOS	NRZ Rail Select	Loop-back Select Bit 1	Loop-back Select Bit 0	Transmit Line Clock Inversion	Receive Line Clock Inversion	Transmit B8ZS Enable	Receive B8ZS Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Force Transmit LOS	R/W	**Force Transmit LOS:** This READ/WRITE bit-field forces the framer to transmit Loss of Signal (LOS) onto the LIU interface. When this bit is set to one: The framer is forced to transmit an LOS signal onto the LIU interface outputs.
6	NRZ Rail Select	R/W	**NRZ Rail Select:** This READ/WRITE bit-field permits the user to select how data are transmitted to and received from the LIU. When this bit is set to zero: The framer is operating in dual-rail mode. The TxPOS pin is carrying the positive data and the TxNEG pin is carrying the negative data. The positive and the negative data combined represent the entire data stream going to the LIU. The received data from the LIU will also be bipolar, that is, the positive data received from RxPOS and the negative data received from RxNEG combined represent the entire data stream. When this bit is set to one: The framer is operating in single-rail mode. The TxPOS pin is carrying the entire data stream. The TxNEG pin is carrying the Multi-frame Synchronization Pulse. The received data from the LIU will also be single-railed. The RxPOS pin is carrying the entire data stream going into the framer from LIU.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	Loop-back Select	R/W	**Loop-back Select:** These READ/WRITE bit-fields permit the user to configure any channel of the framer to operate in different loop-back modes. Each channel of the framer can operate in three loop-back modes: Local Loop-back (LL), Far-End Line Loop-back (FELL) and Payload Loop-back (PL).Local Loop-back connects the transmitter output of the framer back to the receiver input. All payload data as well as data link bits and Frame Alignment bits are directed back into the framer. The Local-Loop-back allows the performance of diagnostic tests on the transmitter and receiver to verify operation of the framer and equipment-side circuitry. Payload Loop-back also connects the transmitter output of the framer back to the receiver input. However, only payload data and Frame Alignment bits are directed back into the framer. The framer can still transmit data link information to the remote terminal. The Payload Loop-back allows the performance of diagnostic tests on the transmitter and receiver to verify operation of the framer and equipment-side circuitry. At the same time, the Payload Loop-back allows performance report and test signal identification message to be sent to remote side. Far-End Line Loop-back connects the receiver input to the transmit output. Only the LIU interface logic inside the framer can be examined using this loop-back mode. During the Far-End Line Loop-back, the Recovered Receive Line Clock will automatically be the source of the Transmit Line Clock. When these bits are set to 00: The framer is operating in normal mode; no loop-back mode is selected. When these bits are set to 01: The framer is operating in Local Loop-back mode. When these bits are set to 10: The framer is operating in Far-End Line Loop-back mode. When these bits are set to 11: The framer is operating in Payload Loop-back mode.
3	Transmit Line Clock Inversion	R/W	**Transmit Line Clock Inversion:** This READ/WRITE bit-field permits the user to select which edge of the Transmit Line Clock will data transition occur. When this bit is set to zero: The transmit data transition occurs at rising edge of the Transmit Line Clock. The user should program the LIU device to sample data at falling edge of the Transmit Line Clock. When this bit is set to one: The transmit data transition occurs at falling edge of the Transmit Line Clock. The user should program the LIU device to sample data at rising edge of the Transmit Line Clock.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Line Clock Inversion	R/W	**Receive Line Clock Inversion:** This READ/WRITE bit-field permits the user to select which edge of the Receive Line Clock will be used by the framer to sample incoming data from LIU. When this bit is set to zero: The receive data transition occurs at rising edge of the Receive Line Clock. The framer will sample data at falling edge of the Receive Line Clock. When this bit is set to one: The receive data transition occurs at falling edge of the Receive Line Clock. The frame will sample data at rising edge of the Receive Line Clock.
1	Transmit B8ZS Enable	R/W	**Transmit B8ZS Enable:** This READ/WRITE bit-field permits the user to enable transmit B8ZS encoding. When this bit is set to zero: The framer will send out transmit data encoded by B8ZS. The user should turn off the B8ZS encoding of the LIU device. When this bit is set to one: The framer will send out transmit data in AMI line code without B8ZS encoding. The user should turn on or off B8ZS encoding of the LIU device depending on system requirement.
0	Receive B8ZS Enable	R/W	**Receive B8ZS Enable:** This READ/WRITE bit-field permits the user to enable receive B8ZS decoding. When this bit is set to zero:The framer will decode the incoming data assuming that they are B8ZS encoded.When this bit is set to one:The framer disables B8ZS decoding of the incoming data.

Line Control Register (LCR) (Indirect Address = 0xn0H, 0x02H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
GPIO Direction Control Bit 3	GPIO Direction Control Bit 2	GPIO Direction Control Bit 1	GPIO Direction Control Bit 0	GPIO Bit 3	GPIO Bit 2	GPIO Bit 1	GPIO Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	1	1	1	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-4	GPIO Direction Control	R/W	**GPIO Direction Control:** These READ/WRITE bit-fields control directions of the four on-chip General Purpose Input/Output pins. When these bits are set to zero: The corresponding GPIO pins are configured as inputs. The user can now apply signals to the GPIO pins by writing to the corresponding GPIO bit-fields. When these bits are set to one: The corresponding GPIO pins are configured as outputs. The user can read the output values by reading the corresponding GPIO bit-fields.
3-0	GPIO	R/W	**GPIO:** These READ/WRITE bit-fields contain values of the four on-chip General Purpose Input/Output pins. When the corresponding GPIO Direction Control bit-fields are set to zero, the GPIO pins are configured as inputs. The GPIO bit-fields contain values to be present on the GPIO pins. For example, if the user wants to pull the pin GPIO_0 HIGH, he/she can write zero into the GPIO Direction Control Bit 0; then write one into the GPIO Bit 0. When the corresponding GPIO Direction Control bit-fields are set to one, the GPIO pins are configured as outputs. The GPIO bit-fields contain values currently present on the GPIO pins.

LIU Access Register 1 (LAR1) (Indirect Address = 0xn0H, 0x03H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
LAR1 Bit 7	LAR1 Bit 6	LAR1 Bit 5	LAR1 Bit 4	LAR1 Bit 3	LAR1 Bit 2	LAR1 Bit 1	LAR1 Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	LAR1	R/W	

LIU Access Register 2 (LAR2) (Indirect Address = 0xn0H, 0x04H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
LAR2 Bit 7	LAR2 Bit 6	LAR2 Bit 5	LAR2 Bit 4	LAR2 Bit 3	LAR2 Bit 2	LAR2 Bit 1	LAR2 Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	LAR2	R/W	

LIU Poll Register 1 (LPR1) (Indirect Address = 0xn0H, 0x05H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
LPR1 Bit 7	LPR1 Bit 6	LPR1 Bit 5	LPR1 Bit 4	LPR1 Bit 3	LPR1 Bit 2	LPR1 Bit 1	LPR1 Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	LPR1	R/W	

LIU Poll Register 2 (LPR2) (Indirect Address = 0xn0H, 0x06H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
LPR2 Bit 7	LPR2 Bit 6	LPR2 Bit 5	LPR2 Bit 4	LPR2 Bit 3	LPR2 Bit 2	LPR2 Bit 1	LPR2 Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	LPR2	R/W	

Framing Select Register (FSR) - T1 Mode (Indirect Address = 0xn0H, 0x07H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Signaling Update on Super-frame Boundary	CRC Diagnostics Select	J1 CRC Calculation	One Synchroniza-tion Candidate Only	Fast Synchroniza-tion	T1 Framing Select Bit 2	T1 Framing Select Bit 1	T1 Framing Select Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Signaling Update on Super-frame Boundary	R/W	**Signaling Update on Super-frame Boundary:** This READ/WRITE bit-field controls the framer to update signaling data only on Super-frame boundaries. The user can insert signaling data to the framer through the TxSIG_n input pins or by writing into the Transmit Signaling Control Registers (TSCR). When this bit is set to zero: The framer will update signaling data once it is received. That is, any value presents on the TxSIG_n pins or any value programmed to the TSCR will be inserted into the outgoing data stream right away. Also, any changes on the TxSIG_n pins or the TSCR will be instantaneously reflected on the outgoing data stream. When this bit is set to one: The framer will only update signaling data on super-frame boundaries. Any changes on the TxSIG_n pins or the TSCR will be ignored until the next super-frame boundary is reached.
6	CRC Diagnostics Select	R/W	**CRC Diagnostics Select:** This READ/WRITE bit-field allows the user to insert CRC errors into outgoing data stream. A transition from zero to one of this bit will prompt the framer to invert the value of one CRC bit. When this bit is set to zero: The framer will operate normally and there is no insertion of erroneous CRC bit. When this bit is set to one: One CRC error will be inserted into the outgoing data stream when this bit is transitioned from zero to one. ***NOTE:*** *To send another CRC error, the framer has to reset this bit to zero and set it to one again.*

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	J1 CRC Calculation	R/W	**J1 CRC Calculation:** This READ/WRITE bit-field forces the framer to calculate CRC-6 bits in J1 format.In J1 format, CRC-6 calculation is done based on the actual values of all payload bits as well as the framing bits. In DS1 format, CRC-6 calculation is done based on the payload bits only while assuming all the framing bits are one. When this bit is set to zero: The framer will perform CRC-6 calculation in DS1 format. When this bit is set to one: The framer will perform CRC-6 calculation in J1 format. This feature permits the driver to comply with J1 standard.
4	One Synchronization Candidate Only	R/W	**One Synchronization Candidate Only:** This READ/WRITE bit-field forces the framing search engine of the framer to declare synchronization while there is one and only one candidate left.
3	Fast Synchronization	R/W	**Fast Synchronization:** This READ/WRITE bit-field permits the framing search engine of the framer to declare synchronization earlier.
2-0	T1 Framing Select	R/W	**T1 Framing Select:** These READ/WRITE bit-fields allow the user to select one of the five T1 framing formats supported by the framer. These framing formats include ESF, SLC®96, SF, N and T1DM mode. **Framing Format** / **Bit 2** / **Bit 1** / **Bit 0** ESF / 0 / X / X SLC®96 / 1 / 0 / 0 SF / 1 / 0 / 1 N / 1 / 1 / 0 T1DM / 1 / 1 / 1 ***NOTE:*** *Changing of framing format will automatically force the framer to RESYNC.*

Framing Select Register (FSR) - E1 Mode (Indirect Address = 0xn0H, 0x07H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Annex B Enable	CRC Diagnostics Select	CAS Selection bit 1	CAS Selection bit 0	CRC-4 Selection bit 1	CRC-4 Selection bit 0	FAS Alignment Frame Check Sequence Enable	FAS Selection bit
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	1	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Annex B Enable	R/W	**Signaling Update on Super-frame Boundary:** This READ/WRITE bit-field controls the framer to be compliant with ITU-T Recommendation G.706 Annex B for CRC-to-non-CRC internetworking detection. When this bit is set to zero: The framer will operate in normal condition. That is, ITU-T G.706 Annex B is disabled. When this bit is set to one: The framer will enable support of ITU-T G.706 Annex B.
6	CRC Diagnostics Select	R/W	**CRC Diagnostics Select:** This READ/WRITE bit-field allows the user to insert CRC errors into outgoing data stream. A transition from zero to one of this bit will prompt the framer to invert the value of one CRC bit. When this bit is set to zero: The framer will operate normally and there is no insertion of erroneous CRC bit. When this bit is set to one: One CRC error will be inserted into the outgoing data stream when this bit is transitioned from zero to one.NOTE:To send another CRC error, the framer has to reset this bit to zero and set it to one again.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	CAS Selection bit	R/W	**CAS Selection:** These Read/Write bit fields allow the user to enable searching of CAS Multi-frame alignment and determine which algorithm of the two are used for locking the CAS Multi-frame alignment pattern. When these bits are set to 00: Searching of CAS Multi-frame alignment is disabled. The XRT84L38 framer will not search for CAS Multi-frame alignment and thus will not declare CAS Multi-frame synchronization. No Receive CAS Multi-frame Synchronization (RxCRCMsync_n) pulse will be generated by the framer. When these bits are set to 01: Searching of CAS Multi-frame alignment is enabled. The XRT84L38 will search for and declare CAS Multi-frame synchronization using Algorithm 1. When these bits are set to 10: Searching of CAS Multi-frame alignment is enabled. The XRT84L38 will search for and declare CAS Multi-frame synchronization using Algorithm 2 (G.732). When these bits are set to 11: Searching of CAS Multi-frame alignment is disabled. The XRT84L38 framer will not search for CAS Multi-frame alignment and thus will not declare CAS Multi-frame synchronization. No Receive CAS Multi-frame Synchronization (RxCRCMsync_n) pulse will be generated by the framer.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	CRC-4 Selection bit	R/W	**CRC-4 Selection:** These Read/Write bit fields allow the user to enable searching of CRC-4 Multi-frame alignment and determine what criteria are used for locking the CRC-4 Multi-frame alignment pattern. When these bit s are set to 00: Searching of CRC-4 Multi-frame alignment is disabled. The XRT84L38 framer will not search for CRC-4 Multi-frame alignment and thus will not declare CRC-4 Multi-frame synchronization. No Receive CRC-4 Multi-frame Synchronization (RxCRCMsync_n) pulse will be generated by the framer. When these bit s are set to 01: Searching of CRC-4 Multi-frame alignment is enabled. The XRT84L38 will search for and declare CRC-4 Multi-frame synchronization if: At least one valid CRC-4 Multi-frame alignment signal is observed within 8 ms. When these bit s are set to 10: Searching of CRC-4 Multi-frame alignment is enabled. The XRT84L38 will search for and declare CRC-4 Multi-frame synchronization if: At least two valid CRC-4 Multi-frame alignment signals are observed within 8 ms. The time separating two CRC-4 Multi-frame alignment signals is multiple of 2 ms. When these bit s are set to 11: Searching of CRC-4 Multi-frame alignment is enabled. The XRT84L38 will search for and declare CRC-4 Multi-frame synchronization if: At least three valid CRC-4 Multi-frame alignment signals are observed within 8 ms. The time separating two CRC-4 Multi-frame alignment signals is multiple of 2 ms.
1	FAS Alignment Frame Check Sequence Enable	R/W	**FAS Alignment Frame Check Sequence Enable:** This READ/WRITE bit-field enables frame check sequence in FAS alignment process. The frame check sequence consists of verifying correct frame alignment for an additional two frames. When this bit is set to 0: The frame check sequence is disabled in FAS alignment process. When this bit is set to 1: The frame check sequence is enabled in FAS alignment process.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	FAS Selection bit	R/W	**FAS Selection:** This Read/Write bit field allows the user to determine which algorithm is used for searching FAS frame alignment pattern. When an FAS alignment pattern is found and locked, the XRT84L38 will generate Receive Synchronization (RxSync_n) pulse. When this bit is set to 0: Algorithm 1 is selected for searching FAS frame alignment pattern. When this bit is set to 1: Algorithm 2 is selected for searching FAS frame alignment pattern.

Alarm Generation Register (AGR) - T1 Mode (Indirect Address = 0xn0H, 0x08H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Reserved	Loss of Frame Declaration Enable	Yellow Alarm Generation Select Bit 1	Yellow Alarm Generation Select Bit 0	Alarm Indication Signal Generation Select Bit 1	Alarm Indication Signal Generation Select Bit 0	Alarm Indication Signal Detection Select Bit 1	Alarm Indication Signal Detection Select Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Reserved	X	
6	Loss of Frame Declaration Enable	R/W	**Loss of Frame Declaration Enable:** This READ/WRITE bit-field permits the framer to declare Red Alarm in case of Loss of Frame Alignment (LOF). When receiver module of the framer detects Loss of Frame Alignment in the incoming data stream, it will generate a Red Alarm. The framer will also generate an RxLOFs interrupt to notify the microprocessor that an LOF condition is occurred. A Yellow Alarm is then returned to the remote transmitter to report that the local receiver detects LOF. When this bit is set to zero: Red Alarm declaration is disabled. When this bit is set to one: Red Alarm declaration is enabled.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	Yellow Alarm Generation Select	R/W	**Yellow Alarm Generation Select:** These READ/WRITE bit-fields activate and de-activate transmission of Yellow Alarm by the framer. In various framing formats, the pattern and duration of Yellow Alarm various. The following text describes how the framer transmits Yellow Alarm by setting these bit-fields to different values. SF Mode: When these bits are set to 00: Transmission of Yellow Alarm is disabled. When these bits are set to 01: The framer transmits Yellow Alarm by converting the second MSB of all outgoing twenty-four DS0 channel into zero. When these bits are set to 10: The framer transmits Yellow Alarm by sending the Super-frame Alignment Bit (Fs) of Frame 12 as one. When these bits are set to 11: The framer transmits Yellow Alarm by converting the second MSB of all outgoing twenty-four DS0 channel into zero.N Mode: When these bits are set to 00: Transmission of Yellow Alarm is disabled. When these bits are set to 01, 10 or 11: The framer transmits Yellow Alarm by converting the second MSB of all outgoing twenty-four DS0 channel into zero. ESF Mode: When the framer is in ESF mode, it transmits Yellow Alarm pattern of eight ones followed by eight zeros (1111_1111_0000_0000) through the 4Kbit/s data link bits. When the Yellow Alarm Generation Select bits are set to 00: Transmission of Yellow Alarm is disabled. When these bits are set to 01: The following scenario will happen: **1.** If Bit 0 of Yellow Alarm Generation Select forms a pulse width shorter or equal to the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm is transmitted for 255 patterns. **2.** If Bit 0 of Yellow Alarm Generation Select forms a pulse width longer than the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm continues until Bit 0 goes LOW. **3.** A second pulse on Bit 0 of Yellow Alarm Generation Select during an alarm transmission resets the pattern counter. The framer will send another 255 patterns of the Yellow Alarm.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
			When these bits are set to 10: Bit 1 of the Yellow Alarm Generation Select forms a pulse that controls the duration of Yellow Alarm transmission. The alarm continues until Bit 1 goes LOW. When these bits are set to 11: The following scenario will happen: **1.** If Bit 0 of Yellow Alarm Generation Select forms a pulse width shorter or equal to the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm is transmitted for 255 patterns. **2.** If Bit 0 of Yellow Alarm Generation Select forms a pulse width longer than the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm continues until Bit 0 goes LOW. **3.** A second pulse on Bit 0 of Yellow Alarm Generation Select during an alarm transmission resets the pattern counter. The framer will send another 255 patterns of the Yellow Alarm. **T1DM Mode:** When these bits are set to 00: Transmission of Yellow Alarm is disabled. When these bits are set to 01, 10 or 11: The framer transmits Yellow Alarm by setting the Yellow Alarm bit (Y-bit) to zero.
3-2	Alarm Indication Signal Generation Select	R/W	**Alarm Indication Signal Generation Select:** These READ/WRITE bit-fields activate and de-activate transmission of Alarm Indication Signal (AIS). There are two types of Alarm Indication Signals - framed and unframed. A unframed AIS signal is all-ones including all the framing bits. A framed AIS signal is all-ones except the framing bits. When these bits are set to 00: The framer will disable AIS alarm generation. When these bits are set to 01: The framer will transmit unframed AIS alarm. When these bits are set to 10: The framer will disable AIS alarm generation. When these bits are set to 11: The framer will transmit framed AIS Alarm.
1-0	Alarm Indication Signal Detection Select	R/W	**Alarm Indication Signal Detection Select:** These READ/WRITE bit-fields activate and de-activate Alarm Indication Signal Detection of the framer. When these bits are set to 00: The framer disables detection of AIS Alarm. When these bits are set to 01: The framer enables detection of unframed AIS Alarm. When these bits are set to 10: The framer disables detection of AIS Alarm. When these bits are set to 11: The framer enables detection of framed AIS Alarm.

Alarm Generation Register (AGR) - E1 Mode (Indirect Address = 0xn0H, 0x08H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
AUXP Enable	Loss of Frame Declaration Enable	Yellow Alarm Generation Select Bit 1	Yellow Alarm Generation Select Bit 0	Alarm Indication Signal Generation Select Bit 1	Alarm Indication Signal Generation Select Bit 0	Alarm Indication Signal Detection Select Bit 1	Alarm Indication Signal Detection Select Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	AUXP Enable	R/W	**AUXP Enable:** AUXP is an unframed 1010 pattern. When this bit is set to zero: AUXP generation is disabled. When this bit is set to one: AUXP generation is enabled.
6	Loss of Frame Declaration Enable	R/W	**Loss of Frame Declaration Enable:** This READ/WRITE bit-field permits the framer to declare Red Alarm in case of Loss of Frame Alignment (LOF). When receiver module of the framer detects Loss of Frame Alignment in the incoming data stream, it will generate a Red Alarm. The framer will also generate an RxLOFs interrupt to notify the microprocessor that an LOF condition is occurred. A Yellow Alarm is then returned to the remote transmitter to report that the local receiver detects LOF. When this bit is set to zero: Red Alarm declaration is disabled. When this bit is set to one: Red Alarm declaration is enabled.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	Yellow Alarm Generation Select	R/W	**Yellow Alarm Generation Select:** These READ/WRITE bit-fields allows the user to choose how the XRT84L38 would generate Yellow Alarm and CAS Multi-frame Yellow Alarm. When these bits are set to 00: Transmission of Yellow Alarm and CAS Multi-frame Yellow Alarm is disabled. When these bits are set to 01: The Yellow Alarm bit is transmitted by echoing the received FAS alignment pattern. If the correct FAS alignment is received, the Yellow Alarm bit is set to zero. If the FAS alignment pattern is missing or corrupted, the Yellow Alarm bit is set to one. The CAS Multi-frame Yellow Alarm bit is transmitted by echoing the received CAS Multi-frame alignment pattern (the four zeros pattern). If the correct CAS Multi-frame alignment is received, the CAS Multi-frame Yellow Alarm bit is set to zero. If the CAS Multi-frame alignment pattern is missing or corrupted, the CAS Multi-frame Yellow Alarm bit is set to one. When these bits are set to 10: The Yellow Alarm and CAS Multi-frame Yellow Alarms are transmitted as zero. When these bits are set to 11: The Yellow Alarm and CAS Multi-frame Yellow Alarms are transmitted as one.
3-2	Alarm Indication Signal Generation Select	R/W	**Alarm Indication Signal Generation Select:** These READ/WRITE bit-fields activate and de-activate transmission of Alarm Indication Signal (AIS). There are two types of Alarm Indication Signals - framed and unframed. A unframed AIS signal is all-ones including all the framing bits. A framed AIS signal is all-ones except the framing bits. When these bits are set to 00: The framer will disable AIS alarm generation. When these bits are set to 01: The framer will transmit unframed AIS alarm. When these bits are set to 10: The framer will generate AIS16. Only time slot 16 is carrying the all ones pattern. The other time slots still carry framing and PCM data. When these bits are set to 11: The framer will transmit framed AIS Alarm.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Alarm Indication Signal Detection Select	R/W	**Alarm Indication Signal Detection Select:** These READ/WRITE bit-fields activate and de-activate Alarm Indication Signal Detection of the framer. When these bits are set to 00: The framer disables detection of AIS Alarm. When these bits are set to 01: The framer enables detection of unframed AIS Alarm. When these bits are set to 10: The framer enables detection of AIS16 Alarm. When these bits are set to 11: The framer enables detection of framed AIS Alarm.

Synchronization Mux Register (SMR) - T1 Mode (Indirect Address = 0xn0H, 0x09H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Reserved	Transmit Multi-frame Alignment	Transmit Super-frame Synchroniza-tion	Synchroniza-tion Signal Direction	Reserved	Reserved	CRC-6 Source	Framing Bit Source
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Reserved	R/W	
6	Transmit Multi-frame Alignment	R/W	**Transmit Multi-frame Alignment:** This READ/WRITE bit-field forces the framer to align the Trans-mit Multi-frame boundary with the back-plane Multi-frame Syn-chronization Pulse. When this bit is set to zero: The Transmit Multi-frame boundary is not aligned with the back-plane Multi-frame Synchronization Pulse. When this bit is set to one: The Transmit Multi-frame boundary is forced to align with the back-plane Multi-frame Synchronization Pulse.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Transmit Super-frame Synchronization	R/W	**Transmit Super-frame Synchronization:** This READ/WRITE bit-field determines the transmit synchronization input signal (TxSync) being either the Frame Synchronization signal or the Multi-frame Synchronization signal. When this bit is set to zero: The transmit synchronization input signal (TxSync) is the Frame Synchronization signal that indicates the frame boundary. In 1.544Mbit/s basic mode, the Transmit Multi-frame Synchronization input signal (TxMSync) indicates the Multi-frame boundary. In other back-plane modes, the TxMSync input is an input transmit clock. When this bit is set to one: The transmit synchronization input signal (TxSync) is the Transmit Multi-frame Synchronization signal indicating the multi-frame boundary.
4	Synchronization Signal Direction	R/W	**Synchronization Signal Direction:** This READ/WRITE bit-field determines the direction of transmit synchronization signal (TxSync_n) and the Transmit Multi-frame Synchronization signal (TxMSync_n). In H.100 interface mode, this READ/WRITE bit-field determines the location of the transmit synchronization pulse. When this bit is set to zero: The transmit synchronization signal is input if the Transmit Line Clock Source Select bits of Clock Select Register (CSR) equal to one. If the Transmit Line Clock Source Select bits of Clock Select Register (CSR) is not equal to one, the transmit synchronization signal is output. In H.100 interface mode, the transmit synchronization pulse occurs at the last and the first clock cycles of each frame. When this bit is set to one: The transmit synchronization signal is output if the Transmit Line Clock Source Select bits of Clock Select Register (CSR) equal to one. If the Transmit Line Clock Source Select bits of Clock Select Register (CSR) is not equal to one, the transmit synchronization signal is input. In H.100 interface mode, the transmit synchronization pulse occurs at the first two clock cycles of each frame.
3-2	Reserved	R/W	
1	CRC-6 Source	R/W	**CRC-6 Source:** This READ/WRITE bit-field permits the user to determine where the CRC-6 bits should be inserted. When this bit is zero: The CRC-6 bits are generated and inserted by the framer internally. When this bit is one: If the framer is operating in normal 1.544Mbit/s mode, the CRC-6 bits are passed through from the Transmit Serial Data input (TxSer_n).

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	Framing Bit Source	R/W	**Framing Bit Source:** This READ/WRITE bit-field permits the user to determine where the framing alignment bits should be inserted. When this bit is zero: The framing alignment bits are generated and inserted by the framer internally. When this bit is one: If the framer is operating in normal 1.544Mbit/s mode, the framing alignment bits are passed through from the Transmit Serial Data input (TxSer_n).

Synchronization Mux Register (SMR) - E1 Mode (Indirect Address = 0xn0H, 0x09H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
E bit Source Select bit 1	E bit Source Select bit 0	Reserved	Synchronization Signal Direction	Transmit Data Link Source Select bit 1	Transmit Data Link Source Select bit 0	CRC-4 Source	Framing Bit Source
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-6	E bit Source Select	R/W	**E Source Select:** These READ/WRITE bit-fields permits the user to determine where the E bits should be inserted and what the E bits should be. When these bits are 00: The E bits are generated and inserted by the framer internally. When these bits are 01: The E bits are forced to be "0" and are inserted by the framer internally. When these bits are 10:The E bits are forced to be "1" and are inserted by the framer internally. When these bits are 11: Source of the E bits is HDLC controller of the framer. The E bits are used to carry data link messages.
5	Reserved		

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Synchronization Signal Direction	R/W	**Synchronization Signal Direction:** This READ/WRITE bit-field determines the direction of transmit synchronization signal (TxSync_n) and the Transmit Multi-frame Synchronization signal (TxMSync_n). In H.100 interface mode, this READ/WRITE bit-field determines the location of the transmit synchronization pulse. When this bit is set to zero: The transmit synchronization signal is input if the Transmit Line Clock Source Select bits of Clock Select Register (CSR) equal to one. That is, if the Transmit Serial Input Clock (TxSerClk_n) is configured as the source of the Transmit Line Clock. If the Transmit Line Clock Source Select bits of Clock Select Register (CSR) is not equal to one, the transmit synchronization signal is output. In H.100 interface mode, the transmit synchronization pulse occurs at the last and the first clock cycles of each frame. When this bit is set to one: The transmit synchronization signal is output if the Transmit Line Clock Source Select bits of Clock Select Register (CSR) equal to one. That is, if the Transmit Serial Input Clock (TxSerClk_n) is configured as the source of the Transmit Line Clock. If the Transmit Line Clock Source Select bits of Clock Select Register (CSR) is not equal to one, the transmit synchronization signal is input. In H.100 interface mode, the transmit synchronization pulse occurs at the first two clock cycles of each frame.
3-2	Transmit Data Link Source Select [1:0]	R/W	**Transmit Data Link Source Select [1:0]:** These READ/WRITE bit-fields permits the user to determine where the data link bits should be inserted from. When these bits are set to 00: The data link bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins. When these bits are set to 01: The data link bits are inserted into the framer through the Transmit HDLC Controller. When these bits are set to 10: The data link bits are inserted into the framer through the Transmit Overhead Input Interface via the TxOH_n pins. When these bits are set to 11: The data link bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	CRC-4 Source Select	R/W	**CRC-4 Source Select:** This READ/WRITE bit-field permits the user to determine where the CRC-4 bits should be inserted. When this bit is set to 0: The CRC-4 bits are generated and inserted by the framer internally. When this bit is set to 1: If the framer is operating in normal 2.048Mbit/s mode, the CRC-4 bits are generated by external equipment and passed through from the Transmit Serial Data Input Interface block via the TxSer_n pin.
0	Framing Bit Source	R/W	**Framing Bit Source:** This READ/WRITE bit-field permits the user to determine where the framing alignment bits should be inserted. When this bit is set to 0: The framing alignment bits are generated and inserted by the framer internally. When this bit is set to 1: If the framer is operating in normal 2.048Mbit/s mode, the framing alignment bits are passed through from the Transmit Serial Data Input Interface block via the TxSer_n pin.

Transmit Signaling And Data Link Select Register (TSDLSR)- T1 Mode (Indirect Address = 0xn0H, 0x0AH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Reserved	Reserved	Transmit Data Link Bandwidth Select Bit 1	Transmit Data Link Bandwidth Select Bit 0	D/E Timeslot Source Select Bit 1	D/E Timeslot Source Select Bit 0	Data Link Source Select Bit 1	Data Link Source Select Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-6	Reserved	R/W	

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	Transmit Data Link Bandwidth Select	R/W	**Transmit Data Link Bandwidth Select:** These READ/WRITE bit-fields determined the bandwidth of Facility Data Link channel of the framer when operating in ESF mode. When these bits are set to 00: The Facility Data Link is a 4KHz channel. All available FDL bits (first bit of every other frame) are used as data link bits. When these bits are set to 01: The Facility Data Link is a 2KHz channel. Only the odd FDL bits (first bit of frame 1, 5, 9…) are used as data link bits. When these bits are set to 10: The Facility Data Link is a 2KHz channel. Only the even FDL bits (first bit of frame 3, 7, 11…) are used as data link bits.
3-2	D/E Timeslot Source Select	R/W	**D/E Timeslot Source Select:** These READ/WRITE bit-fields permit the user to select data source of D or E channel (D/E Timeslot) for the ISDN Primary Rate Interface, if LAPDSEL[1:0] bits in TCCR is 10. ***NOTE:*** *The LAPD Select (LAPDSEL) bits of the Transmit Channel Control Register (TCCR) determine which one of the three LAPD channel are used for D/E timeslot. If LAPDSEL[1:0] = 10, the D/E Timeslot Source Select bits will determine the data source for D/E time slot.* The ISDN Primary Rate Interface (ISDN I.431) can carry B channel, D channel, E channel and H channel. B channel has a bit rate of 64Kbit/s and is equivalent to a DS0 channel in T1 used for payload transmission. D channel has a bit rate of 64Kbit/s and is used primarily for signaling transmission. E channel has a bit rate of 64Kbit/s and is used for signaling for circuit switching. It is used only with multiple-access configuration. H channel has bit rates of 384Kbit/s, 1536Kbit/s for T1 primary rate, and 1920Kbit/s for E1 primary rate. The signaling information presented on D or E channels are provided by several sources. The user can provide the signaling information through the Transmit Serial Data via the TxSer_n pins. The user can also supply the signaling data by writing to the LAPD controller using microprocessor access. Finally, the user can provide the data through Fraction T1 input via the TxFrT1_n pins. When these bits are set to 00: The D or E channel data are inserted from the Transmit Serial Data input. When these bits are set to 01: The D or E channel data are inserted from the LAPD controllers. The user can read or write to the LAPD controller using microprocessor access. When these bits are set to 10: The D or E channel data are inserted from the Transmit Serial Data input. When these bits are set to 11: The D or E channel data are inserted from the Fractional T1 input.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Data Link Source Select	R/W	**Data Link Source Select:** These READ/WRITE bit-fields permit the user to select data source of the Facility Data Link bits. The user can insert Facility Data Link bits into the framer through the LAPD controller or SLCâ96 buffer. Both LAPD controller and SLCâ96 buffer can be programmed through microprocessor access. The user can also insert Facility Data Link bits through Transmit Serial Data directly via TxSer_n pins. Overhead interface of the framer can also be used to input Facility Data Link bits. Finally, the user can force these data link bits to one. When these bits are set to 00: The Facility Data Link bits are inserted into the framer through either the LAPD controller or the SLCâ96 buffer. When these bits are set to 01: The Facility Data Link bits are inserted into the framer through the Transmit Serial Data input. When these bits are set to 10: The Facility Data Link bits are inserted into the framer through the Overhead Interface via the TxOH_n pins. When these bits are set to 11: The Facility Data Link bits are forced to one by the framer.

Transmit Signaling And Data Link Select Register (TSDLSR)- E1 Mode (Indirect Address = 0xn0H, 0x0AH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Transmit Sa8 Data Link Select	Transmit Sa7 Data Link Select	Transmit Sa6 Data Link Select	Transmit Sa5 Data Link Select	Transmit Sa4 Data Link Select	Data Link Source Select Bit 2	Data Link Source Select Bit 1	Data Link Source Select Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Transmit Sa8 Data Link Select	R/W	**Transmit Sa8 Data Link Select:** When this bit is set to 0: Source of the Sa8 Nation bit is not from the data link interface. When this bit is set to 1: Source the Sa8 National bit from the data link interface.
6	Transmit Sa7 Data Link Select	R/W	**Transmit Sa7 Data Link Select:** When this bit is set to 0: Source of the Sa7 Nation bit is not from the data link interface. When this bit is set to 1: Source the Sa7 National bit from the data link interface.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Transmit Sa6 Data Link Select	R/W	**Transmit Sa6 Data Link Select:** When this bit is set to 0: Source of the Sa6 Nation bit is not from the data link interface. When this bit is set to 1: Source the Sa6 National bit from the data link interface.
4	Transmit Sa5 Data Link Select	R/W	**Transmit Sa5 Data Link Select:** When this bit is set to 0: Source of the Sa5 Nation bit is not from the data link interface. When this bit is set to 1: Source the Sa5 National bit from the data link interface.
3	Transmit Sa4 Data Link Select	R/W	**Transmit Sa4 Data Link Select:** When this bit is set to 0: Source of the Sa4 Nation bit is not from the data link interface. When this bit is set to 1: Source the Sa4 National bit from the data link interface.
2-0	Transmit Signaling and Data Link Select	R/W	**Transmit Signaling and Data Link Select:** These READ/WRITE bit-fields permit the user to select data source of the D or E channels, the National bits and the time slot 16 octets. **National Bits** When these bits are set to 000: The data link interface is source of the Sa4 through Sa8 Nation bits, if the corresponding Transmit Sa Data Link Select bit(s) (Bit 3 to Bit 7 of the Transmit Signaling and Data Link Select Register) are set to 1. When these bits are set to 001: The data link interface is source of the Sa4 through Sa8 Nation bits, if the corresponding Transmit Sa Data Link Select bit(s) (Bit 3 to Bit 7 of the Transmit Signaling and Data Link Select Register) are set to 1. When these bits are set to 010: The Sa4 through Sa8 Nation bits are forced to 1. When these bits are set to 011: The Sa4 through Sa8 Nation bits are forced to 1. When these bits are set to 100: The data link interface is source of the Sa4 through Sa8 Nation bits, if the corresponding Transmit Sa Data Link Select bit(s) (Bit 3 to Bit 7 of the Transmit Signaling and Data Link Select Register) are set to 1. When these bits are set to 101: Reserved. When these bits are set to 110: Reserved. When these bits are set to 111: Reserved.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
			Timeslot 16 Octet When these bits are set to 000: Timeslot 16 octet is taken directly from the Transmit Signaling Control Register (TSCR). When these bits are set to 001: Timeslot 16 octet is taken directly from the Transmit Overhead Input Interface through the TxOH_n pin or per-channel signaling registers determined by Transmit Signaling Source bit of the Transmit Signaling Control Register (TSCR)of Timeslot 16. When these bits are set to 010: Timeslot 16 octet is taken directly from the Transmit Signaling Input Interface through the TxSig_n pin. When these bits are set to 011: Timeslot 16 octet is taken directly from the Transmit Overhead Input Interface through the TxOH_n pin or per-channel signaling registers determined by Transmit Signaling Source bit of the Transmit Signaling Control Register (TSCR) of Timeslot 16. When these bits are set to 100: Timeslot 16 octet is taken directly from the Transmit Signaling Control Register (TSCR). When these bits are set to 101: Reserved. When these bits are set to 110: Reserved. When these bits are set to 111: Reserved. **D/E Time Slot** When these bits are set to 000: D or E time slot data are taken through the Transmit Fractional Data Input Interface (TxFrTD_n pin). When these bits are set to 001: D or E time slot data are taken through the Transmit Fractional Data Input Interface (TxFrTD_n pin). When these bits are set to 010: D or E time slot data are taken through the Transmit Fractional Data Input Interface (TxFrTD_n pin). When these bits are set to 011: D or E time slot data are taken through the Transmit Fractional Data Input Interface (TxFrTD_n pin). When these bits are set to 100: D or E time slot data are taken through the Transmit Serial Signaling Input Interface (TxSig_n pin). When these bits are set to 101: Reserved. When these bits are set to 110: Reserved. When these bits are set to 111: Reserved. The following table summaries sources of National bits, Timeslot 16 octet and D or E time slots.T

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION

TxSIGDL [2:0]	National Bits (Sa4-Sa8)	Timeslot 16 Octet	D or E Timeslot
000	Data Link	TSCR	TxFrTD_n
001	Data Link	TxSig_n or TxOH	TxFrTD_n
010	None	TxSig_n or TxOH	TxFrTD_n
011	None	TxSig_n or TxOH	TxFrTD_n
100	Data Link	TSCR	TxSig_n
101	Reserved	Reserved	Reserved
110	Reserved	Reserved	Reserved
111	Reserved	Reserved	Reserved

Framing Control Register (FCR) - T1 Mode (Indirect Address = 0xn0H, 0x0BH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Force Re-synchronization	Synchronization with CRC Verification	Framing Error Tolerance Bit 2	Framing Error Tolerance Bit 1	Framing Error Tolerance Bit 0	Framing Bit Range Bit 2	Framing Bit Range Bit 1	Framing Bit Range Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Force Re-synchronization	R/W	**Force Re-synchronization:** This READ/WRITE bit-field forces the re-synchronization process of the framer. When this bit is set to one: The framer started the re-synchronization process. After synchronization is achieved, the bit is automatically cleared.
6	Synchronization with CRC Verification	R/W	**Synchronization with CRC Verification:** This READ/WRITE bit-field forces the framer to obtain synchronization with CRC verification. When this bit is set to zero: The framer obtains synchronization without CRC match test. When this bit is set to one: CRC match test is included as part of the synchronization process.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-3	Framing Error Tolerance	R/W	**Framing Error Tolerance:** These READ/WRITE bit-fields together with the Range bits form the criteria for Loss of Frame Alignment. In SF mode, a Loss of Frame Alignment is typically declared if two out of four Terminal Framing bits (Ft) or Signaling Framing bits (Fs) are incorrect. Therefore, the Tolerance bits are normally set to two and the Range bits are normally set to four. In ESF mode, a Loss of Frame Alignment is typically declared if two out of four Framing Pattern Sequence bits (FPS) are incorrect. Therefore, the Tolerance bits are normally set to two and the Range bits are normally set to four. In N mode, a Loss of Frame Alignment is typically declared if two out of four Terminal Framing bits (Ft) are incorrect. Therefore, the Tolerance bits are normally set to two and the Range bits are normally set to four. In SLC®96 mode, a Loss of Frame Alignment is typically declared if two out of four Terminal Framing bits (Ft) are incorrect. Therefore, the Tolerance bits are normally set to two and the Range bits are normally set to four. In T1DM mode, a Loss of Frame Alignment is typically declared if TOLR out of RANG bits are incorrect. Therefore, the Tolerance bits are normally set to two and the Range bits are normally set to four.
2-0	Framing Bit Range	R/W	**Framing Bit Range:** These READ/WRITE bit-fields together with the Tolerance bits form the criteria for Loss of Frame Alignment. In SF mode, a Loss of Frame Alignment is typically declared if two out of four Terminal Framing bits (Ft) or Signaling Framing bits (Fs) are incorrect. Therefore, the Tolerance bits are normally set to two and the Range bits are normally set to four. In ESF mode, a Loss of Frame Alignment is typically declared if two out of four Framing Pattern Sequence bits (FPS) are incorrect. Therefore, the Tolerance bits are normally set to two and the Range bits are normally set to four. In N mode, a Loss of Frame Alignment is typically declared if two out of four Terminal Framing bits (Ft) are incorrect. Therefore, the Tolerance bits are normally set to two and the Range bits are normally set to four. In SLC®96 mode, a Loss of Frame Alignment is typically declared if two out of four Terminal Framing bits (Ft) are incorrect. Therefore, the Tolerance bits are normally set to two and the Range bits are normally set to four. In T1DM mode, a Loss of Frame Alignment is typically declared if TOLR out of RANG bits are incorrect. Therefore, the Tolerance bits are normally set to two and the Range bits are normally set to four.

Framing Control Register (FCR) - E1 Mode (Indirect Address = 0xn0H, 0x0BH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Force Re-synchronization	CAS Re-synchronization Criteria Bit 1	CAS Re-synchronization Criteria Bit 0	CRC Re-synchronization Criteria Bit 1	CRC Re-synchronization Criteria Bit 0	FAS Re-synchronization Criteria Bit 2	FAS Re-synchronization Criteria Bit 1	FAS Re-synchronization Criteria Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Force Re-synchronization	R/W	**Force Re-synchronization:** This READ/WRITE bit-field forces the re-synchronization process of the framer. When this bit is set to one: The framer started the re-synchronization process. After synchronization is achieved, the bit is automatically cleared.
6 - 5	CAS Re-synchronization Criteria	R/W	**CAS Re-synchronization Criteria:** These READ/WRITE bit-field determine the criteria of Loss of CAS Multi-frame Synchronization. When these bits are set to 00: Two consecutive CAS Multi-frame Alignment Signal errors in the incoming frame will cause the declaration of Loss of CAS Multi-frame Synchronization. When these bits are set to 01: Three consecutive CAS Multi-frame Alignment Signal errors in the incoming frame will cause the declaration of Loss of CAS Multi-frame Synchronization. When these bits are set to 10: Four consecutive CAS Multi-frame Alignment Signal errors in the incoming frame will cause the declaration of Loss of CAS Multi-frame Synchronization. When these bits are set to 11: Eight consecutive CAS Multi-frame Alignment Signal errors in the incoming frame will cause the declaration of Loss of CAS Multi-frame Synchronization.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4 - 3	CRC Re-synchronization Criteria	R/W	**CRC Re-synchronization Criteria:** These READ/WRITE bit-field determine the criteria of Loss of CRC Multi-frame Synchronization. When these bits are set to 00: If four consecutive CRC Multi-frame Alignment Signal errors in the incoming frames are detected, the framer will declare Loss of CRC Multi-frame Synchronization. When these bits are set to 01: If two consecutive CRC Multi-frame Alignment Signal errors in the incoming frames are detected, the framer will declare Loss of CRC Multi-frame Synchronization. When these bits are set to 10: If eight consecutive CRC Multi-frame Alignment Signal errors in the incoming frames are detected, the framer will declare Loss of CRC Multi-frame Synchronization. When these bits are set to 11: If 915 or more consecutive CRC Multi-frame Alignment Signal errors in the incoming frames are detected in one second, the framer will declare Loss of CRC Multi-frame Synchronization.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2 - 0	FAS Re-synchronization Criteria	R/W	**FAS Re-synchronization Criteria:** These READ/WRITE bit-field determine the criteria of Loss of FAS Multi-frame Synchronization. When these bits are set to 000: It is an illegal entry. The user should not set these bits to 000. When these bits are set to 001: If one FAS Multi-frame Alignment Signal error in the incoming frame is detected, the framer will declare Loss of FAS Multi-frame Synchronization. When these bits are set to 010: If two consecutive FAS Multi-frame Alignment Signal errors in the incoming frames are detected, the framer will declare Loss of FAS Multi-frame Synchronization. When these bits are set to 011: If three consecutive FAS Multi-frame Alignment Signal errors in the incoming frames are detected, the framer will declare Loss of FAS Multi-frame Synchronization. When these bits are set to 100: If four consecutive FAS Multi-frame Alignment Signal errors in the incoming frames are detected, the framer will declare Loss of FAS Multi-frame Synchronization. When these bits are set to 101: If five consecutive FAS Multi-frame Alignment Signal errors in the incoming frames are detected, the framer will declare Loss of FAS Multi-frame Synchronization. When these bits are set to 110: If six consecutive FAS Multi-frame Alignment Signal errors in the incoming frames are detected, the framer will declare Loss of FAS Multi-frame Synchronization. When these bits are set to 111: If seven consecutive FAS Multi-frame Alignment Signal errors in the incoming frames are detected, the framer will declare Loss of FAS Multi-frame Synchronization.

Receive Data Link Select Register (RDLSR) - T1 Mode (Indirect Address = 0xn0H, 0x0CH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Reserved		Receive Data Link Band-width Select Bits [1:0]		D/E Timeslot Destination Select Bits [1:0]		Data Link Destination Select Bits [1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-6	Reserved	X	
5-4	Receive Data Link Bandwidth Select	R/W	**Receive Data Link Bandwidth Select:** These READ/WRITE bit-fields determined the bandwidth of Facility Data Link channel of the framer when operating in ESF mode. When these bits are set to 00: The Facility Data Link is a 4KHz channel. All available FDL bits (first bit of every other frame) are used as data link bits. When these bits are set to 01: The Facility Data Link is a 2KHz channel. Only the odd FDL bits (first bit of frame 1, 5, 9…) are used as data link bits. When these bits are set to 10: The Facility Data Link is a 2KHz channel. Only the even FDL bits (first bit of frame 3, 7, 11…) are used as data link bits.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	D/E Timeslot Source Select	R/W	D/E Timeslot Source Select: These READ/WRITE bit-fields permit the user to select data destination of D or E channel (D/E Timeslot) for the ISDN Primary Rate Interface. The ISDN Primary Rate Interface (ISDN I.431) can carry B channel, D channel, E channel and H channel. B channel has a bit rate of 64Kbit/s and is equivalent to a DS0 channel in T1 used for payload transmission. D channel has a bit rate of 64Kbit/s and is used primarily for signaling transmission. E channel has a bit rate of 64Kbit/s and is used for signaling for circuit switching. It is used only with multiple-access configuration. H channel has bit rates of 384Kbit/s, 1536Kbit/s for T1 primary rate, and 1920Kbit/s for E1 primary rate. The signaling information presented on D or E channels can be directed to several destinations. The user can send the signaling information to the Receive Serial Data via the RxSer_n pins. The user can also direct the signaling data to the Receive LAPD controller. The signaling information can be extracted from the Receive LAPD controller using microprocessor access. Finally, the user can send the signaling information to Fraction T1 output via the RxFrT1_n pins. When these bits are set to 00: The data link bits extracted form the D or E channel of incoming DS1 frame are inserted into the Receive Serial Data Output Interface via the RxSer_n pins. When these bits are set to 01: The data link bits extracted form the D or E channel of incoming DS1 frame are inserted into the Receive HDLC Controller. The user can read the Receive LAPD controller using microprocessor access. When these bits are set to 10: The data link bits extracted form the D or E channel of incoming DS1 frame are inserted into the Receive Fractional T1 Output Interface via the RxFrT1_n pins. When these bits are set to 11: The data link bits extracted form the D or E channel of incoming DS1 frame are inserted into the Receive Serial Data Output Interface via the RxSer_n pins.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Data Link Source Select	R/W	**Data Link Source Select:** These READ/WRITE bit-fields permit the user to select data destination of the Facility Data Link bits. The user can extract Facility Data Link bits of the incoming data to the LAPD controller or SLCâ96 buffer. Both LAPD controller and SLCâ96 buffer can be read through microprocessor access. The user can also direct received Facility Data Link bits to Receive Serial Data via RxSer_n pins. Overhead interface of the framer can also be used to output Facility Data Link bits. Finally, the user can force these data link bits to one. When these bits are set to 00: The Facility Data Link bits of the incoming data stream are extracted to either the LAPD controller or the SLCâ96 buffer. The Facility Data Link bits are also extracted into the Receive Serial Data via the RxSer pin. When these bits are set to 01: The Facility Data Link bits of the incoming data stream are sent to the Receive Serial Data output only. When these bits are set to 10: The Facility Data Link bits of the incoming data stream are directed to the Overhead Interface via the RxOH_n pins. The Facility Data Link bits are also extracted into the Receive Serial Data via the RxSer pin. When these bits are set to 11: The Facility Data Link bits of the incoming data stream are forced to one by the framer and are outputted to the Receive Serial Data output.

Receive Data Link Select Register (RDLSR) - E1 Mode(Indirect Address = 0xn0H, 0x0CH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Receive Sa8 Data Link Select	Receive Sa8 Data Link Select	Receive Sa8 Data Link Select	Receive Sa8 Data Link Select	Receive Sa8 Data Link Select	Receive Signaling and Data Link Select Bits [2:0]		
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Sa8 Data Link Select	R/W	**Receive Sa8 Data Link Select:** This READ/WRITE bit-field permit the user to select data destination of the Sa8 National bit. When this bit is set to 0: Destination of the Sa8 National bit is not the data link interface. When this bit is set to 1: Destination of the Sa8 National bit is the data link interface.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Receive Sa7 Data Link Select	R/W	**Receive Sa7 Data Link Select:** This READ/WRITE bit-field permit the user to select data destination of the Sa7 National bit. When this bit is set to 0: Destination of the Sa7 National bit is not the data link interface. When this bit is set to 1: Destination of the Sa7 National bit is the data link interface.
5	Receive Sa6 Data Link Select	R/W	**Receive Sa6 Data Link Select:** This READ/WRITE bit-field permit the user to select data destination of the Sa6 National bit. When this bit is set to 0: Destination of the Sa6 National bit is not the data link interface. When this bit is set to 1: Destination of the Sa6 National bit is the data link interface.
4	Receive Sa5 Data Link Select	R/W	**Receive Sa5 Data Link Select:** This READ/WRITE bit-field permit the user to select data destination of the Sa5 National bit. When this bit is set to 0: Destination of the Sa5 National bit is not the data link interface. When this bit is set to 1: Destination of the Sa5 National bit is the data link interface.
3	Receive Sa4 Data Link Select	R/W	**Receive Sa4 Data Link Select:** This READ/WRITE bit-field permit the user to select data destination of the Sa4 National bit. When this bit is set to 0: Destination of the Sa4 National bit is not the data link interface. When this bit is set to 1: Destination of the Sa4 National bit is the data link interface.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2-0	Receive Signaling and Data Link Select	R/W	**Receive Signaling and Data Link Select:** These READ/WRITE bit-fields permit the user to select data destination of the National bits, the timeslot 16 octet as well as the D or E time slot. **National Bits** When these bits are set to 000: The data link interface is destination of the Sa4 through Sa8 Nation bits, if the corresponding Receive Sa Data Link Select bit(s) (Bit 3 to Bit 7 of the Receive Signaling and Data Link Select Register) are set to 1. When these bits are set to 001: The data link interface is destination of the Sa4 through Sa8 Nation bits, if the corresponding Receive Sa Data Link Select bit(s) (Bit 3 to Bit 7 of the Receive Signaling and Data Link Select Register) are set to 1. When these bits are set to 010: The Sa4 through Sa8 Nation bits are forced to 1.When these bits are set to 011:The Sa4 through Sa8 Nation bits are forced to 1. When these bits are set to 100: The data link interface is destination of the Sa4 through Sa8 Nation bits, if the corresponding Receive Sa Data Link Select bit(s) (Bit 3 to Bit 7 of the Receive Signaling and Data Link Select Register) are set to 1. When these bits are set to 101: Reserved. When these bits are set to 110: Reserved. When these bits are set to 111: Reserved. **Timeslot 16 Octet** When these bits are set to 000: Timeslot 16 octet is taken directly from the PCM data which in term determines by the Receive Channel Control Register (RCCR). When these bits are set to 001: Timeslot 16 octet is output by the Receive Overhead Input Interface through the RxOH_n pin or by the Receive Signaling Serial Interface through the RxSig_n pin. The Receive Signaling Register Array (RSRA) of each timeslot stores its correspondent Timeslot 16 octet as well. When these bits are set to 010: Timeslot 16 octet is output by the Receive Overhead Input Interface through the RxOH_n pin or by the Receive Signaling Serial Interface through the RxSig_n pin. The Receive Signaling Register Array (RSRA) of each timeslot stores its correspondent Timeslot 16 octet as well. When these bits are set to 011: Timeslot 16 octet is output by the Receive Overhead Input Interface through the RxOH_n pin or by the Receive Signaling Serial Interface through the RxSig_n pin. The Receive Signaling Register Array (RSRA) of each timeslot stores its correspondent Timeslot 16 octet as well.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
			When these bits are set to 100: Timeslot 16 octet is taken directly from the PCM data which in term determines by the Receive Channel Control Register (RCCR). When these bits are set to 101: Reserved. When these bits are set to 110: Reserved. When these bits are set to 111: **Reserved.D/E Time Slot** When these bits are set to 000: D or E time slot data are output through the Receive Fractional Data Input Interface (RxFrTD_n pin). When these bits are set to 001: D or E time slot data are output through the Receive Fractional Data Input Interface (RxFrTD_n pin). When these bits are set to 010: D or E time slot data are output through the Receive Fractional Data Input Interface (RxFrTD_n pin). When these bits are set to 011: D or E time slot data are output through the Receive Fractional Data Input Interface (RxFrTD_n pin). When these bits are set to 100: D or E time slot data are output through the Receive Serial Signaling Input Interface (RxSig_n pin). When these bits are set to 101: Reserved. When these bits are set to 110: Reserved. When these bits are set to 111: Reserved. The following table summaries destinations of National bits, Timeslot 16 octet and D or E time slots.

RxSIGDL[2:0]	National Bits (Sa4-Sa8)	Timeslot 16 Octet	D or E Timeslot
000	Data Link	RCCR	RxFrTD_n
001	Data Link	RxSig_n or RxOH	RxFrTD_n
010	None	RxSig_n or RxOH	RxFrTD_n
011	None	RxSig_n or RxOH	RxFrTD_n
100	Data Link	RCCR	RxSig_n
101	Reserved	Reserved	Reserved
110	Reserved	Reserved	Reserved
111	Reserved	Reserved	Reserved

Signaling Change Register 0 (SCR0) (Indirect Address = 0xn0H, 0x0DH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Signaling Change Bit of Channel 0	Signaling Change Bit of Channel 1	Signaling Change Bit of Channel 2	Signaling Change Bit of Channel 3	Signaling Change Bit of Channel 4	Signaling Change Bit of Channel 5	Signaling Change Bit of Channel 6	Signaling Change Bit of Channel 7
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	Signaling Change Indication	RUR	**Signaling Change Indication:** These Reset Upon Read bit-fields indicate whether the signaling data associated with Channel 0-7 has changed since the last read of this register. When these bits are zero: Signaling data associated with certain channel has not changed since last read of the register. When these bits are one: Signaling data associated with certain channel has changed since last read of the register.

Signaling Change Register 1 (SCR0) (Indirect Address = 0xn0H, 0x0EH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Signaling Change Bit of Channel 8	Signaling Change Bit of Channel 9	Signaling Change Bit of Channel 10	Signaling Change Bit of Channel 11	Signaling Change Bit of Channel 12	Signaling Change Bit of Channel 13	Signaling Change Bit of Channel 14	Signaling Change Bit of Channel 15
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	Signaling Change Indication	RUR	**Signaling Change Indication:** These Reset Upon Read bit-fields indicate whether the signaling data associated with Channel 8-15 has changed since the last read of this register. When these bits are zero: Signaling data associated with certain channel has not changed since last read of the register. When these bits are one: Signaling data associated with certain channel has changed since last read of the register.

Signaling Change Register 2 (SCR2) (Indirect Address = 0xn0H, 0x0FH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Signaling Change Bit of Channel 16	Signaling Change Bit of Channel 17	Signaling Change Bit of Channel 18	Signaling Change Bit of Channel 19	Signaling Change Bit of Channel 20	Signaling Change Bit of Channel 21	Signaling Change Bit of Channel 22	Signaling Change Bit of Channel 23
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	Signaling Change Indication	RUR	**Signaling Change Indication:** These Reset Upon Read bit-fields indicate whether the signaling data associated with Channel 16-23 has changed since the last read of this register. When these bits are zero: Signaling data associated with certain channel has not changed since last read of the register. When these bits are one: Signaling data associated with certain channel has changed since last read of the register.

Signaling Change Register 3 (SCR3) - E1 Mode Only (Indirect Address = 0xn0H, 0x10H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Signaling Change Bit of Channel 24	Signaling Change Bit of Channel 25	Signaling Change Bit of Channel 26	Signaling Change Bit of Channel 27	Signaling Change Bit of Channel 28	Signaling Change Bit of Channel 29	Signaling Change Bit of Channel 30	Signaling Change Bit of Channel 31
RUR	RUR	RUR	RUR	RUR	RUR	RUR	RUR
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	Signaling Change Indication	RUR	**Signaling Change Indication:** These Reset Upon Read bit-fields indicate whether the signaling data associated with Channel 24-31 has changed since the last read of this register. When these bits are zero: Signaling data associated with certain channel has not changed since last read of the register. When these bits are one: Signaling data associated with certain channel has changed since last read of the register.

Receive National Bits Register (RNBR) - E1 Mode Only (Indirect Address = 0xn0H, 0x11H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
International Bit in FAS Frame	International Bit in Non-FAS Frame	Remote Alarm Indication Bit	National Bit Sa4	National Bit Sa3	National Bit Sa2	National Bit Sa1	National Bit Sa0
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	International Bit in FAS Frame	R/O	**International Bit in FAS Frame:** This READ-only bit-field corresponds to the value contained in the International Bit of received FAS Frame.
6	International Bit in non-FAS Frame	R/O	**International Bit in non-FAS Frame:** This READ-only bit-field corresponds to the value contained in the International Bit of received non-FAS Frame.
5	Remote Alarm Indication Bit	R/O	**Remote Alarm Indication Bit:** This READ-only bit-field corresponds to the value contained in the Remote Alarm Indication (frame Yellow Alarm) bit position of the received non-FAS Frame.
4	National Bit Sa4	R/O	**National Bit Sa4:** This READ-only bit-field corresponds to the value contained in the National bit Sa4 position of the received non-FAS frame.
3	National Bit Sa5	R/O	**National Bit Sa5:** This READ-only bit-field corresponds to the value contained in the National bit Sa4 position of the received non-FAS frame.
2	National Bit Sa6	R/O	**National Bit Sa6:** This READ-only bit-field corresponds to the value contained in the National bit Sa4 position of the received non-FAS frame.
1	National Bit Sa7	R/O	**National Bit Sa7:** This READ-only bit-field corresponds to the value contained in the National bit Sa4 position of the received non-FAS frame.
0	National Bit Sa8	R/O	**National Bit Sa8:** This READ-only bit-field corresponds to the value contained in the National bit Sa4 position of the received non-FAS frame.

Receive Extra Bits Register (REBR) - E1 Mode Only (Indirect Address = 0xn0H, 0x12H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Reserved				Extra Bit 1	Far-End Remote Alarm Indication Bit	Extra Bit 2	Extra Bit 3
R/O	R/O	R/O	R/O	R/O	R/O	R/O	R/O
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7 - 4	Reserved	R/O	
3	Extra Bit 1	R/O	**Extra Bit 1:** This READ-only bit-field corresponds to the value contained in the Extra Bit 1 position (bit 5 in timeslot 16 of Frame 0 of the CAS multi-frame) of the received E1 data.
2	Far-End Remote Alarm Indication Bit	R/O	**Far-End Remote Alarm Indication Bit:** This READ-only bit-field corresponds to the value contained in the Far-End Remote Alarm Indication (CAS Multi-frame Yellow Alarm) bit position (bit 6 in timeslot 16 of Frame 0 of the CAS multi-frame) of the received non-FAS Frame.
1	Extra Bit 2	R/O	**Extra Bit 2:** This READ-only bit-field corresponds to the value contained in the Extra Bit 2 position (bit 7 in timeslot 16 of Frame 0 of the CAS multi-frame) of the received E1 data.
0	Extra Bit 3	R/O	**Extra Bit 3:** This READ-only bit-field corresponds to the value contained in the Extra Bit 3 position (bit 8 in timeslot 16 of Frame 0 of the CAS multi-frame) of the received E1 data.

Data Link Control Register (DLCR) (Indirect Address = 0xn0H, 0x13H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
SLCâ96 Enable	MOS ABORT Enable	Receive FCS Verification Enable	Automatic Receive LAPD Message	Transmit ABORT Sequence	Transmit IDLE/FLAG Sequence	Transmit LAPD Message with FCS	MOS or BOS Select
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	SLC®96 Enable	R/W	**SLC®96 Enable:** This READ/WRITE bit-field permits the user to enable SLC®96 data link transmission in SLC®96 framing mode. In ESF framing mode, this READ/WRITE bit-field allows Facility Data Link of the framer to transmit and receive SLC®96-like message. When this bit is set to zero: In SLC®96 framing mode, the SLC®96 data link transmission is disabled. The framer transmits Terminal Framing bits as in SF framing mode. The Signaling Framing bits are forced to ones. In ESF framing mode, Facility Data Link of the framer is configured to transmit and receive regular data link message. When this bit is set to one: In SLC®96 framing mode, the SLC®96 data link transmission is enabled. The framer transmits Terminal Framing bits as in SF framing mode. The Signaling Framing bits are transmitted and received in SLC®96 data link format. In ESF framing mode, Facility Data Link of the framer is configured to transmit and receive SLC®96-like message.
6	MOS ABORT Enable	R/W	**MOS ABORT Enable:** This READ/WRITE bit-field enables and disables the Transmit LAPD Controller of the framer to automatically insert an ABORT sequence anytime it transitions from the Message Oriented Signaling (MOS) mode to the Bit Oriented Signaling (BOS) mode. When this bit is set to zero: The Transmit LAPD Controller inserts an MOS ABORT sequence to the data link message when the framer transitions from MOS to BOS. When this bit is set to one: The Transmit LAPD Controller does not insert an MOS ABORT sequence to the data link message when the framer transitions from MOS to BOS.
5	Receive FCS Verification Enable	R/W	**Receive FCS Verification Enable:** This READ/WRITE bit-field enables and disables the Receive LAPD Controller of the framer to compute and verify the Frame Check Sequence (FCS) value in the incoming LAPD message. When this bit is set to zero: The Receive LAPD Controller computes and verifies the Frame Check Sequence (FCS) of each MOS message. When this bit is set to one: The Receive LAPD Controller does not compute and verify the Frame Check Sequence (FCS) of each MOS message.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Automatic Receive LAPD Message	R/W	**Automatic Receive LAPD Message:** This READ/WRITE bit-field configures the Receive LAPD Controller of the framer to compare and discard any incoming LAPD message that exactly match which is currently stored in the Receive LAPD Controller. When this bit is set to zero: The Receive LAPD Controller does not discard any incoming LAPD message. Every incoming LAPD message automatically stores in the Receive LAPD Controller and overwrites the previous received LAPD message. When this bit is set to one: The Receive LAPD Controller compares any incoming LAPD message with the previous message that is currently stored in the Received LAPD Controller. If the incoming LAPD message is the same as the previous one, it will be automatically discarded.
3	Transmit ABORT Sequence	R/W	**Transmit ABORT Sequence:** This READ/WRITE bit-field configures the Transmit LAPD Controller to transmit an ABORT sequence into the Facility Data Link channel to the remote terminal. An ABORT sequence is a string of seven or more consecutive ones. When this bit is set to zero: The Transmit LAPD Controller does not insert an ABORT sequence into the Facility Data Link channel. When this bit is set to one: The transmit LAPD Controller inserts an ABORT sequence into the Facility Data Link channel.
2	Transmit IDLE/FLAG Sequence	R/W	**Transmit IDLE/FLAG Sequence:** This READ/WRITE bit-field configures the Transmit LAPD Controller to insert a string of IDLE/Flag sequence into the Facility Data Link channel to the remote terminal. An IDLE/FLAG sequence is an octet of with value 0x7E. When this bit is set to zero: The Transmit LAPD Controller does not insert an IDLE/FLAG sequence into the Facility Data Link channel. When this bit is set to one: The Transmit LAPD Controller inserts an IDLE/FLAG sequence into the Facility Data Link channel.
1	Transmit LAPD Message with FCS	R/W	**Transmit LAPD Message with FCS:** This READ/WRITE bit-field forces the Transmit LAPD Controller to include Frame Check Sequence (FCS) octets into the outbound LAPD message. When this bit is set to zero: The Transmit LAPD Controller does not include FCS octets into the outbound LAPD message. When this bit is set to one: The Transmit LAPD Controller inserts FCS octets into the outbound LAPD message. ***NOTE:*** *This bit-field is ignored if the framer is configured to operate in BOS mode.*

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	MOS or BOS Select	R/W	**MOS or BOS Select:** This READ/WRITE bit-field specifies whether the Transmit and Receive LAPD Controller to operate in Message Oriented Signaling (MOS) or Bit Oriented Signaling (BOS) mode. When this bit is set to zero: The Transmit and Receive LAPD Controller transmit and receive LAPD message in MOS mode. When this bit is set to one: The Transmit and Receive LAPD Controller transmit and receive LAPD message in BOS mode.

Transmit Data Link Byte Count Register (TDLBCR) (Indirect Address = 0xn0H, 0x14H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Transmit Data Link Buffer Select	Transmit Data Link Byte Count Bits [6:0]						
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Transmit Data Link Buffer Select	R/W	**Transmit Data Link Buffer Select:** This READ/WRITE bit-field permits the user to select which one of the two Transmit Data Link Buffers will be loaded for transmission. When this bit is set to zero: The Transmit Data Link Buffer 0 will be loaded for transmission of data link bits. When this bit is set to one: The Transmit Data Link Buffer 1 will be loaded for transmission of data link bits.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6 - 0	Transmit Data Link Byte Count [6:0]	R/W	**Transmit Data Link Byte Count [6:0]:** These READ/WRITE bit-fields hold the length of the MOS message to be transmitted or the number of repetitions of BOS to be transmitted. The user should program these bit-fields to equal the length of the MOS message in bytes or the number of repetitions of BOS message. The LAPD controller will load the value of these bits from the Transmit Data Link Byte Count register and use it as its internal counter at the beginning of each transfer. After the entire MOS message is transmitted or x number of repetitions of BOS message transmission is completed, the LAPD controller will generate the Transmit End of Transfer (TxEOT) interrupt. Each Transmit Data Link Buffer is 96-bytes wide. ***NOTE:*** *In the case of BOS messaging, if these bit-fields are equal to zero, the BOS message will be transmitted infinitely and no Transmit End of Transfer (TxEOT) interrupt will be generated.*

Receive Data Link Byte Count Register (TDLBCR) (Indirect Address = 0xn0H, 0x15H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Receive Data Link Buffer Select	Receive Data Link Byte Count Bits [6:0]						
R	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Data Link Buffer Select	R	**Receive Data Link Buffer Select:** This READ/WRITE bit-field informs the user which one of the two Receive Data Link Buffers are available for receiving data link messages. When this bit is set to zero: The Receive Data Link Buffer 0 will be used for received data link bits. When this bit is set to one: The Receive Data Link Buffer 1 will be used for received data link bits.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6 - 0	Receive Data Link Byte Count [6:0]	R/W	**Receive Data Link Byte Count [6:0]:** These READ/WRITE bit-fields hold the length of the MOS message received or the number of repetitions of BOS message received. The user should program these bit-fields to equal the length of the MOS message in bytes or the number of repetitions of BOS message. The LAPD controller will load the value of these bits from the Receive Data Link Byte Count register and use it as its internal counter at the beginning of each transfer. After the entire MOS message is received or x number of repetitions of BOS message is received, the LAPD controller will generate the Receive End of Transfer (RxEOT) interrupt. Each Receive Data Link Buffer is 96-bytes wide. ***NOTE:*** *In the case of BOS messaging, these bit-fields cannot be set to zero. Otherwise, no Receive End of Transfer (RxEOT) interrupt will be generated.*

Slip Buffer Control Register (SBCR) (Indirect Address = 0xn0H, 0x16H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Transmit Slip Buffer is FIFO	Reserved		Force Signaling Freeze	Signaling Freeze Enable	Slip Buffer Receive Synchronization Direction	Slip Buffer Enable Bit [1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Transmit Slip Buffer is FIFO	R/W	**Slip Buffer is FIFO:** This READ/WRITE bit-field allows the user to determine function of the buffer when TxLineClk_n and TxSerClk_n are synchronized with each other. When this bit is 0: The buffer acts as slip buffer if enabled by the Slip Buffer Enable bit [1:0]. When this bit is 1: The buffer acts as FIFO.
6 - 5	Reserved		

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Force Signaling Freeze	R/W	**Force Signaling Freeze:** This READ/WRITE bit-field allows the user to stop further signaling updating. When this bit is 0: The framer continues extracts and updates signaling information received. When this bit is 1: The framer stops extracting signaling information received, this is called Signaling Freeze.
3	Signaling Freeze Enable	R/W	**Signaling Freeze Enable:** This READ/WRITE allows the user to stop the framer from updating signaling information for one multi-frame after buffer slipping. Enabling signaling freeze after buffer slipping can eliminate incorrect signaling information been extracted and updated by the framer. When this bit is 0: Signaling freeze is disabled. The framer will continue to extract and update signaling information for one multi-framer after buffer slipping. When this bit is 1: Signaling freeze is enabled. The framer will not extract and update signaling information for one multi-framer after buffer slipping.
2	Slip Buffer Receive Synchronization Direction	R/W	**Slip Buffer Receive Synchronization Direction:** When this bit is set to 0: The Receive Single-Frame Synchronization signal (RxSync_n) is an output if the Slip Buffer is not in bypass mode. When this bit is set to 1: The Receive Single-Frame Synchronization signal (RxSync_n) is an input if the Slip Buffer is not in bypass mode.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Slip Buffer Enable	R/W	**Slip Buffer Enable:** When these bits are set to 00: Slip Buffer is bypassed. The Receive Payload Data is passing from the Receive Framer Module to the Receive Payload Data Output Interface directly without routing through the Slip Buffer. The Receive Serial Clock signal (RxSerClk_n) is an output. When these bits are set to 01: The Elastic Store (Slip Buffer) is enabled. The Receive Payload Data is passing from the Receive Framer Module through the Slip Buffer to the Receive Payload Data Output Interface. The Receive Serial Clock signal (RxSerClk_n) is an input. When these bits are set to 10: The Slip Buffer acts as a FIFO. The FIFO Latency Register (FLR) determines the data latency. The Receive Payload Data is passing from the Receive Framer Module through the FIFO to the Receive Payload Data Output Interface. The Receive Serial Clock signal (RxSerClk_n) is an input. When these bits are set to 11: Slip Buffer is bypassed. The Receive Payload Data is passing from the Receive Framer Module to the Receive Payload Data Output Interface directly without routing through the Slip Buffer. The Receive Serial Clock signal (RxSerClk_n) is an output.

FIFO Latency Register (FIFOLR) (Indirect Address = 0xn0H, 0x17H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Reserved			FIFO Latency [4:0]				
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-5	Reserved	R/W	
4-0	FIFO Latency	R/W	**FIFO Latency:** These bits determine depth of the FIFO in terms of bytes. The largest possible value is thirty-two bytes or one E1 frame.

Interrupt Control Register (ICR) (Indirect Address = 0xn0H, 0x1AH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Reserved					Clear Interrupt Status Bits By Write	Clear Interrupt Enable Bits	Enable of Interrupt Generation
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-3	Reserved	R/W	
2	Clear Interrupt Status Bits By Write	R/W	***Clear Interrupt Status Bit By Write:*** This Read/Write bit field determines how to clear the interrupt status bits. When this bit is set to 0: The status bits are reset upon read. When this bit is set to 1: The status bits are reset by writing a zero.
1	Clear Interrupt Enable Bits	R/W	**Clear Interrupt Enable Bit:** This Read/Write bit field determines how to clear the interrupt enable bits. When this bit is set to 0: The status bits are not reset upon reading of corresponding status bits. When this bit is set to 1: The status bits are reset upon reading of corresponding status bits.
0	Enable of Interrupt Generation	R/W	**Enable of Interrupt Generation:** This Read/Write bit field is used to enable T1/E1 framer interrupt generation. When this bit is set to 0: XRT84L38 will not generate interrupt. Instead, status polling of the framer will be enabled. When this bit is set to 1: Interrupt generation is enabled.

LAPD Channel Select Register (LCSR) (Indirect Address = 0xn0H, 0x1BH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Reserved						LAPD Channel Select Bit [1:0]	
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-2	Reserved	R/W	
1-0	LAPD Channel Select Bit [1:0]	R/W	**LAPD Channel Select Bit [1:0]:** These Read/Write bit fields determine which one of the three current LAPD channel being accessed. When these bits are set to 00: LAPD Channel 1 is being accessed. When these bits are set to 01: LAPD Channel 2 is being accessed. When these bits are set to 10: LAPD Channel 3 is being accessed. When these bits are set to 11: LAPD Channel 1 is being accessed.

Transmit Interface Control Register (TICR) (Indirect Address = 0xn0H, 0x20H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Transmit Fraction Data Interface Select	Reserved	Transmit Payload Clock Select / Transmit Sync- Pulse Low Active Select	Transmit Fractional E1 Input Enable	Transmit Clock Inversion	Transmit Multiplex Enable	Transmit Interface Mode Select Bit 1	Transmit Interface Mode Select Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Transmit Fraction Data Interface Select	R/W	**Transmit Fraction Data Interface Select:** When this bit is set to 0: The Transmit Serial Fractional Data (TxFrTD_n) input pins are used to accept fractional serial data. The Transmit Timeslot Clock (TxTsClk_n) pins are used to output fractional data clock. When this bit is set to 1: The Transmit Timeslot Clock (TxTSClk_n) pins are used to input fractional serial data enable signal. Fractional serial data is clocked into the framer using ungapped TxSerClk_n signals.
6	Reserved		
5	Transmit Payload Clock Select / Transmit Sync- Pulse Low Active Select	R/W	Transmit Payload Clock Select / Transmit Sync- Pulse Low Active Select: When this bit is set to 0: The TxSerClk_n pins will output ungapped Transmit clock for correspondent DS1/E1 clock rates. In non-1.544 MHz mode for DS1 or non-2.048 MHz mode for E1, the XRT84L38 chip expects a HIGH active pulse for frame synchronization. When this bit is set to 1: The TxSerClk_n pins will output a gapped Transmit clock with OH bit period blocked for correspondent DS1/E1 clock rates. In non-1.544 MHz mode for DS1 or non-2.048 MHz mode for E1, the XRT84L38 chip expects a LOW active pulse for frame synchronization.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Transmit Fractional E1 Input Enable	R/W	**Transmit Fractional E1 Input Enable:** When this bit is set to 0: The Transmit Time-slot Indication bits (TxTSb[4:0] are outputting five-bit binary values of Time-slot number (0-31) being accepted and processed by the Transmit Payload Data Input Interface block of the framer. The Transmit Time-slot Indicator Clock signal (TxTSClk_n) is a 256KHz clock that pulses HIGH for one E1 bit period whenever the Transmit Payload Data Input Interface block is accepting the LSB of each of the twenty-four time slots. When this bit is set to 1: The TxTSb[0]_n bit becomes the Transmit Fractional E1 Input signal (TxFrTD_n) which carries Fractional E1 payload data into the framer. The TxTSb[1]_n bit becomes the Transmit Signaling Data Input signal (TxSig_n) which is used to insert robbed-bit signaling data into the outbound E1 frame. The TxTSb[2]_n bit serially outputs all five-bit binary values of the Time Slot number (0-31) being accepted and processed by the Transmit Payload Data Input Interface block of the framer. The TxTSb[3]_n bit becomes the Transmit Overhead Synchronization Pulse (TxOHSync_n) which is used to output an Overhead Synchronization Pulse that indicates the first bit of each E1multi-frame. The TxTSClk_n will output gaped fractional E1 clock that can be used by Terminal Equipment to clock out Fractional E1 payload data at rising edge of the clock. Or, The TxTSClk_n pin will be a clock enable signal to Transmit Fractional E1 Input signal (TxFrTD_n) when the un-gaped Transmit Serail Input Clock (TxSerClk_n) is used to clock in Fractional E1 Payload Data into the framer.
3	Transmit Clock Inversion	R/W	**Transmit Clock Inversion:** When this bit is set to 0: Serial data transition happens on rising edge of the Transmit Serial Clock. When this bit is set to 1: Serial data transition happens on falling edge of the Transmit Serial Clock.
2	Transmit Multiplex Enable	R/W	**Transmit Multiplex Enable:** When this bit is set to 0: The Transmit Back-plane Interface block is configured to non-channel-multiplexed mode When this bit is set to 1: The Transmit Back-plane Interface block is configured to channel-multiplexed mode

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Interface Mode Select	R/W	**Transmit Interface Mode Select:** When combined with the Transmit Multiplex Enable bit, these bits determine the Transmit Back-plane Interface data rate. The table below illustrates the Transmit Back-plane Interface data rate for E1 mode with different Transmit Multiplex Enable bit and Transmit Interface Mode Select Bits settings.

Transmit Multiplex Enable Bit	Transmit Interface Mode Select Bit 1	Transmit Interface Mode Select Bit 0	Back-plane Interface Data Rate
0	0	0	XRT84V24 Compatible 2.048Mbit/s
0	0	1	MVIP 2.048Mbit/s
0	1	0	4.096Mbit/s
0	1	1	8.192Mbit/s
1	0	0	-
1	0	1	Bit Multiplexed 16.384Mbit/s
1	1	0	HMVIP 16.384Mbit/s
1	1	1	H.100 16.384Mbit/s

Receive Interface Control Register (RICR) (Indirect Address = 0xn0H, 0x22H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Receive Fraction Data Interface Select	Reserved	Receive Payload Clock Select / Receive Sync- Pulse Low Active Select	Receive Fractional E1 Input Enable	Receive Clock Inversion	Receive Multiplex Enable	Receive Interface Mode Select Bit 1	Receive Interface Mode Select Bit 0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Fraction Data Interface Select	R/W	**Receive Fraction Data Interface Select:** When this bit is set to 0: The Receive Serial Fractional Data (RxFrTD_n) output pins are used to output fractional serial data. The Receive Timeslot Clock (RxTsClk_n) pins are used to output fractional data clock. When this bit is set to 1: The Receive Timeslot Clock (RxTSClk_n) pins are used to output fractional serial data enable signal. Fractional serial data is clocked out from the framer using ungapped RxSerClk_n signals.
6	Reserved		
5	Receive Payload Clock Select / Receive Sync- Pulse Low Active Select	R/W	**Receive Payload Clock Select / Receive Sync- Pulse Low Active Select:** When this bit is set to 0: The RxSerClk_n pins will output ungapped Receive clock for correspondent DS1/E1 clock rates. In non-1.544 MHz mode for DS1 or non-2.048 MHz mode for E1, the XRT84L38 chip generates a HIGH active pulse for frame synchronization. When this bit is set to 1: The RxSerClk_n pins will output a gapped Receive clock with OH bit period blocked for correspondent DS1/E1 clock rates. In non-1.544 MHz mode for DS1 or non-2.048 MHz mode for E1, the XRT84L38 chip generates a LOW active pulse for frame synchronization.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Fractional E1 Output Enable	R/W	**Receive Fractional E1 Output Enable:** When this bit is set to 0: The Receive Time-slot Indication bits (RxTSb[4:0] are outputting five-bit binary values of Time-slot number (0-31) being accepted and processed by the Receive Payload Data Output Interface block of the framer. The Receive Time-slot Indicator Clock signal (RxTSClk_n) is a 256KHz clock that pulses HIGH for one E1 bit period whenever the Receive Payload Data Output Interface block is accepting the LSB of each of the twenty-four time slots. When this bit is set to 1: The RxTSb[0]_n bit becomes the Receive Fractional E1 Output signal (RxFrTD_n) which carries Fractional E1 payload data from the framer. The RxTSb[1]_n bit becomes the Receive Signaling Data Output signal (RxSig_n) which is used to carry robbed-bit signaling data extracted from the inbound E1 frame. The RxTSb[2]_n bit serially outputs all five-bit binary values of the Time Slot number (0-31) being accepted and processed by the Receive Payload Data Output Interface block of the framer. The RxTSClk_n will output gaped fractional E1 clock that can be used by Terminal Equipment to latch in Fractional E1 payload data at rising edge of the clock. Or, The RxTSClk_n pin will be a clock enable signal to Receive Fractional E1 Output signal (RxFrTD_n) when the un-gaped Receive Serail Output Clock (RxSerClk_n) is used to latch in Fractional E1 Payload Data into the Terminal Equipment.
3	Receive Clock Inversion	R/W	**Receive Clock Inversion:** When this bit is set to 0: Serial data transition happens on rising edge of the Receive Serial Clock. When this bit is set to 1: Serial data transition happens on falling edge of the Receive Serial Clock.
2	Receive Multiplex Enable	R/W	**Receive Multiplex Enable:** When this bit is set to 0: The Receive Back-plane Interface block is configured to non-channel-multiplexed mode. When this bit is set to 1: The Receive Back-plane Interface block is configured to chan-nel-multiplexed mode

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Receive Interface Mode Select	R/W	**Receive Interface Mode Select:** When combined with the Receive Multiplex Enable bit, these bits determine the Receive Back-plane Interface data rate. The table below illustrates the Receive Back-plane Interface data rate for E1 mode with different Receive Multiplex Enable bit and Receive Interface Mode Select Bits settings.

Receive Multiplex Enable Bit	Receive Interface Mode Select Bit 1	Receive Interface Mode Select Bit 0	Back-plane Interface Data Rate
0	0	0	XRT84V24 Compatible 2.048Mbit/s
0	0	1	MVIP 2.048Mbit/s
0	1	0	4.096Mbit/s
0	1	1	8.192Mbit/s
1	0	0	-
1	0	1	Bit Multiplexed 16.384Mbit/s
1	1	0	HMVIP 16.384Mbit/s
1	1	1	H.100 16.384Mbit/s

General Test Register (GTR) (Indirect Address = 0xn0H, 0x23H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
PRBS Type Select	Error Insertion	Data Inversion Select	Receive PRBS Lock Indication	Receive PRBS Block Enable	Transmit PRBS Block Enable	Receive DS1/ E1 Framer Bypassed	Transmit DS1/ E1 Framer Bypassed
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	PRBS Type Select	R/W	**PRBS Type Select:** When this bit is set to 0: The polynomial for generating the PRBS pattern is X15 + X14 + 1. When this bit is set to 1: A QRTS pattern is generated as the PRBS pattern.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Error Insertion	R/W	**Error Insertion:** A zero to one transition of this bit will cause one bit of the outgoing transmit data inverted.
5	Data Inversion Select	R/W	**Data Inversion Select:** When this bit is set to 0: The outgoing transmit data and incoming receive data are not changed. When this bit is set to 1: The outgoing transmit data and incoming receive data are inverted.
4	Receive PRBS Lock Indication	R/W	**Receive PRBS Lock Indication:** If the Receive PRBS block is enabled, this bit indicates whether a PRBS pattern is found in the incoming received data and the PRBS pattern is locked. When this bit is set to 0: There is no PRBS pattern found and locked in the incoming received data stream. When this bit is set to 1: A PRBS pattern found and locked in the incoming received data stream.
3	Receive PRBS Block Enable	R/W	**Receive PRBS Block Enable :** When this bit is set to 0: The Receive PRBS block is disabled. The framer will not check the incoming received data for PRBS pattern. When this bit is set to 1: The Receive PRBS block is enabled. The framer will check the incoming received data for PRBS pattern.
2	Transmit PRBS Block Enable	R/W	**Transmit PRBS Block Enable :** When this bit is set to 0: The Transmit PRBS block is disabled. The framer will not insert PRBS pattern into the outgoing transmit data stream. When this bit is set to 1: The Transmit PRBS block is enabled. The framer will insert PRBS pattern into the outgoing transmit data stream.
1	Receive DS1/E1 Framer Bypassed	R/W	**Receive DS1/E1 Framer Bypassed:** When this bit is set to 0: The Receive DS1/E1 Framer is not bypassed. When this bit is set to 1: The Receive DS1/E1 Framer is bypassed.
0	Transmit DS1/E1 Framer Bypassed	R/W	**Transmit DS1/E1 Framer Bypassed:** When this bit is set to 0: The Transmit DS1/E1 framer is not bypassed. When this bit is set to 1: The Transmit DS1/E1 framer is bypassed. Unframed DS1/E1 payload data are passed from backplane interface into the DS1/E1 line.

Loop-back Code Control Register (LCCR) (Indirect Address = 0xn0H, 0x24H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Receive Loop-back Code Activation Length Bit 1	Receive Loop-back Code Activation Length Bit 0	Receive Loop-back Code De-Activation Length Bit 1	Receive Loop-back Code De-Activation Length Bit 0	Transmit Loop-back Code Length Bit 1	Transmit Loop-back Code Length Bit 0	Framed Loop-back Code Select	Automatic Loop-back Select
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-6	Receive Loop-back Code Activation Length	R/W	**Receive Loop-back Code Activation Length:** These bits are used to determine the Receive Loop-back Code Activation length. The table below shows length of the Receive Loop-back Activation code according to values of these bits. **Bit Value** / **Length of Loop-back Code** 00 / 4 01 / 5 10 / 6 11 / 7
5-4	Receive Loop-back Code De-Activation Length	R/W	**Receive Loop-back Code Activation Length:** These bits are used to determine the Receive Loop-back Code De-Activation length. The table below shows length of the Receive Loop-back De-Activation code according to values of these bits. **Bit Value** / **Length of Loop-back Code** 00 / 4 01 / 5 10 / 6 11 / 7

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Transmit Loop-back Code Length	R/W	**Transmit Loop-back Code Length:** These bits are used to determine the Transmit Loop-back Code Activation length. The table below shows length of the Transmit Loop-back code according to values of these bits. **Bit Value** / **Length of Loop-back Code** 00 / 4 01 / 5 10 / 6 11 / 7
1	Framed Loop-back Code Select	R/W	**Framed Loop-back Code Select:** When this bit is set to 0: The Loop-back code that transmitted or recieved is unframed. When this bit is set to 1: The Loop-back code that transmitted or received is framed.
0	Automatic Loop-back Select	R/W	**Automatic Loop-back Select:** When this bit is set to 0: Automatic Loop-back is disabled. When this bit is set to 1: Automatic Loop-back is enabled.

Transmit Loop-back Code Register (TLCR) (Indirect Address = 0xn0H, 0x25H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Transmit Loop-back Code Bit[6:0]							Transmit Loop-back Code Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-1	Transmit Loop-back Code Bit[6:0]	R/W	**Transmit Loop-back Code Bit[6:0]:** These bits are the Transmit Loop-back Code sequence.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	Transmit Loop-back Code Enable	R/W	**Transmit Loop-back Code Enable:** When this bit is set to 0: Transmit Loop-back Code is disabled. Transmit Loop-back Code is not sent to the line. When this bit is set to 1: Transmit Loop-back Code is enabled. Transmit Loop-back Code is generated and repeatedly sent to the line instead of payload data.

Receive Loop-back Activation Code Register (RLACR) (Indirect Address = 0xn0H, 0x26H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Receive Loop-back Activation Code Bit[6:0]							Receive Loop-back Activation Code Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-1	Receive Loop-back Activation Code Bit[6:0]	R/W	**Receive Loop-back Activation Code Bit[6:0]:** These bits are the Receive Loop-back Activation Code sequence.
0	Receive Loop-back Activation Code Enable	R/W	**Receive Loop-back Activation Code Enable:** When this bit is set to 0: Receive Loop-back Activation Code is disabled. Receive Loop-back Activation Code is not sent to the line. When this bit is set to 1: Receive Loop-back Activation Code is enabled. Receive Loop-back Activation Code is generated and repeatedly sent to the line instead of payload data.

Receive Loop-back De-Activation Code Register (RLACR) (Indirect Address = 0xn0H, 0x27H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Receive Loop-back De-Activation Code Bit[6:0]							Receive Loop-back De-Activation Code Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
1	0	1	0	1	0	1	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-1	Receive Loop-back De-Activation Code Bit[6:0]	R/W	**Receive Loop-back De-Activation Code Bit[6:0]:** These bits are the Receive Loop-back De-Activation Code sequence.
0	Receive Loop-back De-Activation Code Enable	R/W	**Receive Loop-back De-Activation Code Enable:** When this bit is set to 0: Receive Loop-back De-Activation Code is disabled. Receive Loop-back De-Activation Code is not sent to the line. When this bit is set to 1: Receive Loop-back De-Activation Code is enabled. Receive Loop-back De-Activation Code is generated and repeatedly sent to the line instead of payload data.

Transmit Sa Select Register (TSASR) (Indirect Address = 0xn0H, 0x030H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Transmit Sa8 Select	Transmit Sa7 Select	Transmit Sa6 Select	Transmit Sa5 Select	Transmit Sa4 Select	Loop-back Mode 1 Auto Enable	Loop-back Mode 2 Auto Enable	Loop-back Release Auto Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Transmit Sa8 Select	R/W	**Transmit Sa8 Select:** This bit determines whether the source of Sa8 bit is from transmit serial input or transmit Sa8 register. When this bit is set to 0: The source of .Sa8 bit is from transmit serial input. When this bit is set to 1: The source of .Sa8 bit is from transmit Sa8 register.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Transmit Sa7 Select	R/W	**Transmit Sa7 Select:** This bit determines whether the source of Sa7 bit is from transmit serial input or transmit Sa7 register. When this bit is set to 0: The source of .Sa7 bit is from transmit serial input. When this bit is set to 1: The source of .Sa7 bit is from transmit Sa7 register.
5	Transmit Sa6 Select	R/W	**Transmit Sa6 Select:** This bit determines whether the source of Sa6 bit is from transmit serial input or transmit Sa6 register. When this bit is set to 0: The source of .Sa6 bit is from transmit serial input. When this bit is set to 1: The source of .Sa6 bit is from transmit Sa6 register.
4	Transmit Sa5 Select	R/W	**Transmit Sa5 Select:** This bit determines whether the source of Sa5 bit is from transmit serial input or transmit Sa5 register. When this bit is set to 0: The source of .Sa5 bit is from transmit serial input. When this bit is set to 1: The source of .Sa5 bit is from transmit Sa5 register.
3	Transmit Sa4 Select	R/W	**Transmit Sa4 Select:** This bit determines whether the source of Sa4 bit is from transmit serial input or transmit Sa4 register. When this bit is set to 0: The source of .Sa4 bit is from transmit serial input. When this bit is set to 1: The source of .Sa4 bit is from transmit Sa4 register.
2	Loop-back Mode 1 Auto Enable	R/W	**Loop-back Mode 1 Auto Enable :** The bit enables local loop-back of the framer while a certain condition is happened. When this bit is 0: No local loop-back is activated. When this bit is 1: Local loop-back is activated if the following condition happened from the transmit serial inputs: • Sa5 = 0 for 8 consecutive times. • Sa6 = 1111 for 8 consecutive times. • Remote yellow alarm bit (A bit) is 1.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Loop-back Mode 2 Auto Enable	R/W	**Loop-back Mode 2 Auto Enable :** The bit enables local loop-back of the framer while a certain condition is happened. When this bit is 0: No local loop-back is activated. When this bit is 1: Local loop-back is activated if the following condition happened from the transmit serial inputs: • Sa5 = 0 for 8 consecutive times. • Sa6 = 1010 for 8 consecutive times. • Remote yellow alarm bit (A bit) is 1.
0	Loop-back Mode Release Auto Enable	R/W	**Loop-back Mode Release Auto Enable :** The bit enables local loop-back to be released automatically if a certain condition is happened. When this bit is 0: No local loop-back is released. When this bit is 1: Local loop-back is released if the following condition happened from the transmit serial inputs: • Sa5 = 0 for 8 consecutive times. • Sa6 = 0000 for 8 consecutive times.

Transmit Sa4 Register (TSA4R) (Indirect Address = 0xn0H, 0x33H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Transmit Sa4 Bit[7:0]							
R/W							
1	1	1	1	1	1	1	1

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	Transmit Sa4 Bit[7:0]	R/W	Transmit Sa4 bit[7:0]: These Read/Write bit fields determine contents of the Sa4 bits when Transmit Sa4 Enable bit is 0 and Transmit Sa4 Select bit is 1. Bit 7 of this register is transmitted as Sa4 bit in Frame 2 of the CRC-4 Multi-frame. Bit 6 of this register is transmitted as Sa4 bit in Frame 4 of the CRC-4 Multi-frame, etc.

Transmit Sa5 Register (TSA5R) (Indirect Address = 0xn0H, 0x34H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Transmit Sa5 Bit[7:0]							
R/W							
1	1	1	1	1	1	1	1

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	Transmit Sa5 Bit[7:0]	R/W	**Transmit Sa5 bit[7:0]:** These Read/Write bit fields determine contents of the Sa5 bits when Transmit Sa5 Enable bit is 0 and Transmit Sa5 Select bit is 1. Bit 7 of this register is transmitted as Sa5 bit in Frame 2 of the CRC-4 Multi-frame. Bit 6 of this register is transmitted as Sa5 bit in Frame 4 of the CRC-4 Multi-frame, etc.

Transmit Sa6 Register (TSA6R) (Indirect Address = 0xn0H, 0x35H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Transmit Sa6 Bit[7:0]							
R/W							
1	1	1	1	1	1	1	1

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	Transmit Sa6 Bit[7:0]	R/W	**Transmit Sa6 bit[7:0]:** These Read/Write bit fields determine contents of the Sa6 bits when Transmit Sa6 Enable bit is 0 and Transmit Sa6 Select bit is 1. Bit 7 of this register is transmitted as Sa6 bit in Frame 2 of the CRC-4 Multi-frame. Bit 6 of this register is transmitted as Sa6 bit in Frame 4 of the CRC-4 Multi-frame, etc.

Transmit Sa7 Register (TSA7R) (Indirect Address = 0xn0H, 0x36H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Transmit Sa7 Bit[7:0]							
R/W							
1	1	1	1	1	1	1	1

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	Transmit Sa7 Bit[7:0]	R/W	**Transmit Sa7 bit[7:0]:** These Read/Write bit fields determine contents of the Sa7 bits when Transmit Sa7 Enable bit is 0 and Transmit Sa7 Select bit is 1. Bit 7 of this register is transmitted as Sa7 bit in Frame 2 of the CRC-4 Multi-frame. Bit 6 of this register is transmitted as Sa7 bit in Frame 4 of the CRC-4 Multi-frame, etc.

Transmit Sa8 Register (TSA8R) (Indirect Address = 0xn0H, 0x37H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Transmit Sa8 Bit[7:0]							
R/W							
1	1	1	1	1	1	1	1

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	Transmit Sa8 Bit[7:0]	R/W	**Transmit Sa8 bit[7:0]:** These Read/Write bit fields determine contents of the Sa8 bits when Transmit Sa8 Enable bit is 0 and Transmit Sa8 Select bit is 1. Bit 7 of this register is transmitted as Sa8 bit in Frame 2 of the CRC-4 Multi-frame. Bit 6 of this register is transmitted as Sa8 bit in Frame 4 of the CRC-4 Multi-frame, etc.

Receive Sa4 Register (RSA4R) (Indirect Address = 0xn0H, 0x3BH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Receive Sa4 Bit[7:0]							
R							
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	Receive Sa4 Bit[7:0]	R/W	**Receive Sa4 bit[7:0]:** These Read/Write bit fields store contents of the Sa4 bits received from the incoming serial data. Bit 7 of this register is received as Sa4 bit in Frame 2 of the CRC-4 Multi-frame. Bit 6 of this register is transmitted as Sa4 bit in Frame 4 of the CRC-4 Multi-frame, etc.

Receive Sa5 Register (RSA5R) (Indirect Address = 0xn0H, 0x3CH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Receive Sa5 Bit[7:0]							
R							
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	Receive Sa5 Bit[7:0]	R/W	**Receive Sa5 bit[7:0]:** These Read/Write bit fields store contents of the Sa5 bits received from the incoming serial data. Bit 7 of this register is received as Sa5 bit in Frame 2 of the CRC-4 Multi-frame. Bit 6 of this register is transmitted as Sa5 bit in Frame 4 of the CRC-4 Multi-frame, etc.

Receive Sa6 Register (RSA6R) (Indirect Address = 0xn0H, 0x3DH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Receive Sa6 Bit[7:0]							
R							
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	Receive Sa6 Bit[7:0]	R/W	**Receive Sa6 bit[7:0]:** These Read/Write bit fields store contents of the Sa6 bits received from the incoming serial data. Bit 7 of this register is received as Sa6 bit in Frame 2 of the CRC-4 Multi-frame. Bit 6 of this register is transmitted as Sa6 bit in Frame 4 of the CRC-4 Multi-frame, etc.

Receive Sa7 Register (RSA7R) (Indirect Address = 0xn0H, 0x3EH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Receive Sa7 Bit[7:0]							
R							
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	Receive Sa7 Bit[7:0]	R/W	**Receive Sa7 bit[7:0]:** These Read/Write bit fields store contents of the Sa7 bits received from the incoming serial data. Bit 7 of this register is received as Sa7 bit in Frame 2 of the CRC-4 Multi-frame. Bit 6 of this register is transmitted as Sa7 bit in Frame 4 of the CRC-4 Multi-frame, etc.

Receive Sa8 Register (RSA8R) (Indirect Address = 0xn0H, 0x3FH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Receive Sa8 Bit[7:0]							
R							
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	Receive Sa8 Bit[7:0]	R/W	**Receive Sa8 bit[7:0]:** These Read/Write bit fields store contents of the Sa8 bits received from the incoming serial data. Bit 7 of this register is received as Sa8 bit in Frame 2 of the CRC-4 Multi-frame. Bit 6 of this register is transmitted as Sa8 bit in Frame 4 of the CRC-4 Multi-frame, etc.

Transmit Channel Control Register (RCCR) (Indirect Address = 0xn02H, 0x00H - 0x1FH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
LAPD Select Bit 1	LAPD Select Bit 0	Transmit Zero Code Suppression Select Bit [1:0] (T1 Mode Only)		Transmit Conditioning Select Bit [3:0]			
		R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-6	LAPD Select Bit [1:0]	R/W	**LAPD Select Bit [1:0]:** When these bits are set to 00: The first LAPD channel is used as data source for D or E time slot. When these bits are set to 01: The second LAPD channel is used as data source for D or E time slot. When these bits are set to 10: In T1 mode, the Transmit D/E Timeslot Source Select bits (TxDE[1:0]) of the Transmit Data Link Select Register (TSDLSR) will determine the data source for D/E time slot. In E1 mode, the Transmit Signaling and Data Link Source Select bits (TxSIGDL[2:0]) of the Transmit Data Link Select Register (TSDLSR) will determine the data source for D/E time slot. When these bits are set to 11: The third LAPD channel is used as data source for D or E time slot.
5-4	Transmit Zero Code Suppression Select {T1 Mode Only}	R/W	**Transmit Zero Code Suppression Select:** When these bits are set to 00: The input DS1 PCM data of this DS0 channel is unchanged. No zero code suppression is used. When these bits are set to 01: AT&T Bit 7 stuffing is used and the input DS1 PCM data of this DS0 channel is modified. When these bits are set to 10: GTE zero code suppression is and the input DS1 PCM data of this DS0 channel is modified. When these bits are set to 11: DDS zero code suppression is and the input DS1 PCM data of this DS0 channel is modified.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-0	Transmit Conditioning Select	R/W	Transmit Conditioning Select: When these bits are set to 0000: The input DS1 PCM data of this DS0 channel is unchanged. When these bits are set to 0001: All 8 bits of the input DS1 PCM data of this DS0 channel are inverted. When these bits are set to 0010: The even bits of the input DS1 PCM data of this DS0 channel are inverted. When these bits are set to 0011: The odd bits of the input DS1 PCM data of this DS0 channel are inverted. When these bits are set to 0100: The input DS1 PCM data of this DS0 channel are replaced by the octet stored in User IDLE Code Register (UCR). When these bits are set to 0101: The input DS1 PCM data of this DS0 channel are replaced by BUSY code (0x7F). When these bits are set to 0110: The input DS1 PCM data of this DS0 channel are replaced by VACANT code (0xFF). When these bits are set to 0111: The input DS1 PCM data of this DS0 channel are replaced by BUSY_TS code (111xxxxx). When these bits are set to 1000: The input DS1 PCM data of this DS0 channel are replaced by MUX-Out-Of-Frame (MOOF) code with value 0x1A. When these bits are set to 1001: The input DS1 PCM data of this DS0 channel are replaced by the A-law digital milliwatt pattern. When these bits are set to 1010: The input DS1 PCM data of this DS0 channel are replaced by the u-law digital milliwatt pattern. When these bits are set to 1011: The MSB bit of the input DS1 PCM data of this DS0 channel is inverted. When these bits are set to 1100: All bits of the input DS1 PCM data of this DS0 channel except MSB bit are inverted. When these bits are set to 1101: The input DS1 PCM data of this DS0 channel are replaced by PRBS pattern created by the internal PRBS Generator of XRT84L38 framer. When these bits are set to 1110: The input DS1 PCM data of this DS0 channel is unchanged. When these bits are set to 1111: This channel is configured as D or E timeslot.

User IDLE Code Register (UCR) (Indirect Address = 0xn02H, 0x20H - 0x3FH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
User IDLE Code Bit [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	User IDLE Code	R/W	**User IDLE Code:** These READ/WRITE bit-fields permits the user store any value of IDLE code into the framer. When the Transmit Data Conditioning Select [3:0] bits of TCCR register of a particular DS0 channel are set to 0100, the input E1 PCM data are replaced by contents of this register and sent to the Transmit LIU Interface.

Transmit Signaling Control Register (TSCR) (Indirect Address = 0xn2H, 0x40H - 0x57H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Signaling Bit A	Signaling Bit B	Signaling Bit C	Signaling Bit D	Reserved	Robbed-bit Signaling Enable	Transmit Robbed-bit Signaling Source Control Bit 1	Transmit Robbed-bit Signaling Source Control Bit 0
R/W	R/W	R/W	R/W		R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Signaling Bit A	R/W	**Signaling Bit A:** This bit is used to store Signaling Bit A that is sent as the least significant bit of timeslot of frame number 6.
6	Signaling Bit B	R/W	**Signaling Bit B:** This bit is used to store Signaling Bit B that is sent as the least significant bit of timeslot of frame number 12.
5	Signaling Bit C	R/W	**Signaling Bit C:** This bit is used to store Signaling Bit C that is sent as the least significant bit of timeslot of frame number 18.
4	Signaling Bit D	R/W	**Signaling Bit D:** This bit is used to store Signaling Bit D that is sent as the least significant bit of timeslot of frame number 24.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Robbed-bit Signaling Enable	R/W	**Robbed-bit Signaling Enable:** When these bits are set to 0: Robbed-bit Signaling is disabled. No signaling data will be inserted into the input PCM data no matter what the setting of the Transmit Signaling Source Select [1:0] bits is. When these bits are set to 1: Signaling data is enabled and inserted into the input DS1 PCM data according to setting of the Transmit Signaling Source Select [1:0] bits.
1-0	Transmit Signaling Source Select	R/W	**Transmit Signaling Source Select:** When these bits are set to 00: None of the signaling data, the CAS Multi-frame alignment pattern, the X bit or the CAS Multi-frame Yellow Alarm bit Y is inserted into the outgoing E1 PCM data by the framer. However, the user can embed the signaling data, the CAS Multi-frame alignment pattern, the X bit or the CAS Multi-frame Yellow Alarm bit Y into E1 PCM data before routing the PCM data into the framer. When these bits are set to 01: The signaling data, the CAS Multi-frame alignment pattern, the X bit or the CAS Multi-frame Yellow Alarm bit Y is inserted into the outgoing E1 PCM data from TSCR register of each timeslot. When these bits are set to 10: If the XRT84L38 framer is operating in E1 2.048Mbit/s mode and if the TxFR2048 bit of the Transmit Interface Control Register (TICR) is set to zero: The signaling data, the CAS Multi-frame alignment pattern, the X bit or the CAS Multi-frame Yellow Alarm bit Y is inserted into the outgoing E1 PCM data from the TxOH_n input pin. If the XRT84L38 framer is operating in E1 2.048Mbit/s mode and if the TxFR2048 bit of the Transmit Interface Control Register (TICR) is set to one: The signaling data, the CAS Multi-frame alignment pattern, the X bit or the CAS Multi-frame Yellow Alarm bit Y is inserted into the outgoing E1 PCM data from the TxSig_n input pin. When these bits are set to 11: No signaling data or the CAS Multi-frame alignment pattern is inserted into the input E1 PCM data by the framer. However, the user can embed signaling data into E1 PCM data before routing the PCM data into the framer. The X bit is inserted into the outgoing E1 PCM data from TSCR register. The CAS Multi-frame Yellow Alarm Y bit is generated by the XRT84L38 framer depends on operating condition of the E1 link.

Receive Channel Control Register (RCCR) (Indirect Address = 0xn2H, 0x60H - 0x7FH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Receive LAPD Channel Select Bit 1	Receive LAPD Channel Select Bit 0	Receive Zero Code Suppression Select Bit [1:0] (T1 Mode Only)		Receive Conditioning Select Bit [3:0]			
		R/W	R/W	R/W	R/W	R/W	R/W
1	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-6	Receive LAPD Channel Select [1:0]		**Receive LAPD Channel Select Bit [1:0]:** When these bits are set to 00: The first LAPD channel is used as data destination for D or E time slot. When these bits are set to 01: The second LAPD channel is used as data destination for D or E time slot. When these bits are set to 10: In T1 mode, the Transmit D/E Timeslot Source Select bits (TxDE[1:0]) of the Transmit Data Link Select Register (TSDLSR) will determine the data destination for D/E time slot. In E1 mode, the Transmit Signaling and Data Link Source Select bits (TxSIGDL[2:0]) of the Transmit Data Link Select Register (TSDLSR) will determine the data destination for D/E time slot. When these bits are set to 11: The third LAPD channel is used as data destination for D or E time slot.
6	Reserved		
5-4	Receive Zero Code Suppression Select {T1 Mode Only}	R/W	**Receive Zero Code Suppression Select:** When these bits are set to 00: The received DS1 PAYLOAD data of this DS0 channel is unchanged. No zero code suppression is used. When these bits are set to 01: AT&T Bit 7 stuffing is used. When these bits are set to 10: GTE zero code suppression is used. When these bits are set to 11: DDS zero code suppression is used.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-0	Receive Conditioning Select	R/W	**Receive Conditioning Select:** When these bits are set to 0000: The received DS1 payload data of this DS0 channel is unchanged. When these bits are set to 0001: All 8 bits of the input DS1 payload data of this DS0 channel are inverted. When these bits are set to 0010: The even bits of the input DS1 payload data of this DS0 channel are inverted. When these bits are set to 0011: The odd bits of the input DS1 payload data of this DS0 channel are inverted. When these bits are set to 0100: The input DS1 payload data of this DS0 channel are replaced by the octet stored in User IDLE Code Register (UCR). When these bits are set to 0101: The input DS1 payload data of this DS0 channel are replaced by BUSY code (0x7F). When these bits are set to 0110: The input DS1 payload data of this DS0 channel are replaced by VACANT code (0xFF). When these bits are set to 0111: The input DS1 payload data of this DS0 channel are replaced by BUSY_TS code (111xxxxx). When these bits are set to 1000: The input DS1 payload data of this DS0 channel are replaced by MUX-Out-Of-Frame (MOOF) code with value 0x1A. When these bits are set to 1001: The input DS1 payload data of this DS0 channel are replaced by the A-law digital milliwatt pattern. When these bits are set to 1010: The input DS1 payload data of this DS0 channel are replaced by the u-law digital milliwatt pattern. When these bits are set to 1011: The MSB bit of the input DS1 payload data of this DS0 channel is inverted. When these bits are set to 1100: All bits of the input DS1 payload data of this DS0 channel except MSB bit are inverted. When these bits are set to 1101: The input DS1 payload data of this DS0 channel are replaced by PRBS pattern created by the internal PRBS Generator of XRT84L38 framer. When these bits are set to 1110: The input DS1 payload data of this DS0 channel is unchanged. When these bits are set to 1111: This channel is configured as D or E timeslot.

Receive User IDLE Code Register (UCR) (Indirect Address = 0xn02H, 0x80H - 0x97H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Receive User IDLE Code Bit [7:0]							
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	Receive User IDLE Code	R/W	**Receive User IDLE Code:** These READ/WRITE bit-fields permits the user store any value of IDLE code into the framer. When the Receive Data Conditioning Select [3:0] bits of RCCR register of a particular DS0 channel are set to 0100, the received DS1 payload data are replaced by contents of this register and sent to the Terminal Equipment.

Receive Signaling Control Register (RSCR) (Indirect Address = 0xn2H, 0xA0H - 0xB7H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Reserved	Receive Signaling Substitution Enable	Receive Signaling Output Enable	De-bounce Enable	Receive Signaling Substitution Control Bit 1	Receive Signaling Substitution Control Bit 0	Signaling Extraction Control Bit 1	Signaling Extraction Control Bit 0
	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Reserved		
6	Receive Signaling Substitution Enable	R/W	**Receive Signaling Substitution Enable:** When this bit is set to 0: Signaling Substitution is disabled. The XRT84L38 framer will not replace extracted signaling bits from the incoming DS1 payload data with all ones or with signaling bits stored in RSSR registers. When this bit is set to 1: Signaling Substitution is enabled. The XRT84L38 framer will replace extracted signaling bits from the incoming DS1 payload data with all ones or with signaling bits stored in RSSR registers.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Signaling Output Enable	R/W	**Receive Signaling Output Enable:** When these bits are set to 0: The XRT84L38 framer will not send extracted signaling bits from the incoming DS1 payload data to external equipment through the Receive Signaling Output pin (RxSig_n). When these bits are set to 1: The XRT84L38 framer will send extracted signaling bits from the incoming DS1 payload data to external equipment through the Receive Signaling Output pin (RxSig_n).
4			
3-2	Receive Signaling Substitution Control	R/W	**Receive Signaling Substitution Control:** When these bits are set to 00: The received signaling bits are replaced by all ones and send to the external equipment. When these bits are set to 01: Two-code signaling substitution is applied to the received signaling bits. The replaced signaling information is sent to the external equipment. When these bits are set to 10: Four-code signaling substitution is applied to the received signaling bits. The replaced signaling information is sent to the external equipment. When these bits are set to 11: Sixteen-code signaling substitution is applied to the received signaling bits. The replaced signaling information is sent to the external equipment. ***NOTE:*** *In SF mode, this option is disabled.*
1-0	Signaling Extraction Control	R/W	**Signaling Extraction Control:** When these bits are set to 00: The XRT84L38 framer does not extract signaling information from incoming DS1 payload data. When these bits are set to 01: The XRT84L38 framer extracts sixteen-code signaling information from incoming DS1 payload data. When these bits are set to 10: The XRT84L38 framer extracts four-code signaling information from incoming DS1 payload data. When these bits are set to 11: The XRT84L38 framer extracts two-code signaling information from incoming DS1 payload data.

Receive Substitution Signaling Register (RSSR) (Indirect Address = 0xn02H, 0xC0H - 0xD7H)

7-4	Reserved	R/W	
3	SIG16-A SIG4-A SIG2-A		Sixteen-Code Signaling bit A Four-Code Signaling bit A Two-Code Signaling bit A
2	SIG16-B SIG4-B SIG2-A		Sixteen-Code Signaling bit B Four-Code Signaling bit B Two-Code Signaling bit A
1	SIG16-C SIG4-A SIG2-A		Sixteen-Code Signaling bit C Four-Code Signaling bit A Two-Code Signaling bit A
0	SIG16-D SIG4-B SIG2-A		Sixteen-Code Signaling bit D Four-Code Signaling bit B Two-Code Signaling bit A

Receive Signaling Register Array (RSRA)(Indirect Address = 0xn4H, 0x00H - 0x17H)

3	Signaling Bit A	R/W	**Signaling Bit A:** This bit is used to store Signaling Bit A that is received and extracted as the least significant bit of timeslot of frame number 6.
2	Signaling Bit B	R/W	**Signaling Bit B:** This bit is used to store Signaling Bit B that is received and extracted as the least significant bit of timeslot of frame number 12.
1	Signaling Bit C	R/W	**Signaling Bit C:** This bit is used to store Signaling Bit C that is received and extracted as the least significant bit of timeslot of frame number 18.
0	Signaling Bit D	R/W	**Signaling Bit D:** This bit is used to store Signaling Bit D that is received and extracted as the least significant bit of timeslot of frame number 24.

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
PRBS Type Select	Error Insertion	Data Inversion Select	Receive PRBS Lock Indication	Receive PRBS Block Enable	Transmit PRBS Block Enable	Receive DS1/ E1 Framer Bypassed	Transmit DS1/ E1 Framer Bypassed
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

Block Interrupt Enable Register (BIER) (Indirect Address = 0xnAH, 0x00H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
SA6 Interrupt	Loop-back Code Interrupt	Receive Clock Loss Interrupt	One Second Interrupt	HDLC Controller Interrupt	Slip Buffer Interrupt	Alarm and Error Interrupt	T1/E1 Framer Interrupt
R	R	R	R	R	R	R	R
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	SA6 Interrupt	R	**SA6 Interrupt:** When this bit is set to 0: No SA6 interrupt is generated. When this bit is set to 1: An SA6 Interrupt is generated.
6	Loop-back Code Interrupt	R	**Loop-back Code Interrupt:** When this bit is set to 0: No Loop-back Code interrupt is generated. When this bit is set to 1: A Loop-back Code Interrupt is generated.
5	Receive Clock Loss Interrupt	R	**Receive Clock Loss Interrupt:** When this bit is set to 0: No Receive Clock Loss interrupt is generated. When this bit is set to 1: A Receive Clock Loss Interrupt is generated.
4	One Second Interrupt	R	**One Second Interrupt:** When this bit is set to 0: No One Second interrupt is generated. When this bit is set to 1: A One Second Interrupt is generated.
3	HDLC Controller Interrupt	R	**HDLC Controller Interrupt:** When this bit is set to 0: No HDLC Controller interrupt is generated. When this bit is set to 1: A HDLC Controller Interrupt is generated.
2	Slip Buffer Interrupt	R	**Slip Buffer Interrupt:** When this bit is set to 0: No T1/E1 Framer interrupt is generated. When this bit is set to 1: A Slip Buffer Interrupt is generated.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt	R	**Alarm and Error Interrupt:** When this bit is set to 0: No Alarm and Error interrupt is generated. When this bit is set to 1: An Alarm and Error Interrupt is generated.
0	T1/E1 Framer Interrupt	R	**T1/E1 Framer Interrupt:** When this bit is set to 0: No T1/E1 Framer interrupt is generated. When this bit is set to 1: A T1/E1 Framer Interrupt is generated.

Block Interrupt Enable Register (BIER) (Indirect Address = 0xnAH, 0x01H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
SA6 Interrupt Enable	Loop-back Code Interrupt Enable	Receive Clock Loss Interrupt Enable	One Second Interrupt Enable	HDLC Controller Interrupt Enable	Slip Buffer Interrupt Enable	Alarm and Error Interrupt Enable	T1/E1 Framer Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	SA6 Interrupt Enable	R	**SA6 Interrupt Enable:** When this bit is set to 0: Every interrupt generated by the Receive SA6 Interrupt Register (RSAIR) is disabled. When this bit is set to 1: Every interrupt generated by the Receive SA6 Interrupt Register (RSAIR) enabled.
6	Loop-back Code Interrupt Enable	R	**Loop-back Code Interrupt Enable:** When this bit is set to 0: Every interrupt generated by the Receive Loop-back Code Interrupt and Status Register (RLCISR) is disabled. When this bit is set to 1: Every interrupt generated by the Receive Loop-back Code Interrupt and Status Register (RLCISR) enabled.
5	Receive Clock Loss Interrupt Enable	R	**Receive Clock Loss Interrupt Enable:** When this bit is set to 0: The Receive Clock Loss Interrupt is disabled. When this bit is set to 1:T he Receive Clock Loss Interrupt is enabled.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	One Second Interrupt Enable	R	**One Second Interrupt Enable:** When this bit is set to 0: One Second Interrupt is disabled. When this bit is set to 1: One Second Interrupt is enabled.
3	HDLC Controller Interrupt Enable	R	**HDLC Controller Interrupt Enable:** When this bit is set to 0: Every interrupt generated by the Data Link Status Register (DLSR) is disabled. When this bit is set to 1: Every interrupt generated by the Data Link Status Register (DLSR) is enabled.
2	Slip Buffer Interrupt Enable	R	**Slip Buffer Interrupt Enable:** When this bit is set to 0: Every interrupt generated by the Slip Buffer Status Register (SBSR) is disabled. When this bit is set to 1: Every interrupt generated by the Slip Buffer Status Register (SBSR) is enabled.
1	Alarm and Error Interrupt Enable	R	**Alarm and Error Interrupt Enable:** When this bit is set to 0: Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. When this bit is set to 1: Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.
0	T1/E1 Framer Interrupt Enable	R	**T1/E1 Framer Interrupt Enable:** When this bit is set to 0: Every interrupt generated by the T1/E1 Framer Interrupt Status Register (FISR) is disabled. When this bit is set to 1: Every interrupt generated by the T1/E1 Framer Interrupt Status Register (FISR) is enabled.

Alarm and Error Status Register (AESR) - T1 Mode (Indirect Address = 0xnAH, 0x02H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Receive Red Alarm State	Receive AIS State	Receive Yellow Alarm State	Receive Loss of Signal Change	Receive Bipolar Violation State Change	Receive Red Alarm State Change	Receive AIS State Change	Receive Yellow Alarm State Change
R	R	R	RUR / WC	RUR / WC	RUR / WC	RUR / WC	RUR / WC
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Red Alarm State	R	**Receive Red Alarm State:** When this bit is 0: There is no Red Alarm condition detected in the incoming DS1 payload data. When this bit is 1: There is Red Alarm condition detected in the incoming DS1 payload data.
6	Receive AIS State	R	**Receive AIS State:** When this bit is 0: There is no AIS alarm condition detected in the incoming DS1 payload data. When this bit is 1: There is AIS alarm condition detected in the incoming DS1 payload data.
5	Receive Yellow Alarm State	R	**Receive Yellow Alarm State:** When this bit is 0: There is no Yellow Alarm condition detected in the incoming DS1 payload data. When this bit is 1: There is Yellow Alarm condition detected in the incoming DS1 payload data.
4	Receive Loss of Signal Change	RUR / WC	**Receive Loss of Signal:** When this bit is 0: There is no change of Loss of Signal state in the incoming DS1 payload data. When this bit is 1: There is change of Loss of Signal state in the incoming DS1 payload data.
3	Receive Bipolar Violation State Change	RUR / WC	**Receive Bipolar Violation:** When this bit is 0: There is no change of Bipolar Violation state in the incoming DS1 payload data. When this bit is 1: There is change of Bipolar Violation state in the incoming DS1 payload data.
2	Receive Red Alarm State Change	RUR / WC	**Receive Red Alarm State Change:** When this bit is 0: There is no change of Red Alarm state in the incoming DS1 payload data. When this bit is 1: There is change of Red Alarm state in the incoming DS1 payload data.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive AIS State Change	RUR / WC	**Receive AIS State Change:** When this bit is 0: There is no change of AIS state in the incoming DS1 payload data. When this bit is 1: There is change of AIS state in the incoming DS1 payload data.
0	Receive Yellow Alarm State Change	RUR / WC	**Receive Yellow Alarm State Change:** When this bit is 0: There is no change of Yellow Alarm state in the incoming DS1 payload data. When this bit is 1: There is change of Yellow Alarm state in the incoming DS1 payload data.

Alarm and Error Status Register (AESR) - E1 Mode (Indirect Address = 0xnAH, 0x02H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Receive Red Alarm State	Receive AIS State	Receive CAS Multi-frame Yellow Alarm State Change	Receive Loss of Signal Change	Receive Bipolar Violation State Change	Receive Red Alarm State Change	Receive AIS State Change	Receive Yellow Alarm State Change
R	R	RUR / WC	RUR / WC	RUR / WC	RUR / WC	RUR / WC	RUR / WC
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Red Alarm State	R	**Receive Red Alarm State:** When this bit is 0: There is no Red Alarm condition detected in the incoming DS1 payload data. When this bit is 1: There is Red Alarm condition detected in the incoming DS1 payload data.
6	Receive AIS State	R	**Receive AIS State:** When this bit is 0: There is no AIS alarm condition detected in the incoming DS1 payload data. When this bit is 1: There is AIS alarm condition detected in the incoming DS1 payload data.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive CAS Multi-frame Yellow Alarm State Change	RUR / WC	**Receive CAS Multi-frame Yellow Alarm State Change:** When this bit is 0: There is no change of CAS Multi-frame Yellow Alarm state in the incoming E1 payload data. When this bit is 1: There is change of CAS Multi-frame Yellow Alarm state in the incoming E1 payload data.
4	Receive Loss of Signal Change	RUR / WC	**Receive Loss of Signal:** When this bit is 0: There is no change of Loss of Signal state in the incoming DS1 payload data. When this bit is 1: There is change of Loss of Signal state in the incoming DS1 payload data.
3	Receive Bipolar Violation State Change	RUR / WC	**Receive Bipolar Violation:** When this bit is 0: There is no change of Bipolar Violation state in the incoming DS1 payload data. When this bit is 1: There is change of Bipolar Violation state in the incoming DS1 payload data.
2	Receive Red Alarm State Change	RUR / WC	**Receive Red Alarm State Change:** When this bit is 0: There is no change of Red Alarm state in the incoming DS1 payload data. When this bit is 1: There is change of Red Alarm state in the incoming DS1 payload data.
1	Receive AIS State Change	RUR / WC	**Receive AIS State Change:** When this bit is 0: There is no change of AIS state in the incoming DS1 payload data. When this bit is 1: There is change of AIS state in the incoming DS1 payload data.
0	Receive Yellow Alarm State Change	RUR / WC	**Receive Yellow Alarm State Change:** When this bit is 0: There is no change of Yellow Alarm state in the incoming DS1 payload data. When this bit is 1: There is change of Yellow Alarm state in the incoming DS1 payload data.

Alarm and Error Interrupt Enable Register (AEIER) - T1 Mode (Indirect Address = 0xnAH, 0x03H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Reserved			Receive Loss of Signal Change Interrupt Enable	Receive Bipolar Violation State Change Interrupt Enable	Receive Red Alarm State Change Interrupt Enable	Receive AIS State Change Interrupt Enable	Receive Yellow Alarm State Change Interrupt Enable
			R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-5	Reserved		
4	Receive Loss of Signal Interrupt Enable	R/W	**Receive Loss of Signal Interrupt Enable:** When this bit is set to 0: The Receive Loss of Signal interrupt is disabled. Occurrence of Loss of Signals will not generate an interrupt. When this bit is set to 1: The Receive Loss of Signal interrupt is enabled. Occurrence of Loss of Signals will generate an interrupt.
3	Receive Bipolar Violation Interrupt Enable	R/W	**Receive Bipolar Violation Interrupt Enable:** When this bit is set to 0: The Receive Bipolar Violation interrupt is disabled. Occurrence of one or more bipolar violations will not generate an interrupt. When this bit is set to 1: The Receive Bipolar Violation interrupt is enabled. Occurrence of one or more bipolar violations will generate an interrupt.
2	Receive Red Alarm State Change Interrupt Enable	R/W	**Receive Red Alarm State Change Interrupt Enable:** When this bit is set to 0: The Receive Red Alarm State Change interrupt is disabled. No Receive Loss of Frame (RxLOF) interrupt will be generated upon detection of LOF condition. When this bit is set to 1: The Receive Red Alarm State Change interrupt is enabled. Receive Loss of Frame (RxLOF) interrupt will be generated upon detection of LOF condition.
1	Receive AIS State Change Interrupt Enable	R/W	**Receive AIS State Change Interrupt Enable:** When this bit is set to 0: The Receive AIS State Change interrupt is disabled. When this bit is set to 1: The Receive AIS State Change interrupt is enabled.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	Receive Yellow Alarm State Change Interrupt Enable	R/W	**Receive Yellow Alarm State Change Interrupt Enable:** When this bit is set to 0: The Receive Yellow Alarm State Change interrupt is disabled. Any state change of Receive Yellow Alarm will not generate an interrupt. When this bit is set to 1: The Receive Yellow Alarm State Change interrupt is enabled. Any state change of Receive Yellow Alarm will generate an interrupt.

Alarm and Error Interrupt Enable Register (AEIER) - E1 Mode (Indirect Address = 0xnAH, 0x03H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Reserved		Receive CAS Multi-frame Yellow Alarm State Change Interrupt Enable	Receive Loss of Signal Change Interrupt Enable	Receive Bipolar Violation State Change Interrupt Enable	Receive Red Alarm State Change Interrupt Enable	Receive AIS State Change Interrupt Enable	Receive Yellow Alarm State Change Interrupt Enable
		R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-6	Reserved		
5	Receive CAS Multi-frame Yellow Alarm State Change Interrupt Enable	R/W	**Receive CAS Multi-frame Yellow Alarm State Change Interrupt Enable:** When this bit is set to 0: The Receive CAS Multi-frame Yellow Alarm State Change interrupt is disabled. Any state change of Receive CAS Multi-frame Yellow Alarm will not generate an interrupt. When this bit is set to 1: The Receive CAS Multi-frame Yellow Alarm State Change interrupt is enabled. Any state change of Receive CAS Multi-frame Yellow Alarm will generate an interrupt.
4	Receive Loss of Signal Interrupt Enable	R/W	**Receive Loss of Signal Interrupt Enable:** When this bit is set to 0: The Receive Loss of Signal interrupt is disabled. Occurrence of Loss of Signals will not generate an interrupt. When this bit is set to 1: The Receive Loss of Signal interrupt is enabled. Occurrence of Loss of Signals will generate an interrupt.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Bipolar Violation Interrupt Enable	R/W	**Receive Bipolar Violation Interrupt Enable:** When this bit is set to 0: The Receive Bipolar Violation interrupt is disabled. Occurrence of one or more bipolar violations will not generate an interrupt. When this bit is set to 1: The Receive Bipolar Violation interrupt is enabled. Occurrence of one or more bipolar violations will generate an interrupt.
2	Receive Red Alarm State Change Interrupt Enable	R/W	**Receive Red Alarm State Change Interrupt Enable:** When this bit is set to 0: The Receive Red Alarm State Change interrupt is disabled. No Receive Loss of Frame (RxLOF) interrupt will be generated upon detection of LOF condition. When this bit is set to 1: The Receive Red Alarm State Change interrupt is enabled. Receive Loss of Frame (RxLOF) interrupt will be generated upon detection of LOF condition.
1	Receive AIS State Change Interrupt Enable	R/W	**Receive AIS State Change Interrupt Enable:** When this bit is set to 0: The Receive AIS State Change interrupt is disabled. When this bit is set to 1: The Receive AIS State Change interrupt is enabled.
0	Receive Yellow Alarm State Change Interrupt Enable	R/W	**Receive Yellow Alarm State Change Interrupt Enable:** When this bit is set to 0: The Receive Yellow Alarm State Change interrupt is disabled. Any state change of Receive Yellow Alarm will not generate an interrupt. When this bit is set to 1: The Receive Yellow Alarm State Change interrupt is enabled. Any state change of Receive Yellow Alarm will generate an interrupt.

Framer Interrupt Status Register (FISR) (Indirect Address = 0xnAH, 0x04H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
CAS Multi-frame Alignment Changed (E1 Only)	National Bit Updated (E1 Only)	Signaling Updated	Frame Alignment Changed	Framer In-frame State	Frame Mimic State Changed	Synchroniza-tion Bit Error	Framing Error
RUR / WC	RUR / WC	RUR / WC	RUR / WC	RUR / WC	RUR / WC	RUR / WC	RUR / WC
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	CAS Multi-frame Alignment Changed (E1 Only)	RUR / WC	**CAS Multi-frame Alignment Changed:** When this bit is 0: There is no change of CAS Multi-frame Alignment in the incoming E1 payload data. When this bit is 1: There is change of CAS Multi-frame Alignment in the incoming E1 payload data.
6	National Bit Updated (E1 Only)	RUR / WC	**National Bit Updated:** When this bit is 0: There is no change of National Bits in the incoming E1 payload data. When this bit is 1: There is change of National Bits in the incoming E1 payload data.
5	Signaling Updated	RUR / WC	**Signaling Updated:** When this bit is 0: There is no change of signaling information in the incoming DS1/E1 payload data. When this bit is 1: There is change of signaling information in the incoming DS1/E1 payload data.
4	Frame Alignment Changed	RUR / WC	**Frame Alignment Changed:** When this bit is 0: There is no change of Frame Alignment in the incoming DS1/E1 payload data. When this bit is 1: There is change of Frame Alignment in the incoming DS1/E1 payload data.
3	Framer In-frame State	RUR / WC	**Framer In-frame State:** When this bit is 0: There is no change occur in the in-frame state in the incoming DS1/E1 payload data. That is, if the framer is in-frame before, then it is remained in-frame. When this bit is 1: There is change of in-frame state in the incoming DS1/E1 payload data. That is, if the framer is in-frame before, then it is out-of-frame now.
2	Frame Mimic State Changed	RUR / WC	**Frame Mimic State Changed:** When this bit is 0: There is no change Frame Mimic state in the incoming DS1/E1 payload data. When this bit is 1: There is change of Frame Mimic state in the incoming DS1/E1 payload data.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Synchronization Bit Error	RUR / WC	**Synchronization Bit Error:** When this bit is 0: There is no Synchronization Bit Error in the incoming DS1/E1 payload data. When this bit is 1: There is Synchronization Bit Error in the incoming DS1/E1 payload data.
0	Framing Error	RUR / WC	**Framing Error:** When this bit is 0: There is no Framing Error in the incoming DS1/E1 payload data. When this bit is 1: There is Framing Error in the incoming DS1/E1 payload data.

Framer Interrupt Enable Register (FIER) (Indirect Address = 0xnAH, 0x05H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
CAS Multi-frame Alignment Change Interrupt Enable (E1 Only)	National Bit Update Interrupt Enable (E1 Only)	Signaling Update Interrupt Enable	Frame Alignment Change Interrupt Enable	Framer In-frame State Interrupt Enable	Frame Mimic State Change Interrupt Enable	Synchronization Bit Error Interrupt Enable	Framing Error Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	CAS Multi-frame Alignment Change Interrupt Enable (E1 Only)	RUR / WC	**CAS Multi-frame Alignment Changed Interrupt Enable:** When this bit is set to 0: The CAS Multi-frame Alignment Change interrupt is disabled. When this bit is set to 1: The CAS Multi-frame Alignment Changed interrupt is enabled.
6	National Bit Update Interrupt Enable (E1 Only)	RUR / WC	**National Bit Updated Interrupt Enable:** When this bit is set to 0: The National Bit Update interrupt is disabled. When this bit is set to 1: The National Bit Update interrupt is enabled.
5	Signaling Update Interrupt Enable	RUR / WC	**Signaling Updated Interrupt Enable:** When this bit is set to 0: The Signaling Update interrupt is disabled. When this bit is set to 1: The Signaling Update interrupt is enabled.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Frame Alignment Change Interrupt Enable	RUR / WC	**Frame Alignment Changed Interrupt Enable:** When this bit is set to 0: The Frame Alignment Change interrupt is disabled. When this bit is set to 1: The Frame Alignment Change interrupt is enabled.
3	Framer In-frame State Interrupt Enable	RUR / WC	Framer In-frame State Interrupt Enable:When this bit is set to 0:The Framer In-frame State interrupt is disabled. When this bit is set to 1:The Framer In-frame State interrupt is enabled.
2	Frame Mimic State Change Interrupt Enable	RUR / WC	**Frame Mimic State Changed Interrupt Enable:** When this bit is set to 0: he Frame Mimic State Change interrupt is disabled. When this bit is set to 1: The Frame Mimic State Change interrupt is enabled.
1	Synchronization Bit Error Interrupt Enable	RUR / WC	**Synchronization Bit Error Interrupt Enable:** When this bit is set to 0: The Synchronization Bit Error interrupt is disabled. When this bit is set to 1: The Synchronization Bit Error interrupt is enabled.
0	Framing Error Interrupt Enable	RUR / WC	**Framing Error Interrupt Enable:** When this bit is set to 0: The Framing Error interrupt is disabled. When this bit is set to 1: The Framing Error interrupt is enabled.

Data Link Status Register (DLSR) (Indirect Address = 0xnAH, 0x06H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Message Type	Transmit Start of Transfer	Receive Start of Transfer	Transmit End of Transfer	Receive End of Transfer	Frame Check Sequence Error Detection	Receive ABORT Sequence	Receive IDLE Flag Sequence
RUR / WC	RUR / WC	RUR / WC	RUR / WC	RUR / WC	RUR / WC	RUR / WC	RUR / WC
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Message Type	RUR / WC	**Message Type:** When this bit is set to 0: The Receive HDLC Controller receives and processes Bit-Oriented Signaling (BOS) message. When this bit is set to 1: The Receive HDLC Controller receives and processes LAPD protocol or Message-Oriented Signaling (MOS) message.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Transmit Start of Transfer	RUR / WC	**Transmit Start of Transfer:** When this bit is 0: There is no data link message to be sent to the data link channel. When this bit is 1: The HDLC Controller will send a data link message to the data link channel.
5	Receive Start of Transfer	RUR / WC	**Receive Start of Transfer:** When this bit is 0: There is no data link message in the data link channel. When this bit is 1: The HDLC Controller began to receive a data link message in the data link channel.
4	Transmit End of Transfer	RUR / WC	**Transmit End of Transfer:** When this bit is 0: No data link message was sent to the data link channel. When this bit is 1: The HDLC Controller finished sending a data link message to the data link channel.
3	Receive End of Transfer	RUR / WC	**Receive End of Transfer:** When this bit is 0: No data link message was present in the data link channel. When this bit is 1: The HDLC Controller finished receiving a data link message in the data link channel.
2	Frame Check Sequence Error Detection	RUR / WC	**Frame Check Sequence Error Detection:** When this bit is 0: There is no FCS error detected in the data link channel. When this bit is 1: The HDLC Controller receives an erroneous FCS in the data link channel.
1	Receive ABORT Sequence	RUR / WC	**Receive ABORT Sequence:** When this bit is 0: There is no BOS ABORT sequence received in the data link channel. When this bit is 1: The HDLC Controller receives MOS ABORT sequence in the data link channel.
0	Receive IDLE Flag Sequence	RUR / WC	**Receive IDLE Flag Sequence:** When this bit is 0: The message received in the data link channel is BOS message. When this bit is 1: The message received in the data link channel is MOS message.

Data Link Interrupt Enable Register (DLIER) (Indirect Address = 0xnAH, 0x07H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Reserve	Transmit Start of Transfer Interrupt Enable	Receive Start of Transfer Interrupt Enable	Transmit End of Transfer Interrupt Enable	Receive End of Transfer Interrupt Enable	Frame Check Sequence Error Detection Interrupt Enable	Receive ABORT Sequence Interrupt Enable	Receive IDLE Flag Sequence Interrupt Enable
	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Reserved		
6	Transmit Start of Transfer Interrupt Enable	R/W	**Transmit Start of Transfer Interrupt Enable:** When this bit is set to 0: The Transmit Start of Transfer interrupt is disabled. When this bit is set to 1: The Transmit Start of Transfer interrupt is enabled.
5	Receive Start of Transfer Interrupt Enable	R/W	**Receive Start of Transfer Interrupt Enable:** When this bit is set to 0: The Receive Start of Transfer interrupt is disabled. When this bit is set to 1: The Receive Start of Transfer interrupt is enabled.
4	Transmit End of Transfer Interrupt Enable	R/W	**Transmit End of Transfer Interrupt Enable:** When this bit is set to 0: The Transmit End of Transfer interrupt is disabled. When this bit is set to 1: The Transmit End of Transfer interrupt is enabled.
3	Receive End of Transfer Interrupt Enable	R/W	**Receive End of Transfer Interrupt Enable:** When this bit is set to 0: The Receive End of Transfer interrupt is disabled. When this bit is set to 1: The Receive End of Transfer interrupt is enabled.
2	Frame Check Sequence Error Detection Interrupt Enable	R/W	**Frame Check Sequence Error Detection Interrupt Enable:** When this bit is set to 0: The Frame Check Sequence Error Detection interrupt is disabled. When this bit is set to 1: The Frame Check Sequence Error Detection interrupt is enabled.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive ABORT Sequence Interrupt Enable	R/W	**Receive ABORT Sequence Interrupt Enable:** When this bit is set to 0: The Receive ABORT Sequence interrupt is disabled. When this bit is set to 1: The Receive ABORT Sequence interrupt is enabled.
0	Receive IDLE Flag Sequence Interrupt Enable	R/W	**Receive IDLE Flag Sequence Interrupt Enable:** When this bit is set to 0: The Receive IDLE Flag Sequence interrupt is disabled. When this bit is set to 1: The Receive IDLE Flag Sequence interrupt is enabled.

Slip Buffer Status Register (SBSR) (Indirect Address = 0xnAH, 0x08H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Transmit Slip Buffer Full	Transmit Slip Buffer Empty	Transmit Slip Buffer Slip	SLC96 In Synchroniza-tion	Multi-frame In Synchroniza-tion	Receive Slip Buffer Full	Receive Slip Buffer Empty	Receive Slip Buffer Slip
RUR/WC	RUR/WC	RUR/WC	R	R	RUR/WC	RUR/WC	RUR/WC
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Transmit Slip Buffer Full	RUR/ WC	**Transmit Slip Buffer Full:** When this bit is set to 0: The Transmit Slip Buffer is not full. When this bit is set to 1: The Transmit Slip Buffer is full and one frame of data is dis-carded.
6	Transmit Slip Buffer Empty	RUR/ WC	**Transmit Slip Buffer Empty:** When this bit is set to 0: The Transmit Slip Buffer is not empty. When this bit is set to 1: The Transmit Slip Buffer is empty and one frame of data is repeated.
5	Transmit Slip Buffer Slip	RUR/ WC	**Transmit Slip Buffer Slip:** When this bit is set to 0: The Transmit Slip Buffer does not slip. When this bit is set to 1: The Transmit Slip Buffer slips since either full or emptied.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	SLC96 In Synchronization	R	**SLC96 In Synchronization:** When this bit is set to 0: The framer is not in SLC96 Synchronization. When this bit is set to 1: The framer is in SLC96 Synchronization.
3	Multi-frame In Synchronization	R	**Multi-frame In Synchronization:** When this bit is set to 0: The framer is not in Multi-frame synchronization. When this bit is set to 1: The framer is in Multi-frame synchronization.
2	Receive Slip Buffer Full	RUR/ WC	**Receive Slip Buffer Full:** When this bit is set to 0: The Receive Slip Buffer is not full. When this bit is set to 1: The Receive Slip Buffer is full and one frame of data is discarded.
1	Receive Slip Buffer Empty	RUR/ WC	**Receive Slip Buffer Empty:** When this bit is set to 0: The Receive Slip Buffer is not empty. When this bit is set to 1: The Receive Slip Buffer is empty and one frame of data is repeated.
0	Receive Slip Buffer Slip	RUR/ WC	**Receive Slip Buffer Slip:** When this bit is set to 0: The Receive Slip Buffer does not slip. When this bit is set to 1: The Receive Slip Buffer slips since either full or emptied.

Slip Buffer Interrupt Enable Register (SBIER) (Indirect Address = 0xnAH, 0x09H)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Transmit Slip Buffer Full Interrupt Enable	Transmit Slip Buffer Empty Interrupt Enable	Transmit Slip Buffer Slip Interrupt Enable	Reserved	Reserved	Receive Slip Buffer Full Interrupt Enable	Receive Slip Buffer Empty Interrupt Enable	Receive Slip Buffer Slip Interrupt Enable
R/W	R/W	R/W			R/W	R/W	R/W
0	0	0			0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Transmit Slip Buffer Full Interrupt Enable	R/W	**Transmit Slip Buffer Full Interrupt Enable:** When this bit is set to 0: The Transmit Slip Buffer Full interrupt is disabled. When this bit is set to 1: The Transmit Slip Buffer Full interrupt is enabled.
6	Transmit Slip Buffer Empty Interrupt Enable	R/W	**Transmit Slip Buffer Empty Interrupt Enable:** When this bit is set to 0: The Transmit Slip Buffer Empty interrupt is disabled. When this bit is set to 1: The Transmit Slip Buffer Empty interrupt is enabled.
5	Transmit Slip Buffer Slip Interrupt Enable	R/W	**Transmit Slip Buffer Slip Interrupt Enable:** When this bit is set to 0: The Transmit Slip Buffer Slip interrupt is disabled. When this bit is set to 1: The Transmit Slip Buffer slips Slip interrupt is enabled.
4-3	Reserved		
2	Receive Slip Buffer Full Interrupt Enable	R/W	**Receive Slip Buffer Full Interrupt Enable:** When this bit is set to 0: The Receive Slip Buffer Full interrupt is disabled. When this bit is set to 1: The Receive Slip Buffer Full interrupt is enabled.
1	Receive Slip Buffer Empty Interrupt Enable	R/W	**Receive Slip Buffer Empty Interrupt Enable:** When this bit is set to 0: The Receive Slip Buffer Empty interrupt is disabled. When this bit is set to 1: The Receive Slip Buffer Empty interrupt is enabled.
0	Receive Slip Buffer Slip Interrupt Enable	RUR/ WC	**Receive Slip Buffer Slip Interrupt Enable:** When this bit is set to 0: The Receive Slip Buffer Slip interrupt is disabled. When this bit is set to 1: The Receive Slip Buffer Slip interrupt is enabled.

Receive Loop-back Code Interrupt and Status Register (RLCISR) (Indirect Address = 0xnAH, 0x0AH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Receive AUXP State	Receive AUXP State Change Interrupt	CRC-4 to Non-CRC-4 Inter-network-ing Status	CRC-4 to Non-CRC-4 Inter-network-ing Status Change Interrupt	Receive Loop-back Code Activation Status	Receive Loop-back Code De-Activation Status	Receive Loop-back Code Activation Status Change Interrupt	Receive Loop-back Code De-Activation Status Change Interrupt
R	RUR/WC	R	RUR/WC	R	R	RUR/WC	RUR/WC
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive AUXP State	R	**Receive AUXP State:** This bit indicates status of the Receive AUXP pattern. When this bit is set to 0: There is no AUXP pattern detected in the Receive data stream. When this bit is set to 1: There is AUXP pattern detected in the Receive data stream.
6	Receive AUXP State Change Interrupt	RUR/ WC	**Receive AUXP State Change Interrupt:** When this bit is set to 0: There is no change in Receive AUXP pattern status. When this bit is set to 1: There is change in Receive AUXP pattern status. An interrupt will be generated upon detection of the change in Receive AUXP pattern.
5	CRC-4 to Non-CRC-4 Inter-networking Status	R	**CRC-4 to Non-CRC-4 Inter-networking Status:** This bit indicates status of the CRC-4 Internetworking. When this bit is set to 0: There is no CRC-4 to non-CRC-4 internetworking established. When this bit is set to 1: There is CRC-4 to non-CRC-4 internetworking established.
4	CRC-4 to Non-CRC-4 Inter-networking Status Change Interrupt	RUR/ WC	**CRC-4 to Non-CRC-4 Inter-networking Status Change Interrupt:** When this bit is set to 0: There is no change in CRC-4 to Non-CRC-4 Inter-networking Status. When this bit is set to 1: There is change in CRC-4 to Non-CRC-4 Inter-networking Status. An interrupt will be generated upon detection of the change in CRC-4 to Non-CRC-4 Inter-networking Status.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Loop-back Code Activation Status	R	**Receive Loop-back Code Activation Status:** This bit indicates status of the Receive Loop-back Code Activation. When this bit is set to 0: There is no Loop-back Activation code detected in the Receive data stream. When this bit is set to 1: There is Loop-back Activation code detected in the Receive data stream.
2	Receive Loop-back Code De-Activation Status	R	**Receive Loop-back Code De-activation Status:** This bit indicates status of the Receive Loop-back Code De-activation. When this bit is set to 0: There is no Loop-back De-activation code detected in the Receive data stream. When this bit is set to 1: There is Loop-back De-activation code detected in the Receive data stream.
1	Receive Loop-back Code Activation Status Change Interrupt	RUR/ WC	**Receive Loop-back Code Activation Status Change Interrupt:** When this bit is set to 0: There is no change in Receive Loop-back Activation Code Status. When this bit is set to 1: There is change in Receive Loop-back Activation Code Status. An interrupt will be generated upon detection of the change in Receive Loop-back Activation Code status.
0	Receive Loop-back Code De-activation Status Change Interrupt	RUR/ WC	**Receive Loop-back Code De-activation Status Change Interrupt:** When this bit is set to 0: There is no change in Receive Loop-back De-activation Code Status. When this bit is set to 1: There is change in Receive Loop-back De-activation Code Status. An interrupt will be generated upon detection of the change in Receive Loop-back De-activation Code status.

Receive Loop-back Code Enable Register (RLCER) (Indirect Address = 0xnAH, 0x0BH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Reserved	Receive AUXP State Change Interrupt Enable	Reserved	CRC-4 to Non-CRC-4 Inter-network-ing Status Change Interrupt Enable	Reserved	Reserved	Receive Loop-back Code Activation Status Change Interrupt Enable	Receive Loop-back Code De-Activation Status Change Interrupt Enable
	R/W		R/W			R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Reserved		
6	Receive AUXP State Change Interrupt Enable	R/W	**Receive AUXP State Change Interrupt Enable:** When this bit is set to 0: The Receive AUXP State Change Interrupt is disabled. When this bit is set to 1: The Receive AUXP State Change Interrupt is enabled.
5	Reserved		
4	CRC-4 to Non-CRC-4 Inter-networking Status Change Interrupt Enable	R/W	**CRC-4 to Non-CRC-4 Inter-networking Status Change Interrupt Enable:** When this bit is set to 0: The CRC-4 to Non-CRC-4 Inter-networking Status Change Interrupt is disabled. When this bit is set to 1: The CRC-4 to Non-CRC-4 Inter-networking Status Change Interrupt is enabled.
3	Reserved		
2	Receive Loop-back Code Activation Status Change Interrupt Enable	R/W	**Receive Loop-back Code Activation Status Change Interrupt Enable:** When this bit is set to 0: The Receive Loop-back Code Activation Status Change Interrupt is disabled. When this bit is set to 1: The Receive Loop-back Code Activation Status Change Interrupt is enabled.
1	Reserved		

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	Receive Loop-back Code De-activation Status Change Interrupt Enable	R/W	**Receive Loop-back Code De-activation Status Change Interrupt Enable:** When this bit is set to 0: The Receive Loop-back Code De-activation Status Change Interrupt is disabled. When this bit is set to 1: The Receive Loop-back Code De-activation Status Change Interrupt is enabled.

Receive Sa Interrupt Register (RSAIR) (Indirect Address = 0xnAH, 0x0CH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Received Sa6 = 1111 Interrupt	Received Sa6 = 1110 Interrupt	Received Sa6 = 1100 Interrupt	Received Sa6 = 1010 Interrupt	Received Sa6 = 1000 Interrupt	Received Sa6 = 001X Interrupt	Received Sa6 = others Interrupt	Received Sa6 = 0000 Interrupt
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Received Sa6 = 1111	R/W	**Received Sa6 = 1111:** When this bit is 0: A de-bounced Sa6 bit of value equal to '1111' has not been received from the incoming serial data. When this bit is 1: A de-bounced Sa6 bit of value equal to '1111' has been received from the incoming serial data.
6	Received Sa6 = 1110	R/W	**Received Sa6 = 1110:** When this bit is 0: A de-bounced Sa6 bit of value equal to '1110' has not been received from the incoming serial data. When this bit is 1: A de-bounced Sa6 bit of value equal to '1110' has been received from the incoming serial data.
5	Received Sa6 = 1100	R/W	**Received Sa6 = 1100:** When this bit is 0: A de-bounced Sa6 bit of value equal to '1100' has not been received from the incoming serial data. When this bit is 1: A de-bounced Sa6 bit of value equal to '1100' has been received from the incoming serial data.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Received Sa6 = 1010	R/W	**Received Sa6 = 1010:** When this bit is 0: A de-bounced Sa6 bit of value equal to '1010' has not been received from the incoming serial data. When this bit is 1: A de-bounced Sa6 bit of value equal to '1010' has been received from the incoming serial data.
3	Received Sa6 = 1000	R/W	**Received Sa6 = 1000:** When this bit is 0: A de-bounced Sa6 bit of value equal to '1000' has not been received from the incoming serial data. When this bit is 1: A de-bounced Sa6 bit of value equal to '1000' has been received from the incoming serial data.
2	Received Sa6 = 001X	R/W	**Received Sa6 = 001X:** When this bit is 0: A de-bounced Sa6 bit of value equal to '001X' has not been received from the incoming serial data. When this bit is 1: A de-bounced Sa6 bit of value equal to '001X' has been received from the incoming serial data.Note:X can be either 0 or 1.
1	Received Sa6 = others	R/W	**Received Sa6 = others:** When this bit is 0: A de-bounced Sa6 bit of value equal to anything but other than '1111', '1110', '1100', '1000', '001X' and '0000' has not been received from the incoming serial data. When this bit is 1: A de-bounced Sa6 bit of value equal to anything but other than '1111', '1110', '1100', '1000', '001X' and '0000' has been received from the incoming serial data.
0	Received Sa6 = 0000	R/W	**Received Sa6 = 0000:** When this bit is 0: A de-bounced Sa6 bit of value equal to '0000' has not been received from the incoming serial data. When this bit is 1: A de-bounced Sa6 bit of value equal to '0000' has been received from the incoming serial data.

Receive Sa Interrupt Enable Register (RSAIER) (Indirect Address = 0xnAH, 0x0DH)

BIT 7	BIT 6	BIT 5	BIT 4	BIT3	BIT 2	BIT 1	BIT 0
Received Sa6 = 1111 Interrupt Enable	Received Sa6 = 1110 Interrupt Enable	Received Sa6 = 1100 Interrupt Enable	Received Sa6 = 1010 Interrupt Enable	Received Sa6 = 1000 Interrupt Enable	Received Sa6 = 001X Interrupt Enable	Received Sa6 = others Interrupt Enable	Received Sa6 = 0000 Interrupt Enable
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
0	0	0	0	0	0	0	0

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Received Sa6 = 1111 Interrupt Enable	R/W	**Received Sa6 = 1111 Interrupt Enable:** When this bit is 0: The Received Sa6 = 1111 Interrupt is disabled. When this bit is 1: The Received Sa6 = 1111 Interrupt is enabled.
6	Received Sa6 = 1110 Interrupt Enable	R/W	**Received Sa6 = 1110 Interrupt Enable:** When this bit is 0: The Received Sa6 = 1110 Interrupt is disabled. When this bit is 1: The Received Sa6 = 1110 Interrupt is enabled.
5	Received Sa6 = 1100 Interrupt Enable	R/W	**Received Sa6 = 1100 Interrupt Enable:** When this bit is 0: The Received Sa6 = 1100 Interrupt is disabled. When this bit is 1: The Received Sa6 = 1100 Interrupt is enabled.
4	Received Sa6 = 1010 Interrupt Enable	R/W	**Received Sa6 = 1010 Interrupt Enable:** When this bit is 0: The Received Sa6 = 1010 Interrupt is disabled. When this bit is 1: The Received Sa6 = 1010 Interrupt is enabled.
3	Received Sa6 = 1000 Interrupt Enable	R/W	**Received Sa6 = 1000 Interrupt Enable:** When this bit is 0: The Received Sa6 = 1000 Interrupt is disabled. When this bit is 1: The Received Sa6 = 1000 Interrupt is enabled.
2	Received Sa6 = 001X Interrupt Enable	R/W	**Received Sa6 = 001X Interrupt Enable:** When this bit is 0: The Received Sa6 = 001X Interrupt is disabled. When this bit is 1: The Received Sa6 = 001X Interrupt is enabled.

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Received Sa6 = others Interrupt Enable	R/W	**Received Sa6 = others Interrupt Enable:** When this bit is 0: The Received Sa6 = others Interrupt is disabled. When this bit is 1: The Received Sa6 = others Interrupt is enabled.
0	Received Sa6 = 0000 Interrupt Enable	R/W	**Received Sa6 = 0000 Interrupt Enable:** When this bit is 0: The Received Sa6 = 0000 Interrupt is disabled. When this bit is 1: The Received Sa6 = 0000 Interrupt is enabled.

TABLE 9: PMON T1/E1 RECEIVE LINE CODE (BIPOLAR) VIOLATION COUNTER

REGISTER 303 PMON RECEIVE LINE CODE (BIPOLAR) VIOLATION COUNTER (RLCVCMSB) HEX ADDRESS: 0XN8, 0X00

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Unused	RO	0	
3-0	RxLCV Count - High Byte	RUR	0	These four Reset Upon Read bits along with PMON Receive Line Code Violation Counter - LSB, provides a 12-bit representation of the number of LIne Code violations that have been detected by the Receive Framer block since the last read of these registers. Lower 8 bits. This register contains the lowest four bits within this 12 bit expression

TABLE 10: PMON T1/E1 RECEIVE LINE CODE (BIPOLAR) VIOLATION COUNTER

REGISTER 304 PMON RECEIVE LINE CODE (BIPOLAR) VIOLATION COUNTER (RLCVCLSB) HEX ADDRESS: 0XN8, 0X01

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	RxLCV Count - Low Byte	RUR	0	These eight Reset Upon Read bits along with PMON Receive Line Code Violation Counter - MSB, provides 12-bit representation of the number of LIne Code violations that have been detected by Receive Framer Block since the last read of these registers. Upper 4 bits. This register contains the upper 8 bits within this 12 bit expression.

TABLE 11: PMON T1/E1 RECEIVE FRAMING ALIGNMENT BIT ERROR COUNTER

REGISTER 305 PMON RECEIVE FRAMING ALIGNMENT ERROR COUNTER (RFAECLSB) HEX ADDRESS: 0XN8, 0X02

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Framing Alignment Error Count - High Byte	RUR	0	These eight Reset Upon Read bits along with PMON E1 Receive Framing Alignment Bit Error Counter- LSB, provides a 12-bit representation of the number of Framing Alignment errors that have been detected by Receive E1 Framer number n since the last read of these registers. This register contains the upper 8bits within this 12-bit expression.

TABLE 12: PMON T1/E1 RECEIVE FRAMING ALIGNMENT BIT ERROR COUNTER

REGISTER 306 PMON RECEIVE FRAMING ALIGNMENT BIT ERROR COUNTER (RFAB-ECMSB) HEX ADDRESS: 0XN8, 0X03

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-4	Unused	R/O	0	
3-0	Framing Alignment Error Count - Low Byte	RUR	0	These four Reset Upon Read bits along with PMON E1 Receive Framing Alignment Bit Error Counter- MSB, provides 12-bit representation of the number of Framing Alignment errors that have been detected by Receive E1 Framer Block since the last read of these register. This register contains the lowest four bits within this 12-bit expression

TABLE 13: PMON T1/E1 RECEIVE SEVERELY ERRORED FRAME COUNTER

REGISTER 307 PMON RECEIVE SEVERELY ERRORED FRAME COUNTER (RSEFC) HEX ADDRESS: 0XN8, 0X04

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Severely Errored Frame Count	RUR	0	Severely Errored 8-bit frame accumulation Counter ***Note: A severely errored frame event is defined as the occurrence of two consecutive errored frame alignment signals that are not responsible for loss of frame alignment.***

TABLE 14: PMON T1/E1 RECEIVE CRC-4 BLOCK ERROR COUNTER - MSB

REGISTER 308 PMON RECEIVE SYNCHRONIZATION BIT BLOCK ERROR COUNTER (RSBBECMSB) HEX ADDRESS: 0XN8, 0X05

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	CRC-4 Block Error Count - High Byte	RUR	0	These eight Reset Upon Read bits along with PMON E1 Receive CRC-4 Block Error Counter - LSB, provides a 10-bit representation of the number of CRC-4 Block errors detected by Receive E1 Framer Block since the last read of these registers. This register contains the upper eight bits of this 10 bit expression

TABLE 15: PMON T1/E1 RECEIVE CRC-4 BLOCK ERROR COUNTER - LSB

REGISTER 309 PMON RECEIVE SYNCHRONIZATION BIT BLOCK ERROR COUNTER (RSBBECLSB) HEX ADDRESS: 0XN8, 0X06

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-2	Unused	RO	0	
1-0	CRC-4 Block Error Count - Low Byte	RUR	0	These two Reset upon Read bits along with PMON E1 Receive CRC-4 Block Error Counter - MSB, provides a 10-bit representation of the number of CRC-4 Block errors that have been detected by a Receive E1 Framer Block since the last read of these registers. This register contains the lower two bits within this 10 bit expression. *Note: Counter contains the 10-bit synchronization bit error event. A synchronization bit error event is defined as a CRC-4 error received. Counter is disabled during loss of sync at either the Frame/FAS or ESF/CRC4 level, but it will not be disabled if loss of multiframe sync occurs at the CAS level.*

TABLE 16: PMON T1/E1 RECEIVE FAR-END BLOCK ERROR COUNTER - MSB

REGISTER 310 PMON RECEIVE FAR-END BLOCK ERROR COUNTER (E1RFEBECMSB) HEX ADDRESS: 0XN8, 0X07

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Far-End Block Error Count - High Byte	RUR	0	These eight Reset Upon Read bits along with PMON E1 Receive Far-End Block Error Counter - LSB, provides a 10-bit representation of the number of Far End Block Error events that have been detected by the Receive E1 Framer Block since the last read of these registers. This register contains the upper eight bits within this 10 bit expression.

TABLE 17: PMON T1/E1 RECEIVE FAR END BLOCK ERROR COUNTER

REGISTER 311 PMON RECEIVE FAR END BLOCK ERROR COUNTER (RFEBECLSB) HEX ADDRESS: 0XN8, 0X08

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-2	Unused	RO	0	
1-0	Far-End Block Error Count -Low Byte	RUR	0	These two Reset Upon Read bits along with PMON E1 Receive Far-End Block Error Counter - MSB, provides a 10-bit representation of the number of Far End Block Error events that have been detected by the Receive E1 Framer Block since the last read of these registers. This register contains the lower two bits within this 10 bit expression. ***Note: Counter contains the 10-bit far-end block error event. Counter will increment once each time the received E-bit is set to zero. The counter is disabled during loss of sync at either the FAS or CRC-4 level and it will continue to count if loss of multiframe sync occurs at the CAS level.***

TABLE 18: PMON T1/E1 RECEIVE SLIP COUNTER

REGISTER 312 PMON RECEIVE SLIP COUNTER (RSC) HEX ADDRESS: 0XN8, 0X09

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Slip Count	RUR	0	Note: counter contains the 8-bit receive buffer slip event. A slip event is defined as a replication or deletion of a T1/E1 frame by the receiving slip buffer. ***Note: A 12 bit counter which counts the occurrence of a bipolar violation on the receive data line. This counter is of sufficient length so that the probability of counter saturation over a one second interval at a 10 -3-Bit Error Rate (BER) is less than 0.001%.***

TABLE 19: PMON T1/E1 RECEIVE LOSS OF FRAME COUNTER

REGISTER 313 PMON RECEIVE LOSS OF FRAME COUNTER (RLFC) HEX ADDRESS: 0XN8, 0X0A

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	Loss of Frame Counts	RUR	0	***Note: LOFC is a count of the number of times a "Loss Of FAS Frame" has been declared. This counter provides the capability to measure an accumulation of short failure events.***

TABLE 20: PMON T1/E1 RECEIVE CHANGE OF FRAME ALIGNMENT COUNTER

REGISTER 314 PMON RECEIVE CHANGE OF FRAME ALIGNMENT COUNTER (RCFAC) HEX ADDRESS: 0XN8, 0X0B

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	COFA Count	RUR	0	Change of Frame Alignment Accumulation counter. ***Note: COFA is declared when the newly-locked framing is different from the one offered by off-line framer.***

TABLE 21: PMON LAPD T1/E1 FRAME CHECK SEQUENCE ERROR COUNTER

REGISTER 315 PMON LAPD FRAME CHECK SEQUENCE ERROR COUNTER (FCSEC) HEX ADDRESS: 0XN8, 0X0C

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-0	FCS Error Count	RUR	0	Frame Check Sequence error Accumulation Counter. ***Note: Counter accumulates the times of occurrence of receive frame check sequence error detected by LAPD controller.***

TABLE 22: T1/E1 PRBS BIT ERROR COUNTER MSB

REGISTER 316 T1/E1 PRBS BIT ERROR COUNTER MSB HEX ADDRESS: 0XN8, 0X0D

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	PRBSE[15]	RUR	0	**Most significant bits of PRBS bit error Accumulation counter**
6	PRBSE[14]	RUR	0	
5	PRBSE[13]	RUR	0	
4	PRBSE[12]	RUR	0	
3	PRBSE[11]	RUR	0	
2	PRBSE[10]	RUR	0	
1	PRBSE[9]	RUR	0	
0	PRBSE[8]	RUR	0	

TABLE 23: T1/E1 PRBS BIT ERROR COUNTER LSB

REGISTER 317 **T1/E1 PRBS BIT ERROR COUNTER LSB** **HEX ADDRESS: 0XN8, 0X0E**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	PRBSE[7]	RUR	0	**Least significant byte of PRBS bit error accumulation counter.**
6	PRBSE[6]	RUR	0	
5	PRBSE[5]	RUR	0	
4	PRBSE[4]	RUR	0	
3	PRBSE[3]	RUR	0	
2	PRBSE[2]	RUR	0	
1	PRBSE[1]	RUR	0	
0	PRBSE[0]	RUR	0	

TABLE 24: T1/E1 TRANSMIT SLIP COUNTER

REGISTER 318 **T1/E1 TRANSMIT SLIP COUNTER (T1/E1TSC)** **HEX ADDRESS: 0XN8, 0X0F**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	TxSLIP[7]	RUR	0	**Slip accumulation counter.**
6	TxSLIP[6]	RUR	0	
5	TxSLIP[5]	RUR	0	
4	TxSLIP[4]	RUR	0	
3	TxSLIP[3]	RUR	0	
2	TxSLIP[2]	RUR	0	
1	TxSLIP[1]	RUR	0	
0	TxSLIP[0]	RUR	0	

1.7 THE INTERRUPT STRUCTURE WITHIN THE FRAMER

The XRT84L38 Framer is equipped with a sophisticated Interrupt Servicing Structure. This Interrupt Structure includes an Interrupt Request output pin $\overline{INT}$, numerous Interrupt Enable Registers and numerous Interrupt Status Registers.

The Interrupt Servicing Structure, within the XRT84L38 Framer contains three levels of hierarchy:

- The Framer Level
- The Block Level
- The Source Level.

The Framer Interrupt Structure has been carefully designed to allow the user to quickly determine the exact source of this interrupt (with minimal latency) which will aid the µC/µP in determining the which interrupt service routine to call up in order to eliminate or properly respond to the condition(s) causing the interrupt.

The XRT84L38 Framer comes equipped with registers to support the servicing of this wide array of potential "interrupt request" sources. Table 25 lists the possible conditions that can generate interrupts.

TABLE 25: LIST OF THE POSSIBLE CONDITIONS THAT CAN GENERATE INTERRUPTS, IN EACH FRAMER

INTERRUPT BLOCK	INTERRUPTING CONDITION
Framer Level	Loss of RxLineClk Signal· One Second Interrupt
HDLC Controller Block	Transmit HDLC - Start of Transmission Receive HDLC - Start of Reception Transmit HDLC - End of Transmission Receive HDLC - End of Reception FCS Error Receipt of Abort Sequence Receipt of Idle Sequence
Slip Buffer Block	Slip Buffer Full Slip Buffer Empty Slip Buffer - Slip
Alarm & Error Block	Receipt of CAS Multi-frame Yellow Alarm Detection of Loss of Signal Condition Detection of Line Code Violation Change in Receive Loss of Framer Condition Change in Receive AIS Condition Receipt of FAS Frame Yellow Alarm
T1/E1 Frame Block	Change in CAS Multi-Frame Alignment Change in National Bits· Change in CAS Signaling Bits Change in FAS Frame Alignment· Change in the "In Frame" Condition Detection of "Frame Mimicking Data" Detection of Sync (CRC-4/CRC-6) Errors Detection of Framing Bit Errors

General Flow of Interrupt Servicing

When any of the conditions presented in Table 25 occur, (if their Interrupt is enabled), then the Framer generates an interrupt request to the µP/µC by asserting the active-low interrupt request output pin, $\overline{INT}$. Shortly after the local µC/µP has detected the activated $\overline{INT}$ signal, it will enter into the appropriate user-supplied interrupt service routine. The first task for the µP/µC, while running this interrupt service routine, may be to isolate the source of the interrupt request down to the device level (e.g, the Framer IC), if multiple peripheral ICs exist in the user's system. However, once the interrupting peripheral device has been identified, the next task for the µP/µC is to determine exactly what feature of functional section within the device requested the interrupt.

Determine the Framer(s) Requesting the Interrupt

If the interrupting device turns out to be the Framer, then the µP/µC must determine which of the eight framer channels requested the interrupt. Hence, upon reaching this state, one of the very first things that the µP/µC must do within the user Framer interrupt service routine, is to perform a read of each of the Block Interrupt Status Registers within all of the Framer channels that have been enabled for Interrupt Generation via their respective Interrupt Control Registers.

Table 26 lists the Indirect Address for the Block Interrupt Status Registers associated with each of the Framer channels within the Framer.

TABLE 26: ADDRESS OF THE BLOCK INTERRUPT STATUS REGISTERS

FRAMER NUMBER	ADDRESS OF BLOCK INTERRUPT STATUS REGISTER
0	0x0A, 0x02
1	0x1A, 0x02
2	0x2A, 0x02
3	0x3A, 0x02
4	0x4A, 0x02
5	0x5A, 0x02
6	0x6A, 0x02
7	0x7A, 0x02

The bit-format of each of these Block Interrupt Status Registers is listed below.

TABLE 27: BLOCK INTERRUPT STATUS REGISTER

REGISTER 319 **BLOCK INTERRUPT STATUS REGISTER (BISR)** **HEX ADDRESS: 0XNA, 0X00**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	Sa6	RO	0	**Sa6 Interrupt Status**
7-6	LBCODE	RO	0	**Loopback Code Interrupt**
5	RxClkLOS	RUR	0	**RxClk Los Interrupt Status** Indicates if Framer n has experienced a Loss of Recovered Clock interrupt since last read of this register. 0 = Loss of Recovered Clock interrupt has not occurred since last read of this register 1 = Loss of Recovered Clock interrupt has occurred since last read of this register.
4	ONESEC	RUR	0	**One Second Interrupt Status** Indicates if the XRT84L38 has experienced a One Second interrupt since the last read of this register. 0 = No outstanding One Second interrupts awaiting service 1 = Outstanding One Second interrupt awaits service
3	HDLC	RO	0	**HDLC Block Interrupt Status** Indicates if the HDLC block has an interrupt request awaiting service. 0 = No outstanding interrupt requests awaiting service 1 = HDLC Block has an interrupt request awaiting service. Interrupt Service routine should branch to and read Data LInk Status Register (address xA,06). ***NOTE:*** *This bit-field will be reset to 0 after the microprocessor has performed a read to the Data Link Status Register.*
2	SLIP	RO	0	**Slip Buffer Block Interrupt Status** Indicates if the Slip Buffer block has any outstanding interrupt requests awaiting service. 0 = No outstanding interrupts awaiting service 1 = Slip Buffer block has an interrupt awaiting service. Interrupt Service routine should branch to and read Slip Buffer Interrupt Status register (address 0xXA,0x09. ***NOTE:*** *This bit-field will be reset to 0 after the microprocessor has performed a read of the Slip Buffer Interrupt Status Register.*
1	ALARM	RO	0	**Alarm & Error Block Interrupt Status** Indicates if the Alarm & Error Block has any outstanding interrupts that are awaiting service. 0 = No outstanding interrupts awaiting service 1 = Alarm & Error Block has an interrupt awaiting service. Interrupt SerStatus Register (address xA,02) ***NOTE:*** *This bit-field will be reset to 0 after the microprocessor has performed a read of the Alarm & Error Interrupt Status register.*
0	T1/E1 FRAME	RO	0	**T1/E1 Framer Block Interrupt Status** Indicates if an T1/E1 Frame Status interrupt request is awaiting service. 0 = No T1/E1 Frame Status interrupt is pending 1 = T1/E1 Framer Status interrupt is awaiting service.

For a given Framer, the Block Interrupt Status Register presents the Interrupt Request status of each Interrupt Block within the Framer. The Block Interrupt Status Register helps the µP/µC identify which Interrupt Block(s) have requested the interrupt. Whichever bit(s) are asserted in this register identifies which block(s) have experienced an interrupt generating condition, as presented in Table 27. Once the µP/µC has read this register, it

can determine which branch within the interrupt service routine that it must follow in order to properly service this interrupt.

The Framer IC further supports the Interrupt Block Hierarchy by providing the Block Interrupt Enable Register. The bit-format of this register is identical to that for the Block Interrupt Status Register and is presented below.

TABLE 28: BLOCK INTERRUPT ENABLE REGISTER

REGISTER 320 **BLOCK INTERRUPT ENABLE REGISTER (BIER)** **HEX ADDRESS: 0XNA, 0X01**

BIT	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7	SA6_ENB	R/W	0	**SA6 interrupt enable**
6	LBCODE_ENB	R/W	0	**Loopback code interrupt enable**
5	RXCLKLOSS	R/W	0	**RxLineClk Loss Interrupt Enable** 0 = Disables interrupt 1 = Enables interrupt
4	ONESEC_ENB	R/W	0	**One Second Interrupt Enable** 0 = Disables interrupt 1 = Enables Interrupt
3	HDLC_ENB	R/W	0	**HDLC Block Interrupt Enable** 0 = Disables all HDLC Block interrupts 1 = Enables HDLC Block (for interrupt generation) at the block level
2	SLIP_ENB	R/W	0	**Slip Buffer Block Interrupt Enable** 0 = Disables all Slip Buffer Block Interrupts 1 = Enables Slip Buffer Block at the block level
1	ALARM_ENB	R/W	0	**Alarm & Error Block Interrupt Enable** 0 = Disables all Alarm & Error Block interrupts 1 = Enables Alarm & Error block at the block level
0	T1/E1FRAME_ENB	R/W	0	**T1/E1 Frame Block Enable** 0 = Disables all Frame Block interrupts 1 = Enables the Frame Block at the block level

The Block Interrupt Enable Register permits the user to individually enable or disable the interrupt requesting capability of each of the "interrupt blocks" within the Framer. If a particular bit-field, within this register contains the value "0"; then the corresponding functional block has been disabled from generating any interrupt requests.

1.7.1 Configuring the Interrupt System, at the Framer Level

The XRT84L38 Framer IC permits the user to enable or disable each of the eight Framers for interrupt generation. Further, the chip permits the user to make the following configuration selection.

1. Whether the source-level Interrupt Status bits are Reset-upon-Read or Write-to-Clear.
2. Whether or not an activated interrupt is automatically cleared.

1.7.1.1 Enabling/Disabling the Framer for Interrupt Generation

Each of the eight (8) Framers of the XRT84L38 Framer can be enabled or disabled for interrupt generation. This selection is made by writing the appropriate “0” or “1” to bit 0 (INTRUP_EN) of the Interrupt Control Register corresponding to that framer, (see Table 29).

NOTE: *Setting this bit-field to "1" does not enable all of the interrupts within the Framer. A given interrupt must also be enabled at the block and source-level before it is enabled for interrupt generation.*

TABLE 29: INTERRUPT CONTROL REGISTER

REGISTER 26 **INTERRUPT CONTROL REGISTER (ICR)** **HEX ADDRESS: 0XN0, 0X1A**

BIT	MODE	FUNCTION	TYPE	DEFAULT	DESCRIPTION-OPERATION
7-3		Unused	RO	0	
2		INT_WC_RUR	R/W	0	**Interrupt Write-to-Clear or Reset-upon-Read Select** Configures Interrupt Status bits to either RUR or Write-to-Clear 0=Interrupt Status bit RUR 1=Interrupt Status bit Write-to-Clear
1		ENBCLR	R/W	0	**Interrupt Enable Auto Clear** 0=Interrupt Enable bits are not cleared after status reading 1=Interrupt Enable bits are cleared after status reading
0		INTRUP_ENB	R/W	0	**Interrupt Enable for Framer_n** Enables Framer n for Interrupt Generation. 0 = Disables corresponding framer block for Interrupt Generation 1 = Enables corresponding framer block for Interrupt Generation

1.7.1.2 Configuring the Interrupt Status Bits within a given Framer to be Reset-upon-Read or Write-to-Clear.

The XRT84L38 Source-Level Interrupt Status Register bits can be configured to be either Reset-upon-Read or Write-to-Clear. If the user configures the Interrupt Status Registers to be Reset-upon-Read, then when the µP/µC is reading the interrupt status register, the following happens:

1. The contents of the Source-Level Interrupt Status Register automatically is reset to “0x00" following the read operation.
2. The Interrupt Request Output pin ($\overline{INT}$) automatically toggles false, or "High", upon reading the Interrupt Status Register containing the last activated interrupt status bit.

If the user configures the Interrupt Status Registers to be Write-to-Clear, then when the µP/µC is reading the interrupt status register, the following happens.

1. The contents of the Source-Level Interrupt Status Register is not cleared to "0x00" following the read operation. The µP/µC has to write 0x00 to the interrupt status register in order to reset the contents of the register to 0x00.
2. Reading the Interrupt Status Register, which contains the activated bit(s) does not cause the Interrupt Request Output pin ($\overline{INT}$) to toggle false. The Interrupt Request Output pin does not toggle false until the µP/µC has written 0x00 into this register. The Interrupt Service Routine must include this write operation.

The Interrupt Status Register associated with a given framer can be configured to be either Reset-upon-Read or Write-to-Clear by writing the appropriate value into Bit 2 within the Interrupt Control Register (see Table 29).

1.7.1.3 Automatic Reset of Interrupt Enable Bits

Occasionally, the user's system which includes the Framer, may experience a fault condition, such that a Framer Interrupt Condition continuously exists. If this particular interrupt has been enabled, then the Framer will generate an interrupt request to the µP/µC. Afterwards, the µP/µC attempts to service this interrupt by reading the appropriate Block-level and Source-Level Interrupt Status Register. Additionally, the local µP/µC attempts to perform some system-related tasks in order to try to resolve these conditions causing the interrupt. After the local µC/µP has attempted all of these things, the Framer negates the $\overline{\text{INT}}$ output pin. However, because this system fault still remains, the condition causing the Framer to issue this interrupt also exists. Consequently, the Framer generates another interrupt request which forces the µP/µC to once again attempt to service this interrupt. This results in the local µP/µC being tied up in a continuous cycle of executing this one interrupt service routine. Consequently, the µP/µC, along with portions of the overall system, now becomes non-functional.

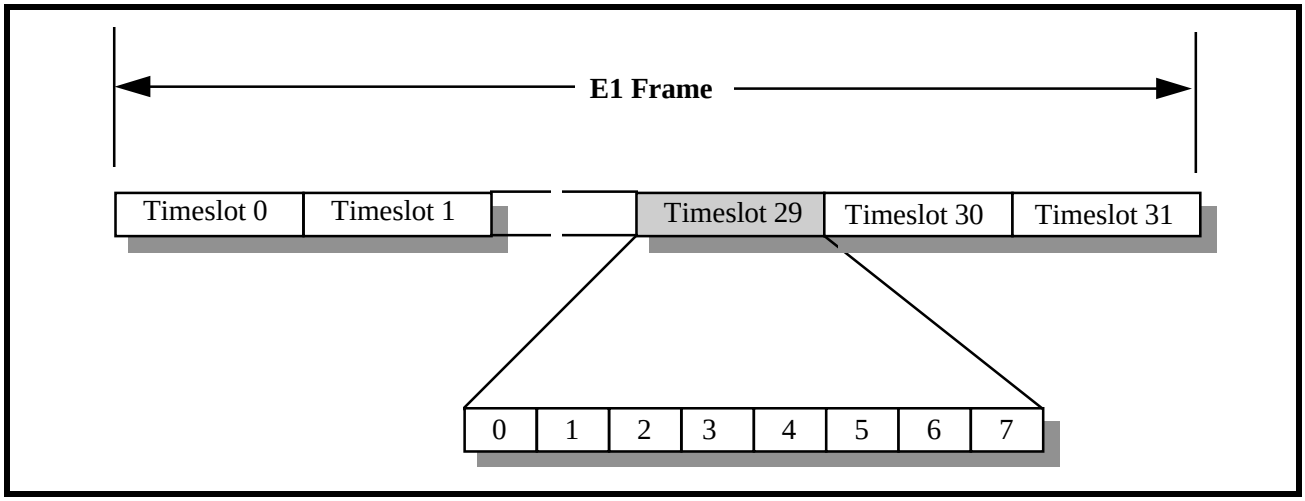
To prevent this from occurring, the Framer can be configured to automatically reset the interrupt enable bits following their activation by writing the appropriate value to bit 1 of the Interrupt Control Register (see Table 29). Writing a "1" to this bit-field configures the Framer to reset a given interrupt following activation. Writing a "0" to this bit-field configures the Framer to leave the interrupt enabled, following its activation.

2.0 THE E1 FRAMING STRUCTURE

2.1 THE SINGLE E1 FRAME

A single E1 frame consists of 256 bits which is created 8000 times a second; thereby yielding a bit-rate of 2.048Mbps. The 256 bits within each E1 frame is grouped into 32 octets or timeslots. These timeslots are numbered from 0 to 31. Figure 17 presents a diagram of a single E1 frame.

FIGURE 17. SINGLE E1 FRAME DIAGRAM



A single E1 frame consists of 32 timeslots. However, not all of these timeslots are available to transmit voice or user data. For instance, timeslot 0 is always reserved for system use and timeslot 16 is sometimes used (reserved) by the system. Hence, within each E1 frame, either 30 or 31 of the 32 timeslots are available for transporting user or voice data.

TIMESLOT 0

In general, there are two types of E1 frames.

- FAS (Frame Alignment Signaling) frames
- non-FAS frames

In any E1 data stream, the E1 frame type alternates between the FAS and non-FAS frames.

The timeslot 0 octet within the FAS E1 frame contains a framing alignment pattern and therefore supports framing. The timeslot 0 octet within the non-FAS E1 frame contains bits that support signaling or data link message transmission.

TIMESLOT 0 OCTETS WITHIN FAS FRAMES

The bit-format of a timeslot 0 octet within a FAS frame is presented in Table 30.

TABLE 30: BIT FORMAT OF TIMESLOT 0 OCTET WITHIN A FAS E1 FRAME

BIT	7	6	5	4	3	2	1	0
Value	1	1	0	1	1	0	0	SI
Function	Frame Alignment Signaling (FAS) Pattern							International Bit
DESCRIPTION-OPERATION	The fixed framing pattern (e.g., 0, 0, 1, 1, 0, 1, 1) is used by the Receive E1 Framer at the Remote terminal for frame synchronization/alignment purposes.							In practice, the Si bit within the FAS E1 Frame carries the results of a CRC-4 calculation, which is discussed in greater detail in Section 2.2.1.

The table above indicates that the FAS frame timeslot 0 octet consists of a single International Bit within bit-field 0, Si, followed by a fixed 7-bit pattern within bit-fields 1 through 7.

BIT 0—SI (INTERNATIONAL BIT)

The Si bit within the FAS E1 Frame typically carries the results of a CRC-4 calculation, which is discussed in greater detail in Section 2.2.1. The fixed framing pattern (e.g., 0, 0, 1, 1, 0, 1, 1) will be used by the Receive E1 Framer at the Remote terminal for frame synchronization/alignment purposes. Section discusses how the Receive E1 Framer uses these bits.

Timeslot 0 octets within non-FAS frames

The bit-format of a timeslot 0 octet within a non-FAS frame is presented in Table 31.

TABLE 31: BIT FORMAT OF TIMESLOT 0 OCTET WITHIN A NON-FAS E1 FRAME

BIT	7	6	5	4	3	2	1	0
Value	Sa8	Sa7	Sa6	Sa5	Sa4	A	1	Si
Function6	National bits					Yellow Alarm	Fixed Value	International Bit
Description-Operation	**National Bits** These bit-fields can be used to carry data link information from the Local transmitting terminal to the Remote receiving terminal. Since the National bits only exist in the non-FAS frames, they offer a maximum signaling data link bandwidth of 20kbps.					**FAS Frame Yellow Alarm Bit** This bit-field is used to transmit a Yellow alarm to the Remote Terminal. This bit-field is set to "0" during normal conditions, and is set to "1" whenever the Receive E1 Framer detects an LOS (Loss of Signal) or LOF (Loss of Framing) condition in the incoming E1 frame data.	**Fixed at "1"** Bit-field "1" contains a fixed value "1". This bit-field will be used for FAS framing synchronization/ alignment purposes by the Remote Receive E1 Framer.	**International Bit** The Si bit within the non-FAS E1 Frame typically carries a specific value that will be used by the Receive E1 Framer for CRC Multi-frame alignment purposes.

The table above indicates the non-FAS frame timeslot 0 octet consists of a single international bit, Si, within bit-field 0.

BIT 0—SI (INTERNATIONAL BIT)

The Si bit, within the non-FAS E1 Frame carries a specific value that will be used by the Receive E1 Framer, for CRC Multi-frame alignment purposes. Section 7 discusses the exact role of the Si bit-field within the non-FAS frames.

BIT 1—FIXED AT "1"

Bit-field "1" contains a fixed value "1". This bit-field will be used for FAS framing synchronization/alignment purposes by the Remote Receive E1 Framer. Section _ discusses how the Receive E1 Framer uses this bit-field.

BIT 2—A (FAS FRAME YELLOW ALARM BIT)

This bit-field is used to transmit a Yellow alarm to the Remote Terminal. This bit-field is set to "0" during normal conditions, and is set to "1" whenever the Receive E1 Framer detects an LOS (Loss of Signal) or LOF (Loss of Framing) condition in the incoming E1 frame data.

BIT 3 THROUGH 7—SA4–SA8 (NATIONAL BITS)

These bit-fields can be used to carry data link information from the Local transmitting terminal to the Remote receiving terminal. Since the National bits only exist in the non-FAS frames, they offer a maximum signaling data link bandwidth of 20kbps.

2.2 THE E1 MULTI-FRAME STRUCTURES

The 84L38 Octal Framer supports two kinds of E1 Multi-frame structures:

- CRC Multi-frame
- CAS Multi-frame

2.2.1 The CRC Multi-frame Structure

A CRC Multi-frame consists of 16 consecutive E1 frames, with the first of these frames being a FAS frame. From a Frame Alignment point of view, the timeslot 0 octets of each of these E1 frames within the Multi-frame are the most important 16 octets. Table 32 presents the bit-format for all timeslot 0 octets within a 16 frame CRC Multi-frame.

TABLE 32: BIT FORMAT OF ALL TIMESLOT 0 OCTETS WITHIN A CRC MULTI-FRAME

SMF	FRAME NUMBER	BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1	0	C1	0	0	1	1	0	1	1
	1	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	2	C2	0	0	1	1	0	1	1
	3	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	4	C3	0	0	1	1	0	1	1
	5	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	6	C4	0	0	1	1	0	1	1
	7	0	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
2	8	C1	0	0	1	1	0	1	1
	9	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	10	C2	0	0	1	1	0	1	1
	11	1	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	12	C3	0	0	1	1	0	1	1
	13	E	1	A	Sa4	Sa5	Sa6	Sa7	Sa8
	14	C4	0	0	1	1	0	1	1
	15	E	1	A	Sa4	Sa5	Sa6	Sa7	Sa8

Table 32 has the CRC Multi-frame divided into 2 sub Multi-Frames. Sub-Multi-Frame 1 is designated as SMF1 and Sub-Multi-Frame 2 is designated as SMF2.

SMF1 consists of E1 frames 0 through 7 consisting of 4 FAS frames and 4 non-FAS frames.

There are two interesting things to note in Table 32. First, all of the bit-field 0 positions within each of the FAS frames are designated as C1, C2, C3 and C4. These four bit-fields contain the CRC-4 values which has been computed over the previous SMF. Hence, while the Transmit E1 Framer is assembling a given SMF, it computes the CRC-4 value for that SMF and inserts these results into the C1 through C4 bit-fields within the very next SMF. These CRC-4 values ultimately are used by the Remote Receive E3 Framer for error-detection purposes.

NOTE: *This framing structure is referred to as a CRC Multi-Frame because it permits the remote receiving terminal to locate and verify the CRC-4 bit-fields.*

The second interesting thing to note regarding Table 32 is that the bit-field 0 positions within each of the non-FAS frames are of a fixed six (6) bit pattern: 0, 0, 1, 0, 1, 1; along with two bits, each designated at “E”. This six bit pattern is referred to as the CRC Multi-Frame alignment pattern. This six-bit pattern will ultimately be used by the Remote Receive E1 Framer for CRC Multi-Frame synchronization/alignment. Section discusses how the Receive E1 Framer uses this 6-bit CRC Multi-frame alignment pattern for frame synchronization/alignment. The "E" bits are used to indicate that the Local Receive E1 framer has detected errored sub-Multi-Frames.

2.2.2 CAS Multi-Frames and Channel Associated Signaling

CAS Multi-Frames are only relevant if the user is using CAS or Channel Associated Signaling. If the user is implementing Common Channel Signaling then the CAS Multi-Frame is not available. The exact role of CAS Multi-Frames is discussed in some detail in the next section.

2.2.2.1 Channel Associated Signaling

If the user operates an E1 channel in Channel Associated Signaling (CAS) mode, then the timeslot 16 octets within each E1 frame will be reserved for signaling. Such signaling would convey information such as On-Hook, Off-Hook conditions, call set-up, control, etc. In CAS, this type of signaling data that is associated with a particular voice channel will be carried within timeslot 16 of a particular E1 frame within a CAS Multi-Frame.

The CAS is carried in a Multi-Frame structure which consists of 16 consecutive E1 frames. The framing/byte format of a CAS Multi-Frame is presented in Figure 18.

FIGURE 18. FRAME/BYTE FORMAT OF THE CAS MULTI-FRAME STRUCTURE

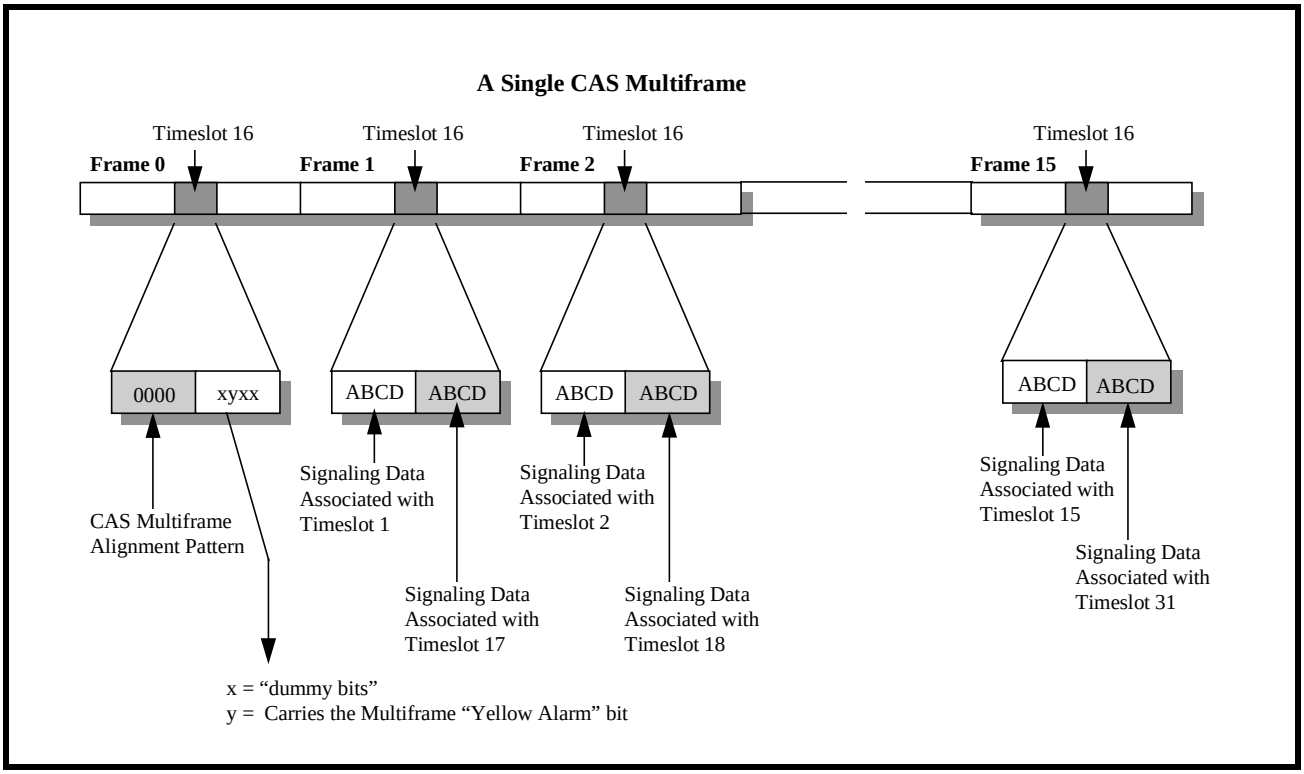


Figure 18 indicates that timeslot 16 within Frame 1 of the CAS Multi-Frame, contains 4 bits of signaling data for voice channel 1 and 4 bits of signaling data for voice channel 17. Likewise, timeslot 16 within Frame 2 contains 4 bits of signaling data for voice channel 2 and 4 bits of signaling data for voice channel 18; and so on. Timeslot 16 within frame 0 is a special octet that is used for two purposes.

1. To convey CAS Multi-Frame alignment information, and
2. To convey Multi-Frame alarm information to the Remote Terminal.

The bit-format of timeslot 16 within frame 0 of a CAS Multi-Frame is 0000 xyxx.

The upper nibble of this octet contains all zeros and is used to identify itself as the CAS Multi-Frame alignment signal. If CAS is used, then the user is advised to insure that none of the other timeslot 16 octets contain the value "0000". The lower nibble of this octet contains the expression "xyxx". In this case, the x-bits are the spare bits and should be set to "0" if not used. The y-bit is used to indicate a Multi-Frame alarm condition to the Remote terminal. During normal operation, this bit-field is cleared to "0". However, if the Local Receive E1 Framer detects a problem with the incoming Multi-Frames, then the Local Transmit E1 Framer will set this bit-field within the next outbound CAS Multi-Frame to "1".

NOTE: *The Local Transmit E1 Framer will continue to set the y-bit to "1" for the duration that the Local Receive E1 Framer detects this problem.*

2.2.2.2 Common Channel Signaling (CCS)

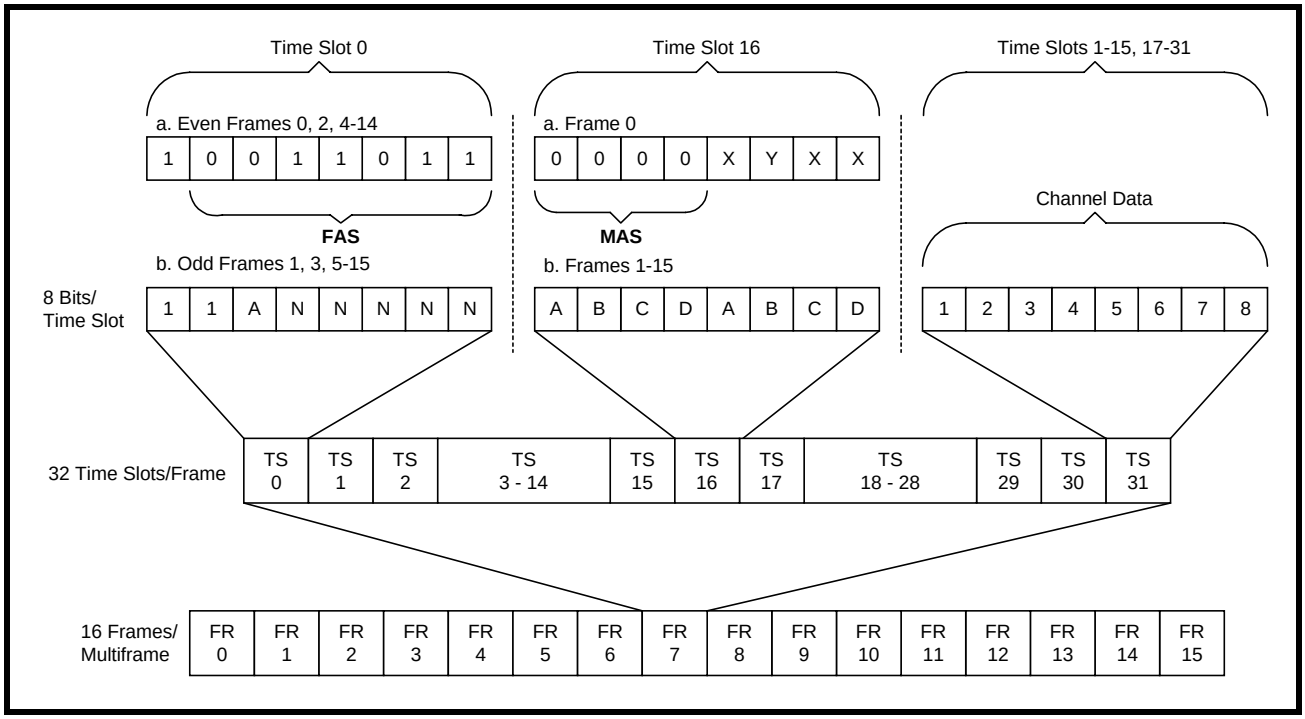
Common Channel Signaling is an alternative form of signaling from Channel Associated Signaling. In CCS, whatever signaling data which is transported via the outbound E1 data stream, carries information that applies to all of the voice channels as a set (e.g., timeslots 1 through 15 and 17 through 31) in the E1 frame. There are numerous other variations of Common Channel Signaling that are available. Some of these are listed below.

- 31 Voice Channels with the common channel signaling being transported via the National Bits.

- 30 Voice Channels with the common channel signaling data being transported via the National Bits and CAS data being transported via timeslot 16.
- 30 Voice Channels with the Common Channel Signaling being processed via timeslot 16. (e.g., Primary Rate ISDN Signaling).

A more detailed discussion of these forms of Common Channel signaling are discussed in Section 10.0.

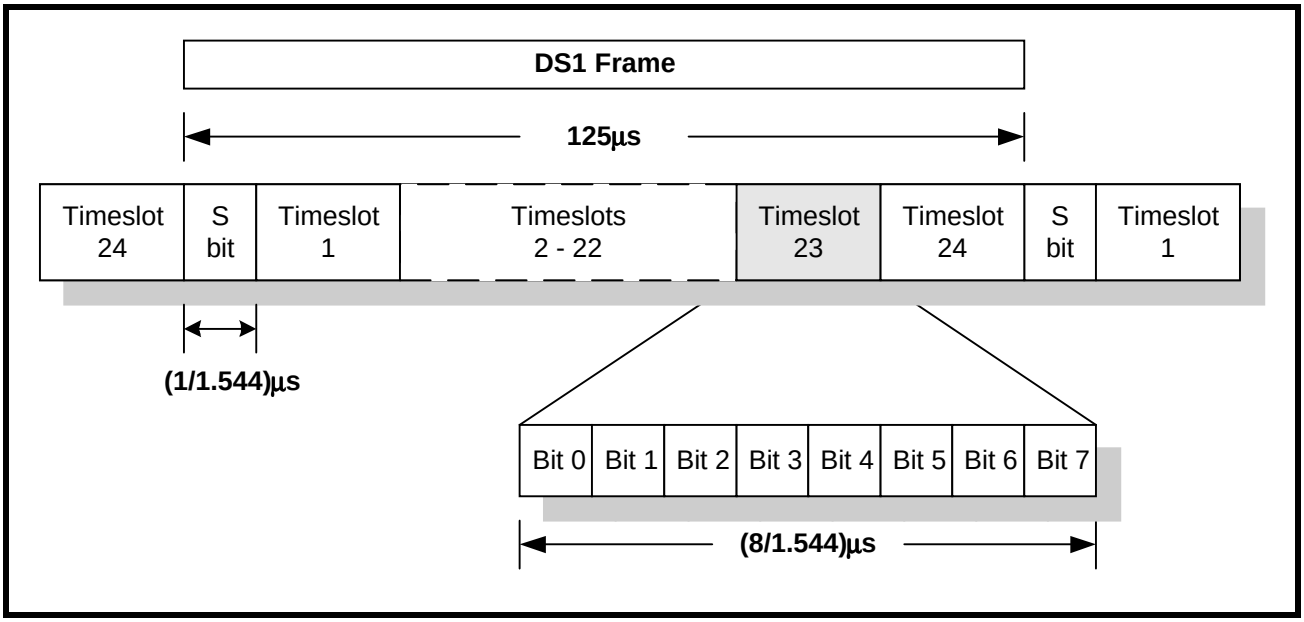
FIGURE 19. E1 FRAME FORMAT



3.0 THE DS1 FRAMING STRUCTURE

A single T1 frame is 193 bits long and is transmitted at a frame rate of 8000Hz. This results in an aggregate bit rate of 193 bits X 8000/sec = 1.544 Mbits/sec. Basic frames are divided into 24 timeslots numbered 1 thru 24 and a framing bit, see Figure 20. Each timeslot is 8 bits in length and is transmitted most significant bit first, numbered bit 0. This results in a single timeslot data rate of 8 bits x 8000/sec = 64 kbits/sec.

FIGURE 20. T1 FRAME FORMAT



3.1 T1 SUPER FRAME FORMAT (SF)

The Superframe Format (SF), is also referred to as the D4 format. The requirement for associated signaling in frames 6 and 12 dictates that the frames be distinguishable. This leads to a multiframe structure consisting of 12 frames per superframe (SF). See Figure 21 and Table 33.

The SF structure consists of a multiframe of 12 frames. Each frame has 24 timeslots, plus an F-bit and 8 bits per timeslot. A timeslot is equivalent to one voice circuit or one 64kb/s data circuit.

This structure of frames and multiframes is defined by the F-bit pattern. The F-bit is designated alternately as an Ft bit (terminal framing bit) or Fs bit (signalling framing bit). The Ft bit carries a pattern of alternating zeros and ones (101010) in odd frames that defines the boundaries so that one timeslot may be distinguished from another. The Fs bit carries a pattern of (001110) in even frames and defines the multiframe boundaries so that one frame may be distinguished from another.

FIGURE 21. T1 SUPERFRAME PCM FORMAT

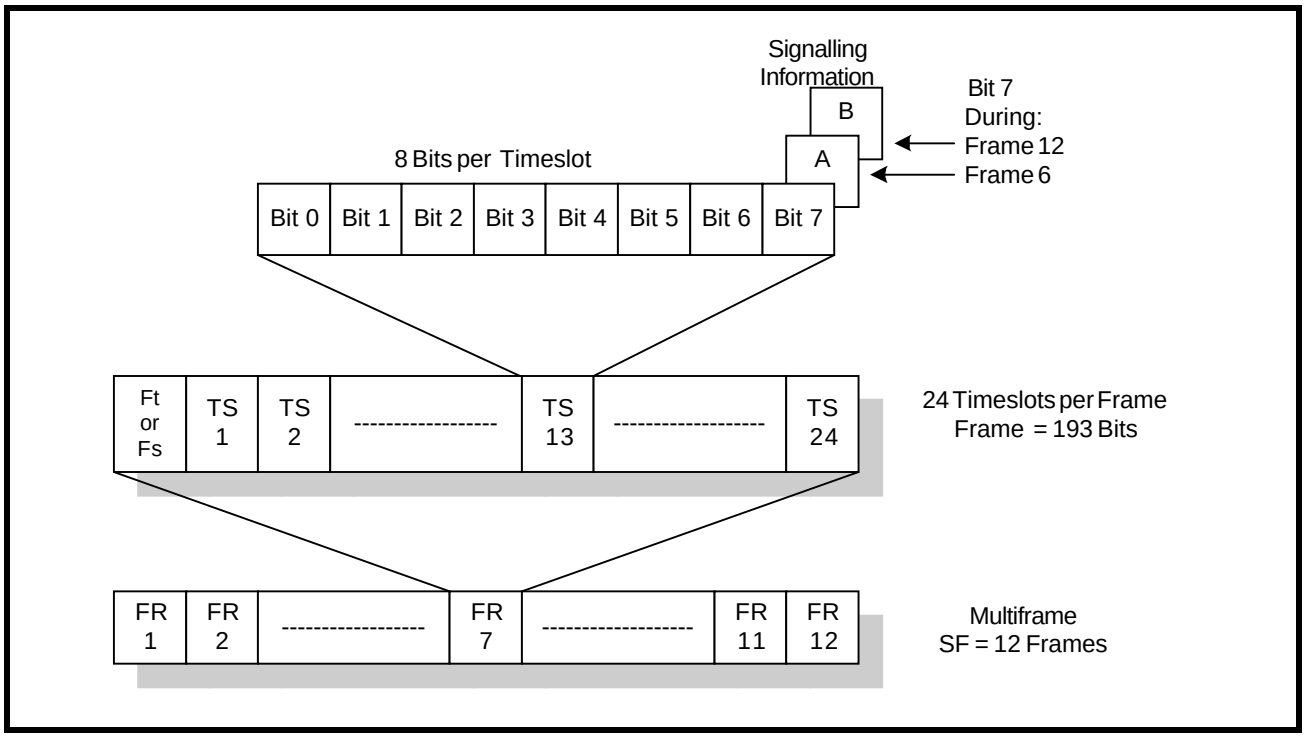


TABLE 33: SUPERFRAME FORMAT

FRAME	BIT	F-BITS		BIT USE IN EACH TIMESLOT		SIGNALLING CHANNEL
		TERMINAL FRAMING FT	TERMINAL FRAMING FS	TRAFFIC	SIG	
1	0	1	----	1-8	----	----
2	193	----	0	1-8	----	----
3	386	0	----	1-8	----	----
4	579	----	0	1-8	----	----
5	772	1	----	1-8	----	----
6	965	----	1	1-7	8	A
7	1158	0	----	1-8	----	----
8	1351	----	1	1-8	----	----
9	1544	1	----	1-8	----	----
10	1737	----	1	1-8	----	----
11	1930	0	----	1-8	----	----
12	2123	----	0	1-7	8	B

3.2 T1 EXTENDED SUPERFRAME FORMAT

In Extended Superframe Format (ESF), as shown in Figure 22 and Table 34, the multiframe structure is extended to 24 frames. The timeslot structure is identical to D4 (SF) format. Robbed-bit signaling is accommodated in frame 6 (A-bit), frame 12 (B-bit), frame 18 (C-bit) and frame 24 (D-bit).

The F-bit pattern of ESF contains three functions:

1. Framing Pattern Sequence (FPS), which defines the frame and multiframe boundaries.
2. Facility Data Link (FDL), which allows data such as error-performance to be passed within the T1 link.
3. Cyclic Redundancy Check (CRC), which allows error performance to be monitored and enhances the reliability of the receiver's framing algorithm.

FIGURE 22. T1 EXTENDED SUPERFRAME FORMAT

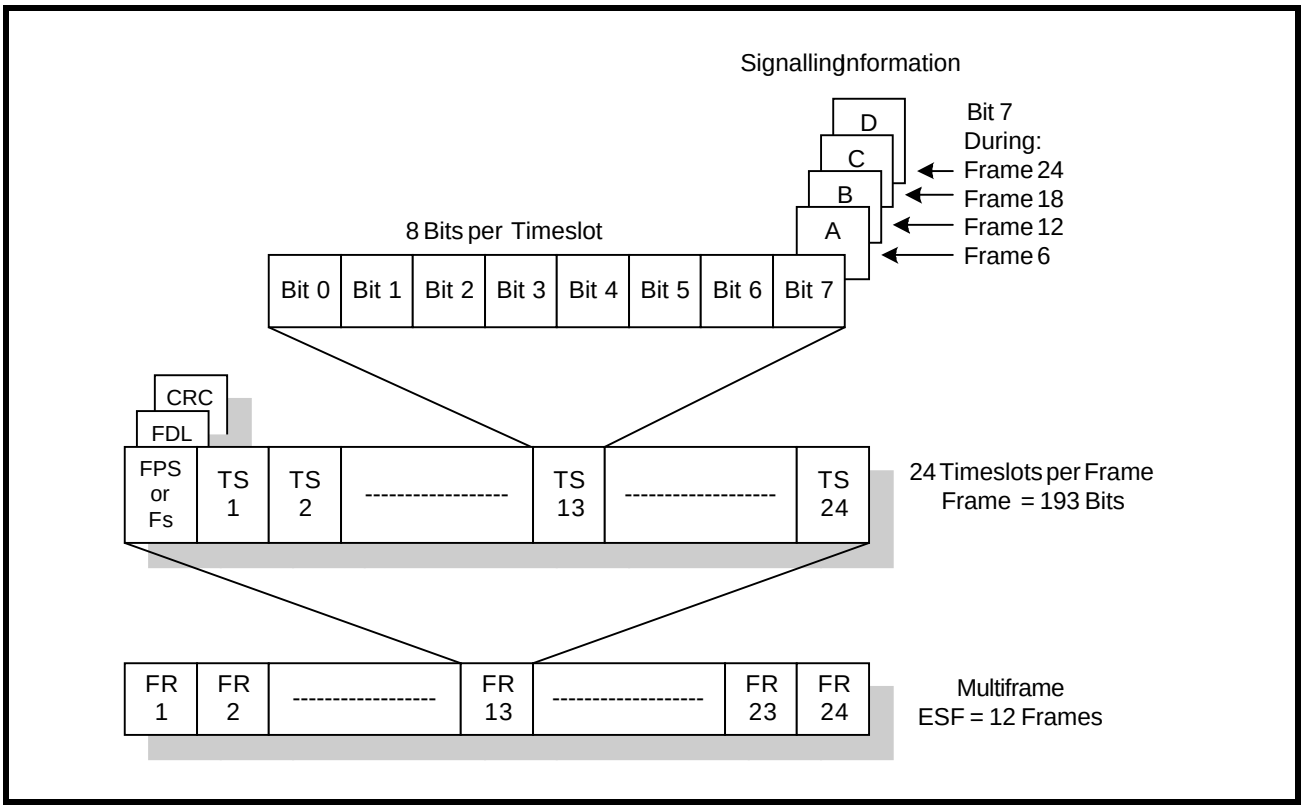


TABLE 34: EXTENDED SUPERFRAME FORMAT

FRAME	BIT	F-BITS			BIT USE IN EACH TIMESLOT		SIGNALLING CHANNEL		
		FPS	DL	CRC	TRAFFIC	SIG	16	4	2
1	0	----	m	----	1-8	----	----	----	----
2	193	----	----	C1	1-8	----	----	----	----
3	386	----	m	----	1-8	----	----	----	----
4	579	0	----	----	1-8	----	----	----	----
5	772	----	m	----	1-8	----	----	----	----
6	965	----	----	C2	1-7	8	A	A	A
7	1158	----	m	----	1-8	----	----	----	----
8	1351	0	----	----	1-8	----	----	----	----
9	1544	----	m	----	1-8	----	----	----	----
10	1737	----	----	C3	1-8	----	----	----	----
11	1930	----	m	----	1-8	----	----	----	----
12	2123	1	----	----	1-7	8	B	B	B
13	2316	----	m	----	1-8	----	----	----	----
14	2509	----	----	C4	1-8	----	----	----	----
15	2702	----	m	----	1-8	----	----	----	----
16	2895	0	----	----	1-8	----	----	----	----
17	3088	----	m	----	1-8	----	----	----	----
18	3281	----	----	C5	1-7	8	C	C	A
19	3474	----	m	----	1-8	----	----	----	----
20	3667	1	----	----	1-8	----	----	----	----
21	3860	----	m	----	1-8	----	----	----	----
22	4053	----	----	C6	1-8	----	----	----	----
23	4246	----	m	----	1-8	----	----	----	----
24	4439	1	----	----	1-7	8	D	B	A

NOTES:

1. *FPS indicates the Framing Pattern Sequence (...001011...)*
2. *DL indicates the 4kb/s Data Link with message bits m.*
3. *CRC indicates the cyclic redundancy check with bits C1 to C6*
4. *Signaling options include 16 state, 4 state and 2 state.*

3.3 SLC 96 FORMAT (SLC)

SLC framing mode allows synchronization to the SLC®96 data link pattern. This pattern described in the Bellcore TR-TSY-000008, contains both signaling information and a framing pattern that overwrites the Fs bit of the SF framer pattern. See Table 35.

TABLE 35: SLC®96 FS BIT CONTENTS

FRAME #	FS BIT	FRAME #	FS BIT	FRAME #	FS BIT
2	0	26	C2	50	0
4	0	28	C3	52	M1
6	1	30	C4	54	M2
8	1	32	C5	56	M3
10	1	34	C6	58	A1
12	0	36	C7	60	A2
14	0	38	C8	62	S1
16	0	40	C9	64	S2
18	1	42	C10	66	S3
20	1	44	C11	68	S4
22	1	46	0	70	1
24	C1	48	1	72	0

NOTES:

1. *The SLC®96 frame format is similar to that of SF as shown in Table 33 with the exceptions shown in this table.*
2. *C1 to C11 are concentrator bit fields.*
3. *M1 to M3 are Maintenance bit fields.*
4. *A1 and A2 are alarm bit fields.*
5. *S1 to S4 are line switch bit fields.*
6. *The Fs bits in frames 46, 48 and 70 are spoiler bitswhich are used to protect against false muti-framing.*

4.0 THE DS1 TRANSMIT SECTION

4.1 THE DS1 TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK

4.1.1 Description of the Transmit Payload Data Input Interface Block

Each of the eight framers within the XRT84L38 includes a Transmit Payload Data Input Interface block. The function of this block is to provide an interface to the local Terminal Equipment (for example, a Central Office or switching equipment) that has data to send to a Far End terminal over a DS1 or E1 transport medium.

The Payload Data Input Interface module (also known as the Back-plane Interface module) supports payload data to be taken from or presented to the system. In DS1 mode, supported data rates are 1.544Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 12.352Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s. In E1 mode, supported data rates are XRT84V24 compatible 2.048Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s.

The Transmit Payload Data Input Interface block supplies or accepts the following signals to the local Terminal Equipment circuitry:

- Transmit Serial Data Input (TxSer_n)
- Transmit Serial Clock (TxSerClk_n)
- Transmit Single-frame Synchronization Signal (TxSync_n)
- Transmit Multi-frame Synchronization Signal (TxMSync_n)
- Transmit Time-slot Indicator Clock (TxTSClk_n)
- Transmit Time-slot Indication Bits (TxTSb[4:0]_n)

The Transmit Serial Data is an input pin carrying payload, signaling and sometimes Data Link data supplied by the local Terminal Equipment to the XRT84L38.

The Transmit Serial Clock is an input or output signal used by the Transmit Payload Data Input Interface block to latch in incoming serial data from the local Terminal Equipment. The Transmit Clock Inversion bit of the Transmit Interface Control Register (TICR) determines at which edge of the Transmit Serial Clock would data transition on the Transmit Serial Data pin occur.

The table below shows configurations of the Transmit Clock Inversion bit of the Transmit Interface Control Register (TICR).

TRANSMIT INTERFACE CONTROL REGISTER (TICR) (INDIRECT ADDRESS = 0xn0H, 0x20H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Transmit Clock Inversion	R/W	0 - Serial data transition happens on rising edge of the Transmit Serial Clock. 1 - Serial data transition happens on falling edge of the Transmit Serial Clock.

Throughout the discussion of this datasheet, we assume that serial data transition happens on the rising edge of the Transmit Serial Clock unless stated otherwise.

The Transmit Single-frame Synchronization signal is either input or output. When configured as input, it indicates the beginning of a DS1 frame. When configured as output, it indicates the end of a DS1 frame.

The Transmit Multi-frame Synchronization signal is either input or output. When configured as input, it indicates the beginning of a DS1 multi-frame. When configured as output, it indicates the end of a DS1 multi-frame.

The Transmit Input Clock signal is multiplexed into the Transmit Multi-frame Synchronization pin (TxMSync_n) of XRT84L38. When the framer is running at High-speed Back-plane Interface mode, the Transmit Input Clock functions as the timing source for the High-speed Back-plane Interface.

By connecting these signals with the local Terminal Equipment, the Transmit Payload Data Input Interface accepts payload data from the Terminal Equipment and routes it to the Transmit Framer module inside the device.

4.1.2 Brief Discussion of the Transmit Payload Data Input Interface Block Operating at 1.544Mbit/s mode

If the framer is operating in normal 1.544Mbit/s Back-plane interface mode for DS1, timing source of the transmit section can be one of the three clocks:

- Transmit Serial Input Clock
- OSCCLK Driven Divided Clock
- Recovered Receive Line Clock

The Transmit Timing Source Select [1:0] bits of the Clock Select Register (CSR) determine which clock is used as the timing source. The following table shows configurations of the Transmit Timing Source Select [1:0] bits of the Clock Select Register.

CLOCK SELECT REGISTER (CSR) (INDIRECT ADDRESS = 0xn0H, 0x00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Timing Source Select	R/W	These two READ/WRITE bit-fields permit the user to select the timing source of Transmit section of the framer. When the Transmit Back-plane interface is operating at a clock rate of 1.544MHz for T1, these two READ/WRITE bit-fields also determine the direction of Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk). When the framer is operating at other Back-plane mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all inputs. 00 - The Recovered Receive Line Clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 1.544MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all outputs. Upon losing of the Recovered Receiver Line Clock, the OSCCLK Driven Divided clock is automatically chosen to be the timing source of the Transmit section of the framer. 01 - The Transmit Serial Clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 1.544MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all inputs. 10 - The OSCCLK Driven Divided clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 1.544MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all outputs. Upon losing of the Recovered Receiver Line Clock, the OSCCLK Driven Divided clock is automatically chosen to be the timing source of the Transmit section of the framer. 11 - The Recovered Receive Line Clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 1.544MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all outputs. Upon losing of the Recovered Receiver Line Clock, the OSCCLK Driven Divided clock is automatically chosen to be the timing source of the Transmit section of the framer.

The Transmit Serial Clock (TxSerClk_n), Transmit Single-frame Synchronization Signal (TxSync_n) and Transmit Multi-frame Synchronization Signal (TxMSync_n) can be either inputs or outputs depend on the timing source of the Transmit section of the framer.

With the OSCCLK Driven Divided Clock or the Recovered Receive Line Clock being the timing source of the transmit section, the Transmit Serial Clock (TxSerClk_n), Transmit Single-frame Synchronization Signal (TxSync_n) and Transmit Multi-frame Synchronization Signal (TxMSync_n) are all outputs.

With the timing source of the transmit section being the Transmit Serial Input Clock, the Transmit Serial Clock (TxSerClk_n), Transmit Single-frame Synchronization Signal (TxSync_n) and Transmit Multi-frame Synchronization Signal (TxMSync_n) are all inputs.

The following table illustrates the input and output nature of these signals for different Transmit timing sources.

TABLE 36: SIGNALS FOR DIFFERENT TRANSMIT TIMING SOURCES

TRANSMIT TIMING SOURCE	TXSERCLK_N	TXSYNC_N	TXMSYNC_N
Terminal Equipment Driven TxSerClk	Input	Input	Input
OSCCLK Driven Divided Clock	Output	Output	Output
Recovered Receive Line Clock	Output	Output	Output

The Transmit Time-slot Indication Bits (TxTSb[4:0]_n) are multiplexed I/O pins. The functionality of these pins is governed by the value of Transmit Fractional T1 Input Enable bit of the Transmit Interface Control Register (TICR).

The following table illustrates the configurations of the Transmit Fractional DS1 Input Enable bit.

TRANSMIT INTERFACE CONTROL REGISTER (TICR) (INDIRECT ADDRESS = 0xn0H, 0x20H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Transmit Fractional DS1 Input Enable	R/W	0 - The Transmit Time-slot Indication bits (TxTSb[4:0] are outputting five-bit binary values of Time-slot number (0-23) being accepted and processed by the Transmit Payload Data Input Interface block of the framer. The Transmit Time-slot Indicator Clock signal (TxTSClk_n) is a 192KHz clock that pulses HIGH for one DS1 bit period whenever the Transmit Payload Data Input Interface block is accepting the LSB of each of the twenty-four time slots. 1 - The TxTSb[0]_n bit becomes the Transmit Fractional T1 Input signal (TxFrTD_n) which carries Fractional DS1 payload data into the framer. The TxTSb[1]_n bit becomes the Transmit Signaling Data Input signal (TxSig_n) which is used to insert robbed-bit signaling data into the outbound DS1 frame. The TxTSb[2]_n bit serially outputs all five-bit binary values of the Time Slot number (0-23) being accepted and processed by the Transmit Payload Data Input Interface block of the framer. The TxTSb[3]_n bit becomes the Transmit Overhead Synchronization Pulse (TxOHSync_n) which is used to output an Overhead Synchronization Pulse that indicates the first bit of each DS1multi-frame. The TxTSClk_n will output gaped fractional DS1 clock that can be used by Terminal Equipment to clock out Fractional DS1 payload data at rising edge of the clock. Or,The TxTSClk_n pin will be a clock enable signal to Transmit Fractional DS1 Input signal (TxFrTD_n) when the un-gaped Transmit Serail Input Clock (TxSerClk_n) is used to clock in Fractional DS1 Payload Data into the framer.

When configured to operate in normal condition (that is, when the Transmit Fractional T1 Input Enable bit is equal to zero), these bits reflect the five-bit binary value of the Time Slot number (0 - 23) being accepted and processed by the Transmit Payload Data Input Interface block of the framer. TxTSb[4] represents the MSB of the binary value and TxTSb[0] represents the LSB.

When the Transmit Fractional T1 Input Enable bit is equal to one, the TxTSb[0]_n bit becomes the Transmit Fractional T1 Input signal (TxFrTD_n). This input pin carries Fractional T1 Input data to be inserted into the outbound DS1 data stream. The Fraction T1 Input Interface allows certain time-slots of outbound DS1 data stream to have a different source other than the local Terminal Equipment. Function of the Fractional T1 Input signal will be discussed in details in later sections.

When the Transmit Fractional T1 Input Enable bit is equal to one, the TxTSb[1]_n bit becomes the Transmit Signaling Data Input signal (TxSig_n). These input pins can be used to insert robbed-bit signaling data into the outbound DS1 frame. Function of the Transmit Signaling Data Input signal will be discussed in details in later sections.

When the Transmit Fractional T1 Input Enable bit is equal to one, the TxTSb[2]_n bit serially outputs all five-bit binary values of the Time Slot number (0-23) being accepted and processed by the Transmit Payload Data Input Interface block of the framer. MSB of the binary value is presented first and the LSB is presented last.

When the Transmit Fractional T1 Input Enable bit is equal to one, the TxTSb[3]_n bit becomes the Transmit Overhead Synchronization Pulse (TxOHSync_n). These pins can be used to output an Overhead Synchronization Pulse that indicates the first bit of each DS1multi-frame. Function of the Transmit Overhead Synchronization Output signal will be discussed in details in later sections.

The TxTSb[4]_n bit is not multiplexed.

The table below shows functionality of the TxTSb[3:0] bits when the Transmit Fractional T1 Input bit is set to different values.

TABLE 37: THE TXTSB[3:0] BITS WHEN THE TRANSMIT FRACTIONAL T1 INPUT BIT IS SET TO DIFFERENT VALUES

TRANSMIT FRACTIONAL T1 INPUT BIT = 0		TRANSMIT FRACTIONAL T1 INPUT BIT = 1	
TxTSb[0]	Output	TxFrTD	Input
TxTSb[1]	Output	TxSig	Input
TxTSb[2]	Output	TxTS	Output
TxTSb[3]	Output	TxOHSync	Output

The Transmit Time-slot Indicator Clock signal (TxTSClk_n) is a multi-function output pin. When configured to operate in normal condition (that is, when the Transmit Fractional T1 Input Enable bit is equal to zero), the TxTSClk_n is a 192KHz clock that pulses HIGH for one DS1 bit period whenever the Transmit Payload Data Input Interface block is accepting the LSB of each of the twenty-four time slots. The local Terminal Equipment should use this clock signal to sample the TxTSb[0] through TxTSb[4] bits and identify the time-slot being processed via the Transmit Section of the framer.

When the Transmit Fractional T1 Input Enable bit is equal to one, the TxTSClk_n will output gaped fractional DS1 clock at time-slots where Fractional T1 Input data is present. This clock can be used by Terminal Equipment to clock out Fractional DS1 payload data at rising edge of the clock. The framer will then input Fractional DS1 payload data using falling edge of the clock. Otherwise, this pin can be configured as a clock enable signal to Transmit Fractional DS1 Input signal (TxFrTD_n) if the framer is set accordingly. In this way, Fractional DS1 payload data is clocked into the framer using un-gaped Transmit Serail Input Clock (TxSerClk_n). A detailed discussion of the Fractional DS1 Payload Data Input Interface can be found in later sections.

Both the Transmit Time-slot Indicator Clock (TxTSClk_n) and the Transmit Time-slot Indication Bits (TxTSbb[4:0]_n) are output signals in normal 1.544Mbit/s Back-plane mode regardless of the timing source of the Transmit Section of framer.

4.1.2.1 Connect the Transmit Payload Data Input Interface block to the Local Terminal Equipment if Transmit Timing Source = TxSerClk_n

By setting the Transmit Timing Source [1:0] bits of the Clock Select Register to 01, the TxSerClk_n input signal is configured to be the timing source for the Transmit section of the framer. The Terminal Equipment should supply an external free-running clock with frequency of 1.544MHz to the TxSerClk_n input pin. The Transmit Single-frame Synchronization signal and the Transmit Multi-frame Synchronization signal are inputs to the framer.

The Transmit Single-frame Synchronization signal should pulse “High” for one DS1 bit period (648ns) at the Framing bit position of each DS1 frame. By sampling the “High” pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of a DS1 frame.

The Transmit Multi-frame Synchronization signal should pulse HIGH for one DS1 bit period (648ns) at the Framing bit position of the first frame of a DS1 multi-frame. By sampling the HIGH pulse on the Transmit Multi-frame Synchronization signal, the framer can position the beginning of a DS1 super-frame.

It is the responsibility of the Terminal Equipment to provide serial input data through the TxSer_n pin aligned with the Transmit Single-frame Synchronization signal and the Transmit Multi-frame Synchronization signal. See Figure 23 below for how to connect the Transmit Payload Data Input Interface block to the local Terminal Equipment with the Transmit Serial clock being the timing source of transmit section.

FIGURE 23. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT WITH TXSERCLK_N AS TRANSMIT TIMING SOURCE

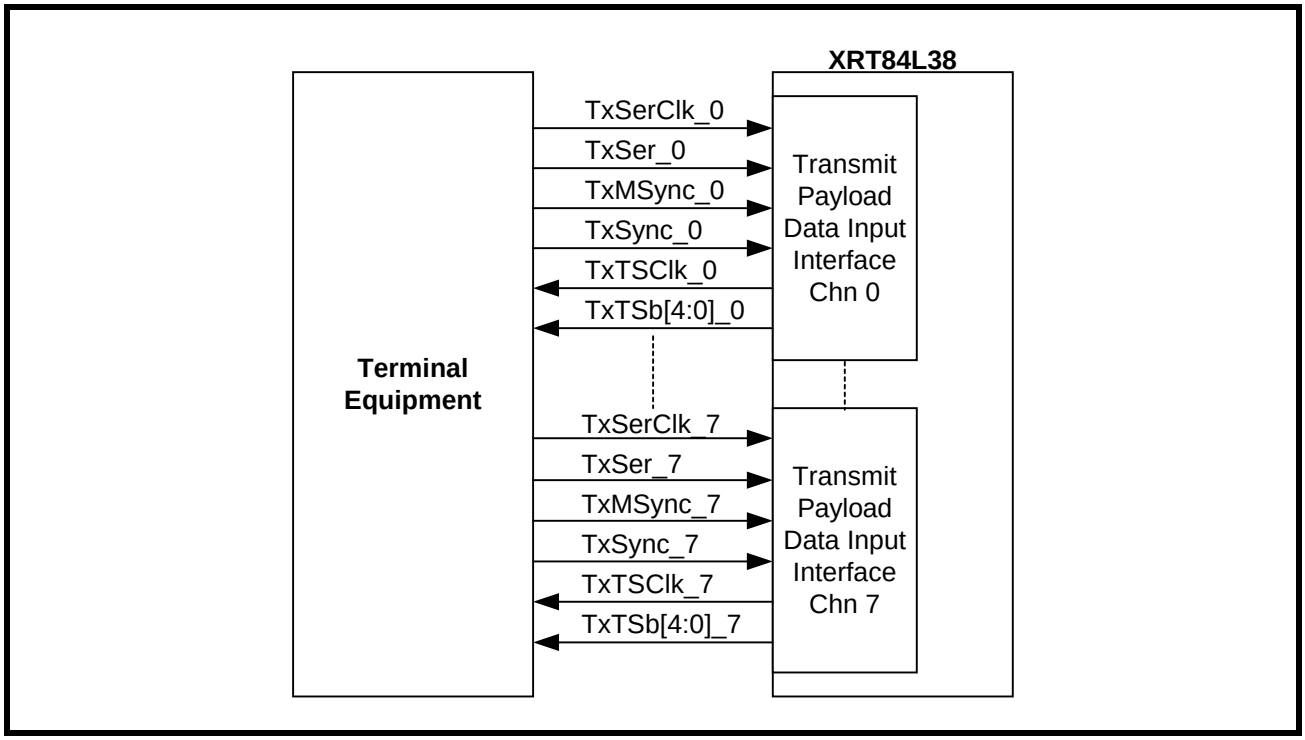
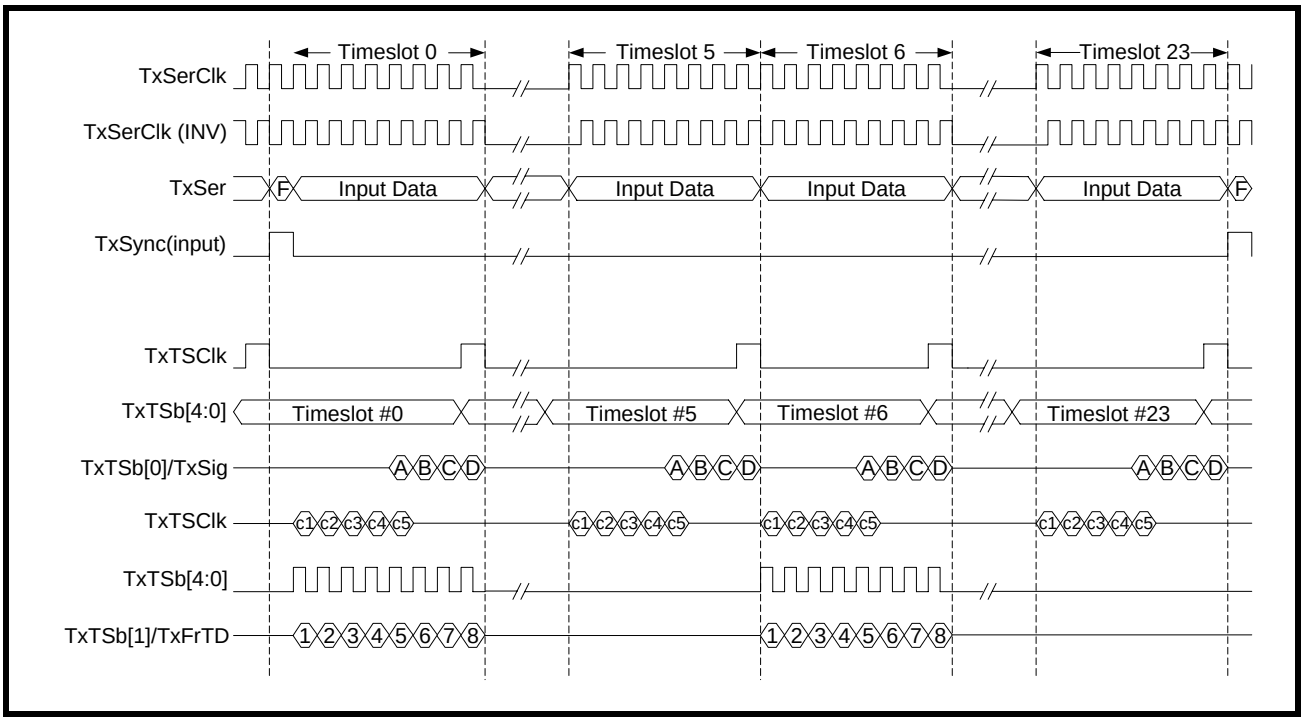


Figure 24 shows waveforms of the signals (TxSerClk_n, TxSer_n, TxSync_n, TxTSClk_n and TxTSb[4:0]_n) that connect the Transmit Payload Data Input Interface block to the local Terminal Equipment with the Transmit Serial clock being the timing source of transmit section.

FIGURE 24. WAVEFORMS OF THE SIGNALS THAT CONNECT THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WITH THE TRANSMIT SERIAL CLOCK BEING THE TIMING SOURCE OF THE TRANSMIT SECTION



4.1.2.2 Connect the Transmit Payload Data Input Interface block to the Local Terminal Equipment if the Transmit Timing Source = OSCCLK

By setting the Transmit Timing Source [1:0] bits of the Clock Select Register (CSR) to 10, the OSCCLK Driven Divided clock is configured to be the timing source for the Transmit section of the framer. A free-running clock should apply to the OSCCLK input pin with frequencies of 12.352MHz, 24.704MHz and 49.408MHz depending on the setting of OSCCLK Frequency Select [1:0] bits of the Clock Select Register (CSR).

The free-running OSCCLK is divided inside the XRT84L38 and routed to all eight framers. This OSCCLK Driven Divided Clock has to be 12.352MHz in frequency. When these bits are set to 00, the framer will internally divide the incoming OSCCLK by one. Therefore, the external oscillator clock applied to the OSCCLK pin should be 12.352MHz. When these bits are set to 01, the framer will internally divide the incoming OSCCLK by two. Therefore, the external oscillator clock applied to the OSCCLK pin should be 24.704MHz. When these bits are set to 10, the framer will internally divide the incoming OSCCLK by four. Therefore, the external oscillator clock applied to the OSCCLK pin should be 49.408MHz.

The following table shows configurations of the OSCCLK Frequency Select [1:0] bits of the Clock Select Register.

CLOCK SELECT REGISTER (CSR) (INDIRECT ADDRESS = 0xn0H, 0x00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	OSCCLK Frequency Select	R/W	**OSCCLK Frequency Select:** These two READ/WRITE bit-fields permit the user to select internal clock dividing logic of the framer depending on the frequency of incoming oscillator clock (OSCCLK). The frequency of internal clock used by the framer should be 12.352MHz. 00 - The framer will internally divide the incoming OSCCLK by one. Therefore, the external oscillator clock applied to the OSCCLK pin should be 12.352MHz. 01 - The framer will internally divide the incoming OSCCLK by two. Therefore, the external oscillator clock applied to the OSCCLK pin should be 24.704MHz. 10 - The framer will internally divide the incoming OSCCLK by four. Therefore, the external oscillator clock applied to the OSCCLK pin should be 49.408MHz.

The Transmit Serial clock signal pin (TxSerClk_n) is output from the framer. The framer outputs a 1.544MHz clock through this pin to the local Terminal Equipment. The Transmit Single-frame Synchronization signal and the Transmit Multi-frame Synchronization signal are also automatically configured to be output signals.

The Transmit Single-frame Synchronization signal should pulse HIGH for one DS1 bit period (648ns) at the last bit position of each DS1 frame. By triggering on the HIGH pulse on the Transmit Single-frame Synchronization signal, the local Terminal Equipment can identify the end of a DS1 frame and should start inserting payload data of the next DS1 frame to the framer.

The Transmit Multi-frame Synchronization signal should pulse HIGH for one DS1 bit period (648ns) at the last bit position of the last frame of a DS1 multi-frame. By triggering on the HIGH pulse on the Transmit Multi-frame Synchronization signal, the local Terminal Equipment can identify the end of a DS1 super-frame and should start inserting payload data of the next DS1 multi-frame into the framer.

See Figure 25 for how to connect the Transmit Payload Data Input Interface block to the local Terminal Equipment with the OSCCLK Driven Divided clock as the timing source of transmit section.

FIGURE 25. INTERFACING XRT84L38 TO THE LOCAL TERMINAL EQUIPMENT WITH THE OSCCLK DRIVEN DIVIDED CLOCK AS TRANSMIT TIMING SOURCE

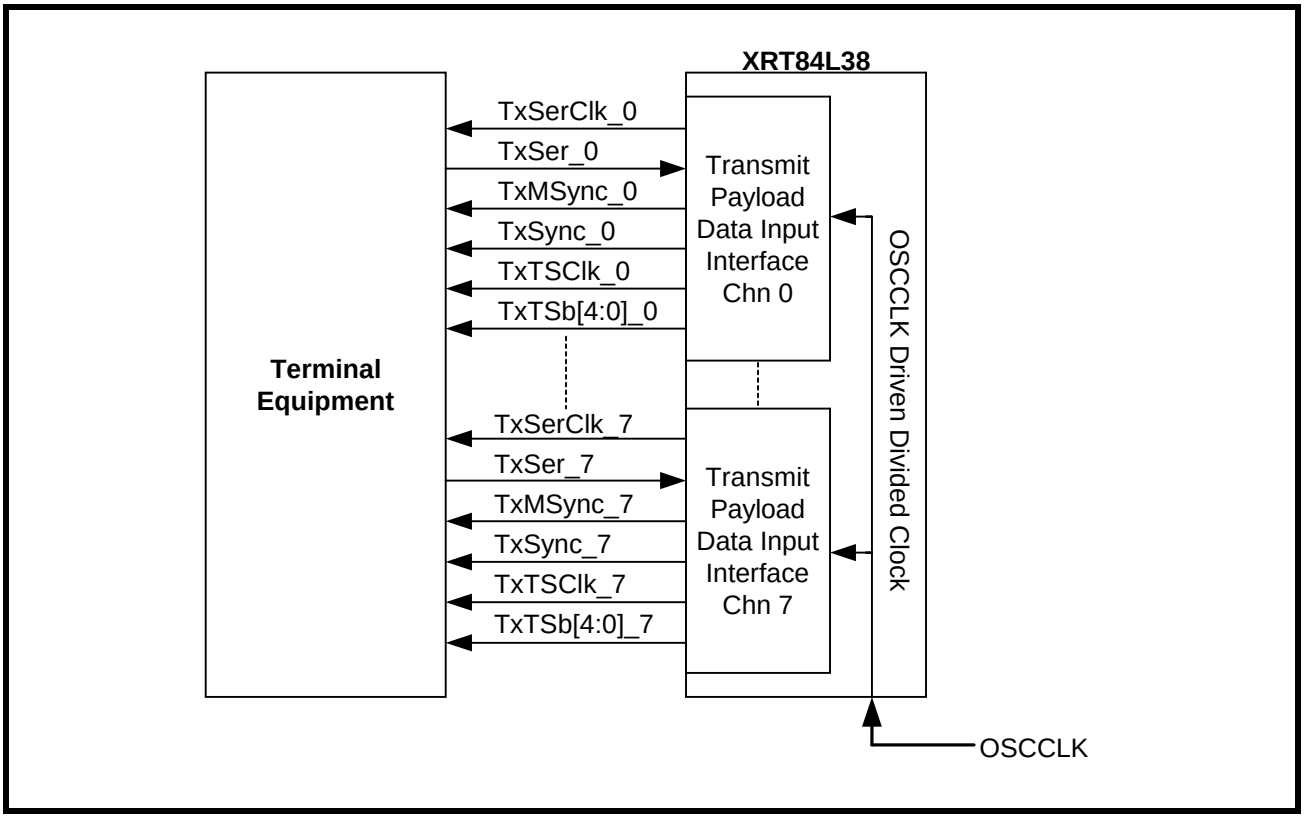
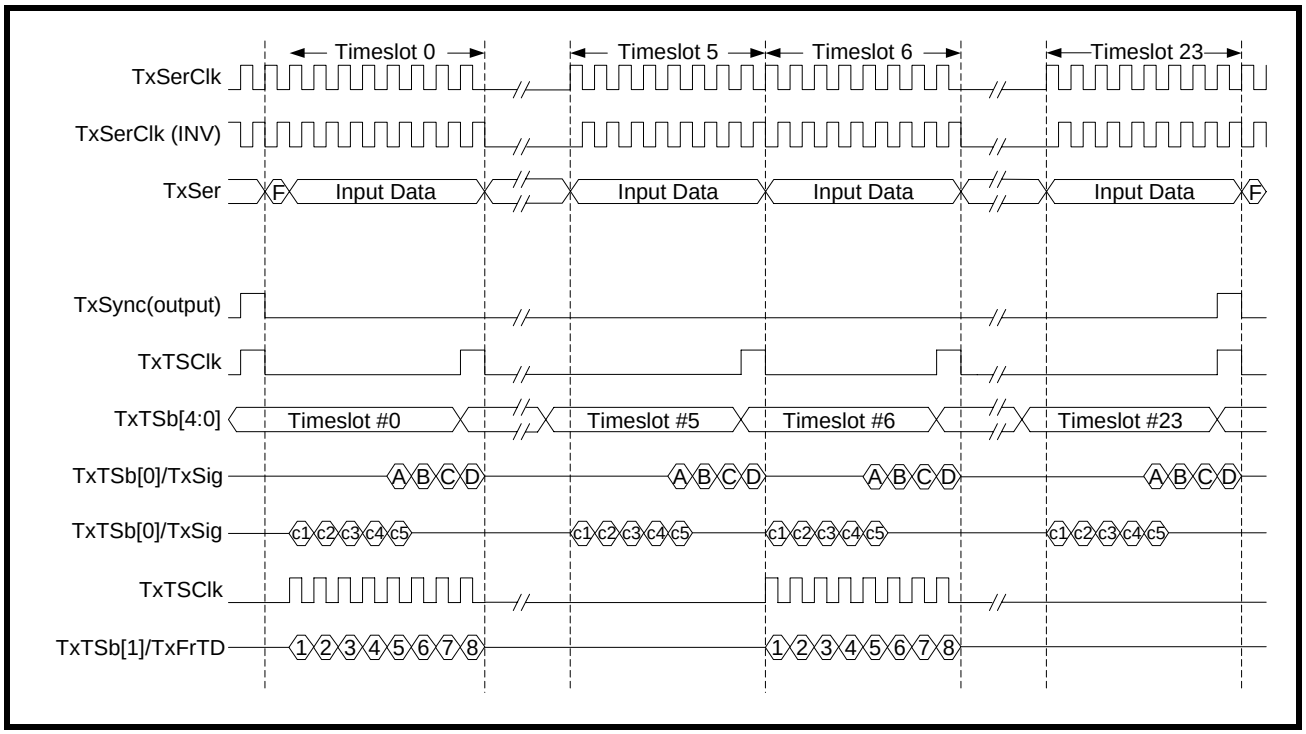


Figure 26 shows waveforms of the signals (TxSerClk_n, TxSer_n, TxSync_n, TxTSClk_n and TxTSb[4:0]_n) that connect the Transmit Payload Data Input Interface block to the local Terminal Equipment with the OSCCLK Driven Divided clock as the timing source of transmit section.

FIGURE 26. WAVEFORMS OF THE SIGNALS CONNECTING THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WITH THE OSCCLK DRIVEN DIVIDED CLOCK AS THE TIMING SOURCE OF THE TRANSMIT SECTION



4.1.2.3 Connect the Transmit Payload Data Input Interface block to the Local Terminal Equipment for Loop-timing applications

If the Transmit Timing Source [1:0] bits of the Clock Select Register are set to 00 or 11, the Recovered Receive Line Clock is configured to be the timing source for the Transmit section of the framer. This is also known as the Loop-timing mode.

If the Clock Loss Detection Enable bit of the Clock Select Register is set to one, and if the Recovered Receive Line Clock from the LIU is lost, the framer will automatically begin to use the OSCCLK Driven Divided clock as transmit timing source until the LIU is able to regain clock recovery.

The following table shows configuration of the Clock Loss Detection Enable bit of the Clock Select Register (CSR).

CLOCK SELECT REGISTER (CSR) (INDIRECT ADDRESS = 0xn0H, 0x00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Clock Loss Detection Enable	R/W	**Clock Loss Detection Enable:** This READ/WRITE bit-field permits the user to enable the Clock Loss Detection logic for the framer when the Recovered Receive Line Clock is used as transmit timing source of the framer. 0 - The framer disables the Clock Loss Detection logic. 1 - The framer enables the Clock Loss Detection logic. If the Recovered Receive Line Clock is used as transmit timing source of the framer, and if clock recovered from the LIU is lost, the framer can detect loss of the Recovered Receive Line Clock. Upon detecting of this occurrence, the framer will automatically begin to use the OSCCLK Driven Divided clock as transmit timing source until the LIU is able to regain clock recovery. ***NOTE:*** *This bit-field is ignored if the TxSerClk or the OSCCLK Driven Divided Clock is chosen to be the timing source of Transmit Section of the framer.*

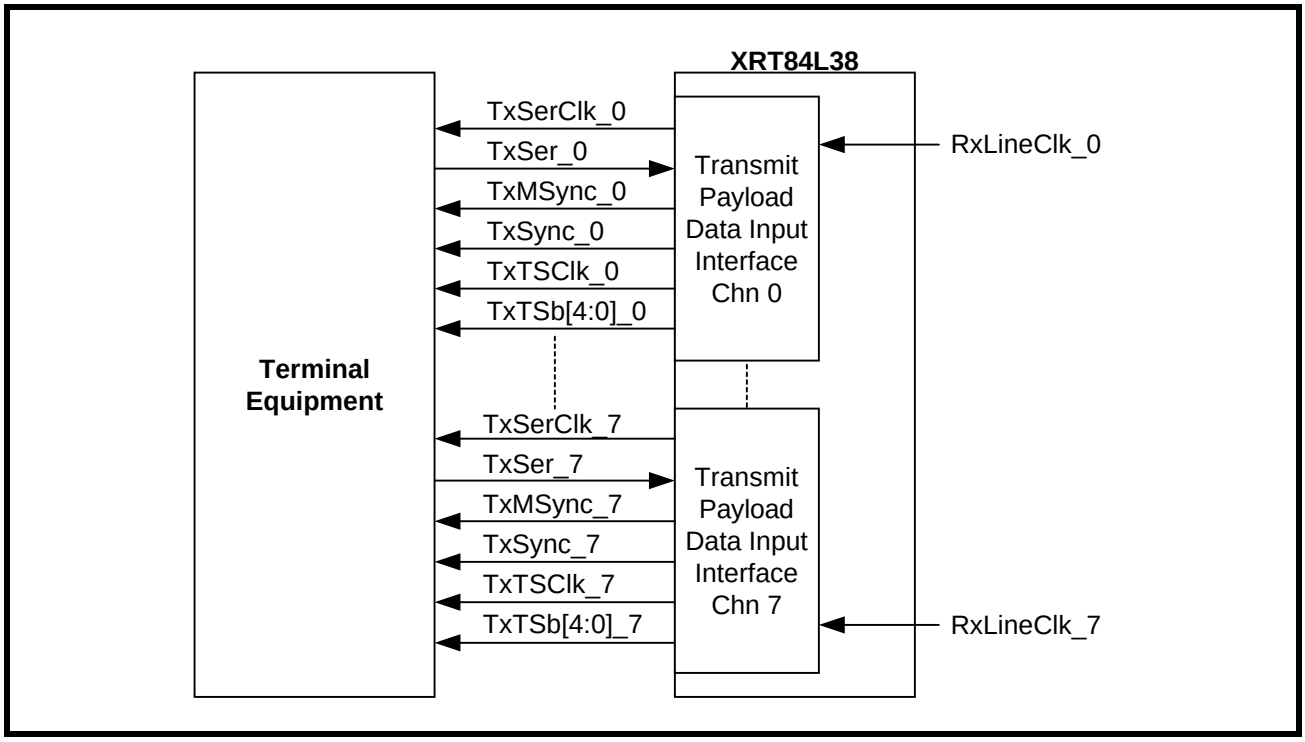
The Transmit Serial Clock signal pin (TxSerClk_n) is output from the framer. The XRT84L38 routes the Recovered Receive Line Clock internally across the framer and output through the Transmit Serial Clock signal pin to the local Terminal Equipment. The Transmit Single-frame Synchronization signal and the Transmit Multi-frame Synchronization signal are automatically configured to be output signals.

The Transmit Single-frame Synchronization signal should pulse HIGH for one DS1 bit period (648ns) at the last bit position of each DS1 frame. By triggering on the HIGH pulse on the Transmit Single-frame Synchronization signal, the local Terminal Equipment can identify the end of a DS1 frame and should start inserting payload data of the next DS1 frame to the framer.

The Transmit Multi-frame Synchronization signal should pulse HIGH for one DS1 bit period (648ns) at the last bit position of the last frame of a DS1 multi-frame. By triggering on the HIGH pulse on the Transmit Multi-frame Synchronization signal, the local Terminal Equipment can identify the end of a DS1 super-frame and should start inserting payload data of the next DS1 multi-frame into the framer.

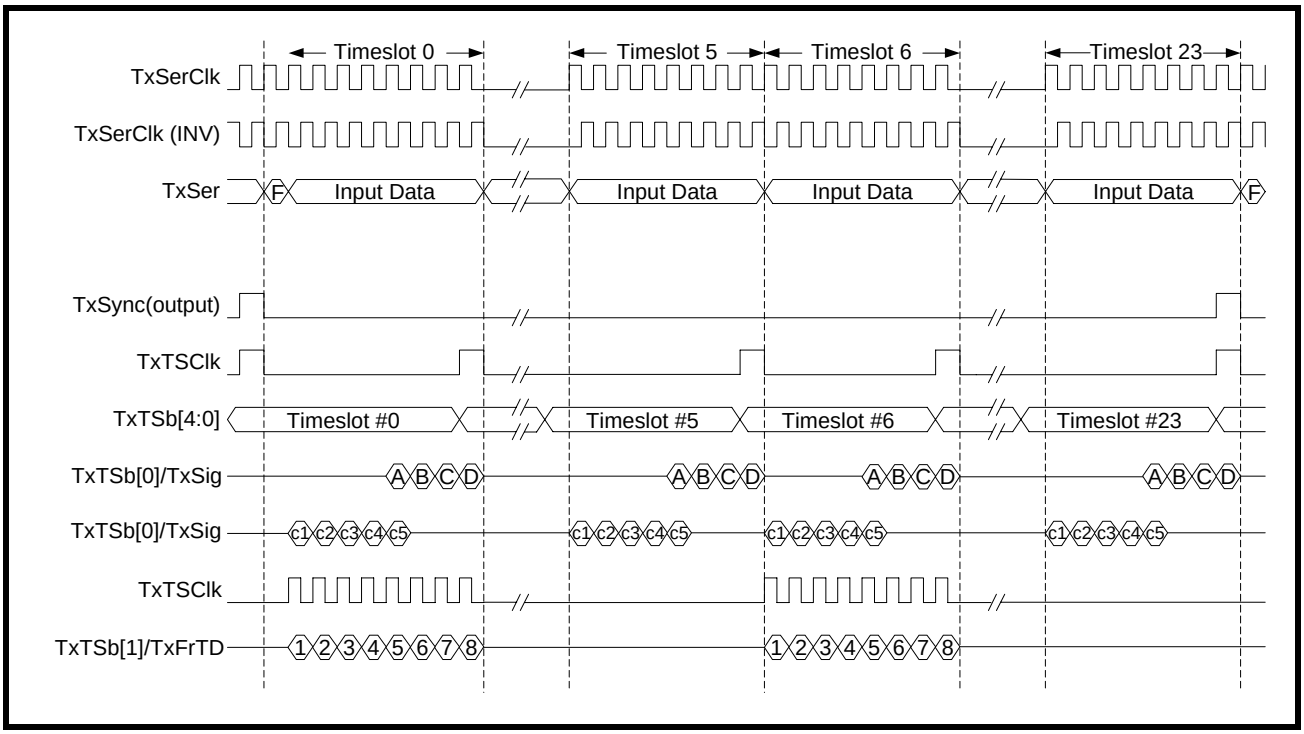
See Figure 27 for how to connect the Transmit Payload Data Input Interface block to the local Terminal Equipment with the Recovered Receive Line Clock being the timing source of transmit section.

FIGURE 27. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT WITH RECOVERED RECEIVE LINE CLOCK AS TRANSMIT TIMING SOURCE



The following Figure 28 shows waveforms of the signals (TxSerClk_n, TxSer_n, TxSync_n, TxTSClk_n and TxTSb[4:0]_n) that connecting the Transmit Payload Data Input Interface block to the local Terminal Equipment with the Recovered Receive Line Clock being the timing source of transmit section.

FIGURE 28. WAVEFORMS OF THE SIGNALS CONNECTING THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WITH THE RECOVERED RECEIVE LINE CLOCK BEING THE TIMING SOURCE OF THE TRANSMIT SECTION



4.1.3 Brief Discussion of the Transmit High-Speed Back-Plane Interface

The High-speed Back-plane Interface supports payload data to be taken from or presented to the Terminal Equipment at a rate higher than 1.544Mbit/s. In DS1 mode, supported High-speed data rates are MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 12.352Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s. The Transmit Multiplex Enable bit and the Transmit Interface Mode Select [1:0] bits of the Transmit Interface Control Register (TICR) determine the Transmit Back-plane Interface data rate.

The following table shows configurations of the Transmit Multiplex Enable bit and the Transmit Interface Mode Select [1:0] bits of the Transmit Interface Control Register (TICR).

TRANSMIT INTERFACE CONTROL REGISTER (TICR) (INDIRECT ADDRESS = 0xn0H, 0x20H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Transmit Multiplex Enable	R/W	0 - The Transmit Back-plane Interface block is configured to non-channel-multiplexed mode. 1 - The Transmit Back-plane Interface block is configured to channel-multiplexed mode
1-0	Transmit Interface Mode Select	R/W	When combined with the Transmit Multiplex Enable bit, these bits determine the Transmit Back-plane Interface data rate.

The table below shows the combinations of Transmit Multiplex Enable bit and Transmit Interface Mode Select [1:0] bits and the resulting Transmit Back-plane Interface data rates.

TABLE 38: TRANSMIT MULTIPLEX ENABLE BIT AND TRANSMIT INTERFACE MODE SELECT [1:0] BITS WITH THE RESULTING TRANSMIT BACK-PLANE INTERFACE DATA RATES

TRANSMIT MULTIPLEX ENABLE BIT	TRANSMIT INTERFACE MODE SELECT BIT 1	TRANSMIT INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE
0	0	0	1.544Mbit/s
0	0	1	MVIP 2.048Mbit/s
0	1	0	4.096Mbit/s
0	1	1	8.192Mbit/s
1	0	0	Multiplexed 12.352Mbit/s
1	0	1	Bit Multiplexed 16.384Mbit/s
1	1	0	HMVIP 16.384Mbit/s
1	1	1	H.100 16.384Mbit/s

When the Transmit Multiplex Enable bit is set to zero, the framer is configured in non-channel-multiplexed mode. The possible data rates are 1.544Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s and 8.192Mbit/s. In non-channel-multiplexed mode, payload data of each channel are taken from the Terminal Equipment separately. Each channel uses its own Transmit Serial Clock, Transmit Serial Data, Transmit Single-frame Synchronization signal and Transmit Multi-frame Synchronization signal as interface between the framer and the Terminal Equipment. Section 4.1.2.1, 4.1.2.2 and 4.1.2.3 provide details on how to connect the Transmit Payload Data Interface block with the Terminal Equipment when the Back-plane interface data rate is 1.544Mbit/s.

When the Back-plane interface data rate is MVIP 2.048Mbit/s, 4.096Mbit/s and 8.192Mbit/s, the Transmit Serial Clock, Transmit Serial Data, Transmit Single-frame Synchronization signal and Transmit Multi-frame Synchronization signal are all configured as inputs. The Transmit Serial Clock is always an input clock with frequency of 1.544 MHz for all data rates. The TxMSync_n signal is configured as the Transmit Input Clock with frequencies of 2.048 MHz, 4.096 MHz and 8.192 MHz respectively. It serves as the primary clock source for the High-speed Back-plane Interface.

The table below summaries the clock frequencies of TxSerClk_n and TxInClk_n inputs when the framer is operating in non-multiplexed High-speed Back-plane mode.

TRANSMIT MULTIPLEX ENABLE BIT = 0

TRANSMIT INTERFACE MODE SELECT BIT 1	TRANSMIT INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE	TXSERCLK	TXMSYNC/TXINCLK
0	0	1.544Mbit/s	1.544 MHz	-
0	1	MVIP 2.048Mbit/s	1.544 MHz	2.048 MHz
1	0	4.096Mbit/s	1.544 MHz	4.096 MHz
1	1	8.192Mbit/s	1.544 MHz	8.192 MHz

When the Transmit Multiplex Enable bit is set to one, the framer is configured in channel-multiplexed mode. The possible data rates are multiplexed 12.352Mbit/s, bit-multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s and H.100 16.384Mbit/s. In channel-multiplexed mode, every four channels share the Transmit Serial Data and Transmit Single-frame Synchronization signal of one channel as interface between the framer and the local Terminal Equipment. The TxMSync_n signal of one channel is configured as the Transmit Input Clock with frequencies of 12.352 MHz or 16.384. It serves as the primary clock source for the High-speed Back-plane Interface.

Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4. The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH at the beginning of the frame with data from Channel 0-3 multiplexed together. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH at the beginning of the frame with data from Channel 4-7 multiplexed together. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse. Additionally, each channel requires the local Terminal Equipment to provide a free-running 1.544 MHz clock into the Transmit Serial Clock input.

The table below summaries the clock frequencies of TxSerClk_n and TxInClk_n inputs when the framer is operating in multiplexed High-speed Back-plane mode.

TRANSMIT MULTIPLEX ENABLE BIT = 1

TRANSMIT INTERFACE MODE SELECT BIT 1	TRANSMIT INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE	TXSERCLK	TXMSYNC/TXINCLK
0	0	Multiplexed 12.352Mbit/s	1.544 MHz	12.352 MHz
0	1	Bit-multiplexed 16.384Mbit/s	1.544 MHz	16.384 MHz
1	0	HMVIP 16.384Mbit/s	1.544 MHz	16.384 MHz
1	1	H.100 16.384Mbit/s	1.544 MHz	16.384 MHz

The Transmit Serial Clock is always running at 1.544MHz for all the High-speed Back-plane Interface modes. It is automatically the timing source of the Transmit Section of the framer in High-speed Back-plane Interface mode.

The Transmit Single-frame Synchronization signal should pulse HIGH or LOW for one bit period at the Framing bit position of each DS1 frame. Length of the bit period depends on data rate of the High-speed Back-plane Interface. The Transmit Synchronization Pulse Low bit of the Transmit Interface Control Register (TICR) determines whether the Transmit Single-frame Synchronization signal is HIGH active or LOW active.

The table below shows configurations of the Transmit Synchronization Pulse LOW bit of the Transmit Interface Control Register (TICR).

TRANSMIT INTERFACE CONTROL REGISTER (TICR) (INDIRECT ADDRESS = 0xn0H, 0x20H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Transmit Synchronization Pulse LOW	R/W	0 - The Transmit Single-frame Synchronization signal will pulse HIGH indicating the beginning of a DS1 frame when the High-speed Back-plane Interface is running at a mode other than the 1.544Mbit/s. 1 - The Transmit Single-frame Synchronization signal will pulse LOW indicating the beginning of a DS1 frame when the High-speed Back-plane Interface is running at a mode other than the 1.544Mbit/s.

Throughout the discussion of this datasheet, we assume that the Transmit Single-frame Synchronization signal pulses HIGH unless stated otherwise.

The TxMSync_n signal, which is a multiplexed I/O pin, no longer functions as the Transmit Multi-frame Synchronization Signal. Indeed, it becomes the Transmit Input Clock signal (TxInClk) of the High-speed Back-plane Interface of the framer. The local Terminal Equipment should provide a free-running clock with the same frequency as the High-speed Back-plane Interface to this input pin.

The following sections discuss details of how to operate the framer in different Back-plane interface speed mode and how to connect the Transmit Payload Data Input Interface block to the local Terminal Equipment.

4.1.3.1 T1 Transmit Input Interface - MVIP 2.048 MHz

When the Transmit Multiplex Enable bit is set to zero and the Transmit Interface Mode Select [1:0] bits are set to 01, the Transmit Back-plane interface of framer is running at a data rate of 2.048Mbit/s.

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane interface is accepting data through TxSer_n at an E1 equivalent data rate of 2.048Mbit/s. The local Terminal Equipment supplies a free-running 2.048MHz clock to the Transmit Input Clock pin of the framer. The local Terminal Equipment also provides synchronized payload data at rising edge of the clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the Transmit Input Clock. The local Terminal Equipment should pump in data grouped in 256-bit frame 8000 times every second. Each frame consists of thirty-two octets as in E1. The local Terminal Equipment maps a 193-bit T1 frame into this 256-bit format as described below:

1. The Framing (F-bit) is mapped into MSB of the first E1 Time-slot. The local Terminal Equipment will stuff the rest seven bits of the first octet with "don't care" bits that would be ignored by the framer.
2. Payload data of T1 Time-slot 0, 1 and 2 are mapped into E1 Time-slot 1, 2 and 3.
3. The local Terminal Equipment will stuff E1 Time-slot 4 with eight "don't care" bits that would be ignored by the framer.
4. Following the same rules of Step 2 and 3, the local Terminal Equipment maps every three time-slots of T1 payload data into four E1 time-slots.

The mapping of T1 frame into E1 framing format is shown in the table below.

TABLE 39: THE MAPPING OF T1 FRAME INTO E1 FRAMING FORMAT

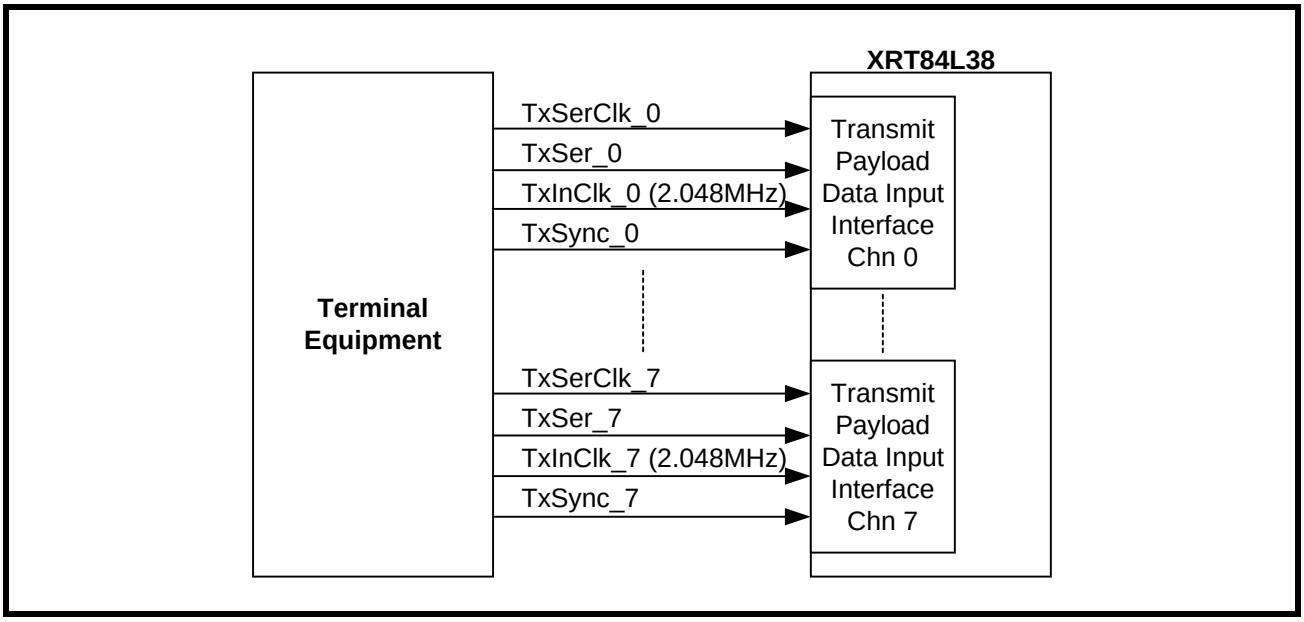
T1	F-Bit	TS0	TS1	TS2	Don't Care Bits	TS3	TS4	TS5
E1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7
T1	Don't Care Bits	TS6	TS7	TS8	Don't Care Bits	TS9	TS10	TS11
E1	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15
T1	Don't Care Bits	TS12	TS13	TS14	Don't Care Bits	TS15	TS16	TS17
E1	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23
T1	Don't Care Bits	TS18	TS19	TS20	Don't Care Bits	TS21	TS22	TS23
E1	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31

The Transmit Single-frame Synchronization input signal (TxSync_n) should pulse HIGH at the beginning (F-bit position) of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of a DS1 frame. It is responsibility of the local Terminal Equipment to align the Transmit Single-frame Synchronization signal with serial data stream going into the framer.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are then processed by the framer and send to LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

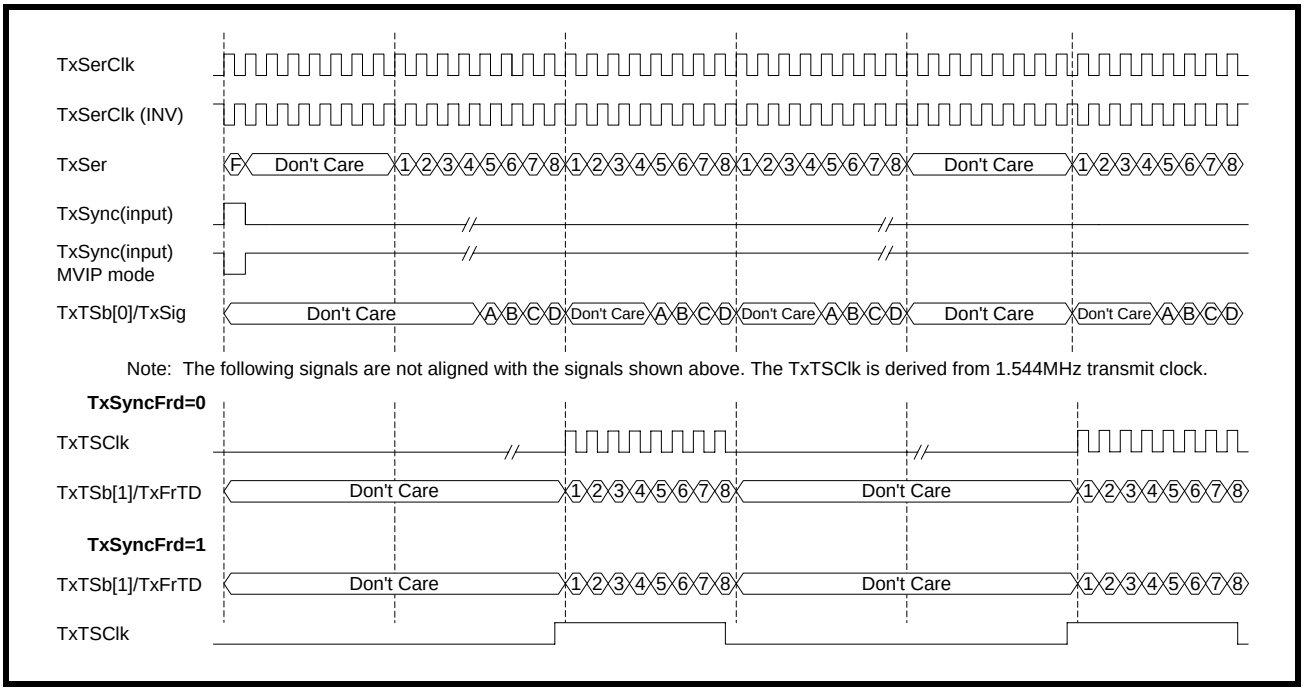
See Figure 29 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in MVIP 2.048Mbit/s mode.

FIGURE 29. INTERFACING XRT84L38 TO THE LOCAL TERMINAL EQUIPMENT USING MVIP 2.048MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at MVIP 2.048Mbit/s mode is shown in Figure 30.

FIGURE 30. TIMING DIAGRAM OF THE INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT MVIP 2.048MBIT/S MODE



4.1.3.2 T1 Transmit Input Interface - 4.096 MHz

This interface mode is the same as running at 2.048 MHz. The only difference is that the Transmit Input Clock runs two times faster at 4.096 MHz.

When the Transmit Multiplex Enable bit is set to zero and the Transmit Interface Mode Select [1:0] bits are set to 10, the Transmit Back-plane interface of framer is running at a clock rate of 4.096MHz.

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane interface is still accepting data through TxSer_n at an E1 equivalent data rate of 2.048Mbit/s. However, the local Terminal Equipment supplies a free-running 4.096MHz clock to the Transmit Input Clock pin of the framer. The local Terminal Equipment provides synchronized payload data at every other rising edge of the Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches in-coming serial data at every other falling edge of the clock. The local Terminal Equipment should pump in data grouped in 256-bit frame 8000 times every second. Each frame consists of thirty-two octets as in E1. The local Terminal Equipment maps a 193-bit T1 frame into this 256-bit format as described below:

1. The Framing (F-bit) is mapped into MSB of the first E1 Time-slot. The local Terminal Equipment will stuff the rest seven bits of the first octet with "don't care" bits that would be ignored by the framer.
2. Payload data of T1 Time-slot 0, 1 and 2 are mapped into E1 Time-slot 1, 2 and 3.
3. The local Terminal Equipment will stuff E1 Time-slot 4 with eight "don't care" bits that would be ignored by the framer.
4. Following the same rules of Step 2 and 3, the local Terminal Equipment maps every three time-slots of T1 payload data into four E1 time-slots.

The mapping of T1 frame into E1 framing format is shown in the table below.

TABLE 40: THE MAPPING OF T1 FRAME INTO E1 FRAMING FORMAT

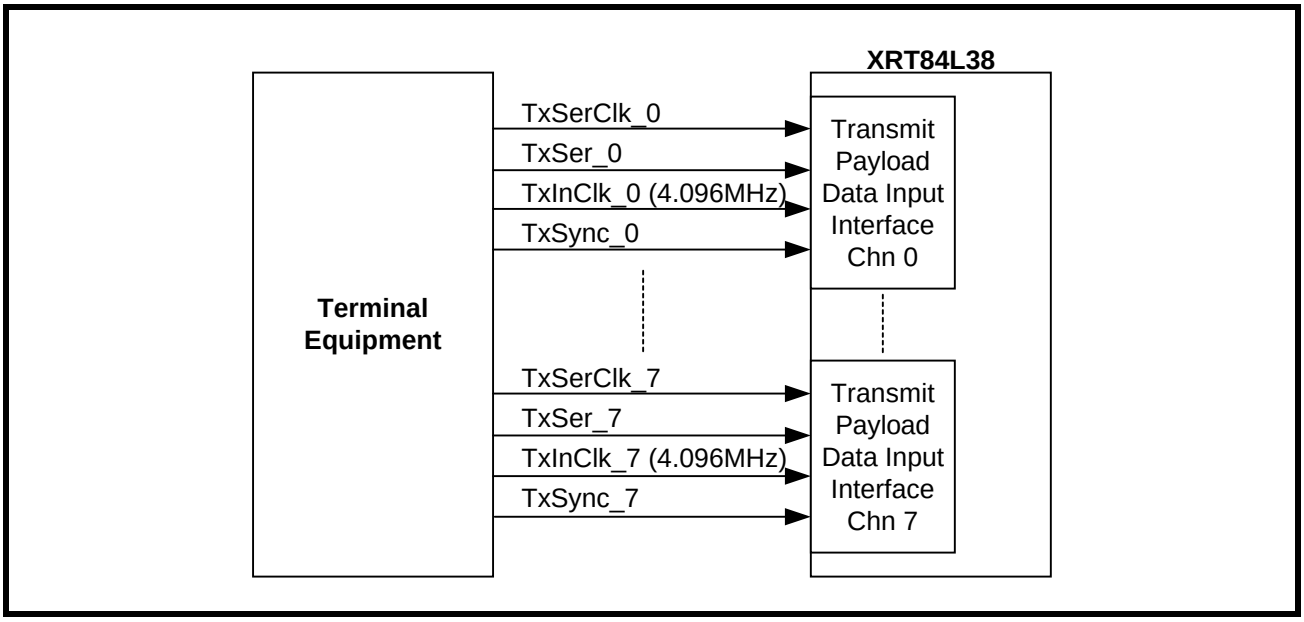
T1	F-BIT	TS0	TS1	TS2	DON'T CARE BITS	TS3	TS4	TS5
E1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7
T1	Don't Care Bits	TS6	TS7	TS8	Don't Care Bits	TS9	TS10	TS11
E1	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15
T1	Don't Care Bits	TS12	TS13	TS14	Don't Care Bits	TS15	TS16	TS17
E1	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23
T1	Don't Care Bits	TS18	TS19	TS20	Don't Care Bits	TS21	TS22	TS23
E1	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31

The Transmit Single-frame Synchronization input signal (TxSync_n) should pulse HIGH at the beginning (F-bit position) of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of a DS1 frame. It is responsibility of the local Terminal Equipment to align the Transmit Single-frame Synchronization signal with serial data stream going into the framer.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are then processed by the framer and send to LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

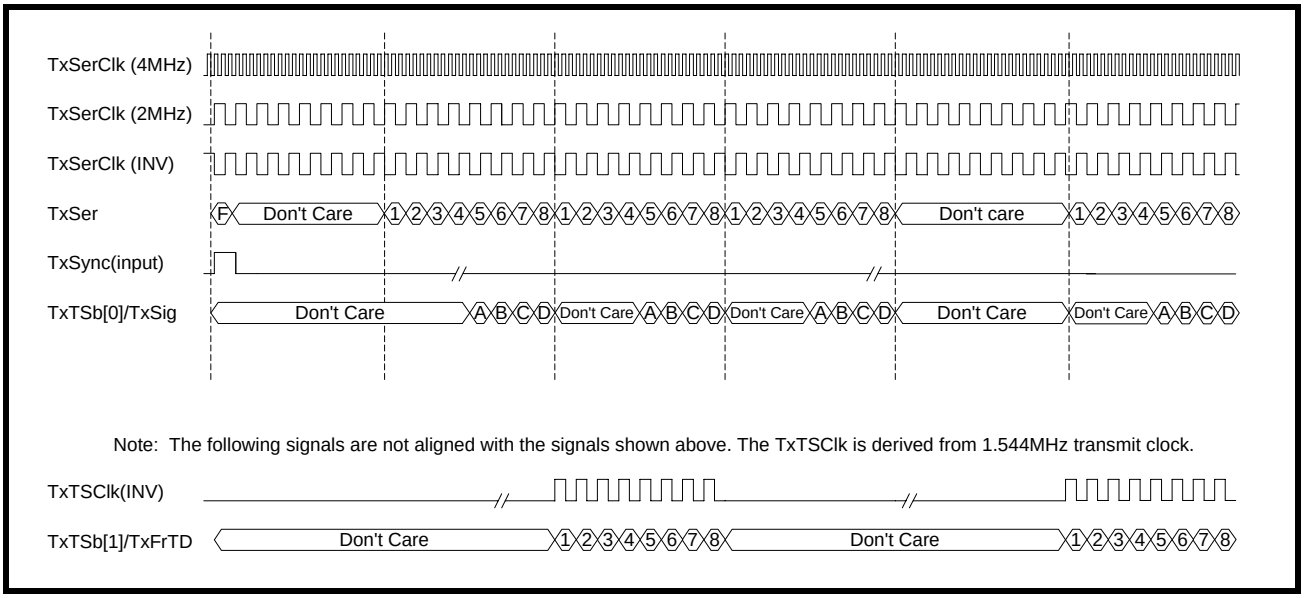
See Figure 31 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in MVIP 4.096Mbit/s mode.

FIGURE 31. INTERFACING XRT84L38 TO THE LOCAL TERMINAL EQUIPMENT USING 4.096MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at 4.096Mbit/s mode is shown in Figure 32

FIGURE 32. TIMING DIAGRAM OF THE INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 4.096MBIT/S MODE



4.1.3.3 T1 Transmit Input Interface - 8.192 MHz

This interface mode is the same as running at 2.048 MHz. The only difference is that the Transmit Input Clock runs four times faster at 8.192MHz.

When the Transmit Multiplex Enable bit is set to zero and the Transmit Interface Mode Select [1:0] bits are set to 11, the Transmit Back-plane interface of framer is running at a clock rate of 8.192MHz.

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane interface is still accepting data through TxSer_n at an E1 equivalent data rate of 2.048Mbit/s. However, the local Terminal Equipment supplies a free-running 8.192MHz clock to the Transmit Input Clock pin of the framer. The local Terminal Equipment provides synchronized payload data at every other four rising edge of the Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at every other four falling edge of the clock. The local Terminal Equipment should pump in data grouped in 256-bit frame 8000 times every second. Each frame consists of thirty-two octets as in E1. The local Terminal Equipment maps a 193-bit T1 frame into this 256-bit format as described below:

1. The Framing (F-bit) is mapped into MSB of the first E1 Time-slot. The local Terminal Equipment will stuff the rest seven bits of the first octet with "don't care" bits that would be ignored by the framer.
2. Payload data of T1 Time-slot 0, 1 and 2 are mapped into E1 Time-slot 1, 2 and 3.
3. The local Terminal Equipment will stuff E1 Time-slot 4 with eight "don't care" bits that would be ignored by the framer.
4. Following the same rules of Step 2 and 3, the local Terminal Equipment maps every three time-slots of T1 payload data into four E1 time-slots.

The mapping of T1 frame into E1 framing format is shown in the table below.

TABLE 41: THE MAPPING OF T1 FRAME INTO E1 FRAMING FORMAT

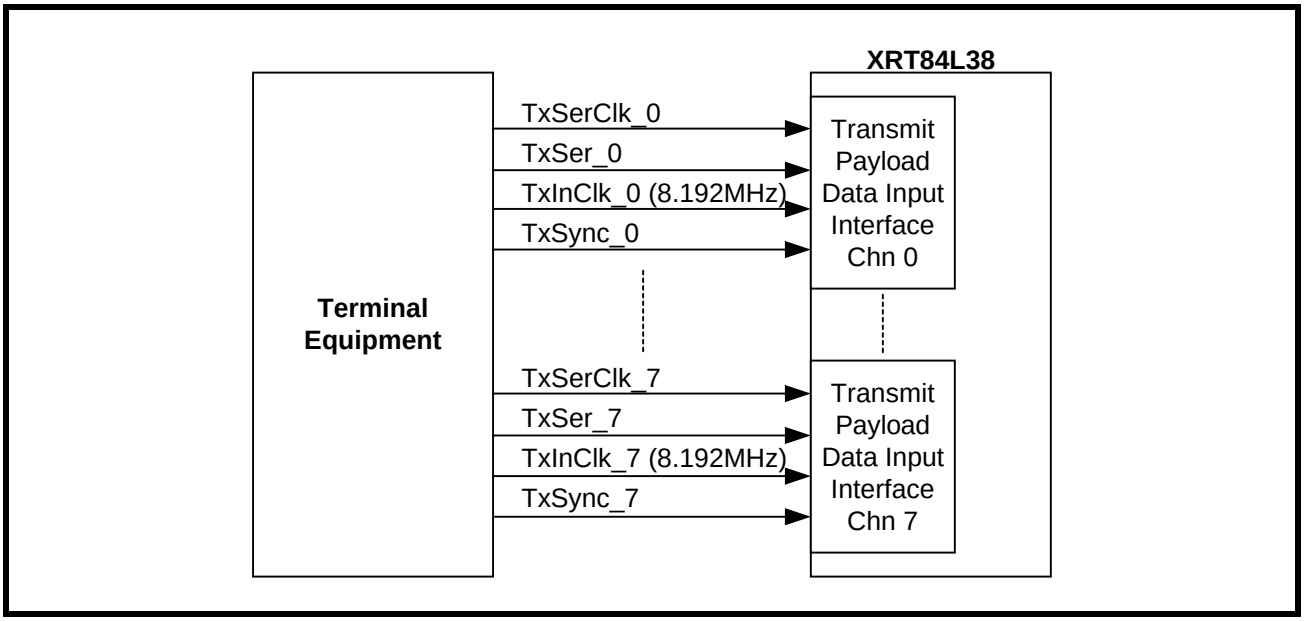
T1	F-Bit	TS0	TS1	TS2	Don't Care Bits	TS3	TS4	TS5
E1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7
T1	Don't Care Bits	TS6	TS7	TS8	Don't Care Bits	TS9	TS10	TS11
E1	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15
T1	Don't Care Bits	TS12	TS13	TS14	Don't Care Bits	TS15	TS16	TS17
E1	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23
T1	Don't Care Bits	TS18	TS19	TS20	Don't Care Bits	TS21	TS22	TS23
E1	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31

The Transmit Single-frame Synchronization input signal (TxSync_n) should pulse HIGH at the beginning (F-bit position) of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of a DS1 frame. It is responsibility of the local Terminal Equipment to align the Transmit Single-frame Synchronization signal with serial data stream going into the framer.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are then processed by the framer and send to LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

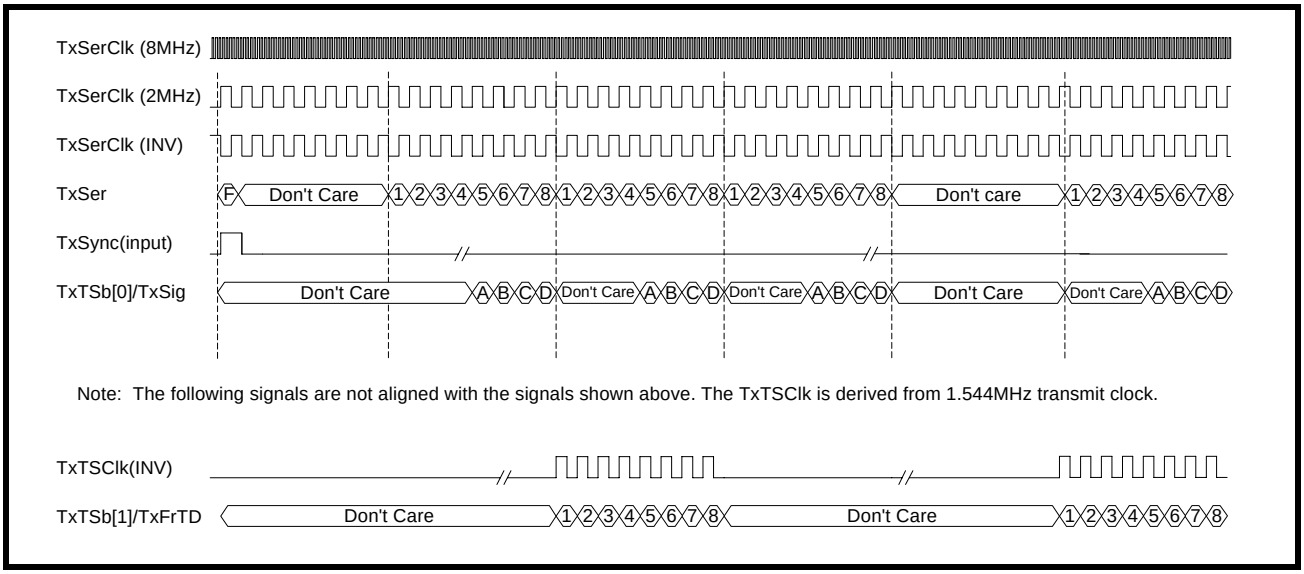
See Figure 33 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in MVIP 8.192Mbit/s mode.

FIGURE 33. INTERFACING XRT84L38 TO THE LOCAL TERMINAL EQUIPMENT USING 8.192MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at 8.192Mbit/s mode is shown in Figure 34.

FIGURE 34. TIMING DIAGRAM OF THE INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 8.192MBIT/S MODE



4.1.3.4 T1 Transmit Input Interface - Multiplexed 12.352Mbit/s

When the Transmit Multiplex Enable bit is set to one and the Transmit Interface Mode Select [1:0] bits are set to 00, the Transmit Back-plane interface of framer is running at a clock rate of 12.352MHz.

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)

- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane Interface is accepting data through TxSer_0 or TxSer_4 pins at 12.352Mbit/s. The local Terminal Equipment multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4.

Free-running clocks of 12.352MHz is supplied to the Transmit Input Clock pin of Channel 0 and Channel 4 of the framer. The local Terminal Equipment provides multiplexed payload data at rising edge of this Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the clock.

The local Terminal Equipment maps four 1.544Mbit/s DS1 data streams into this 12.352Mbit/s data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

FIRST OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

F_X: F-bit of Channel X

2. Payload data of four channels are repeated and grouped together in a bit-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the first payload bit of Timeslot 0 of Channel 1 and 2. The first payload bit of Timeslot 0 of Channel 3 is sent last. After the first bits of Timeslot 0 of all four channels are sent, it comes the second bit of Timeslot 0 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 12.352Mbit/s data stream.

SECOND OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	1_1	1_1	1_2	1_2	1_3	1_3

THIRD OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
2_0	2_0	2_1	2_1	2_2	2_2	2_3	2_3

X_Y: The Xth payload bit of Channel Y

3. The local Terminal Equipment also multiplexed signaling bits with payload bits and sent them together through the 12.352Mbit/s data stream. When the Terminal Equipment is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Simi-

larly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 12.352Mbit/s data stream.

SIXTH OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	5_1	A_1	5_2	A_2	5_3	A_3

SEVENTH OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
6_0	B_0	6_1	B_1	6_2	B_2	6_3	B_3

EIGHTH OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
7_0	C_0	7_1	C_1	7_2	C_2	7_3	C_3

NINETH OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
8_0	D_0	8_1	D_1	8_2	D_2	8_3	D_3

X_Y: The Xth payload bit of Channel Y

A_Y: The signaling bit A of Channel Y

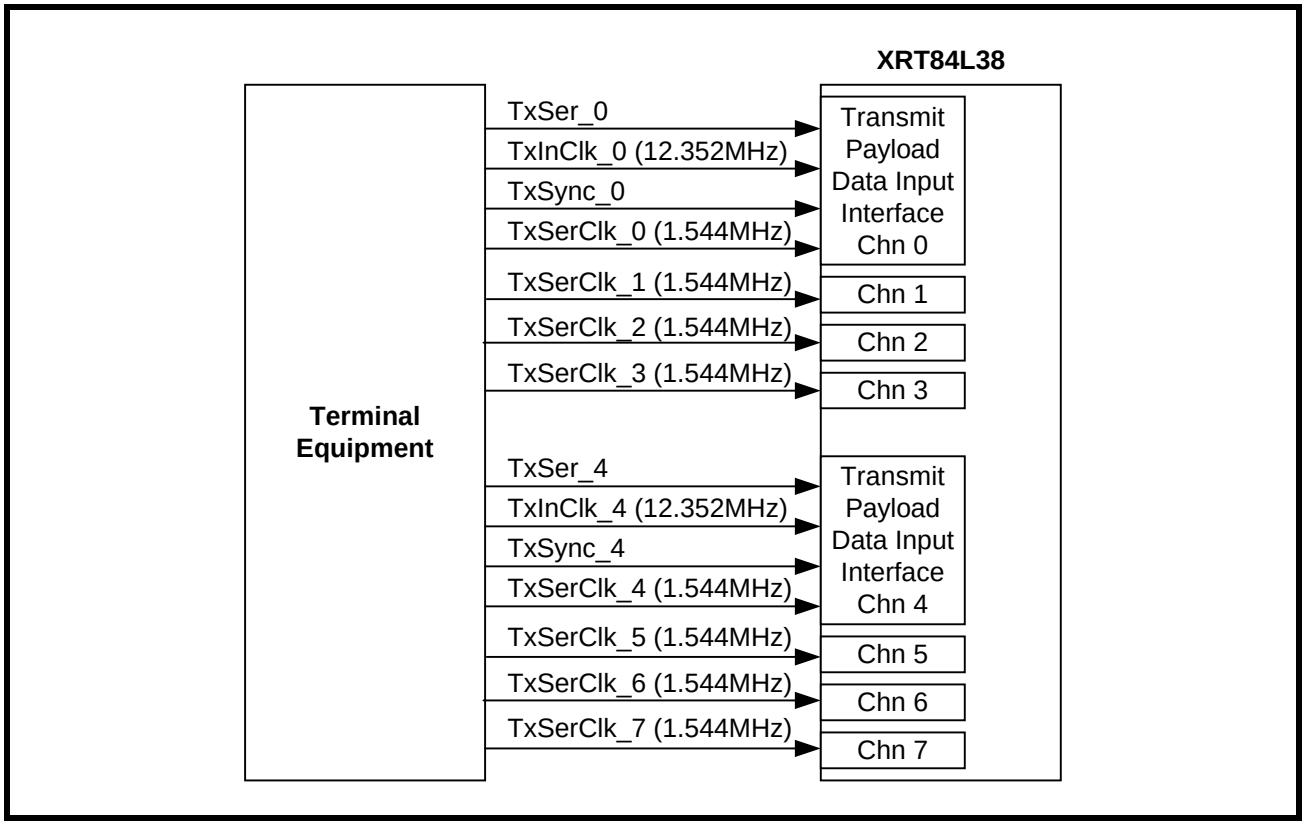
4. Following the same rules of Step 2 and 3, the local Terminal Equipment maps the payload data and signaling data of four channels into a 12.352Mbit/s data stream.

The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH for one clock cycle at the first bit position (F-bit of channel 0) of the data stream with data from Channel 0-3 multiplexed together. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH for one clock cycle at the first bit position (F-bit of Channel 4) of the data stream with data from Channel 4-7 multiplexed together. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of the multiplexed DS1 frame. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT84L38 and send to each individual channel. These data will be processed by each individual framer and send to LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

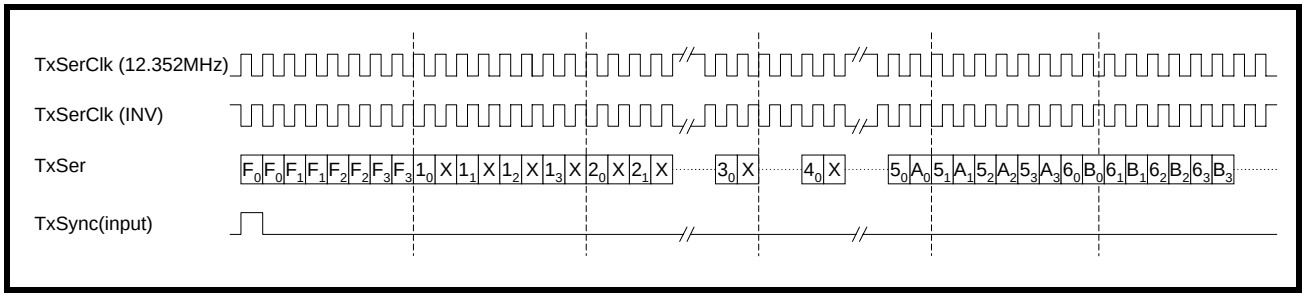
See Figure 35 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in 12.352Mbit/s mode.

FIGURE 35. INTERFACING XRT84L38 TO THE LOCAL TERMINAL EQUIPMENT USING BIT-MULTIPLEXED 12.352MBIT/S DATA BUS



The Input signal timing is shown in Figure 36 below when the framer is running at 12.352Mbit/s mode.

FIGURE 36. TIMING DIAGRAM OF THE INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 12.352MBIT/S MODE



4.1.3.5 T1 Transmit Input Interface - Bit-Multiplexed 16.384Mbit/s

When the Transmit Multiplex Enable bit is set to one and the Transmit Interface Mode Select [1:0] bits are set to 01, the Transmit Back-plane interface of framer is running at a clock rate of 16.384MHz.

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)

- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane Interface is accepting data through TxSer_0 or TxSer_4 pins at 16.384Mbit/s. The local Terminal Equipment multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz is supplied to the Transmit Input Clock pin of Channel 0 and Channel 4 of the framer. The local Terminal Equipment provides multiplexed payload data at rising edge of this Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the clock.

The local Terminal Equipment maps four 1.544Mbit/s DS1 data streams into this 16.384Mbit/s data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

F_X: F-bit of Channel X

2. After the first octet of data is sent, the local Terminal Equipment should insert seven octets (fifty-six bits) of "don't care" data into the outgoing data stream.
3. Payload data of four channels are repeated and grouped together in a bit-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the first payload bit of Timeslot 0 of Channel 1 and 2. The first payload bit of Timeslot 0 of Channel 3 is sent last. After the first bits of Timeslot 0 of all four channels are sent, it comes the second bit of Timeslot 0 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

NINETH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	1_1	1_1	1_2	1_2	1_3	1_3

TENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
2_0	2_0	2_1	2_1	2_2	2_2	2_3	2_3

X_Y: The Xth payload bit of Channel Y

4. The local Terminal Equipment also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream. When the Terminal Equipment is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

THIRTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	5_1	A_1	5_2	A_2	5_3	A_3

FOURTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
6_0	B_0	6_1	B_1	6_2	B_2	6_3	B_3

FIFTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
7_0	C_0	7_1	C_1	7_2	C_2	7_3	C_3

SIXTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
8_0	D_0	8_1	D_1	8_2	D_2	8_3	D_3

X_Y: The Xth payload bit of Channel Y

A_Y: The signaling bit A of Channel Y

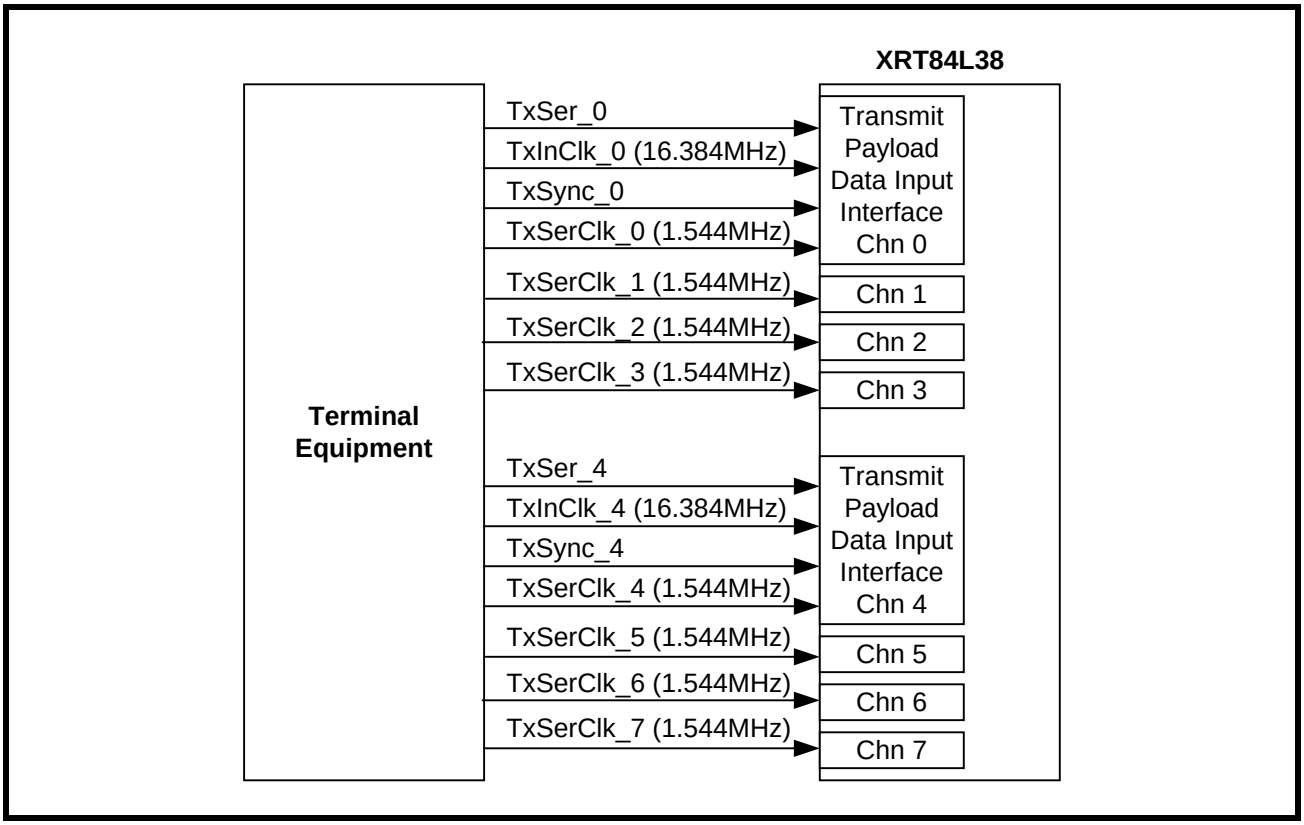
5. After payload bits of Timeslot 0, 1 and 2 of all four channels are sent, the Terminal Equipment should stuff another eight octets (sixty-four bits) of "don't care" data into the outgoing data stream.
6. Following the same rules of Step 2 to 5, the local Terminal Equipment stuffs eight octets of "don't care" data after sending twenty-four octets of multiplexed payload and signaling data. A 16.384Mbit/s data stream is thus created.

The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH for one clock cycle at the first bit position (F-bit of channel 0) of the data stream with data from Channel 0-3 multiplexed together. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH for one clock cycle at the first bit position (F-bit of Channel 4) of the data stream with data from Channel 4-7 multiplexed together. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of the multiplexed DS1 frame. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT84L38 and send to each individual channel. These data will be processed by each individual framer and send to LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

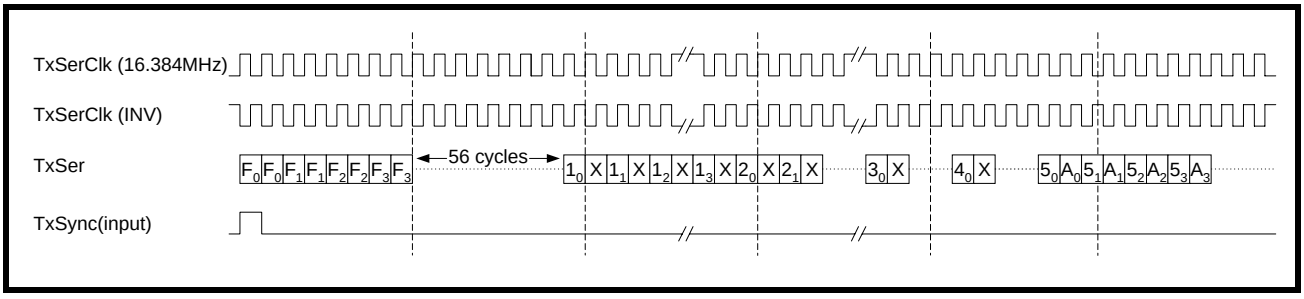
See Figure 37 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in Bit-multiplexed 16.384Mbit/s mode.

FIGURE 37. INTERFACING XRT84L38 TO THE LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 38 below when the framer is running at Bit-Multiplexed 16.384Mbit/s mode.

FIGURE 38. TIMING DIAGRAM OF THE INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT BIT-MULTIPLEXED 16.384MBIT/S MODE



4.1.3.6 T1 Transmit Input Interface - HMVIP 16.384Mbit/s

When the Transmit Multiplex Enable bit is set to one and the Transmit Interface Mode Select [1:0] bits are set to 10, the Transmit Back-plane interface of framer is running at a clock rate of 16.384MHz.

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane Interface is accepting data through TxSer_0 or TxSer_4 pins at 16.384Mbit/s. The local Terminal Equipment multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz is supplied to the Transmit Input Clock pin of Channel 0 and Channel 4 of the framer. The local Terminal Equipment provides multiplexed payload data at rising edge of this Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the clock.

The local Terminal Equipment maps four 1.544Mbit/s DS1 data streams into this 16.384Mbit/s data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

F_X: F-bit of Channel X

2. After the first octet of data is sent, the local Terminal Equipment should insert seven octets (fifty-six bits) of "don't care" data into the outgoing data stream.
3. Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0 and so on. After all the bits of Timeslot 0 of Channel 0 is sent repeatedly, the Terminal Equipment will start sending the payload bits of Timeslot 0 of Channel 1 and 2. The payload bits of Timeslot 0 of Channel 3 are sent the last. After the payload bits of Timeslot 0 of all four channels are sent, it comes the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

NINTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0

ELEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1

THIRTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2

FIFTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3

X_Y: The Xth payload bit of Channel Y

4. The local Terminal Equipment also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream. When the Terminal Equipment is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

TENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	6_0	B_0	7_0	C_0	8_0	D_0

TWELFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_1	A_1	6_1	B_1	7_1	C_1	8_1	D_1

FOURTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_2	A_2	6_2	B_2	7_2	C_2	8_2	D_2

SIXTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_3	A_3	6_3	B_3	7_3	C_3	8_3	D_3

X_Y: The Xth payload bit of Channel Y

A_Y: The signaling bit A of Channel Y

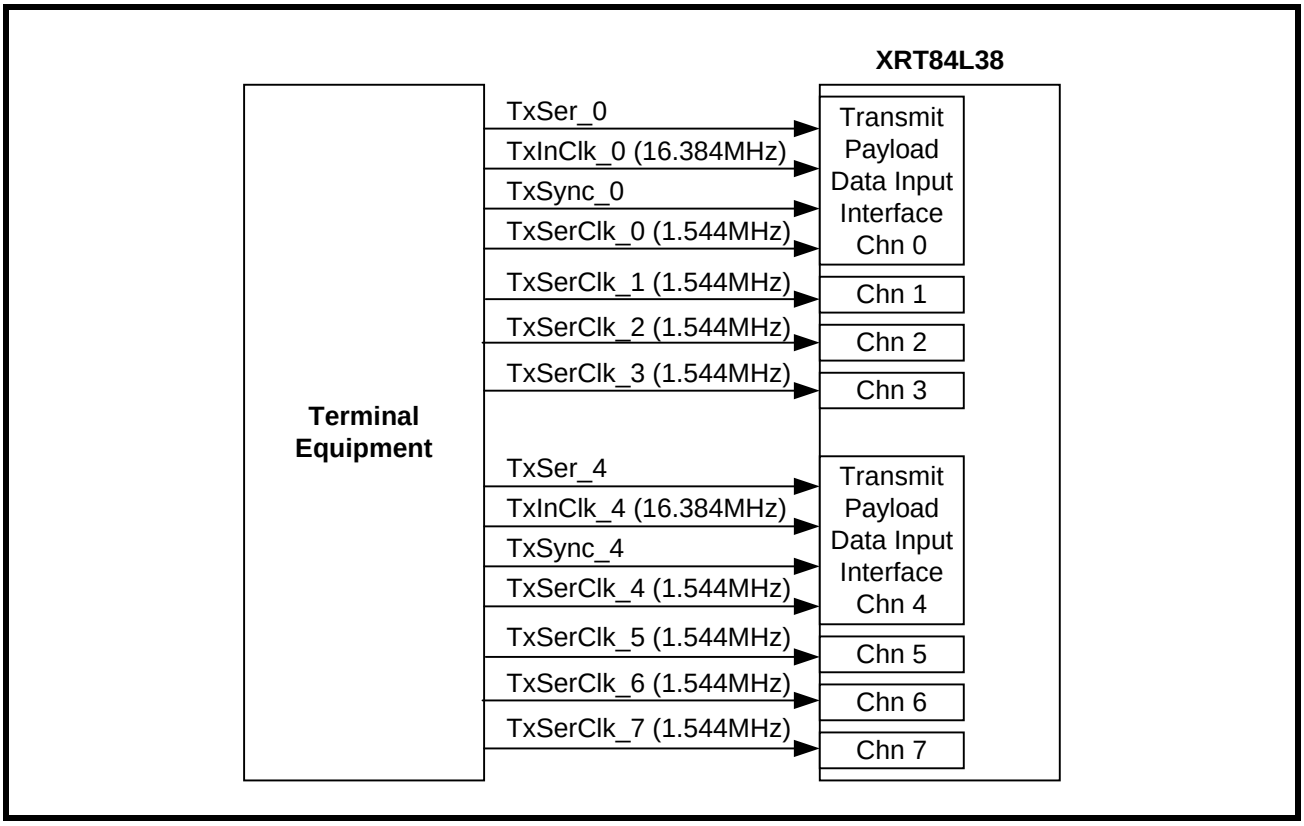
5. After payload bits of Timeslot 0, 1 and 2 of all four channels are sent, the Terminal Equipment should stuff another eight octets (sixty-four bits) of "don't care" data into the outgoing data stream.
6. Following the same rules of Step 2 to 5, the local Terminal Equipment stuffs eight octets of "don't care" data after sending twenty-four octets of multiplexed payload and signaling data. A 16.384Mbit/s data stream is thus created.

The Transmit Single-frame Synchronization signal should pulse HIGH for four clock cycles (the last two bit positions of the previous multiplexed frame and the first two bits of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH to identify the start of multiplexed data stream of Channel 4-7. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of the multiplexed DS1 frame. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT84L38 and send to each individual channel. These data will be processed by each individual framer and send to LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

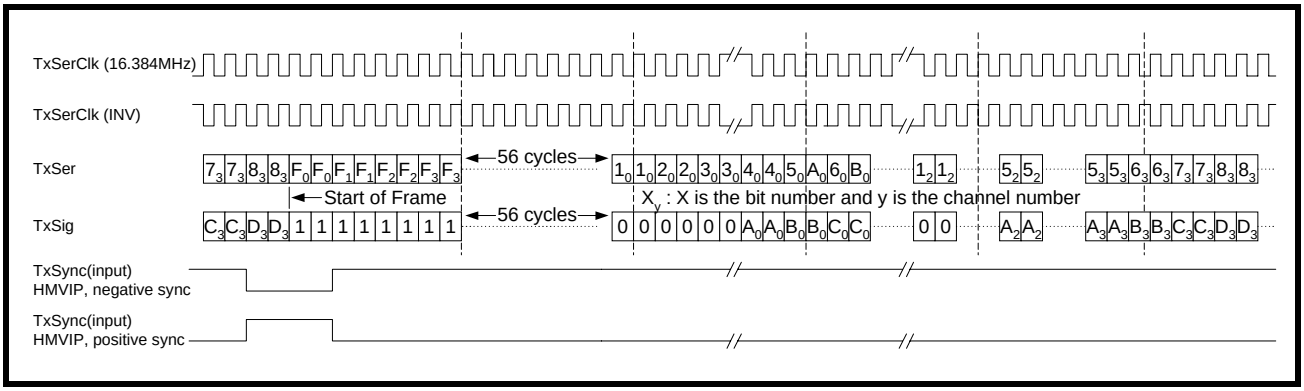
See Figure 39 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in HMVIP 16.384Mbit/s mode.

FIGURE 39. INTERFACING XRT84L38 TO THE LOCAL TERMINAL EQUIPMENT USING HMVIP 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 40 below when the framer is running at HMVIP 16.384Mbit/s mode.

FIGURE 40. TIMING DIAGRAM OF THE INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT HMVIP 16.384MBIT/S MODE



4.1.3.7 T1 Transmit Input Interface - H.100 16.384Mbit/s

When the Transmit Multiplex Enable bit is set to one and the Transmit Interface Mode Select [1:0] bits are set to 11, the Transmit Back-plane interface of framer is running at H.100 16.384Mbit/s mode.

(The HMVIP mode and the H.100 mode are essential the same except for the HIGH pulse position of the Transmit Single-frame Synchronization Signal)

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane Interface is accepting data through TxSer_0 or TxSer_4 pins at 16.384Mbit/s. The local Terminal Equipment multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz is supplied to the Transmit Input Clock pin of Channel 0 and Channel 4 of the framer. The local Terminal Equipment provides multiplexed payload data at rising edge of this Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the clock.

The local Terminal Equipment maps four 1.544Mbit/s DS1 data streams into this 16.384Mbit/s data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

FX: F-bit of Channel X

2. After the first octet of data is sent, the local Terminal Equipment should insert seven octets (fifty-six bits) of "don't care" data into the outgoing data stream.

3. 3.Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0 and so on. After all the bits of Timeslot 0 of Channel 0 is sent repeatedly, the Terminal Equipment will start sending the payload bits of Timeslot 0 of Channel 1 and 2. The payload bits of Timeslot 0 of Channel 3 are sent the last. After the payload bits of Timeslot 0 of all four channels are sent, it comes the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

NINTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0

ELEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1

THIRTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2

FIFTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3

X_Y: The Xth payload bit of Channel Y

4. The local Terminal Equipment also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream. When the Terminal Equipment is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

TENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	6_0	B_0	7_0	C_0	8_0	D_0

TWELFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_1	A_1	6_1	B_1	7_1	C_1	8_1	D_1

FOURTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_2	A_2	6_2	B_2	7_2	C_2	8_2	D_2

SIXTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_3	A_3	6_3	B_3	7_3	C_3	8_3	D_3

X_Y: The Xth payload bit of Channel Y

A_Y: The signaling bit A of Channel Y

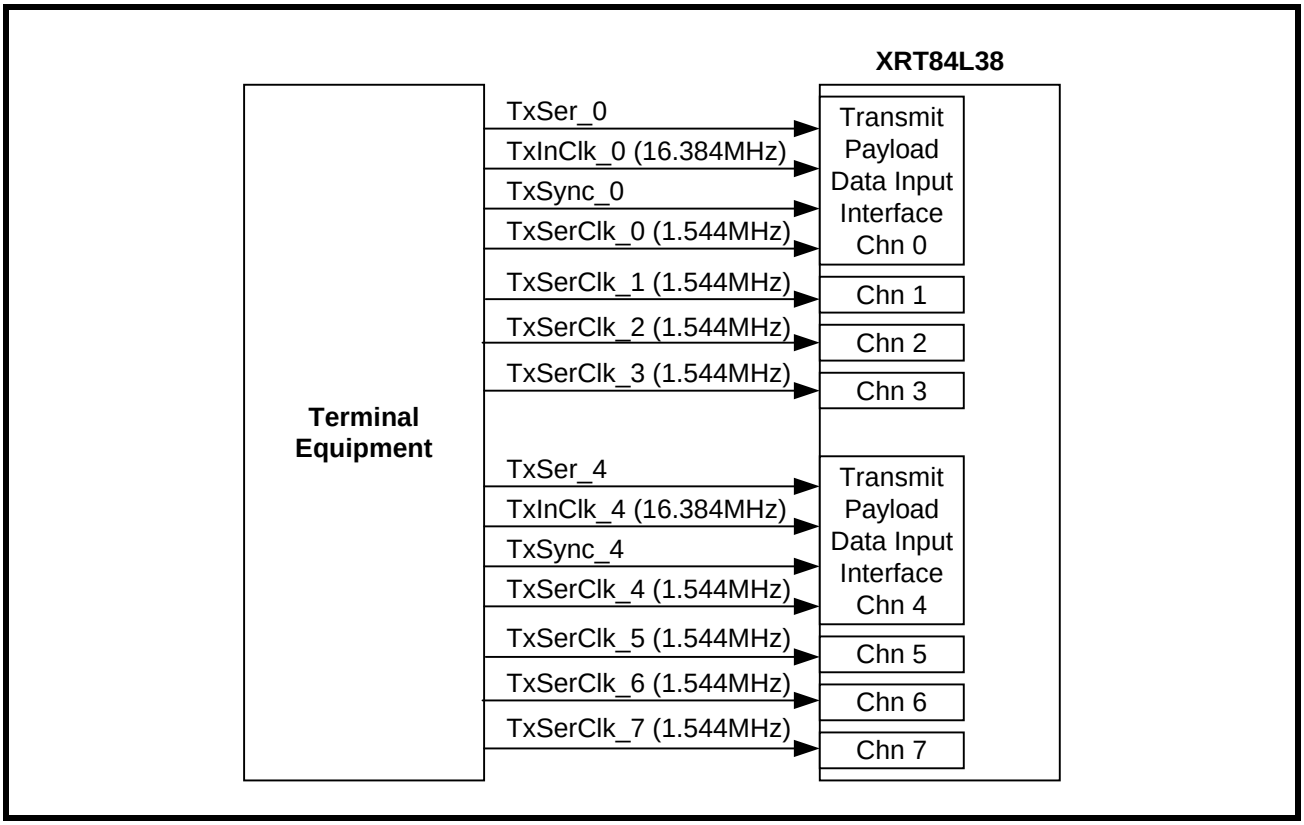
5. After payload bits of Timeslot 0, 1 and 2 of all four channels are sent, the Terminal Equipment should stuff another eight octets (sixty-four bits) of "don't care" data into the outgoing data stream.
6. Following the same rules of Step 2 to 5, the local Terminal Equipment stuffs eight octets of "don't care" data after sending twenty-four octets of multiplexed payload and signaling data. A 16.384Mbit/s data stream is thus created.

The Transmit Single-frame Synchronization signal should pulse HIGH for two clock cycles (the last bit position of the previous multiplexed frame and the first bit position of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH to identify the start of multiplexed data stream of Channel 4-7. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of the multiplexed DS1 frame. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT84L38 and send to each individual channel. These data will be processed by each individual framer and send to LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

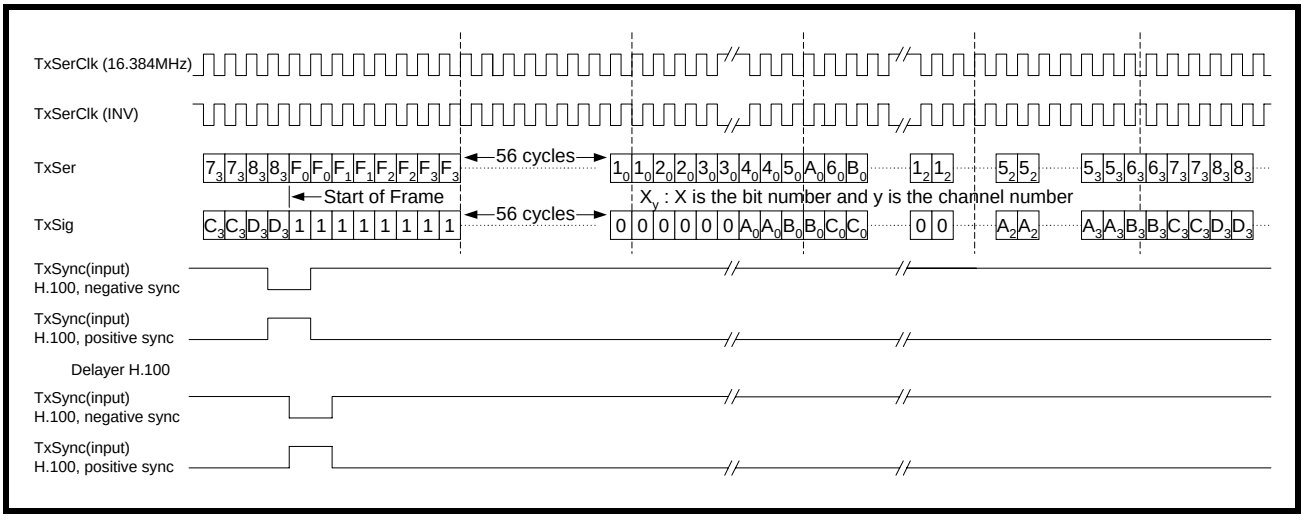
See Figure 41 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in H.100 16.384Mbit/s mode.

FIGURE 41. INTERFACING XRT84L38 TO THE LOCAL TERMINAL EQUIPMENT USING H.100 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 42 below when the framer is running at H.100 16.384Mbit/s mode.

FIGURE 42. TIMING DIAGRAM OF THE INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT H.100 16.384MBIT/S MODE



5.0 THE DS1 RECEIVE SECTION

5.1 THE DS1 RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK

5.1.1 Description of the Receive Payload Data Output Interface Block

Each of the eight framers within the XRT84L38 includes a Receive Payload Data Output Interface block. The function of the block is to provide an interface to the Terminal Equipment (for example, a Central Office or switching equipment) that has data to receive from a "Far End" terminal over a DS1 or E1 transport medium.

The Payload Data Output Interface module (also known as the Back-plane Interface module) supports payload data to be taken from or presented to the system. In DS1 mode, supported data rates are 1.544Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 12.352Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s. In E1 mode, supported data rates are XRT84V24 compatible 2.048Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s.

The Receive Payload Data Output Interface block supplies or accepts the following signals to the Terminal Equipment circuitry:

- Receive Serial Data Input (RxSer_n)
- Receive Serial Clock (RxSerClk_n)
- Receive Single-frame Synchronization Signal (RxSync_n)
- Receive Multi-frame Synchronization Signal (RxMSync_n)
- Receive Time-slot Indicator Clock (RxTSClk_n)
- Receive Time-slot Indication Bits (RxTSb[4:0]_n)

The Receive Serial Data is an output pin carrying payload, signaling and sometimes Data Link data supplied by XRT84L38 to the local Terminal Equipment.

The Receive Serial Clock is an input or output signal used by the Receive Payload Data Input Interface block to send out serial data to the local Terminal Equipment. The Receive Clock Inversion bit of the Receive Interface Control Register (TICR) determines at which edge of the Receive Serial Clock would data transition on the Receive Serial Data pin occur.

The table below shows configurations of the Receive Clock Inversion bit of the Receive Interface Control Register (RICR).

RECEIVE INTERFACE CONTROL REGISTER (RICR) (INDIRECT ADDRESS = 0xn0H, 0x22H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Clock Inversion	R/W	0 - Serial data transition happens on rising edge of the Receive Serial Clock. 1 - Serial data transition happens on falling edge of the Receive Serial Clock.

Throughout the discussion of this datasheet, we assume that serial data transition happens on the rising edge of the Receive Serial Clock unless stated otherwise.

The Receive Single-frame Synchronization signal is either input or output. When configured as input, it indicates beginning of a DS1 frame. When configured as output, it indicates the end of a DS1 frame.

The Receive Multi-frame Synchronization signal is an output pin from XRT84L38 indicating the end of a DS1 multi-frame.

By connecting these signals with the local Terminal Equipment, the Receive Payload Data Output Interface routes received payload data from the Receive Framer Module to the local Terminal Equipment.

5.1.2 The Receive Payload Data Output Interface Block Operating at 1.544Mbit/s mode

The incoming Receive Payload Data is taken into the framer from the LIU interface using the Recovered Receive Line Clock. The payload data is then routed through the Receive Farmer Module and presented to the Receive Payload Data Output Interface through the Receive Serial Data output pin (RxSer_n). This data is then clocked out using the Receive Serial Clock (RxSerClk_n).

There is a two-frame (512 bits) elastic buffer between the Receive Framer Module and the Receive Payload Data Output Interface. This buffer can be enabled or disabled via programming the Slip Buffer Enable [1:0] bits in Slip Buffer Control Register (SBCR).

The following table shows configurations of the Slip Buffer Enable [1:0] bits in Slip Buffer Control Register.

SLIP BUFFER CONTROL REGISTER (SBCR) (INDIRECT ADDRESS = 0xn0H, 0x16H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Slip Buffer Enable	R/W	00 - Slip Buffer is bypassed. The Receive Payload Data is passing from the Receive Framer Module to the Receive Payload Data Output Interface directly without routing through the Slip Buffer. The Receive Serial Clock signal (RxSerClk_n) is an output. 01 - The Elastic Store (Slip Buffer) is enabled. The Receive Payload Data is passing from the Receive Framer Module through the Slip Buffer to the Receive Payload Data Output Interface. The Receive Serial Clock signal (RxSerClk_n) is an input. 10 - The Slip Buffer acts as a FIFO. The FIFO Latency Register (FLR) determines the data latency. The Receive Payload Data is passing from the Receive Framer Module through the FIFO to the Receive Payload Data Output Interface. The Receive Serial Clock signal (RxSerClk_n) is an input. 11 - Slip Buffer is bypassed. The Receive Payload Data is passing from the Receive Framer Module to the Receive Payload Data Output Interface directly without routing through the Slip Buffer. The Receive Serial Clock signal (RxSerClk_n) is an output.

If the Slip Buffer is not in bypass mode, then the user has the option of either providing the Receive Single-Frame Synchronization pulse or getting the Receive Single-Frame Synchronization pulse on frame boundary at the RxSync_n pin. The Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register (SBCR) determines whether the Receive Single-Frame Synchronization signal is input or output.

The table below demonstrates settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register.

SLIP BUFFER CONTROL REGISTER (SBCR) (INDIRECT ADDRESS = 0xn0H, 0x16H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Slip Buffer Receive Synchronization Direction	R/W	0 - The Receive Single-Frame Synchronization signal (RxSync_n) is an output if the Slip Buffer is not in bypass mode. 1 - The Receive Single-Frame Synchronization signal (RxSync_n) is an input if the Slip Buffer is not in bypass mode.

If the Slip Buffer is in bypass mode, the Receive Payload Data is routed to the Receive Payload Data Output Interface from the Receive Framer Module directly. The Recovered Line Clock is used to carry the Receive Payload Data all the way from the LIU interface, to the Receive Framer Module and eventually output through the Receive Serial Data output pin. The Receive Serial Clock signal is therefore an output using the Recovered Receive Line Clock as timing source. The Receive Single-Frame Synchronization signal is also output in Slip Buffer bypass mode.

If the Slip Buffer is enabled, the Receive Payload Data is latched into the Elastic Store using the Recovered Receive Line Clock. The local Terminal Equipment supplies a free-running 1.544MHz clock to the Receive Serial Clock pin to latch the Receive Payload Data out from the Elastic Store. Since the Recovered Receive Line Clock and the Receive Serial Clock are coming from different timing sources, the Slip Buffer will gradually fill or empty. If the elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties and a read occurs, then a full frame of data will be repeated and a status bit will be updated. If the buffer fills and a write comes, then a full frame of data will be deleted and another status bit will be set. A detailed description of the

Elastic Buffer can be found in later sections. In this mode, the Receive Single-Frame Synchronization signal can be either input or output depending on the settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register.

If the Slip Buffer is put into a FIFO mode, it is acting like a standard First-In-First-Out storage. A fixed READ and WRITE latency is maintained in a programmable fashion controlled by the FIFO Latency Register (FIFOLR). The local Terminal Equipment supplies a 1.544MHz clock to the Receive Serial Clock pin to latch the Receive Payload Data out from the FIFO. However, it is the responsibility of the user to phase lock the input Receive Serial Clock to the Recovered Receive Line Clock to avoid either over-run or under-run of the FIFO. In this mode, the Receive Single-Frame Synchronization signal can be either input or output depending on the settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register.

The following table summaries the input or output nature of the Receive Serial Clock and Receive Single-Frame Synchronization signals for different Slip Buffer settings.

TABLE 42: THE RECEIVE SERIAL CLOCK AND RECEIVE SINGLE-FRAME SYNCHRONIZATION SIGNALS FOR DIFFERENT SLIP BUFFER SETTINGS

RECEIVE TIMING SOURCE	RXSERCLK_N	RXSYNC_N	
		SLIP BUFFER SYNCHRONIZATION DIRECTION BIT = 0	SLIP BUFFER SYNCHRONIZATION DIRECTION BIT = 1
Slip Buffer Bypassed	Output	Output	Output
Slip Buffer Enabled	Input	Output	Input
Slip Buffer Acts as FIFO	Input	Output	Input

The Receive Time-slot Indication Bits (RxTSb[4:0]_n) are multiplexed I/O pins. The functionality of these pins is governed by the value of Receive Fractional T1 Output Enable bit of the Receive Interface Control Register (RICR). The following table illustrates the configurations of the Receive Fractional DS1 Input Enable bit.

RECEIVE INTERFACE CONTROL REGISTER (RICR) (INDIRECT ADDRESS = 0xn0H, 0x22H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Fractional DS1 Output Enable	R/W	0 - The Receive Time-slot Indication bits (RxTSb[4:0] are outputting five-bit binary values of Time-slot number (0-23) being accepted and processed by the Receive Payload Data Output Interface block of the framer. The Receive Time-slot Indicator Clock signal (RxTSClk_n) is a 192KHz clock that pulses HIGH for one DS1 bit period whenever the Receive Payload Data Output Interface block is accepting the LSB of each of the twenty-four time slots. 1 - The RxTSb[0]_n bit becomes the Receive Fractional T1 Output signal (RxFrTD_n) which carries Fractional DS1 payload data from the framer. The RxTSb[1]_n bit becomes the Receive Signaling Data Output signal (RxSig_n) which is used to carry robbed-bit signaling data extracted from the inbound DS1 frame. The RxTSb[2]_n bit serially outputs all five-bit binary values of the Time Slot number (0-23) being accepted and processed by the Receive Payload Data Output Interface block of the framer. The RxTSClk_n will output gaped fractional DS1 clock that can be used by Terminal Equipment to latch in Fractional DS1 payload data at rising edge of the clock. Or, The RxTSClk_n pin will be a clock enable signal to Receive Fractional DS1 Output signal (RxFrTD_n) when the un-gaped Receive Serial Output Clock (RxSerClk_n) is used to latch in Fractional DS1 Payload Data into the Terminal Equipment.

When configured to operate in normal condition (that is, when the Receive Fractional T1 Input Enable bit is equal to zero), these bits reflect the five-bit binary value of the Time Slot number (0 - 23) being outputted and processed by the Receive Payload Data Output Interface block of the framer. RxTSb[4] represents the MSB of the binary value and RxTSb[0] represents the LSB.

When the Receive Fractional T1 Output Enable bit is equal to one, the RxTSb[0]_n bit becomes the Receive Fractional T1 Output signal (RxFrTD_n). This output pin carries Fractional T1 Output data extracted by the framer from the incoming DS1 data stream. The Fractional T1 Output Interface allows certain time-slots of DS1 data to be routed to destinations other than the local Terminal Equipment. Function of the Fractional T1 Output signal will be discussed in details in later sections.

When the Receive Fractional T1 Output Enable bit is equal to one, the RxTSb[1]_n bit becomes the Receive Signaling Data Output signal (RxSig_n). These output pins can be used to carry robbed-bit signaling data extracted from the inbound DS1 frame. Function of the Receive Signaling Data Output signal will be discussed in details in later sections.

When the Receive Fractional T1 Output Enable bit is equal to one, the RxTSb[2]_n bit serially outputs all five-bit binary values of the Time Slot number (0-23) being outputted and processed by the Receive Payload Data Output Interface block of the framer. MSB of the binary value is presented first and the LSB is presented last.

The RxTSb[3]_n and RxTSb[4}_n pins are not multiplexed.

The table below shows functionality of the RxTSb[2:0] bits when the Receive Fractional T1 Output bit is set to different values.

TABLE 43: THE RXTSB[2:0] BITS WHEN THE RECEIVE FRACTIONAL T1 OUTPUT BIT IS SET TO DIFFERENT VALUES

RECEIVE FRACTIONAL T1 OUTPUT BIT = 0		RECEIVE FRACTIONAL T1 OUTPUT BIT = 1	
RxTSb[0]	Output	RxFrTD	Output
RxTSb[1]	Output	RxSig	Output
RxTSb[2]	Output	RxTS	Output

The Receive Time-slot Indicator Clock signal (RxTSClk_n) is a multi-function output pin. When configured to operate in normal condition (that is, when the Receive Fractional T1 Input Enable bit is equal to zero), the RxTSClk_n is a 192KHz clock that pulses HIGH for one DS1 bit period whenever the Receive Payload Data Output Interface block is outputting the LSB of each of the twenty-four time slots. The local Terminal Equipment should use this clock signal to sample the RxTSb[0] through RxTSb[4] bits and identify the time-slot being processed via the Receive Section of the framer.

When the Receive Fractional T1 Output Enable bit is equal to one, the RxTSClk_n will output gaped fractional DS1 clock whenever Fractional DS1 payload data is present at the RxFrTD_n pin. The local Terminal Equipment can latch in Fractional DS1 payload data at falling edge of the clock. Otherwise, this pin will be a clock enable signal to Receive Fractional DS1 output signal (RxFrTD_n) if the framer is configured accordingly. In this way, Fractional DS1 payload data is clocked into the Terminal Equipment using un-gaped Receive Serial Output Clock (RxSerClk_n). A detailed discussion of the Fractional DS1 Payload Data Output Interface can be found in later sections.

A detailed discussion of how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment with Slip Buffer enabled or disabled can be found in the later sections.

5.1.2.1 Connect the Receive Payload Data Output Interface block to the Local Terminal Equipment if the Slip Buffer is bypassed

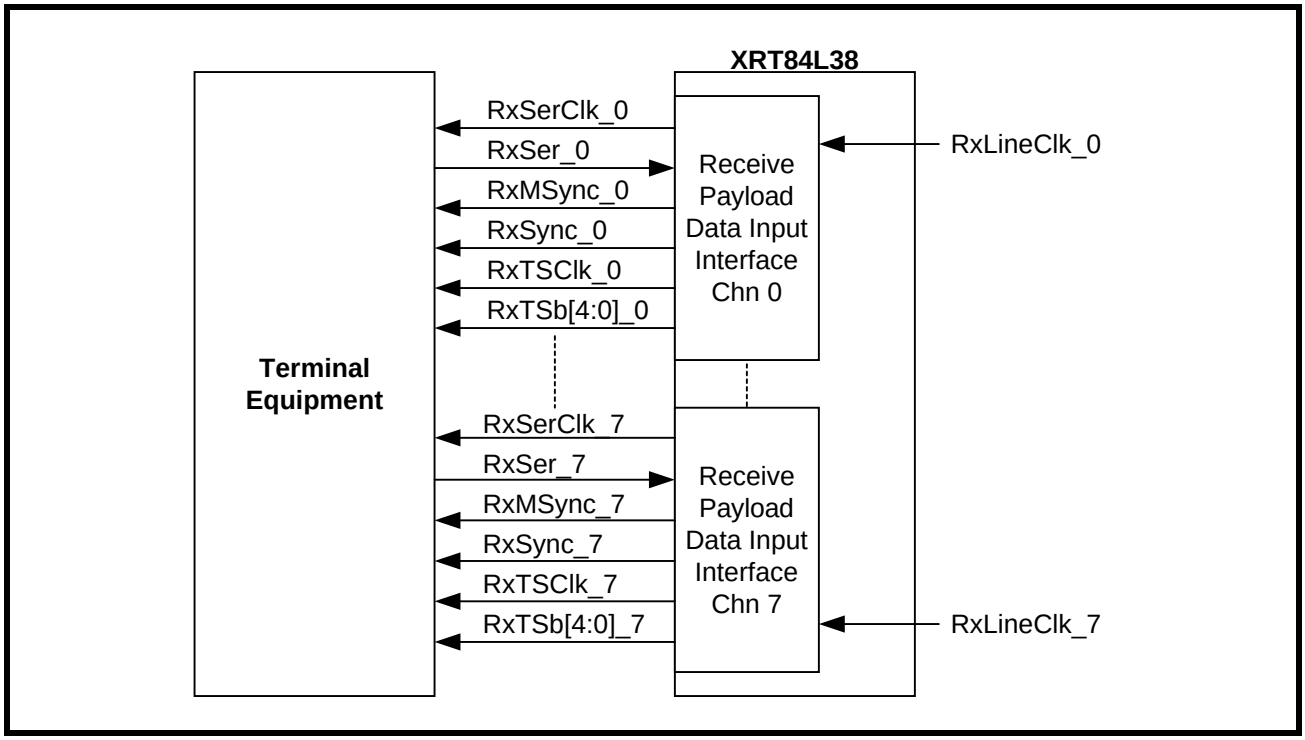
By setting the Slip Buffer Enable [1:0] bits of the Slip Buffer Control Register to 00 or 11, the Receive Framer Module routes the Receive Payload Data directly to the Receive Payload Data Output Interface without passing through the Elastic Buffer. The XRT84L38 uses the Recovered Receive Line Clock internally to carry the Receive Payload Data directly across the whole chip. The Recovered Receive Line Clock is essentially become timing source of the Receive Serial Clock output.

If the Slip Buffer is bypassed, the Receive Single-frame Synchronization signal is automatically configured to be output signals. It should pulse HIGH for one DS1 bit period (648ns) at the last bit position of each DS1 frame. By triggering on the HIGH pulse on the Receive Single-frame Synchronization signal, the Terminal Equipment can identify the end of a DS1 frame and should prepare to accept payload data of the next DS1 frame from the framer.

The Receive Multi-frame Synchronization signal should pulse HIGH for one DS1 bit period (648ns) at the last bit position of a DS1 multi-frame. By triggering on the HIGH pulse on the Receive Multi-frame Synchronization signal, the framer can identify the end of a DS1 super-frame and should prepare to accept payload data of the next DS1 super-frame from the framer.

See Figure 43 for how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is bypassed and the Recovered Receive Line Clock is timing source of the Receive section.

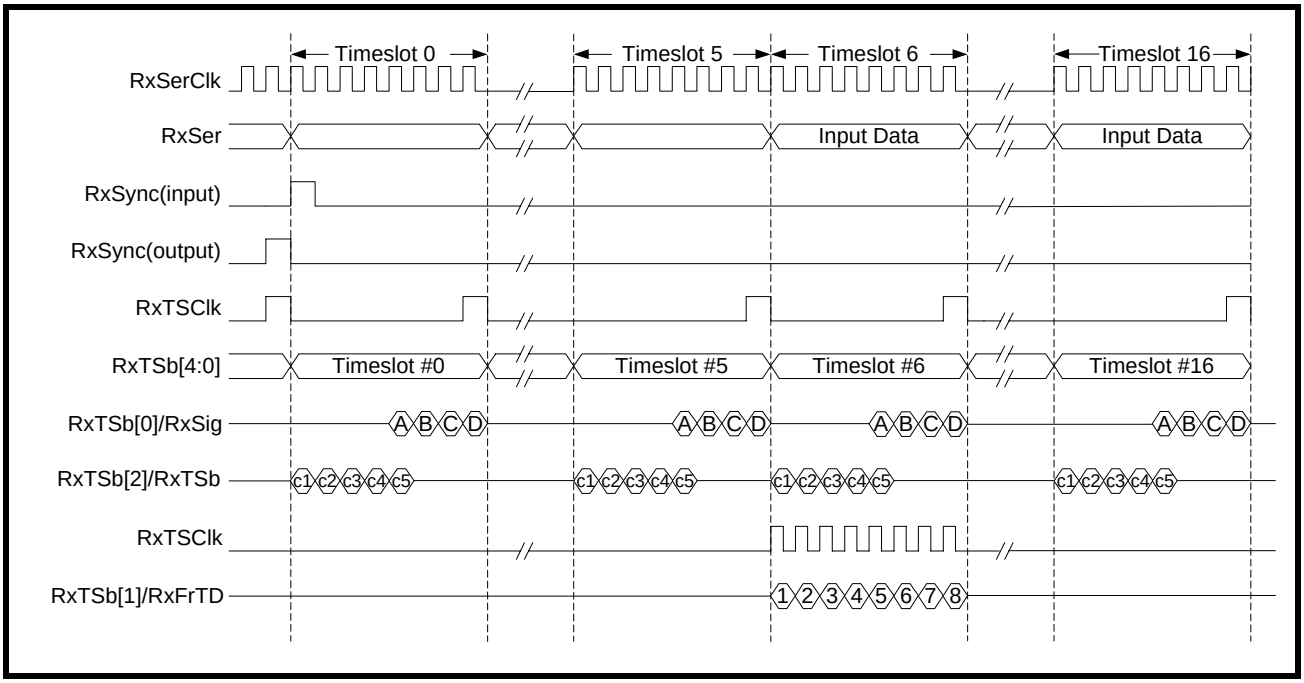
FIGURE 43. INTERFACING XRT84L38 LOCAL TERMINAL EQUIPMENT WITH SLIP BUFFER BYPASSED AND RECOVERED RECEIVE LINE CLOCK AS RECEIVE TIMING SOURCE



The following Figure 44 shows waveforms of the signals (RxSerClk_n, RxSer_n, RxSync_n, RxTSClk_n and RxTSb[4:0]_n) which connecting the Receive Payload Data Output Interface block to the local Terminal Equip-

ment when the Slip Buffer is bypassed and the Recovered Receive Line Clock is timing source of the Receive section.

FIGURE 44. WAVEFORMS OF THE SIGNALS CONNECTING THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WHEN THE SLIP BUFFER IS BYPASSED AND THE RECOVERED LINE CLOCK IS THE TIMING SOURCE OF THE RECEIVE SECTION



5.1.2.2 Connect the Receive Payload Data Output Interface block to the Local Terminal Equipment if the Slip Buffer is enabled

By setting the Slip Buffer Enable [1:0] bits of the Slip Buffer Control Register to 01, the framer includes the two-frame Elastic Buffer into its data path. The Receive Framer Module routes the Receive Payload Data to the Elastic Buffer first. The Receive Payload Data is then presented to the Receive Payload Data Output Interface. The XRT84L38 uses the Recovered Receive Line Clock internally to clock in the Receive Payload Data into the Elastic Buffer. The Terminal Equipment should provide a 1.544MHz clock to the Receive Serial Clock input pin to latch data out from the Elastic Buffer.

The Recovered Receive Line Clock and the Receive Serial Clock are generated from two different timing sources. That is, the Recovered Receive Line Clock is originating from a remote site while Receive Serial Clock generating by a local oscillator. Any mismatch in frequencies of these two clocks will result in the Slip Buffer to gradually fill or deplete.

Overtime, the Elastic Buffer either fills or empties completely. Once that happened, a controlled slip by the XRT84L38 will occur. The Receive Slip Buffer Slip bit of the Slip Buffer Status Register (SBSR) is set to 1.

If the buffer empties and a read occurs, then a full frame of data will be repeated and the Receive Slip Buffer Empty bit of the Slip Buffer Status Register (SBSR) will be forced HIGH. If the buffer fills and a write comes, then a full frame of data will be deleted and the Receive Slip Buffer Full bit of the Slip Buffer Status Register (SBSR) will be forced HIGH.

The following table demonstrates settings of the Receive Slip Buffer Slip bit, Receive Slip Buffer Empty bit and Receive Slip Buffer Full bit of the Slip Buffer Status Register.

SLIP BUFFER STATUS REGISTER (SBSR) (INDIRECT ADDRESS = 0xnAH, 0x08H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Slip Buffer Full	R/W	0 - The Receive Slip Buffer is not full. 1 - The Receive Slip Buffer is full and one frame of data is discarded.
1	Receive Slip Buffer Empty	R/W	0 - The Receive Slip Buffer is not empty. 1 - The Receive Slip Buffer is empty and one frame of data is repeated.
0	Receive Slip Buffer Slip	R/W	0 - The Receive Slip Buffer does not slip. 1 - The Receive Slip Buffer slips since either full or emptied.

In this mode, the Receive Single-Frame Synchronization signal can be either input or output depending on the settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register. When the Slip Buffer Receive Synchronization Direction bit is set to 0, the Receive Single-Frame Synchronization signal (RxSync_n) is an output. When the Slip Buffer Receive Synchronization Direction bit is set to 1,the Receive Single-Frame Synchronization signal (RxSync_n) is an input.

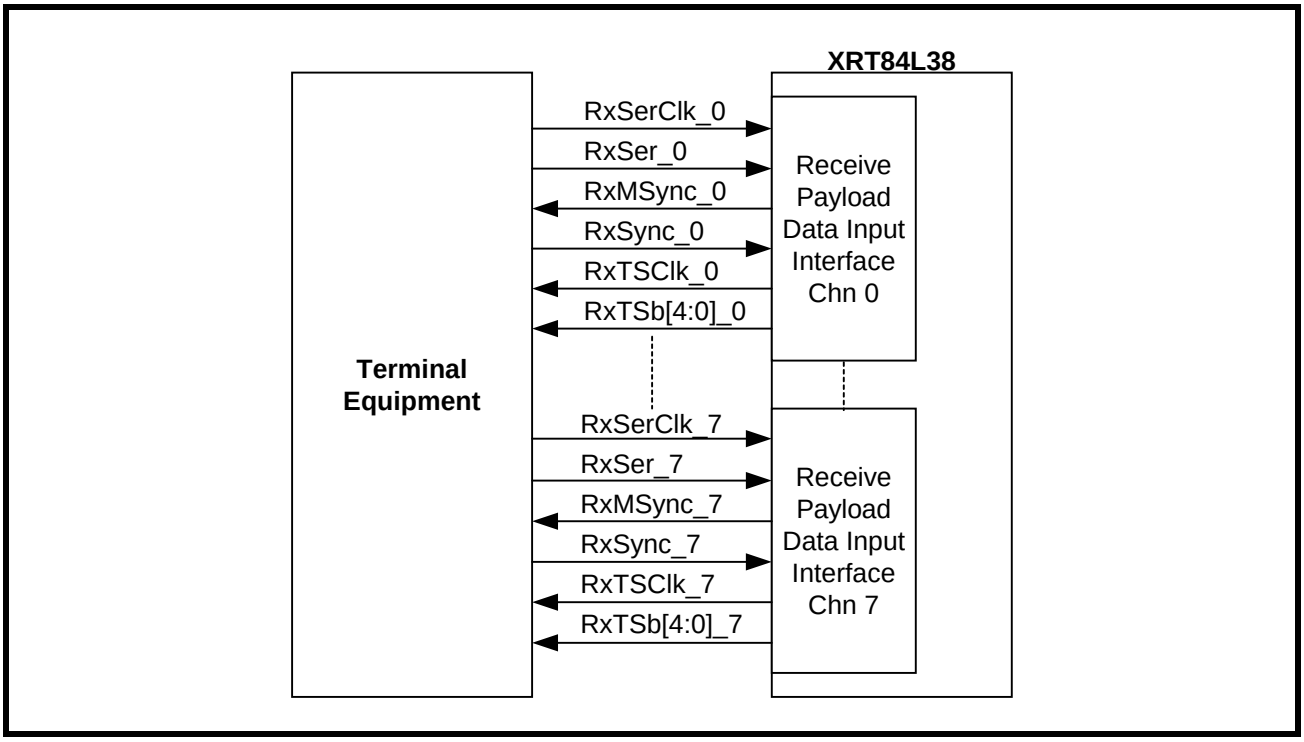
If the Receive Single-Frame Synchronization signal is an output, it should pulse HIGH for one DS1 bit period (648ns) at the last bit position of each DS1 frame. By triggering on the HIGH pulse on the Receive Single-frame Synchronization signal, the Terminal Equipment can identify the end of a DS1 frame and should prepare to accept payload data of the next DS1 frame from the framer.

If the Receive Single-Frame Synchronization signal is an input, it should pulse HIGH for one DS1 bit period (648ns) at the first bit position (F-bit) of each DS1 frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer should identify the beginning of a DS1 frame and can send out data in a synchronized way. It is the responsibility of the local Terminal Equipment to align the start of a DS1 frame with the Receive Single-Frame Synchronization pulse.

The Receive Multi-frame Synchronization signal should pulse HIGH for one DS1 bit period (648ns) at the last bit position of Frame number one of a DS1 multi-frame. By triggering on the HIGH pulse on the Receive Multi-frame Synchronization signal, the framer can identify the end of a DS1 super-frame and should prepare to accept payload data of the next DS1 super-frame from the framer.

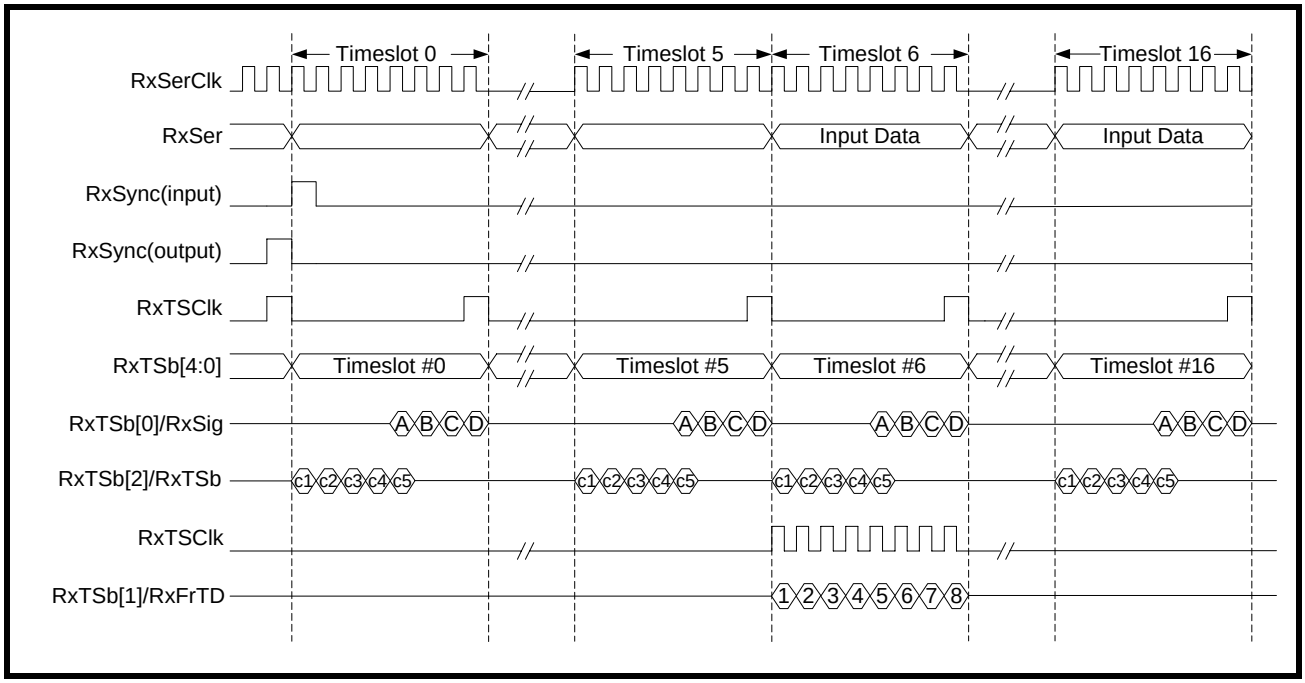
See Figure 45 for how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is enabled.

FIGURE 45. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT WITH SLIP BUFFER ENABLED OR ACTS AS FIFO



The following Figure 46 shows waveforms of the signals (RxSerClk_n, RxSer_n, RxSync_n, RxTSClk_n and RxTSb[4:0]_n) which connecting the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is enabled.

FIGURE 46. WAVEFORMS OF THE SIGNALS THAT CONNECT THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WHEN THE SLIP BUFFER IS ENABLED



5.1.2.3 Connect the Receive Payload Data Output Interface block to the Local Terminal Equipment if the Slip Buffer is configured as FIFO

By setting the Slip Buffer Enable [1:0] bits of the Slip Buffer Control Register to 10, the framer puts the Elastic Buffer into FIFO mode. Receive Framer Module routes the Receive Payload Data through the First-In-First-Out storage to the Receive Payload Data Output Interface. The XRT84L38 uses the Recovered Receive Line Clock internally to clock in the Receive Payload Data into the FIFO. The Terminal Equipment should provide an external 1.544MHz clock to the Receive Serial Clock input pin to latch data out from the FIFO.

It is the responsibility of the user to phase lock the input Receive Serial Clock to the Recovered Receive Line Clock to avoid either over-run or under-run of the FIFO. The latency between writing a bit into the FIFO and reading the same bit from it (READ and WRITE latency) is actually depth of the FIFO, which is maintained in a programmable fashion controlled by the FIFO Latency Register (FIFOLR). The largest possible depth of the FIFO is thirty-two bytes or one E1 frame. The default depth of the FIFO when XRT84L38 first powered up is four bytes. The table below shows the FIFO Latency Register.

FIFO LATENCY REGISTER (FIFOLR) (INDIRECT ADDRESS = 0xn0H, 0x17H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4-0	FIFO Latency	R/W	These bits determine depth of the FIFO in terms of bytes. The largest possible value is thirty-two bytes or one E1 frame.

In this mode, the Receive Single-Frame Synchronization signal can be either input or output depending on the settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register. When the Slip Buffer Receive Synchronization Direction bit is set to 0, the Receive Single-Frame Synchronization signal

(RxSync_n) is an. When the Slip Buffer Receive Synchronization Direction bit is set to 1,the Receive Single-Frame Synchronization signal (RxSync_n) is an input.

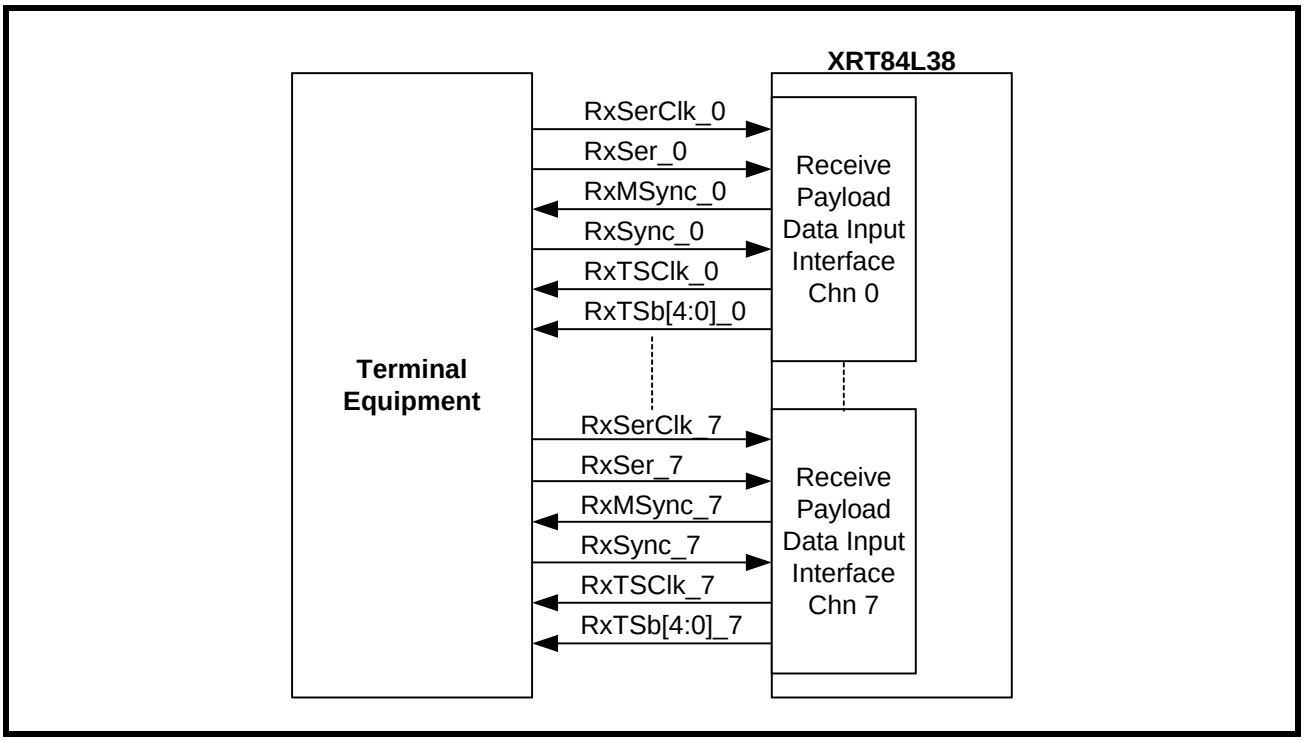
If the Receive Single-Frame Synchronization signal is an output, it should pulse HIGH for one DS1 bit period (648ns) at the last bit position of each DS1 frame. By triggering on the HIGH pulse on the Receive Single-frame Synchronization signal, the Terminal Equipment can identify the end of a DS1 frame and should prepare to accept payload data of the next DS1 frame from the framer.

If the Receive Single-Frame Synchronization signal is an input, it should pulse HIGH for one DS1 bit period (648ns) at the first bit position (F-bit) of each DS1 frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer should identity the beginning of a DS1 frame and can send out data in a synchronized way. It is the responsibility of the local Terminal Equipment to align the start of a DS1 frame with the Receive Single-Frame Synchronization pulse.

The Receive Multi-frame Synchronization signal should pulse HIGH for one DS1 bit period (648ns) at the last bit position of Frame number one of a DS1 multi-frame. By triggering on the HIGH pulse on the Receive Multi-frame Synchronization signal, the framer can identify the end of a DS1 super-frame and should prepare to accept payload data of the next DS1 super-frame from the framer.

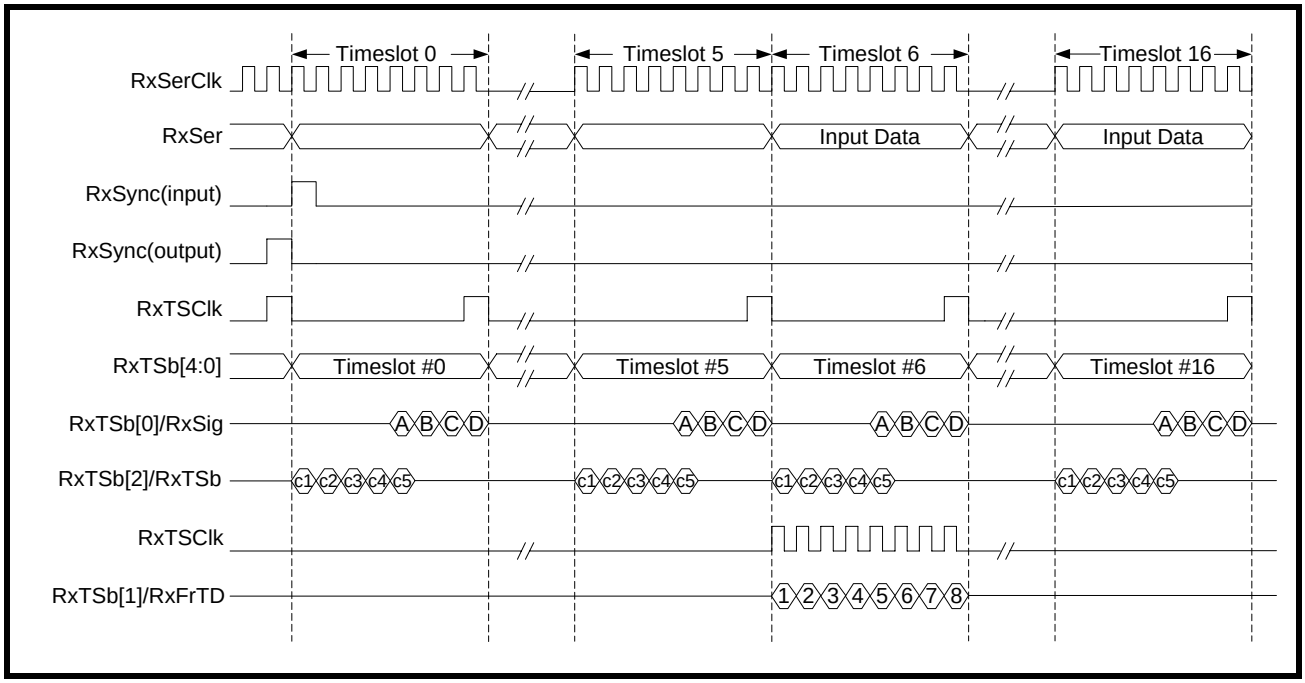
See Figure 47 for how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is acted as FIFO.

FIGURE 47. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT WITH SLIP BUFFER ENABLED OR ACTS AS FIFO



The following Figure 48 shows waveforms of the signals (RxSerClk_n, RxSer_n, RxSync_n, RxTSClk_n and RxTSb[4:0]_n) which connecting the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is acted as FIFO.

FIGURE 48. WAVEFORMS OF THE SIGNALS THAT CONNECT THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WHEN THE SLIP BUFFER IS ACTED AS FIFO



5.1.3 High Speed Receive Back-plane Interface

The High-speed Back-plane Interface supports payload data to be taken from or presented to the local Terminal Equipment at a rate higher than 1.544Mbit/s. In DS1 mode, supported High-speed data rates are MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 12.352Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s. The Receive Multiplex Enable bit and the Receive Interface Mode Select [1:0] bits of the Receive Interface Control Register (RICR) determine the Receive Back-plane Interface data rate.

The following table shows configurations of the Receive Multiplex Enable bit and the Receive Interface Mode Select [1:0] bits of the Receive Interface Control Register (RICR).

RECEIVE INTERFACE CONTROL REGISTER (RICR) (INDIRECT ADDRESS = 0xn0H, 0x22H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Multiplex Enable	R/W	0 - The Receive Back-plane Interface block is configured to non-channel-multiplexed mode. 1 - The Receive Back-plane Interface block is configured to channel-multiplexed mode
1-0	Receive Interface Mode Select	R/W	When combined with the Receive Multiplex Enable bit, these bits determine the Receive Back-plane Interface data rate.

The table below shows the combinations of Receive Multiplex Enable bit and Receive Interface Mode Select [1:0] bits and the resulting Receive Back-plane Interface data rates.

TABLE 44: RECEIVE MULTIPLEX ENABLE BIT AND RECEIVE INTERFACE MODE SELECT [1:0] BITS WITH THE RESULTING RECEIVE BACK-PLANE INTERFACE DATA RATES

RECEIVE MULTIPLEX ENABLE BIT	RECEIVE INTERFACE MODE SELECT BIT 1	RECEIVE INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE
0	0	0	1.544Mbit/s
0	0	1	MVIP 2.048Mbit/s
0	1	0	4.096Mbit/s
0	1	1	8.192Mbit/s
1	0	0	Multiplexed 12.352Mbit/s
1	0	1	Bit Multiplexed 16.384Mbit/s
1	1	0	HMVIP 16.384Mbit/s
1	1	1	H.100 16.384Mbit/s

When the Receive Multiplex Enable bit is set to zero, the framer is configured in non-channel-multiplexed mode. The possible data rates are 1.544Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s and 8.192Mbit/s. In non-channel-multiplexed mode, payload data of each channel are sending out from the Receive High-speed Back-plane Interface separately. Each channel uses its own Receive Serial Clock, Receive Serial Data, Receive Single-frame Synchronization signal and Receive Multi-frame Synchronization signal as interface between the framer and the Terminal Equipment. Section 5.1.1.1, 5.1.1.2 and 5.1.1.3 provide details on how to connect the Receive Payload Data Interface block with the local Terminal Equipment when the Back-plane interface data rate is 1.544Mbit/s.

When the Back-plane interface data rate is MVIP 2.048Mbit/s, 4.096Mbit/s and 8.192Mbit/s, the Receive Serial Clock, Receive Serial Data and Receive Single-frame Synchronization are all configured as inputs. The Receive Multi-frame Synchronization signal is still output. The Receive Serial Clock is configured as an input timing source for the High-speed Back-plane Interface with frequencies of 2.048 MHz, 4.096 MHz and 8.192 MHz respectively.

The table below summaries the clock frequencies of RxSerClk_n input when the framer is operating in non-multiplexed High-speed Back-plane mode.

RECEIVE MULTIPLEX ENABLE BIT = 0

RECEIVE INTERFACE MODE SELECT BIT 1	RECEIVE INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE	RXSERCLK
0	0	1.544Mbit/s	1.544MHz
0	1	MVIP 2.048Mbit/s	2.048 MHz
1	0	4.096Mbit/s	4.096 MHz
1	1	8.192Mbit/s	8.192 MHz

When the Receive Multiplex Enable bit is set to one, the framer is configured in channel-multiplexed mode. The possible data rates are multiplexed 12.352Mbit/s, bit-multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s and H.100 16.384Mbit/s. In channel-multiplexed mode, four channels share the Receive Serial Data, Receive Single-frame Synchronization signal and Receive Serial Clock of one channel as interface between the framer and the Terminal Equipment. The Receive Serial Clock runs at frequencies of 12.352 MHz or 16.384 MHz. It serves as the primary clock source for the High-speed Back-plane Interface.

Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4. The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH at the beginning of the frame with data from Channel 0-3 multiplexed together. The Receive Single-frame Synchronization signal of Channel 4 pulses HIGH at the beginning of the frame with data from Channel 4-7 multiplexed together.

The table below summaries the clock frequencies of RxSerClk_n input when the framer is operating in multiplexed High-speed Back-plane mode.

RECEIVE MULTIPLEX ENABLE BIT = 1

RECEIVE INTERFACE MODE SELECT BIT 1	RECEIVE INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE	RXSERCLK
0	0	Multiplexed 12.352Mbit/s	12.352 MHz
0	1	Bit-multiplexed 16.384Mbit/s	16.384 MHz
1	0	HMVIP 16.384Mbit/s	16.384 MHz
1	1	H.100 16.384Mbit/s	16.384 MHz

When the frame is running at High-speed Back-plane Interface mode other than the 1.544Mbit/s data rate, the Receive Single-frame Synchronization signal could pulse HIGH or LOW indicating boundaries of DS1 frames. The Receive Synchronization Pulse Low bit of the Receive Interface Control Register (TICR) determines whether the Receive Single-frame Synchronization signal is HIGH active or LOW active.

The table below shows configurations of the Receive Synchronization Pulse LOW bit of the Receive Interface Control Register (RICR).

RECEIVE INTERFACE CONTROL REGISTER (RICR) (INDIRECT ADDRESS = 0xn0H, 0x22H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Synchronization Pulse LOW	R/W	0 - The Receive Single-frame Synchronization signal will pulse HIGH indicating the beginning of a DS1 frame when the High-speed Back-plane Interface is running at a mode other than the 1.544Mbit/s. 1 - The Receive Single-frame Synchronization signal will pulse LOW indicating the beginning of a DS1 frame when the High-speed Back-plane Interface is running at a mode other than the 1.544Mbit/s.

Throughout the discussion of this datasheet, we assume that the Receive Single-frame Synchronization signal pulses HIGH unless stated otherwise.

The following sections discuss details of how to operate the framer in different Back-plane interface speed mode and how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment.

5.1.3.1 T1 Receive Input Interface - MVIP 2.048 MHz

When the Receive Multiplex Enable bit is set to zero and the Receive Interface Mode Select [1:0] bits are set to 01, the Receive Back-plane interface of framer is running at a data rate of 2.048Mbit/s.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)

- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane interface is pumping out data through RxSer_n at an E1 equivalent data rate of 2.048Mbit/s. The local Terminal Equipment supplies a free-running 2.048MHz clock to the Receive Serial Clock input. The Receive High-speed Back-plane Interface of the framer then sends out serial data at rising edge of the Receive Serial Clock. The local Terminal Equipment samples the serial data at falling edge of the clock.

The Terminal Equipment take in data grouped in 256-bit frame 8000 times every second. Each frame consists of thirty-two octets as in E1. The Receive High-speed Back-plane Interface maps a 193-bit T1 frame into this 256-bit format as described below:

1. The F-bit is mapped into MSB of the first E1 Time-slot. The framer will insert seven "don't care" bits to the rest of the first octet that would be ignored by the local Terminal Equipment.
2. Payload data of T1 Time-slot 0, 1 and 2 are mapped into E1 Time-slot 1, 2 and 3.
3. The Receive High-speed Back-plane Interface will stuff E1 Time-slot 4 with eight "don't care" bits that would be ignored by the local Terminal Equipment.
4. Following the same rules of Step 2 and 3, the Receive High-speed Back-plane Interface maps every three time-slots of T1 payload data into four E1 time-slots.

The mapping of T1 frame into E1 framing format is shown in the table below.

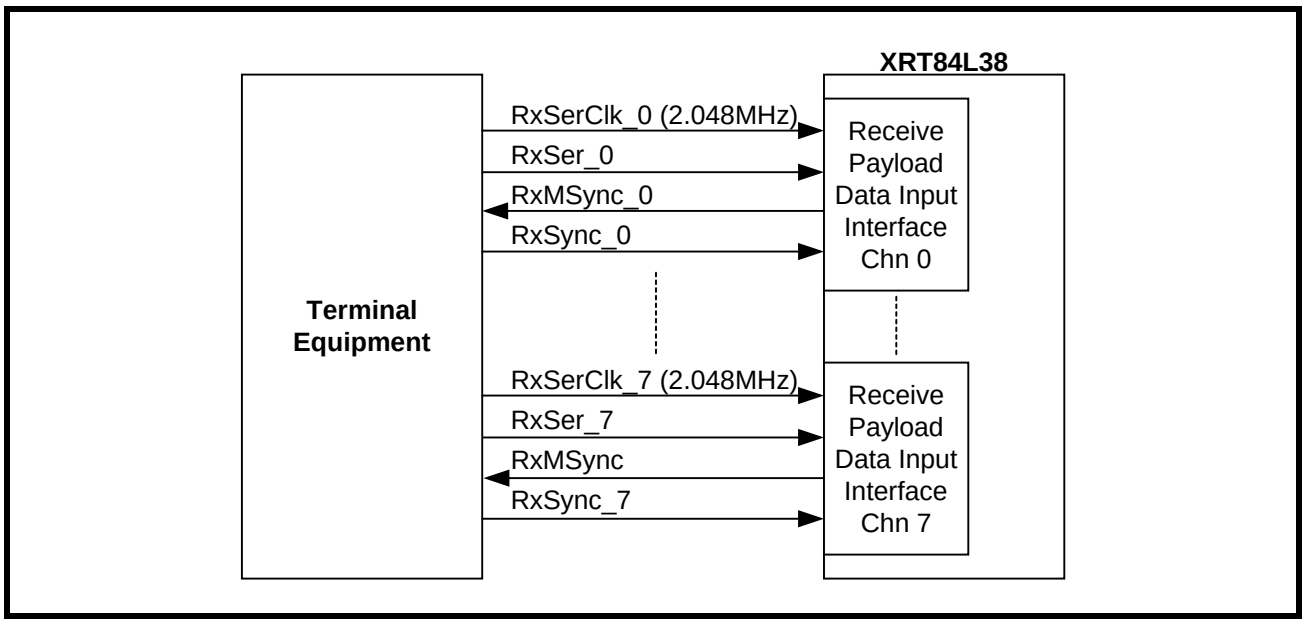
TABLE 45: THE MAPPING OF T1 FRAME INTO E1 FRAMING FORMAT

T1	F-Bit	TS0	TS1	TS2	Don't Care Bits	TS3	TS4	TS5
E1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7
T1	Don't Care Bits	TS6	TS7	TS8	Don't Care Bits	TS9	TS10	TS11
E1	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15
T1	Don't Care Bits	TS12	TS13	TS14	Don't Care Bits	TS15	TS16	TS17
E1	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23
T1	Don't Care Bits	TS18	TS19	TS20	Don't Care Bits	TS21	TS22	TS23
E1	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31

The Receive Single-frame Synchronization input signal (RxSync_n) should pulse HIGH at the beginning of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer can identity the beginning of a DS1 frame and start pumping payload data out.

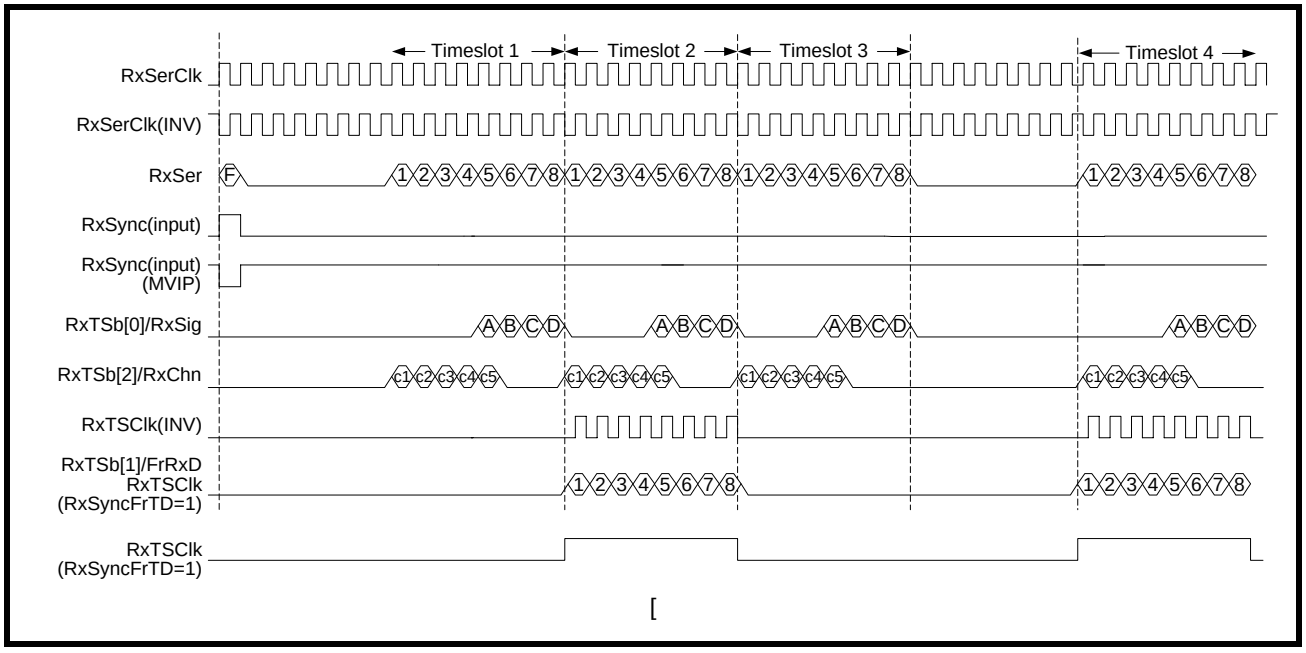
See Figure 49 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in MVIP 2.048Mbit/s mode.

FIGURE 49. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING MVIP 2.048MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at MVIP 2.048Mbit/s mode is shown in Figure 50.

FIGURE 50. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT MVIP 2.048MBIT/S



5.1.3.2 T1 Receive Input Interface - 4.096 MHz

This interface mode is the same as running at 2.048 MHz. The only difference is that the Receive Serial Clock runs two times faster at 4.096 MHz.

When the Receive Multiplex Enable bit is set to zero and the Receive Interface Mode Select [1:0] bits are set to 10, the Receive Back-plane interface of framer is running at a clock rate of 4.096MHz.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane interface is pumping out data through RxSer_n at an E1 equivalent data rate of 2.048Mbit/s. The local Terminal Equipment supplies a free-running 4.096MHz clock to the Receive Serial Clock input. The Receive High-speed Back-plane Interface of the framer then sends out serial data at every other rising edge of the Receive Serial Clock. The local Terminal Equipment samples the serial data at every other falling edge of the clock.

The Terminal Equipment take in data grouped in 256-bit frame 8000 times every second. Each frame consists of thirty-two octets as in E1. The Receive High-speed Back-plane Interface maps a 193-bit T1 frame into this 256-bit format as described below:

1. The F-bit is mapped into MSB of the first E1 Time-slot. The framer will insert seven "don't care" bits to the rest of the first octet that would be ignored by the local Terminal Equipment.
2. Payload data of T1 Time-slot 0, 1 and 2 are mapped into E1 Time-slot 1, 2 and 3.
3. The Receive High-speed Back-plane Interface will stuff E1 Time-slot 4 with eight "don't care" bits that would be ignored by the local Terminal Equipment.
4. Following the same rules of Step 2 and 3, the Receive High-speed Back-plane Interface maps every three time-slots of T1 payload data into four E1 time-slots.

The mapping of T1 frame into E1 framing format is shown in the table below.

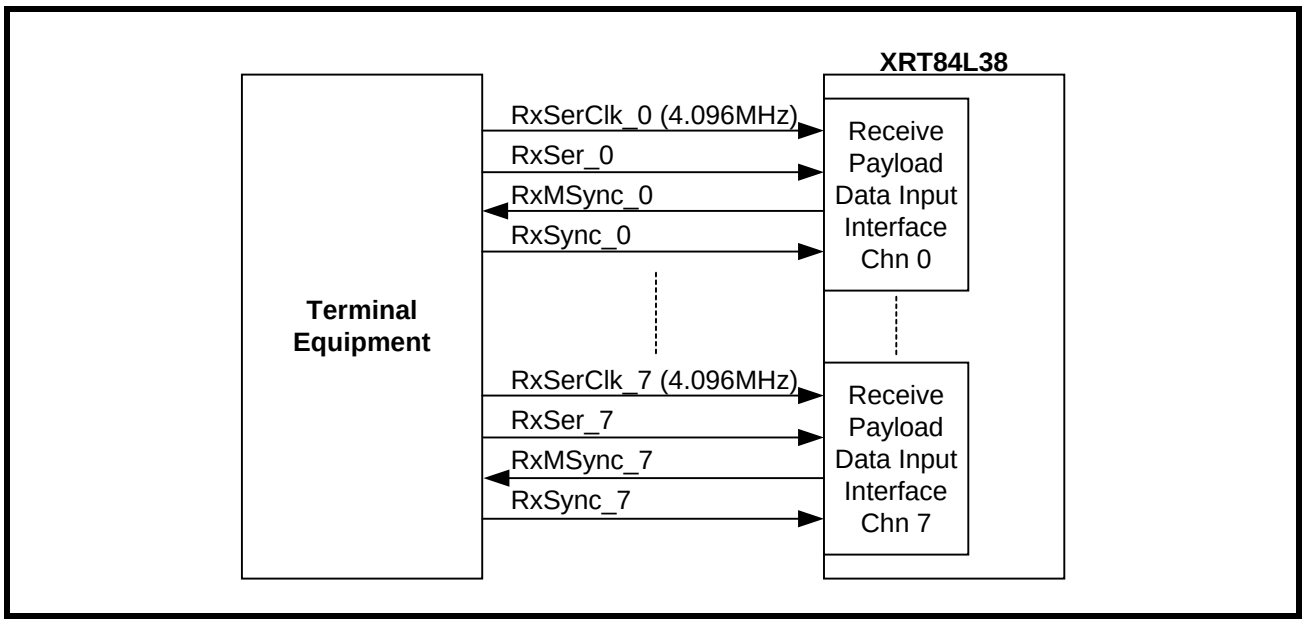
TABLE 46: THE MAPPING OF T1 FRAME INTO E1 FRAMING FORMAT

T1	F-Bit	TS0	TS1	TS2	Don't Care Bits	TS3	TS4	TS5
E1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7
T1	Don't Care Bits	TS6	TS7	TS8	Don't Care Bits	TS9	TS10	TS11
E1	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15
T1	Don't Care Bits	TS12	TS13	TS14	Don't Care Bits	TS15	TS16	TS17
E1	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23
T1	Don't Care Bits	TS18	TS19	TS20	Don't Care Bits	TS21	TS22	TS23
E1	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31

The Receive Single-frame Synchronization input signal (RxSync_n) should pulse HIGH at the beginning of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer can identity the beginning of a DS1 frame and start pumping payload data out.

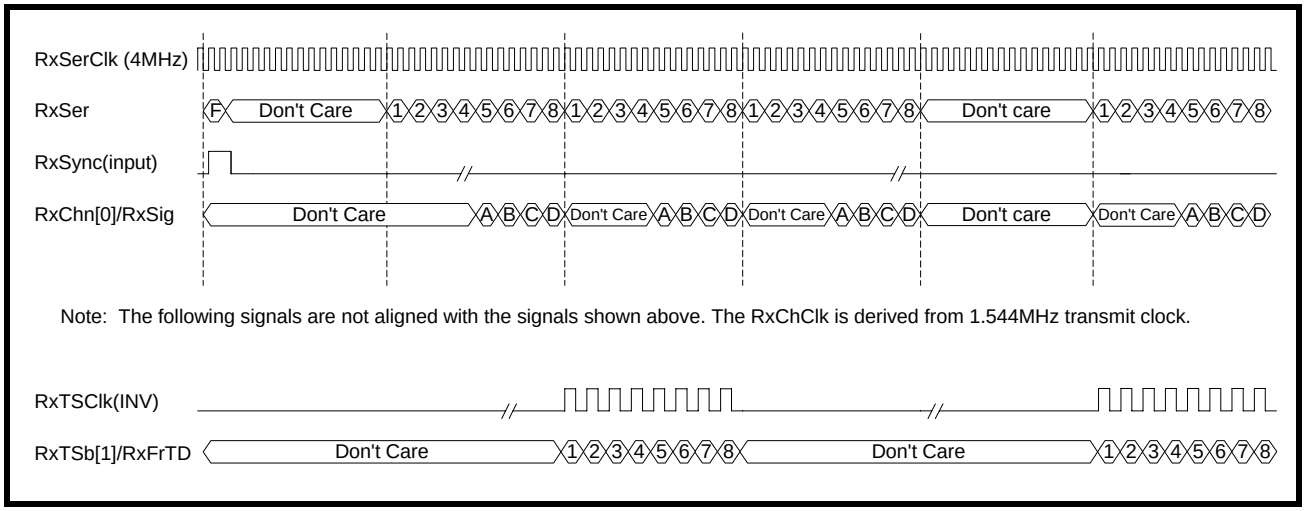
See Figure 51 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in 4.096Mbit/s mode.

FIGURE 51. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING 4.096MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at 4.096Mbit/s mode is shown in Figure 52.

FIGURE 52. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 4.096MBIT/S



5.1.3.3 T1 Receive Input Interface - 8.192 MHz

This interface mode is the same as running at 2.048 MHz. The only difference is that the Receive Serial Clock runs four times faster at 8.192MHz.

When the Receive Multiplex Enable bit is set to zero and the Receive Interface Mode Select [1:0] bits are set to 11, the Receive Back-plane interface of framer is running at a clock rate of 8.192MHz.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)

- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane interface is pumping out data through RxSer_n at an E1 equivalent data rate of 2.048Mbit/s. The local Terminal Equipment supplies a free-running 8.192MHz clock to the Receive Serial Clock input. The Receive High-speed Back-plane Interface of the framer then sends out serial data at every other four rising edge of the Receive Serial Clock. The local Terminal Equipment samples the serial data at every other four falling edge of the clock.

The Terminal Equipment take in data grouped in 256-bit frame 8000 times every second. Each frame consists of thirty-two octets as in E1. The Receive High-speed Back-plane Interface maps a 193-bit T1 frame into this 256-bit format as described below:

1. The F-bit is mapped into MSB of the first E1 Time-slot. The framer will insert seven "don't care" bits to the rest of the first octet that would be ignored by the local Terminal Equipment.
2. Payload data of T1 Time-slot 0, 1 and 2 are mapped into E1 Time-slot 1, 2 and 3.
3. The Receive High-speed Back-plane Interface will stuff E1 Time-slot 4 with eight "don't care" bits that would be ignored by the local Terminal Equipment.
4. Following the same rules of Step 2 and 3, the Receive High-speed Back-plane Interface maps every three time-slots of T1 payload data into four E1 time-slots.

The mapping of T1 frame into E1 framing format is shown in the table below.

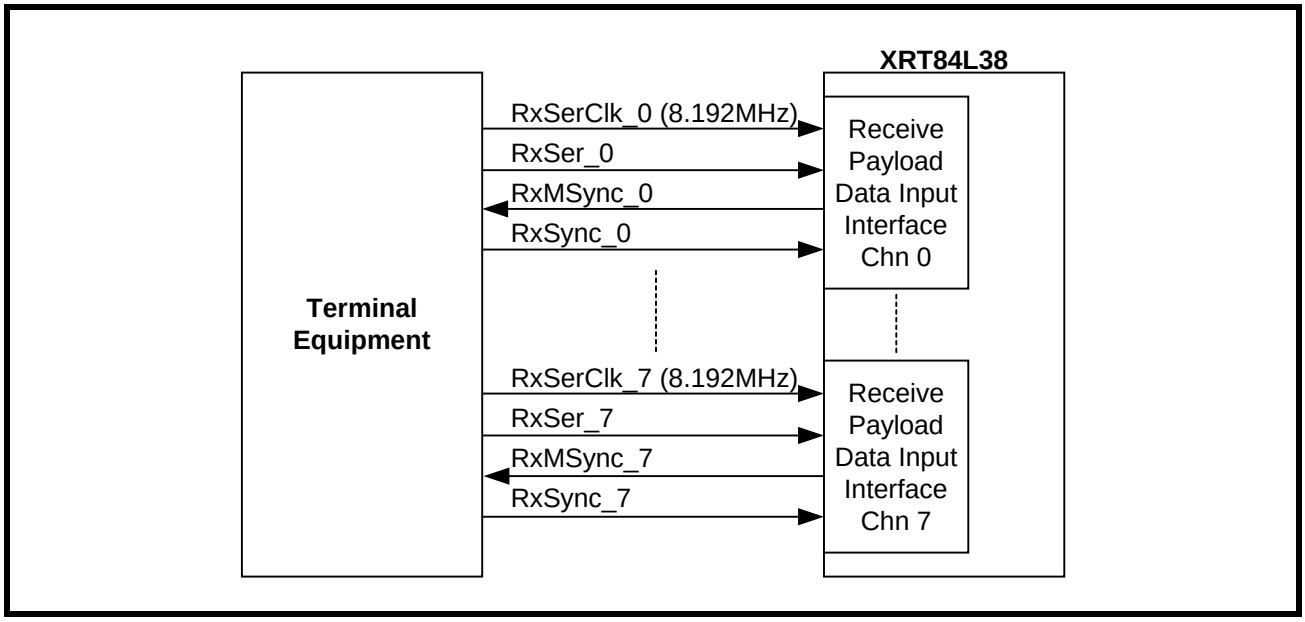
TABLE 47: THE MAPPING OF T1 FRAME INTO E1 FRAMING FORMAT

T1	F-Bit	TS0	TS1	TS2	Don't Care Bits	TS3	TS4	TS5
E1	TS0	TS1	TS2	TS3	TS4	TS5	TS6	TS7
T1	Don't Care Bits	TS6	TS7	TS8	Don't Care Bits	TS9	TS10	TS11
E1	TS8	TS9	TS10	TS11	TS12	TS13	TS14	TS15
T1	Don't Care Bits	TS12	TS13	TS14	Don't Care Bits	TS15	TS16	TS17
E1	TS16	TS17	TS18	TS19	TS20	TS21	TS22	TS23
T1	Don't Care Bits	TS18	TS19	TS20	Don't Care Bits	TS21	TS22	TS23
E1	TS24	TS25	TS26	TS27	TS28	TS29	TS30	TS31

The Receive Single-frame Synchronization input signal (RxSync_n) should pulse HIGH at the beginning of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer can identity the beginning of a DS1 frame and start pumping payload data out.

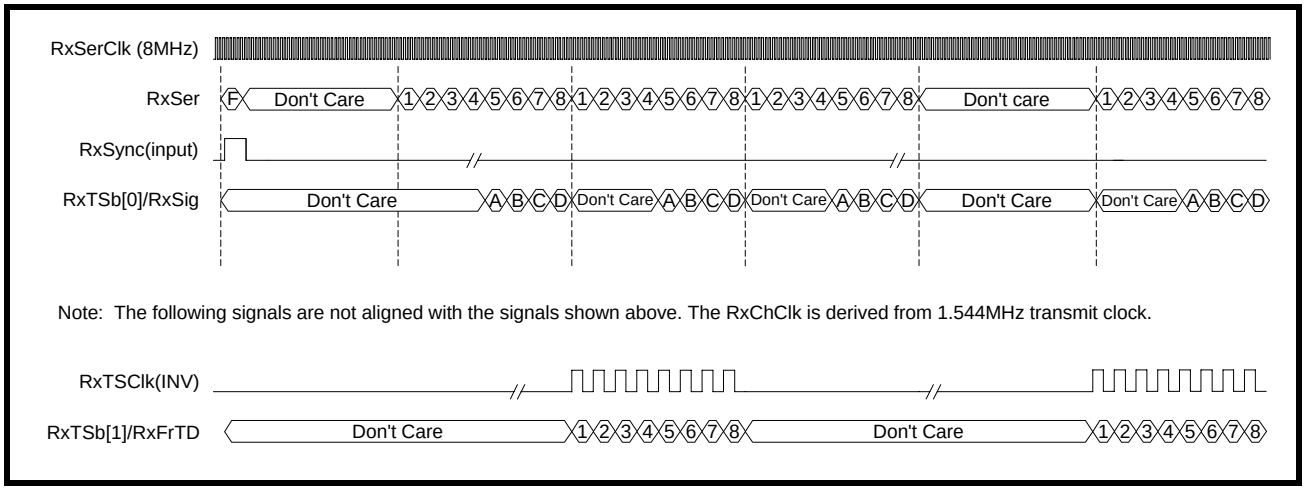
See Figure 53 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in 8.192Mbit/s mode.

FIGURE 53. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING 8.192MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at 8.192Mbit/s mode is shown in Figure 54.

FIGURE 54. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 8.192MBIT/S



5.1.3.4 T1 Receive Input Interface - Multiplexed 12.352Mbit/s

When the Receive Multiplex Enable bit is set to one and the Receive Interface Mode Select [1:0] bits are set to 00, the Receive Back-plane interface of framer is running at a clock rate of 12.352MHz.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)

- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane Interface is pumping data through RxSer_0 or RxSer_4 pins at 12.352Mbit/s. It multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4.

Free-running clocks of 12.352MHz are supplied to the Receive Serial Clock pin of Channel 0 and Channel 4 of the framer. The Receive High-speed Back-plane Interface of the farmer provides data at rising edge of this Receive Serial Clock. The local Terminal Equipment then latches incoming serial data at falling edge of the clock.

The Receive High-speed Back-plane Interface multiplexes four 1.544Mbit/s DS1 data streams into this 12.352Mbit/s data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

FIRST OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

F_X: F-bit of Channel X

2. Payload data of four channels are repeated and grouped together in a bit-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the first payload bit of Timeslot 0 of Channel 1 and 2. The first payload bit of Timeslot 0 of Channel 3 is sent last. After the first bits of Timeslot 0 of all four channels are sent, it comes the second bit of Timeslot 0 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 12.352Mbit/s data stream.

SECOND OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	1_1	1_1	1_2	1_2	1_3	1_3

THIRD OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
2_0	2_0	2_1	2_1	2_2	2_2	2_3	2_3

X_Y: The Xth payload bit of Channel Y

3. The Receive High-speed Back-plane Interface also multiplexed signaling bits with payload bits and sent them together through the 12.352Mbit/s data stream. When Receive High-speed Back-plane Interface is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 12.352Mbit/s data stream.

SIXTH OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	5_1	A_1	5_2	A_2	5_3	A_3

SEVENTH OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
6_0	B_0	6_1	B_1	6_2	B_2	6_3	B_3

EIGHTH OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
7_0	C_0	7_1	C_1	7_2	C_2	7_3	C_3

NINETH OCTET OF 12.352MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
8_0	D_0	8_1	D_1	8_2	D_2	8_3	D_3

X_Y: The Xth payload bit of Channel Y

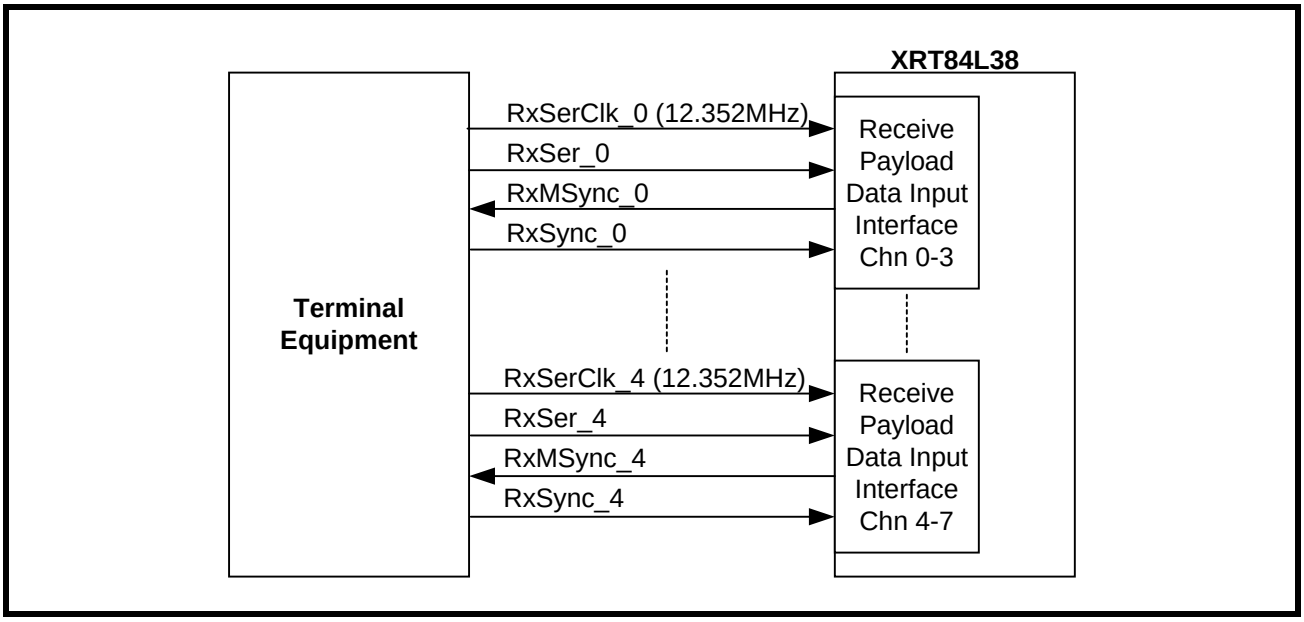
A_Y: The signaling bit A of Channel Y

4. Following the same rules of Step 2 and 3, the Receive High-speed Back-plane Interface maps the payload data and signaling data of four channels into a 12.352Mbit/s data stream.

The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH for one clock cycle at the first bit position (F-bit of channel 0) of the data stream with data from Channel 0-3 multiplexed together. The Receive Single-frame Synchronization signal of Channel 4 pulses HIGH for one clock cycle at the first bit position (F-bit of Channel 4) of the data stream with data from Channel 4-7 multiplexed together. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the Receive High-speed Back-plane Interface of the framer can identify the beginning of a multiplexed frame and can start sending payload data of that frame.

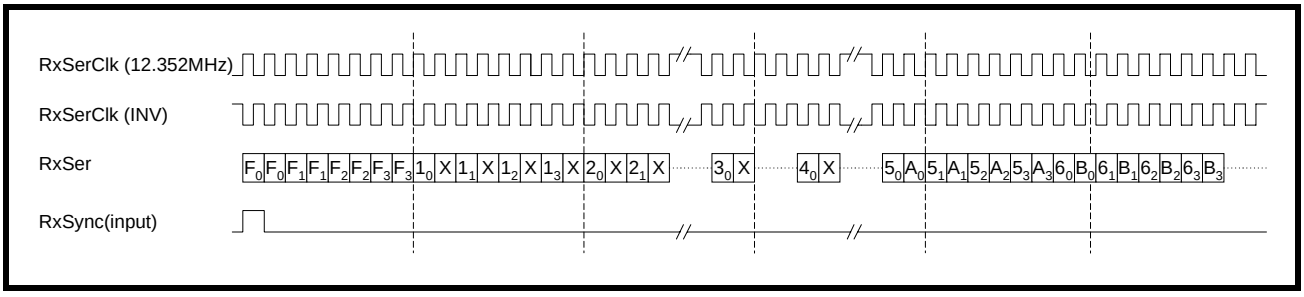
See Figure 55 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in 12.352Mbit/s mode.

FIGURE 55. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING 12.352MBIT/S DATA BUS



The Input signal timing is shown in Figure 56 below when the framer is running at 12.352Mbit/s mode.

FIGURE 56. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 12.352MBIT/S



5.1.3.5 T1 Receive Input Interface - Bit-Multiplexed 16.384Mbit/s

When the Receive Multiplex Enable bit is set to one and the Receive Interface Mode Select [1:0] bits are set to 01, the Receive Back-plane interface of framer is running at a clock rate of 16.384MHz.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane Interface is pumping out data through RxSer_0 or RxSer_4 pins at 16.384Mbit/s. It multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz are supplied to the Receive Serial Clock pin of Channel 0 and Channel 4 of the framer. The Receive High-speed Back-plane Interface of the farmer provides data at rising edge of this Receive Serial Clock. The local Terminal Equipment then latches incoming serial data at falling edge of the clock.

The Receive High-speed Back-plane Interface maps four 1.544Mbit/s DS1 data streams into this 16.384Mbit/s data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

F_X: F-bit of Channel X

2. After the first octet of data is sent, the Receive High-speed Back-plane Interface should insert seven octets (fifty-six bits) of "don't care" data into the outgoing data stream.
3. Payload data of four channels are repeated and grouped together in a bit-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the first payload bit of Timeslot 0 of Channel 1 and 2. The first payload bit of Timeslot 0 of Channel 3 is sent last. After the first bits of Timeslot 0 of all four channels are sent, it comes the second bit of Timeslot 0 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

NINTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	1_1	1_1	1_2	1_2	1_3	1_3

TENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
2_0	2_0	2_1	2_1	2_2	2_2	2_3	2_3

XY: The Xth payload bit of Channel Y

4. The Receive High-speed Back-plane Interface also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream. When the Receive High-speed Back-plane Interface is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

THIRTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	5_1	A_1	5_2	A_2	5_3	A_3

FOURTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
6_0	B_0	6_1	B_1	6_2	B_2	6_3	B_3

FIFTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
7_0	C_0	7_1	C_1	7_2	C_2	7_3	C_3

SIXTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
8_0	D_0	8_1	D_1	8_2	D_2	8_3	D_3

X_Y: The Xth payload bit of Channel Y

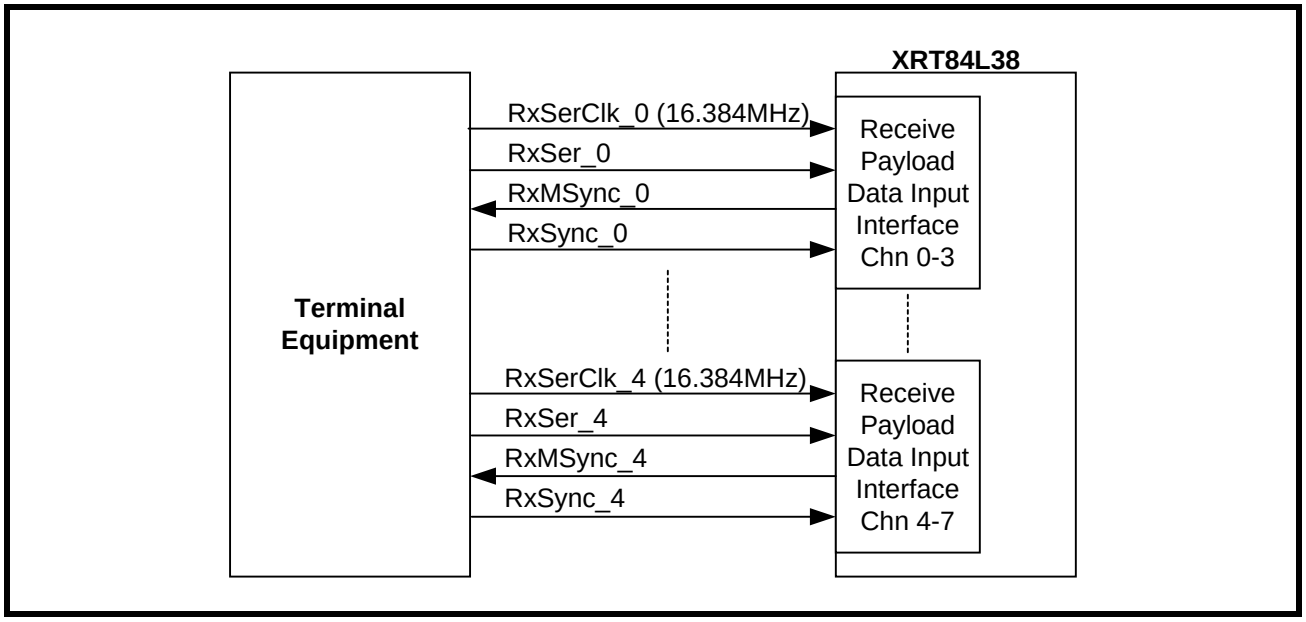
A_Y: The signaling bit A of Channel Y

5. After payload bits of Timeslot 0, 1 and 2 of all four channels are sent, the Receive High-speed Back-plane Interface should stuff another eight octets (sixty-four bits) of "don't care" data into the outgoing data stream.
6. Following the same rules of Step 2 to 5, the Receive High-speed Back-plane Interface stuffs eight octets of "don't care" data after sending twenty-four octets of multiplexed payload and signaling data. A 16.384Mbit/s data stream is thus created.

The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH for one clock cycle at the first bit position (F-bit of channel 0) of the data stream with data from Channel 0-3 multiplexed together. The Receive Single-frame Synchronization signal of Channel 4 pulses HIGH for one clock cycle at the first bit position (F-bit of Channel 4) of the data stream with data from Channel 4-7 multiplexed together. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the Receive High-speed Back-plane Interface of the framer can identify the beginning of a multiplexed frame and can start sending payload data of that frame.

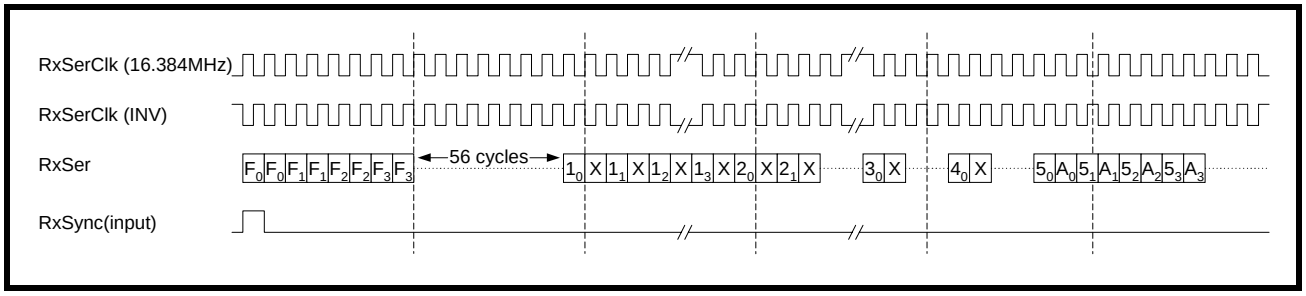
See Figure 57 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in Bit-multiplexed 16.384Mbit/s mode.

FIGURE 57. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 58 below when the framer is running at Bit-Multiplexed 16.384Mbit/s mode.

FIGURE 58. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT BIT-MULTIPLEXED 16.384MBIT/S



5.1.3.6 T1 Receive Input Interface - HMVIP 16.384Mbit/s

When the Receive Multiplex Enable bit is set to one and the Receive Interface Mode Select [1:0] bits are set to 10, the Receive Back-plane interface of framer is running at a clock rate of 16.384MHz.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane Interface is pumping out data through RxSer_0 or RxSer_4 pins at 16.384Mbit/s. The Receive High-speed Back-plane Interface multiplexes payload and signaling data of every four channels into

one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz are supplied to the Receive Serial Clock pin of Channel 0 and Channel 4 of the framer. The Receive High-speed Back-plane Interface of the farmer provides data at rising edge of this Receive Serial Clock. The local Terminal Equipment then latches incoming serial data at falling edge of the clock.

The Receive High-speed Back-plane Interface maps four 1.544Mbit/s DS1 data streams into this 16.384Mbit/s data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

FX: F-bit of Channel X

2. After the first octet of data is sent, the Receive High-speed Back-plane Interface insert seven octets (fifty-six bits) of "don't care" data into the outgoing data stream.
3. Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0 and so on. After all the bits of Timeslot 0 of Channel 0 is sent repeatedly, the Terminal Equipment will start sending the payload bits of Timeslot 0 of Channel 1 and 2. The payload bits of Timeslot 0 of Channel 3 are sent the last. After the payload bits of Timeslot 0 of all four channels are sent, it comes the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

NINTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0

ELEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1

THIRTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2

FIFTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3

XY: The Xth payload bit of Channel Y

4. The Receive High-speed Back-plane Interface also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream. When the Receive High-speed Back-plane Interface is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

TENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	6_0	B_0	7_0	C_0	8_0	D_0

TWELFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_1	A_1	6_1	B_1	7_1	C_1	8_1	D_1

FOURTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_2	A_2	6_2	B_2	7_2	C_2	8_2	D_2

SIXTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_3	A_3	6_3	B_3	7_3	C_3	8_3	D_3

X_Y: The Xth payload bit of Channel Y

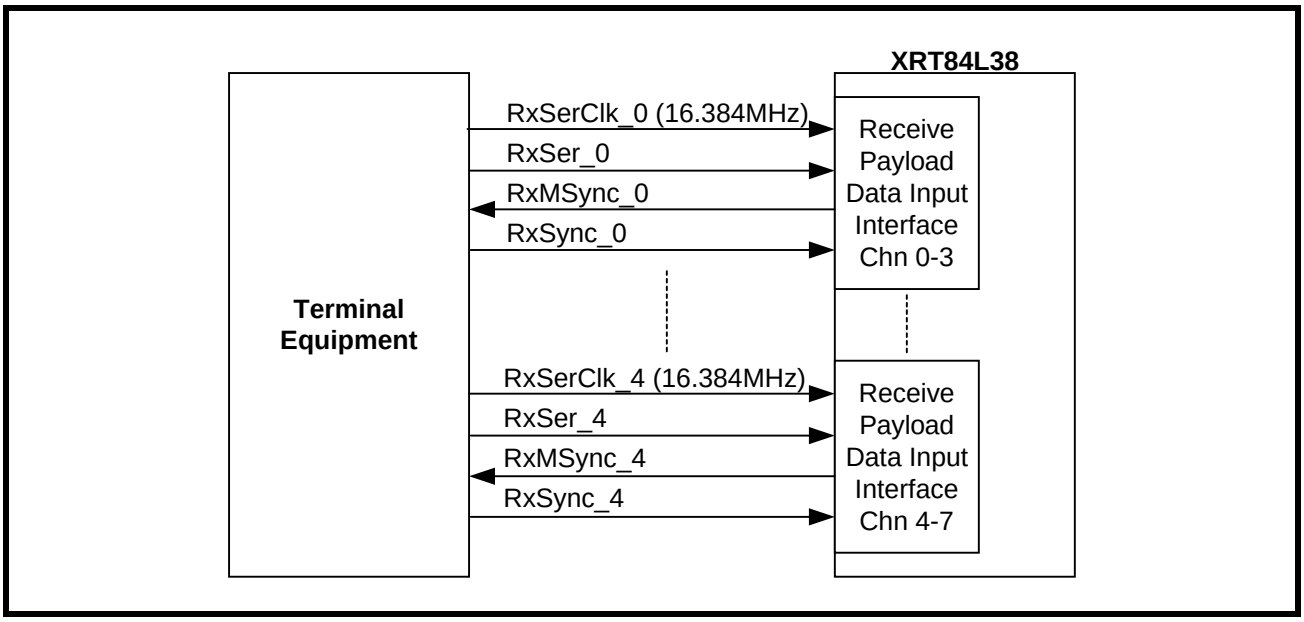
A_Y: The signaling bit A of Channel Y

5. After payload bits of Timeslot 0, 1 and 2 of all four channels are sent, the Receive High-speed Back-plane Interface should stuff another eight octets (sixty-four bits) of "don't care" data into the outgoing data stream.
6. Following the same rules of Step 2 to 5, Receive High-speed Back-plane Interface stuffs eight octets of "don't care" data after sending twenty-four octets of multiplexed payload and signaling data. A 16.384Mbit/s data stream is thus created.

The Receive Single-frame Synchronization signal should pulse HIGH for four clock cycles (the last two bit positions of the previous multiplexed frame and the first two bits of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the Receive High-speed Back-plane Interface of the framer can identify the beginning of a multiplexed frame and can start sending payload data of that frame.

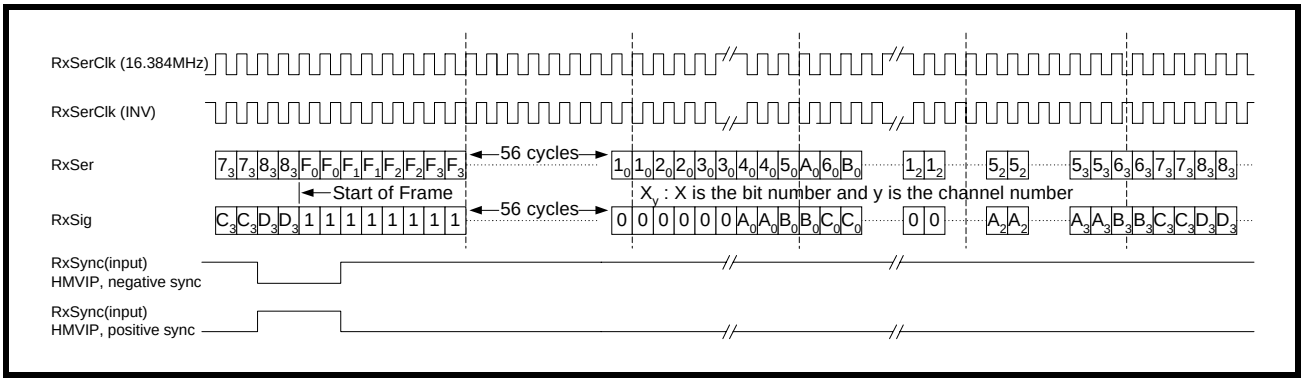
See Figure 59 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in HMVIP 16.384Mbit/s mode.

FIGURE 59. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 60 below when the framer is running at HMVIP 16.384Mbit/s mode.

FIGURE 60. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT HMVIP 16.384MBIT/S



5.1.3.7 T1 Receive Input Interface - H.100 16.384Mbit/s

When the Receive Multiplex Enable bit is set to one and the Receive Interface Mode Select [1:0] bits are set to 11, the Receive Back-plane interface of framer is running at H.100 16.384Mbit/s mode.

The HMVIP mode and the H.100 mode are essential the same except for the HIGH pulse position of the Receive Single-frame Synchronization Signal.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane Interface is pumping out data through RxSer_0 or RxSer_4 pins at 16.384Mbit/s. The Receive High-speed Back-plane Interface multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz are supplied to the Receive Serial Clock pin of Channel 0 and Channel 4 of the framer. The Receive High-speed Back-plane Interface of the farmer provides data at rising edge of this Receive Serial Clock. The local Terminal Equipment then latches incoming serial data at falling edge of the clock.

The Receive High-speed Back-plane Interface maps four 1.544Mbit/s DS1 data streams into this 16.384Mbit/s data stream as described below:

1. The F-bit of four channels are repeated and grouped together to form the first octet of the multiplexed data stream. The F-bit of Channel 0 is sent first, followed by F-bit of Channel 1 and 2. The F-bit of Channel 3 is sent last. The table below shows bit-pattern of the first octet.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
F_0	F_0	F_1	F_1	F_2	F_2	F_3	F_3

F_X: F-bit of Channel X

2. After the first octet of data is sent, the Receive High-speed Back-plane Interface insert seven octets (fifty-six bits) of "don't care" data into the outgoing data stream.
3. Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0 and so on. After all the bits of Timeslot 0 of Channel 0 is sent repeatedly, the Receive High-speed Back-plane Interface will start sending the payload bits of Timeslot 0 of Channel 1 and 2. The payload bits of Timeslot 0 of Channel 3 are sent the last. After the payload bits of Timeslot 0 of all four channels are sent,

it comes the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

NINTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0

ELEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1

THIRTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2

FIFTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3

X_Y: The Xth payload bit of Channel Y

4. The Receive High-speed Back-plane Interface also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream. When the Receive High-speed Back-plane Interface is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

TENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	6_0	B_0	7_0	C_0	8_0	D_0

TWELFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_1	A_1	6_1	B_1	7_1	C_1	8_1	D_1

FOURTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_2	A_2	6_2	B_2	7_2	C_2	8_2	D_2

SIXTEENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_3	A_3	6_3	B_3	7_3	C_3	8_3	D_3

X_Y: The Xth payload bit of Channel Y

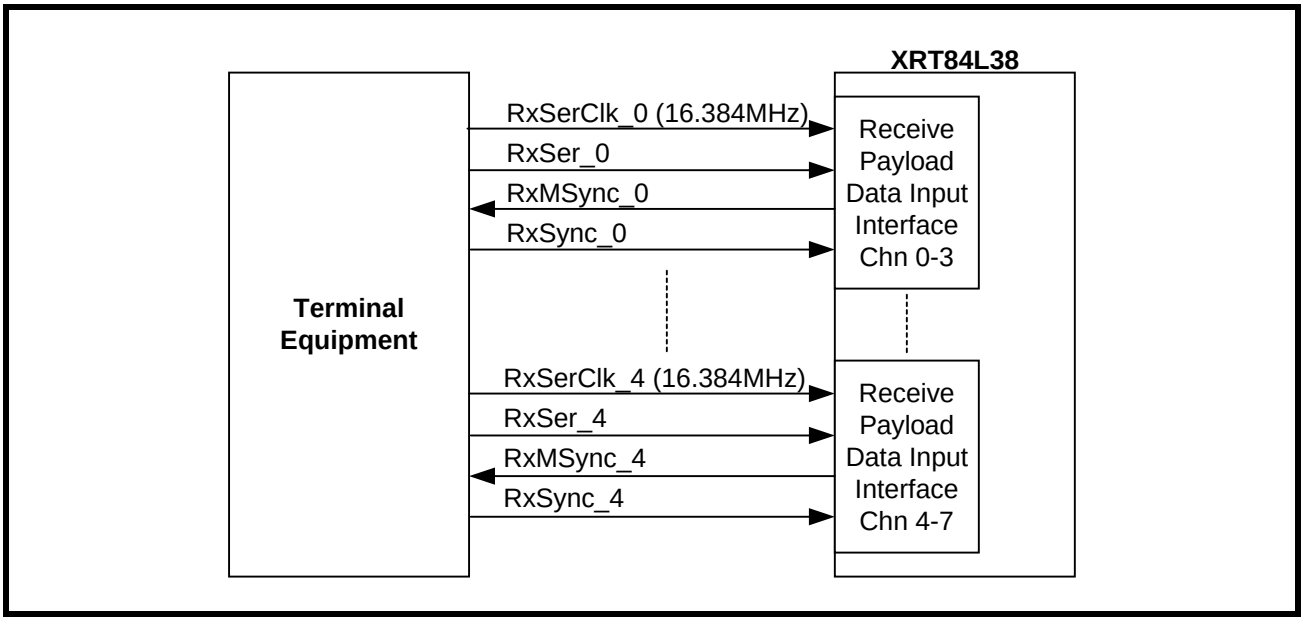
A_Y: The signaling bit A of Channel Y

5. After payload bits of Timeslot 0, 1 and 2 of all four channels are sent, the Terminal Equipment should stuff another eight octets (sixty-four bits) of "don't care" data into the outgoing data stream.
6. Following the same rules of Step 2 to 5, the Receive High-speed Back-plane Interface stuffs eight octets of "don't care" data after sending twenty-four octets of multiplexed payload and signaling data. A 16.384Mbit/s data stream is thus created.

The Receive Single-frame Synchronization signal should pulse HIGH for two clock cycles (the last bit position of the previous multiplexed frame and the first bit position of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the Receive High-speed Back-plane Interface of the framer can identify the beginning of a multiplexed frame and can start sending payload data of that frame.

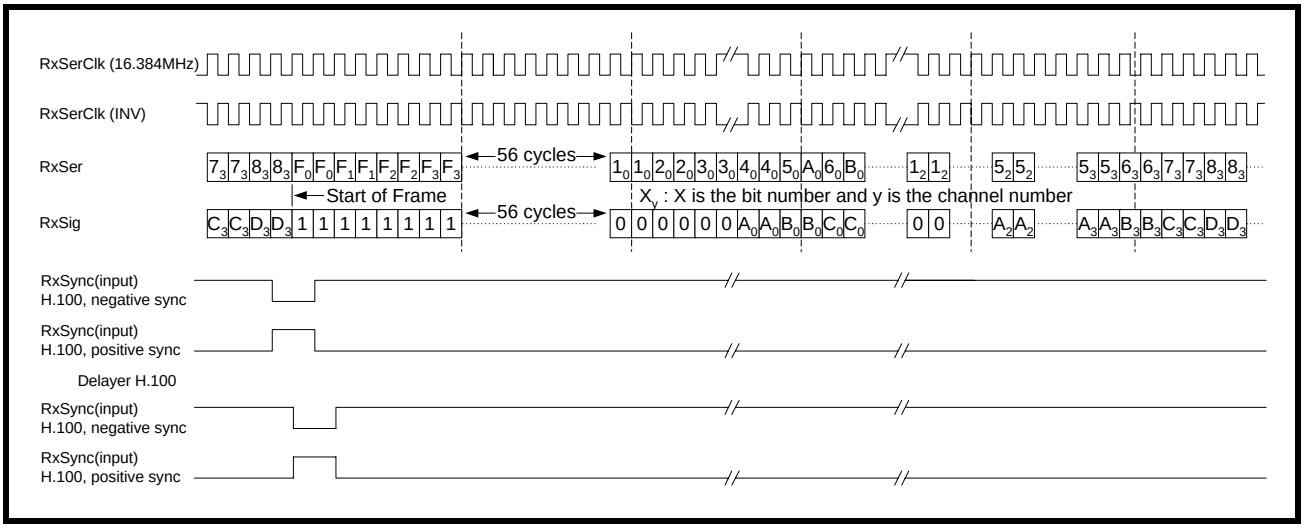
See Figure 61 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in H.100 16.384Mbit/s mode.

FIGURE 61. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING H.100 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 62 below when the framer is running at H.100 16.384Mbit/s mode.

FIGURE 62. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT H.100 16.384MBIT/S



6.0 THE E1 TRANSMIT SECTION

6.1 THE E1 TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK

6.1.1 Description of the Transmit Payload Data Input Interface Block

Each of the eight framers within the XRT84L38 device includes a Transmit Payload Data Input Interface block. The function of this block is to provide an interface to the local Terminal Equipment (for example, a Central Office or switching equipment) that has data to send to a "Far End" terminal over a DS1 or E1 transport medium.

The Payload Data Input Interface module (also known as the Back-plane Interface module) supports payload data to be taken from or presented to the system. In DS1 mode, supported data rates are 1.544Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 12.352Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s. In E1 mode, supported data rates are XRT84V24 compatible 2.048Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s.

The Transmit Payload Data Input Interface block supplies or accepts the following signals to the local Terminal Equipment circuitry:

- Transmit Serial Data Input (TxSer_n)
- Transmit Serial Clock (TxSerClk_n)
- Transmit Single-frame Synchronization Signal (TxSync_n)
- Transmit Multi-frame Synchronization Signal (TxMSync_n)
- Transmit Time-slot Indicator Clock (TxTSClk_n)
- Transmit Time-slot Indication Bits (TxTSb[4:0]_n)

The Transmit Serial Data is an input pin carrying payload, signaling and sometimes Data Link data supplied by the local Terminal Equipment to the XRT84L38 device.

The Transmit Serial Clock is an input or output signal used by the Transmit Payload Data Input Interface block to latch in incoming serial data from the local Terminal Equipment. The Transmit Clock Inversion bit of the Transmit Interface Control Register (TICR) determines at which edge of the Transmit Serial Clock would data transition on the Transmit Serial Data pin occur.

The table below shows configurations of the Transmit Clock Inversion bit of the Transmit Interface Control Register (TICR).

TRANSMIT INTERFACE CONTROL REGISTER (TICR) (INDIRECT ADDRESS = 0XN0H, 0X20H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Transmit Clock Inversion	R/W	0 - Serial data transition happens on rising edge of the Transmit Serial Clock. 1 - Serial data transition happens on falling edge of the Transmit Serial Clock.

Throughout the discussion of this datasheet, we assume that serial data transition happens on rising edge of the Transmit Serial Clock unless stated otherwise.

The Transmit Single-frame Synchronization signal is either input or output. When configured as input, it indicates the beginning of an E1 frame. When configured as output, it indicates the end of an E1 frame.

The Transmit Multi-frame Synchronization signal is either input or output. When configured as input, it indicates the beginning of an E1 multi-frame. When configure as output, it indicates the end of an E1 multi-frame.

The Transmit Input Clock signal is multiplexed into the Transmit Multi-frame Synchronization pin (TxMSync_n) of the XRT84L38. When the framer is running at High-speed Back-plane Interface mode, the Transmit Input Clock functions as the timing source for the High-speed Back-plane Interface.

By connecting these signals with the local Terminal Equipment, the Transmit Payload Data Input Interface accepts payload data from the Terminal Equipment and routes it to the Transmit Framer module inside the device.

6.1.2 Brief Discussion of the Transmit Payload Data Input Interface Block Operating at XRT84V24 Compatible 2.048Mbit/s mode

If the framer is operating in normal 2.048Mbit/s Back-plane interface mode for E1, timing source of the transmit section can be one of the three clocks:

- Transmit Serial Input Clock
- OSCCLK Driven Divided Clock
- Recovered Receive Line Clock

The Transmit Timing Source Select [1:0] bits of the Clock Select Register (CSR) determine which clock is used as the timing source. The following table shows configurations of the Transmit Timing Source Select [1:0] bits of the Clock Select Register.

CLOCK SELECT REGISTER (CSR) (INDIRECT ADDRESS = 0XN0H, 0X00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Timing Source Select	R/W	**Transmit Timing Source Select:** These two READ/WRITE bit-fields permit the user to select the timing source of Transmit section of the framer. When the Transmit Back-plane interface is operating at a clock rate of 2.048MHz for E1, these two READ/WRITE bit-fields also determine the direction of Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk). When the framer is operating at other Back-plane mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all inputs. 00 - The Recovered Receive Line Clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 2.048MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all outputs. Upon losing of the Recovered Receiver Line Clock, the OSCCLK Driven Divided clock is automatically chosen to be the timing source of the Transmit section of the framer. 01 - The Transmit Serial Clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 2.048MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all inputs. 10 - The OSCCLK Driven Divided clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 2.048MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all outputs. Upon losing of the Recovered Receiver Line Clock, the OSCCLK Driven Divided clock is automatically chosen to be the timing source of the Transmit section of the framer. 11 - The Recovered Receive Line Clock is the timing source of Transmit section of the framer. When operating at the non-multiplexed 2.048MHz Back-plane Interface mode, the Single Frame Synchronization Pulse (TxSync), Multi-frame Synchronization Pulse (TxMSync) and Transmit Serial Clock Input (TxSerClk) are all outputs. Upon losing of the Recovered Receiver Line Clock, the OSCCLK Driven Divided clock is automatically chosen to be the timing source of the Transmit section of the framer.

The Transmit Serial Clock (TxSerClk_n), Transmit Single-frame Synchronization Signal (TxSync_n) and Transmit Multi-frame Synchronization Signal (TxMSync_n) can be either inputs or outputs depend on the timing source of the Transmit section of the framer.

With the OSCCLK Driven Divided Clock or the Recovered Receive Line Clock being the timing source of the transmit section, the Transmit Serial Clock (TxSerClk_n), Transmit Single-frame Synchronization Signal (TxSync_n) and Transmit Multi-frame Synchronization Signal (TxMSync_n) are all outputs.

With the timing source of the transmit section being the Transmit Serial Input Clock, the Transmit Serial Clock (TxSerClk_n), Transmit Single-frame Synchronization Signal (TxSync_n) and Transmit Multi-frame Synchronization Signal (TxMSync_n) are all inputs.

The following table illustrates the input and output nature of these signals for different Transmit timing sources.

TRANSMIT TIMING SOURCE	TXSERCLK_N	TXSYNC_N	TXMSYNC_N
Terminal Equipment Driven TxSerClk	Input	Input	Input
OSCCLK Driven Divided Clock	Output	Output	Output
Recovered Receive Line Clock	Output	Output	Output

The Transmit Time-slot Indication Bits (TxTSb[4:0]_n) are multiplexed I/O pins. The functionality of these pins is governed by the value of Transmit Fractional E1 Input Enable bit of the Transmit Interface Control Register (TICR).

The following table illustrates the configurations of the Transmit Fractional E1 Input Enable bit.

TRANSMIT INTERFACE CONTROL REGISTER (TICR) (INDIRECT ADDRESS = 0XN0H, 0X20H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Transmit Fractional E1 Input Enable	R/W	0 - The Transmit Time-slot Indication bits (TxTSb[4:0] are outputting five-bit binary values of Time-slot number (0-31) being accepted and processed by the Transmit Payload Data Input Interface block of the framer. The Transmit Time-slot Indicator Clock signal (TxTSClk_n) is a 256KHz clock that pulses HIGH for one E1 bit period whenever the Transmit Payload Data Input Interface block is accepting the LSB of each of the twenty-four time slots. 1 - The TxTSb[0]_n bit becomes the Transmit Fractional E1 Input signal (TxFrTD_n) which carries Fractional E1 payload data into the framer. The TxTSb[1]_n bit becomes the Transmit Signaling Data Input signal (TxSig_n) which is used to insert robbed-bit signaling data into the outbound E1 frame. The TxTSb[2]_n bit serially outputs all five-bit binary values of the Time Slot number (0-31) being accepted and processed by the Transmit Payload Data Input Interface block of the framer. The TxTSb[3]_n bit becomes the Transmit Overhead Synchronization Pulse (TxOHSync_n) which is used to output an Overhead Synchronization Pulse that indicates the first bit of each E1multi-frame. The TxTSClk_n will output gaped fractional E1 clock that can be used by Terminal Equipment to clock out Fractional E1 payload data at rising edge of the clock. Or, The TxTSClk_n pin will be a clock enable signal to Transmit Fractional E1 Input signal (TxFrTD_n) when the un-gaped Transmit Serail Input Clock (TxSerClk_n) is used to clock in Fractional E1 Payload Data into the framer.

When configured to operate in normal condition (that is, when the Transmit Fractional E1 Input Enable bit is equal to zero), these bits reflect the five-bit binary value of the Time Slot number (0-31) being accepted and processed by the Transmit Payload Data Input Interface block of the framer. TxTSb[4] represents the MSB of the binary value and TxTSb[0] represents the LSB.

When the Transmit Fractional E1 Input Enable bit is equal to one, the TxTSb[0]_n bit becomes the Transmit Fractional E1 Input signal (TxFrTD_n). This input pin carries Fractional E1 Input data to be inserted into the outbound E1 data stream. The Fraction E1 Input Interface allows certain time-slots of outbound E1 data stream to have a different source other than the local Terminal Equipment. Function of the Fractional E1 Input signal will be discussed in details in later sections.

When the Transmit Fractional E1 Input Enable bit is equal to one, the TxTSb[1]_n bit becomes the Transmit Signaling Data Input signal (TxSig_n). These input pins can be used to insert robbed-bit signaling data into the

outbound E1 frame. Function of the Transmit Signaling Data Input signal will be discussed in details in later sections.

When the Transmit Fractional E1 Input Enable bit is equal to one, the TxTSb[2]_n bit serially outputs all five-bit binary values of the Time Slot number (0-31) being accepted and processed by the Transmit Payload Data Input Interface block of the framer. MSB of the binary value is presented first and the LSB is presented last.

When the Transmit Fractional E1 Input Enable bit is equal to one, the TxTSb[3]_n bit becomes the Transmit Overhead Synchronization Pulse (TxOHSync_n). These pins can be used to output an Overhead Synchronization Pulse that indicates the first bit of each E1multi-frame. Function of the Transmit Overhead Synchronization Output signal will be discussed in details in later sections.

The TxTSb[4]_n bit is not multiplexed.

The table below shows functionality of the TxTSb[3:0] bits when the Transmit Fractional E1 Input bit is set to different values.

TRANSMIT FRACTIONAL E1 INPUT BIT = 0		TRANSMIT FRACTIONAL E1 INPUT BIT = 1	
TxTSb[0]	Output	TxFrTD	Input
TxTSb[1]	Output	TxSig	Input
TxTSb[2]	Output	TxTS	Output
TxTSb[3]	Output	TxOHSync	Output

The Transmit Time-slot Indicator Clock signal (TxTSClk_n) is a multi-function output pin. When configured to operate in normal condition (that is, when the Transmit Fractional E1 Input Enable bit is equal to zero), the TxTSClk_n is a 256KHz clock that pulses HIGH for one E1 bit period whenever the Transmit Payload Data Input Interface block is accepting the LSB of each of the twenty-four time slots. The local Terminal Equipment should use this clock signal to sample the TxTSb[0] through TxTSb[4] bits and identify the time-slot being processed via the Transmit Section of the framer.

When the Transmit Fractional E1 Input Enable bit is equal to one, the TxTSClk_n will output gaped fractional E1 clock at time-slots where Fractional E1 Input data is present. This clock can be used by Terminal Equipment to clock out Fractional E1 payload data at rising edge of the clock. The framer will then input Fractional E1 payload data using falling edge of the clock. Otherwise, this pin can be configured as a clock enable signal to Transmit Fractional E1 Input signal (TxFrTD_n) if the framer is set accordingly. In this way, Fractional E1 payload data is clocked into the framer using un-gaped Transmit Serail Input Clock (TxSerClk_n). A detailed discussion of the Fractional E1 Payload Data Input Interface can be found in later sections.

Both the Transmit Time-slot Indicator Clock (TxTSClk_n) and the Transmit Time-slot Indication Bits (TxTSbb[4:0]_n) are output signals in normal 2.048Mbit/s Back-plane mode regardless of the timing source of the Transmit Section of framer.

A detailed discussion of how to connect the Transmit Payload Data Input Interface block to the local Terminal Equipment using different timing sources can be found in the later sections.

6.1.2.1 Connect the Transmit Payload Data Input Interface block to the Local Terminal Equipment if Transmit Timing Source = TxSerClk_n

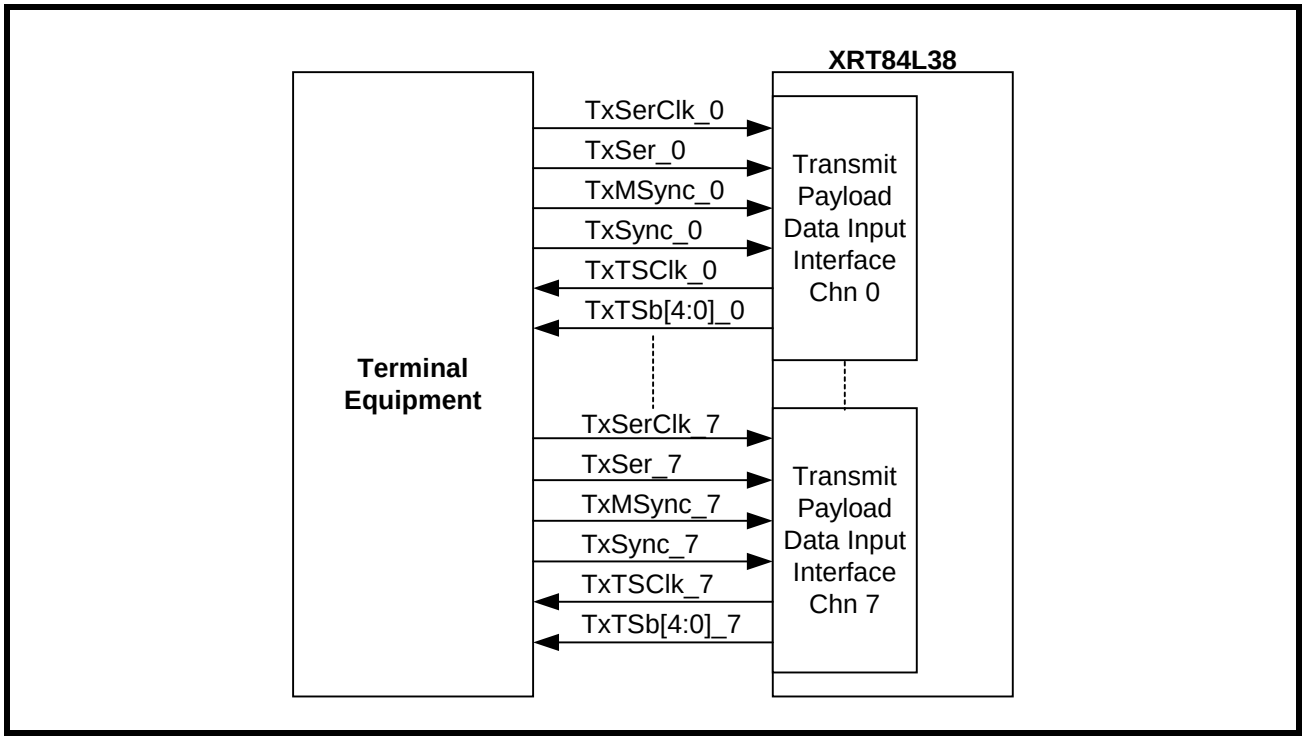
By setting the Transmit Timing Source [1:0] bits of the Clock Select Register to 01, the TxSerClk_n input signal is configured to be the timing source for the Transmit section of the framer. The Terminal Equipment should supply an external free-running clock with frequency of 2.048MHz to the TxSerClk_n input pin. The Transmit Single-frame Synchronization signal and the Transmit Multi-frame Synchronization signal are inputs to the framer.

The Transmit Single-frame Synchronization signal should pulse HIGH for one E1 bit period (488ns) at the first bit position of each E1 frame. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of an E1 frame.

The Transmit Multi-frame Synchronization signal should pulse HIGH for one E1 bit period (488ns) at the first bit position of the first frame of an E1 multi-frame. By sampling the HIGH pulse on the Transmit Multi-frame Synchronization signal, the framer can position the beginning of an E1 super-frame.

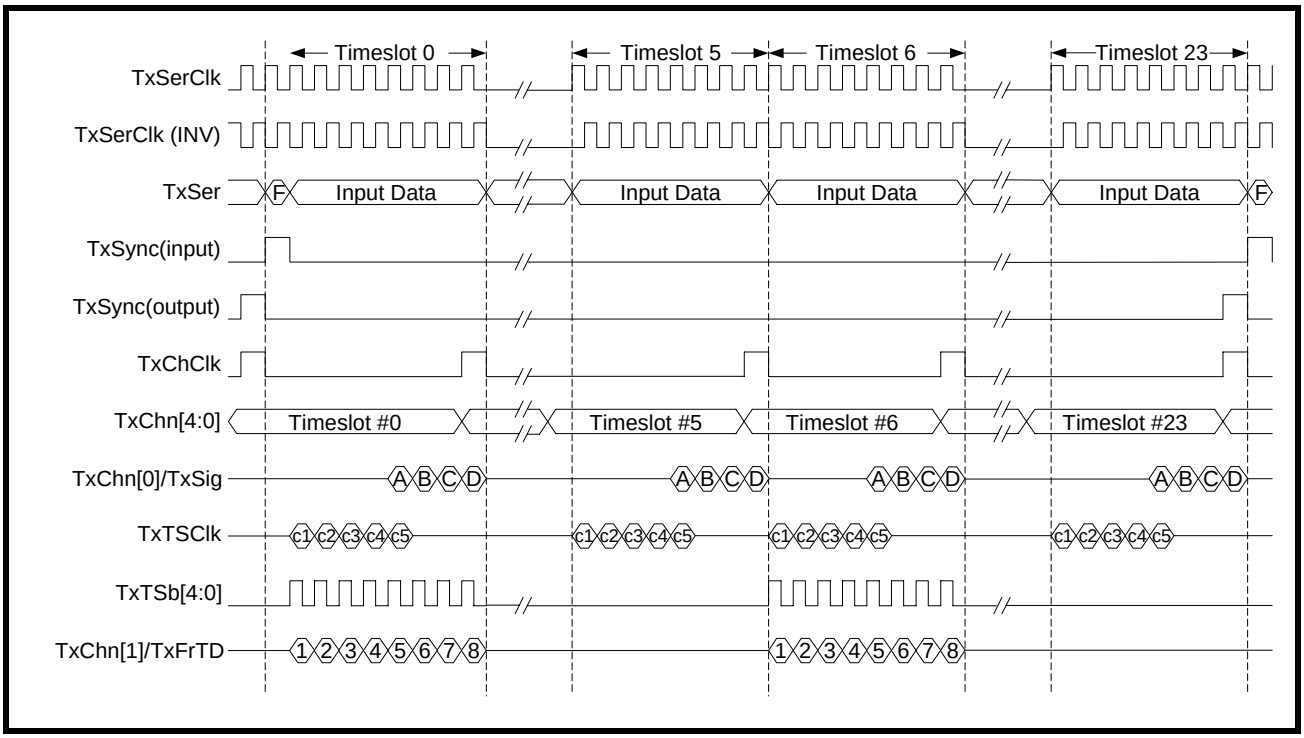
It is the responsibility of the Terminal Equipment to provide serial input data through the TxSer_n pin aligned with the Transmit Single-frame Synchronization signal and the Transmit Multi-frame Synchronization signal. See Figure 63 below for how to connect the Transmit Payload Data Input Interface block to the local Terminal Equipment with the Transmit Serial clock being the timing source of transmit section.

FIGURE 63. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT WITH TXSERCLK_N AS TRANSMIT TIMING SOURCE



The following Figure 64 shows waveforms of the signals (TxSerClk_n, TxSer_n, TxSync_n, TxTSClk_n and TxTSb[4:0]_n) that connecting the Transmit Payload Data Input Interface block to the local Terminal Equipment with the Transmit Serial clock being the timing source of transmit section.

FIGURE 64. WAVEFORMS OF THE SIGNALS THAT CONNECT THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WITH THE TRANSMIT SERIAL CLOCK BEING THE TIMING SOURCE OF THE TRANSMIT SECTION



6.1.2.2 Connect the Transmit Payload Data Input Interface block to the Local Terminal Equipment if the Transmit Timing Source = OSCCLK

By setting the Transmit Timing Source [1:0] bits of the Clock Select Register (CSR) to 10, the OSCCLK Driven Divided clock is configured to be the timing source for the Transmit section of the framer. A free-running clock should apply to the OSCCLK input pin with frequencies of 16.384MHz, 32.768MHz and 65.536MHz depending on the setting of OSCCLK Frequency Select [1:0] bits of the Clock Select Register (CSR).

The free-running OSCCLK is divided inside the XRT84L38 and routed to all eight framers. This OSCCLK Driven Divided Clock has to be 16.384MHz in frequency. When these bits are set to 00, the framer will internally divide the incoming OSCCLK by one. Therefore, the external oscillator clock applied to the OSCCLK pin should be 16.384MHz. When these bits are set to 01, the framer will internally divide the incoming OSCCLK by two. Therefore, the external oscillator clock applied to the OSCCLK pin should be 32.768MHz. When these bits are set to 10, the framer will internally divide the incoming OSCCLK by four. Therefore, the external oscillator clock applied to the OSCCLK pin should be 65.536MHz.

The following table shows configurations of the OSCCLK Frequency Select [1:0] bits of the Clock Select Register.

CLOCK SELECT REGISTER (CSR) (INDIRECT ADDRESS = 0XN0H, 0X00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	OSCCLK Frequency Select	R/W	These two READ/WRITE bit-fields permit the user to select internal clock dividing logic of the framer depending on the frequency of incoming oscillator clock (OSCCLK). The frequency of internal clock used by the framer should be 16.384MHz. 00 - The framer will internally divide the incoming OSCCLK by one. Therefore, the external oscillator clock applied to the OSCCLK pin should be 16.384MHz. 01 - The framer will internally divide the incoming OSCCLK by two. Therefore, the external oscillator clock applied to the OSCCLK pin should be 32.768MHz. 10 - The framer will internally divide the incoming OSCCLK by four. Therefore, the external oscillator clock applied to the OSCCLK pin should be 65.536MHz.

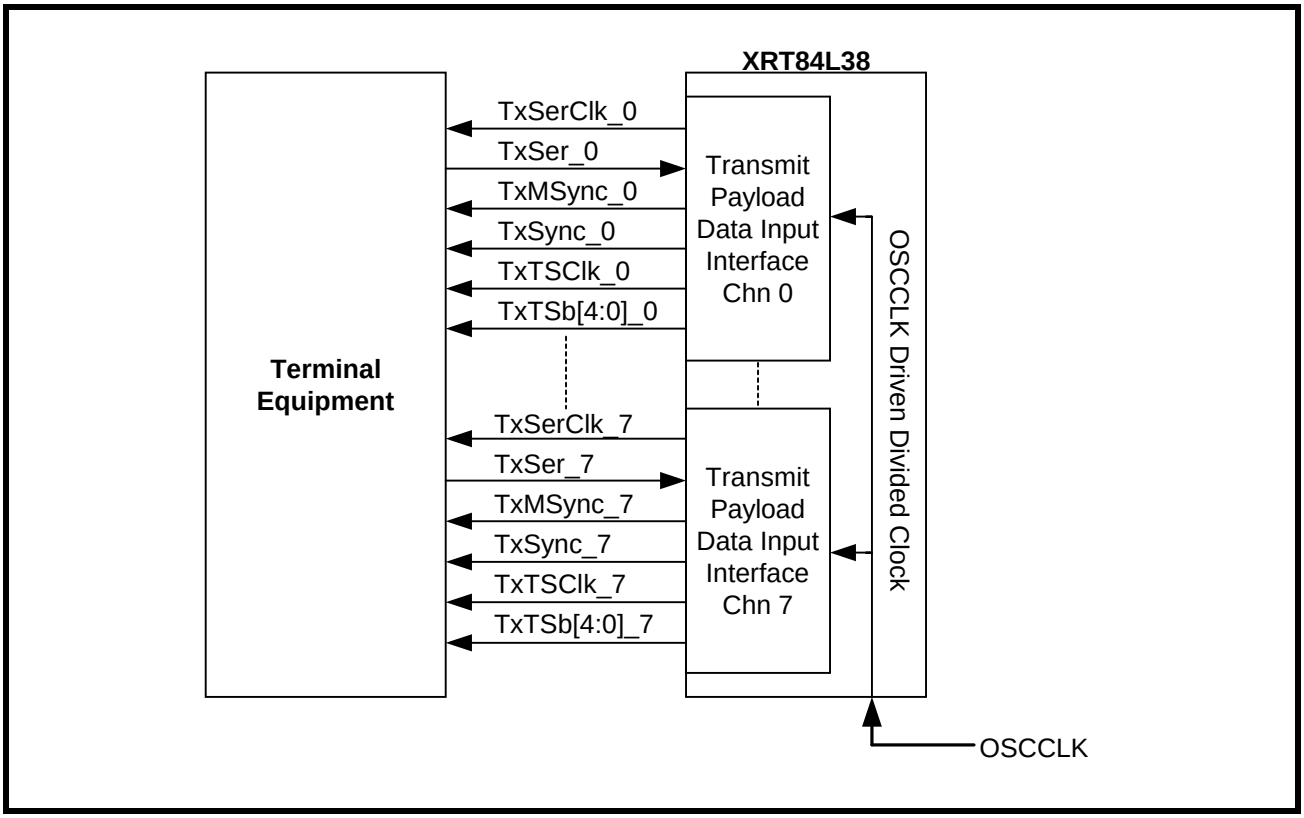
The Transmit Serial clock signal pin (TxSerClk_n) is output from the framer. The framer outputs a 2.048MHz clock through this pin to the local Terminal Equipment. The Transmit Single-frame Synchronization signal and the Transmit Multi-frame Synchronization signal are also automatically configured to be output signals.

The Transmit Single-frame Synchronization signal should pulse HIGH for one E1 bit period (488ns) at the last bit position of each E1 frame. By triggering on the HIGH pulse on the Transmit Single-frame Synchronization signal, the local Terminal Equipment can identify the end of an E1 frame and should start inserting payload data of the next E1 frame to the framer.

The Transmit Multi-frame Synchronization signal should pulse HIGH for one E1 bit period (488ns) at the last bit position of the last frame of an E1 multi-frame. By triggering on the HIGH pulse on the Transmit Multi-frame Synchronization signal, the local Terminal Equipment can identify the end of an E1 super-frame and should start inserting payload data of the next E1 multi-frame into the framer.

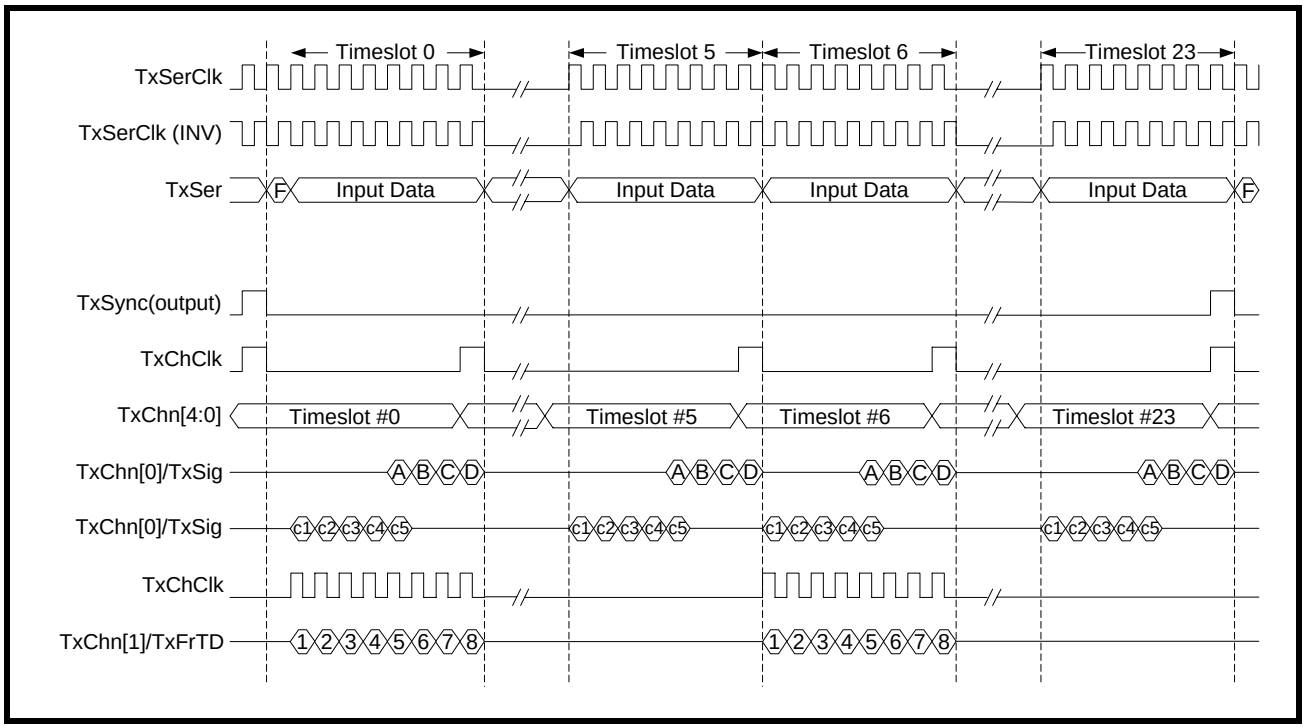
See Figure 65 for how to connect the Transmit Payload Data Input Interface block to the local Terminal Equipment with the OSCCLK Driven Divided clock as the timing source of transmit section.

FIGURE 65. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT WITH OSCCLK DRIVEN DIVIDED CLOCK AS TRANSMIT TIMING SOURCE



The following Figure 66 shows waveforms of the signals (TxSerClk_n, TxSer_n, TxSync_n, TxTSClk_n and TxTSb[4:0]_n) that connecting the Transmit Payload Data Input Interface block to the local Terminal Equipment with the OSCCLK Driven Divided clock as the timing source of transmit section.

FIGURE 66. WAVEFORMS OF THE SIGNALS CONNECTING THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WITH THE OSCCLK DRIVEN DIVIDED CLOCK AS THE TIMING SOURCE OF THE TRANSMIT SECTION



6.1.2.3 Connect the Transmit Payload Data Input Interface block to the Local Terminal Equipment for Loop-timing applications

If the Transmit Timing Source [1:0] bits of the Clock Select Register are set to 00 or 11, the Recovered Receive Line Clock is configured to be the timing source for the Transmit section of the framer. This is also known as the Loop-timing mode.

If the Clock Loss Detection Enable bit of the Clock Select Register is set to one, and if the Recovered Receive Line Clock from the LIU is lost, the framer will automatically begin to use the OSCCLK Driven Divided clock as transmit timing source until the LIU is able to regain clock recovery.

The following table shows configuration of the Clock Loss Detection Enable bit of the Clock Select Register (CSR).

CLOCK SELECT REGISTER (CSR) (INDIRECT ADDRESS = 0XN0H, 0X00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Clock Loss Detection Enable	R/W	This READ/WRITE bit-field permits the user to enable the Clock Loss Detection logic for the framer when the Recovered Receive Line Clock is used as transmit timing source of the framer. 0 - The framer disables the Clock Loss Detection logic. 1 - The framer enables the Clock Loss Detection logic. If the Recovered Receive Line Clock is used as transmit timing source of the framer, and if clock recovered from the LIU is lost, the framer can detect loss of the Recovered Receive Line Clock. Upon detecting of this occurrence, the framer will automatically begin to use the OSCCLK Driven Divided clock as transmit timing source until the LIU is able to regain clock recovery. ***NOTE:*** *This bit-field is ignored if the TxSerClk or the OSCCLK Driven Divided Clock is chosen to be the timing source of Transmit Section of the framer.*

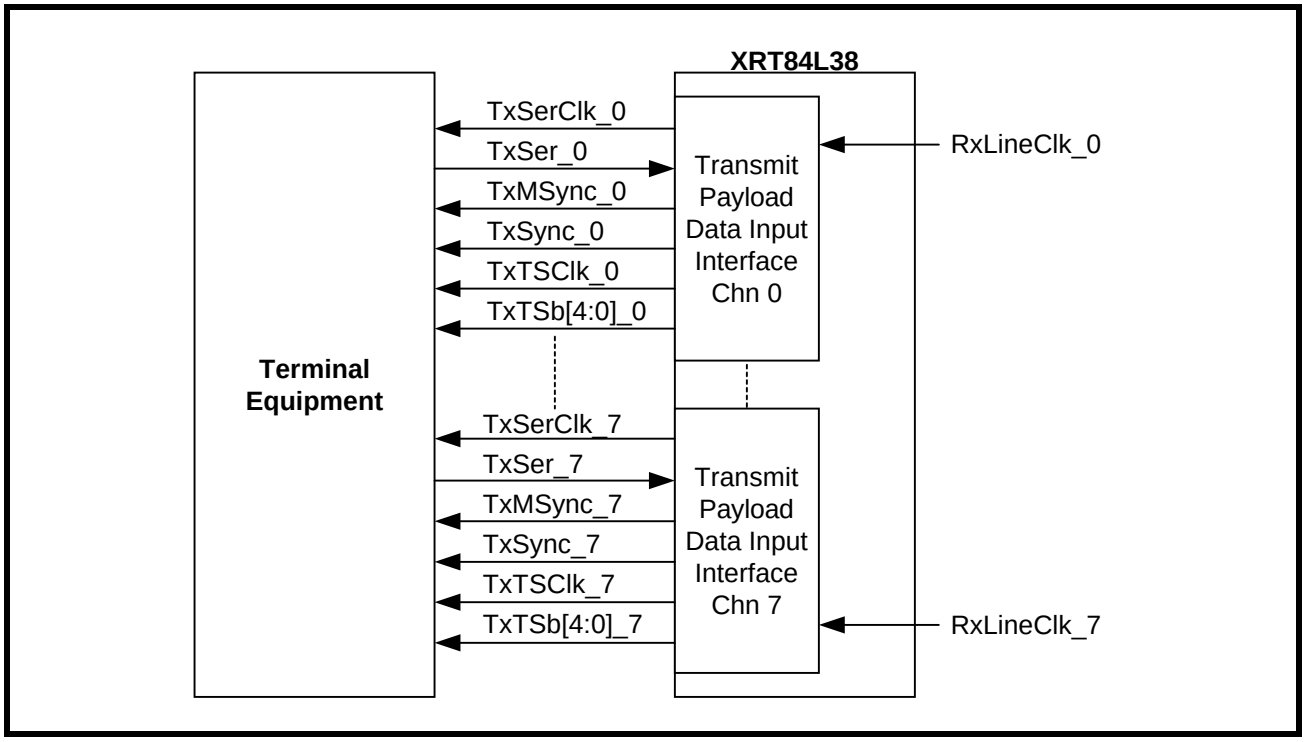
The Transmit Serial Clock signal pin (TxSerClk_n) is output from the framer. The XRT84L38 device routes the Recovered Receive Line Clock internally across the framer and output through the Transmit Serial Clock signal pin to the local Terminal Equipment. The Transmit Single-frame Synchronization signal and the Transmit Multi-frame Synchronization signal are automatically configured to be output signals.

The Transmit Single-frame Synchronization signal should pulse HIGH for one E1 bit period (488ns) at the last bit position of each E1 frame. By triggering on the HIGH pulse on the Transmit Single-frame Synchronization signal, the local Terminal Equipment can identify the end of an E1 frame and should start inserting payload data of the next E1 frame to the framer.

The Transmit Multi-frame Synchronization signal should pulse HIGH for one E1 bit period (488ns) at the last bit position of the last frame of an E1 multi-frame. By triggering on the HIGH pulse on the Transmit Multi-frame Synchronization signal, the local Terminal Equipment can identify the end of an E1 super-frame and should start inserting payload data of the next E1 multi-frame into the framer.

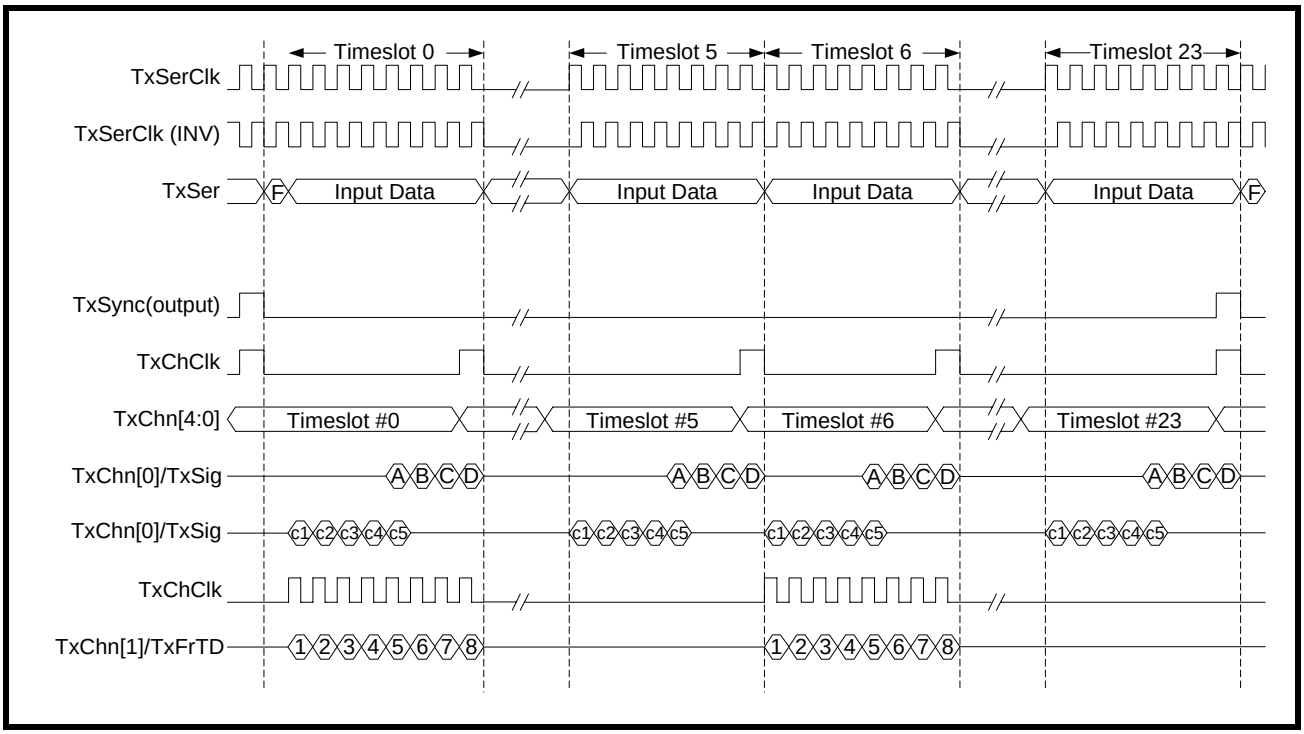
See Figure 67 for how to connect the Transmit Payload Data Input Interface block to the local Terminal Equipment with the Recovered Receive Line Clock being the timing source of transmit section.

FIGURE 67. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT WITH RECOVERED RECEIVE LINE CLOCK AS TRANSMIT TIMING SOURCE



The following Figure 68 shows waveforms of the signals (TxSerClk_n, TxSer_n, TxSync_n, TxTSClk_n and TxTSb[4:0]_n) that connecting the Transmit Payload Data Input Interface block to the local Terminal Equipment with the Recovered Receive Line Clock being the timing source of transmit section.

FIGURE 68. WAVERFORMS OF THE SIGNALS CONNECTING THE TRANSMIT PAYLOAD DATA INPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WITH THE RECOVERED RECEIVE LINE CLOCK BEING THE TIMING SOURCE OF TRANSMIT SECTION



6.1.3 Brief Discussion of the Transmit High-Speed Back-Plane Interface

The High-speed Back-plane Interface supports payload data to be taken from or presented to the Terminal Equipment at different data rates. In E1 mode, supported High-speed data rates are MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s. The Transmit Multiplex Enable bit and the Transmit Interface Mode Select [1:0] bits of the Transmit Interface Control Register (TICR) determine the Transmit Back-plane Interface data rate.

The following table shows configurations of the Transmit Multiplex Enable bit and the Transmit Interface Mode Select [1:0] bits of the Transmit Interface Control Register (TICR).

TRANSMIT INTERFACE CONTROL REGISTER (TICR) (INDIRECT ADDRESS = 0XN0H, 0X20H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Transmit Multiplex Enable	R/W	0 - The Transmit Back-plane Interface block is configured to non-channel-multiplexed mode 1 - The Transmit Back-plane Interface block is configured to channel-multiplexed mode
1-0	Transmit Interface Mode Select	R/W	When combined with the Transmit Multiplex Enable bit, these bits determine the Transmit Back-plane Interface data rate.

The table below shows the combinations of Transmit Multiplex Enable bit and Transmit Interface Mode Select [1:0] bits and the resulting Transmit Back-plane Interface data rates.

TRANSMIT MULTIPLEX ENABLE BIT	TRANSMIT INTERFACE MODE SELECT BIT 1	TRANSMIT INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE
0	0	0	XRT84V24 Compatible 2.048Mbit/s
0	0	1	MVIP 2.048Mbit/s
0	1	0	4.096Mbit/s
0	1	1	8.192Mbit/s
1	0	0	-
1	0	1	Bit Multiplexed 16.384Mbit/s
1	1	0	HMVIP 16.384Mbit/s
1	1	1	H.100 16.384Mbit/s

When the Transmit Multiplex Enable bit is set to zero, the framer is configured in non-channel-multiplexed mode. The possible data rates are XRT84V24 Compatible 2.048Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s and 8.192Mbit/s. In non-channel-multiplexed mode, payload data of each channel are taken from the Terminal Equipment separately. Each channel uses its own Transmit Serial Clock, Transmit Serial Data, Transmit Single-frame Synchronization signal and Transmit Multi-frame Synchronization signal as interface between the framer and the Terminal Equipment. Section 1.1.2.1, 1.1.2.2 and 1.1.2.3 provide details on how to connect the Transmit Payload Data Interface block with the Terminal Equipment when the Back-plane interface data rate is 1.544Mbit/s.

When the Back-plane interface data rate is MVIP 2.048Mbit/s, 4.096Mbit/s and 8.192Mbit/s, the Transmit Serial Clock, Transmit Serial Data, Transmit Single-frame Synchronization signal and Transmit Multi-frame Synchronization signal are all configured as inputs. The Transmit Serial Clock is always an input clock with frequency of 2.048 MHz for all data rates. The TxMSync_n signal is configured as the Transmit Input Clock with frequencies of 2.048 MHz, 4.096 MHz and 8.192 MHz respectively. It serves as the primary clock source for the High-speed Back-plane Interface.

The table below summaries the clock frequencies of TxSerClk_n and TxInClk_n inputs when the framer is operating in non-multiplexed High-speed Back-plane mode.

TRANSMIT MULTIPLEX ENABLE BIT = 0

TRANSMIT INTERFACE MODE SELECT BIT 1	TRANSMIT INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE	TXSERCLK	TXMSYNC/TXINCLK
0	0	2.048Mbit/s	2.048 MHz	-
0	1	MVIP 2.048Mbit/s	2.048 MHz	2.048 MHz
1	0	4.096Mbit/s	2.048 MHz	4.096 MHz
1	1	8.192Mbit/s	2.048 MHz	8.192 MHz

When the Transmit Multiplex Enable bit is set to one, the framer is configured in channel-multiplexed mode. The possible data rates are bit-multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s and H.100 16.384Mbit/s. In channel-multiplexed mode, every four channels share the Transmit Serial Data and Transmit Single-frame Synchronization signal of one channel as interface between the framer and the local Terminal Equipment. The TxMSync_n signal of one channel is configured as the Transmit Input Clock with frequencies of 16.384 MHz. It serves as the primary clock source for the High-speed Back-plane Interface.

Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4. The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH at the beginning of the frame with data from Channel 0-3 multiplexed together. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH at the beginning of the frame with data from Channel 4-7 multiplexed together. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse. Additionally, each channel requires the local Terminal Equipment to provide a free-running 2.048 MHz clock into the Transmit Serial Clock input.

The table below summaries the clock frequencies of TxSerClk_n and TxInClk_n inputs when the framer is operating in multiplexed High-speed Back-plane mode.

TRANSMIT MULTIPLEX ENABLE BIT = 1

TRANSMIT INTERFACE MODE SELECT BIT 1	TRANSMIT INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE	TXSERCLK	TXMSYNC/TXCLK
0	0	-	-	-
0	1	Bit-multiplexed 16.384Mbit/s	2.048 MHz	16.384 MHz
1	0	HMVIP 16.384Mbit/s	2.048 MHz	16.384 MHz
1	1	H.100 16.384Mbit/s	2.048 MHz	16.384 MHz

The Transmit Serial Clock is always running at 1.544MHz for all the High-speed Back-plane Interface modes. It is automatically the timing source of the Transmit Section of the framer in High-speed Back-plane Interface mode.

The Transmit Single-frame Synchronization signal should pulse HIGH or LOW for one bit period at the First bit position of each E1 frame. Length of the bit period depends on data rate of the High-speed Back-plane Interface. The Transmit Synchronization Pulse Low bit of the Transmit Interface Control Register (TICR) determines whether the Transmit Single-frame Synchronization signal is HIGH active or LOW active.

The table below shows configurations of the Transmit Synchronization Pulse LOW bit of the Transmit Interface Control Register (TICR).

TRANSMIT INTERFACE CONTROL REGISTER (TICR)(INDIRECT ADDRESS = 0XN0H, 0X20H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Transmit Synchronization Pulse LOW	R/W	0 - The Transmit Single-frame Synchronization signal will pulse HIGH indicating the beginning of an E1 frame when the High-speed Back-plane Interface is running at a mode other than the XRT84V24 Compatible 2.048Mbit/s. 1 - The Transmit Single-frame Synchronization signal will pulse LOW indicating the beginning of an E1 frame when the High-speed Back-plane Interface is running at a mode other than the XRT84V24 Compatible 2.048Mbit/s.

Throughout the discussion of this datasheet, we assume that the Transmit Single-frame Synchronization signal pulses HIGH unless stated otherwise.

The TxMSync_n signal, which is a multiplexed I/O pin, no longer functions as the Transmit Multi-frame Synchronization Signal. Indeed, it becomes the Transmit Input Clock signal (TxInClk) of the High-speed Back-plane Interface of the framer. The local Terminal Equipment should provide a free-running clock with the same frequency as the High-speed Back-plane Interface to this input pin.

The following sections discuss details of how to operate the framer in different Back-plane interface speed mode and how to connect the Transmit Payload Data Input Interface block to the local Terminal Equipment.

6.1.3.1 E1 Transmit Input Interface - MVIP 2.048 MHz

When the Transmit Multiplex Enable bit is set to zero and the Transmit Interface Mode Select [1:0] bits are set to 01, the Transmit Back-plane interface of framer is running at a data rate of 2.048Mbit/s.

The interface consists of the following pins:

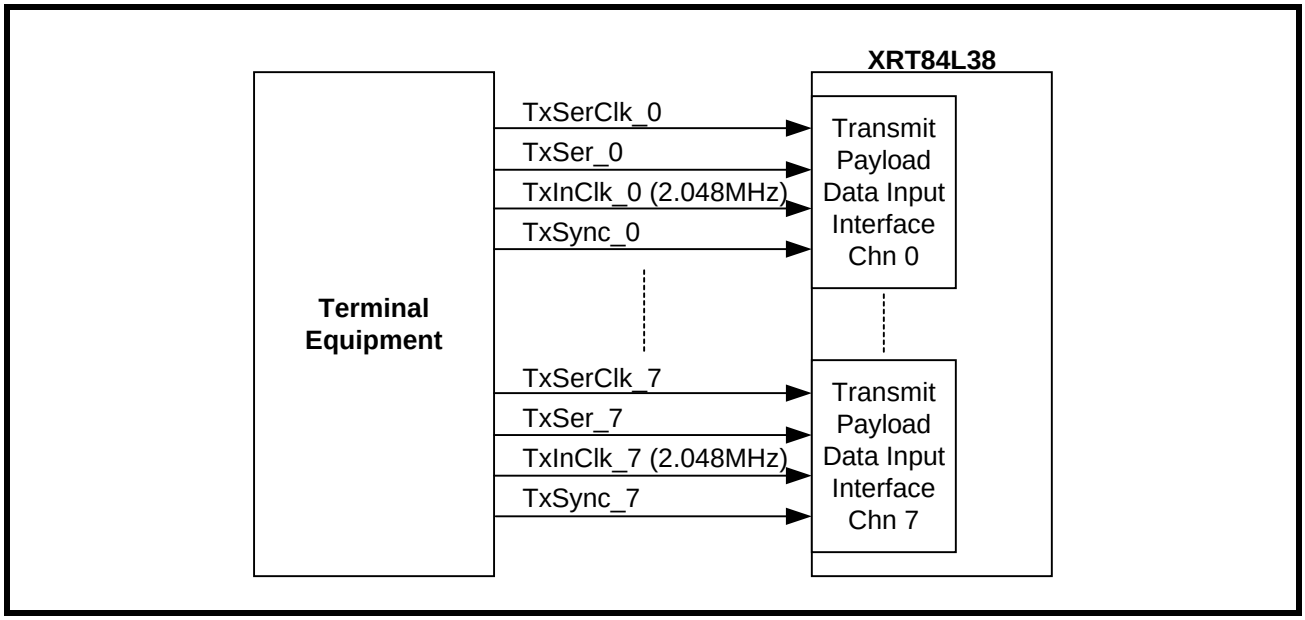
- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane interface is accepting data through TxSer_n at 2.048Mbit/s. The local Terminal Equipment supplies a free-running 2.048MHz clock to he Transmit Input Clock pin of the framer. The local Terminal Equipment also provides synchronized payload data at rising edge of the clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the Transmit Input Clock.

The Transmit Single-frame Synchronization input signal (TxSync_n) should pulse HIGH at the beginning of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of an E1 frame. It is responsibility of the local Terminal Equipment to align the Transmit Single-frame Synchronization signal with serial data stream going into the framer.

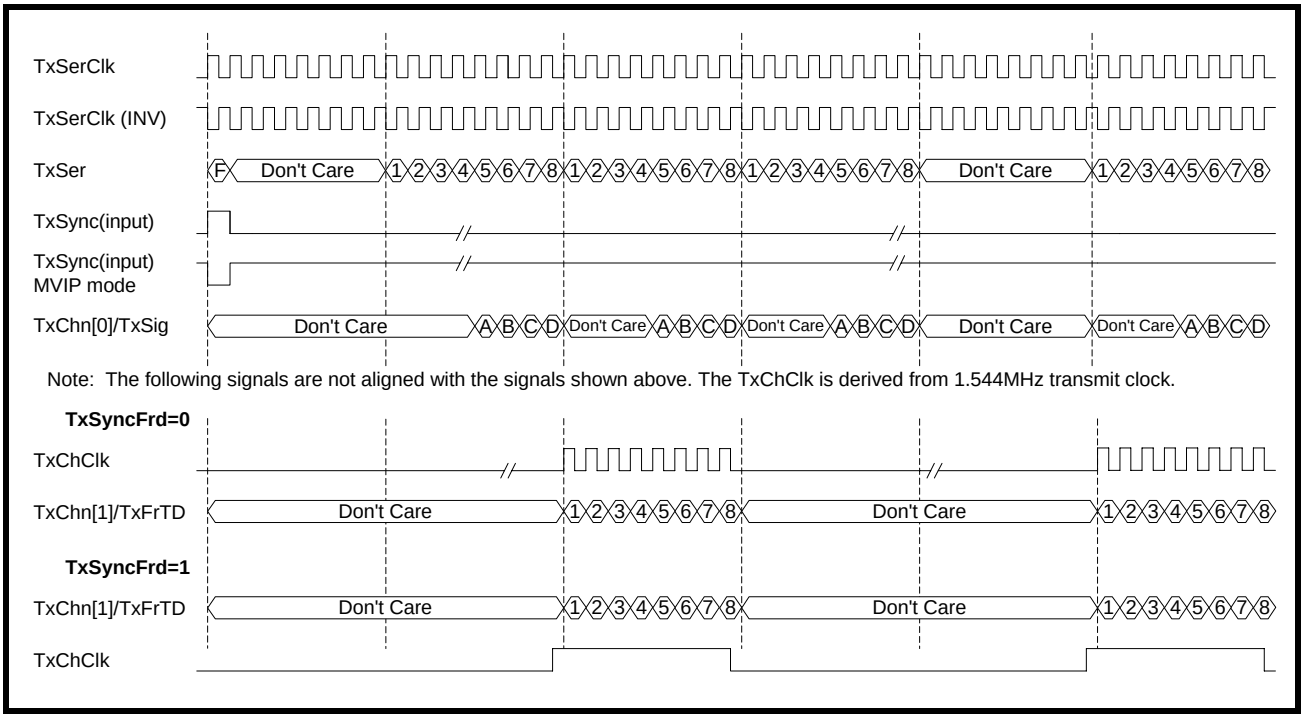
See Figure 69 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in MVIP 2.048Mbit/s mode.

FIGURE 69. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING MVIP 2.048MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at MVIP 2.048Mbit/s mode is shown in Figure 70.

FIGURE 70. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT MVIP 2.048MBIT/S



6.1.3.2 E1 Transmit Input Interface - 4.096 MHz

(This interface mode is the same as running at 2.048 MHz. The only difference is that the Transmit Input Clock runs two times faster at 4.096 MHz)

When the Transmit Multiplex Enable bit is set to zero and the Transmit Interface Mode Select [1:0] bits are set to 10, the Transmit Back-plane interface of framer is running at a clock rate of 4.096MHz.

The interface consists of the following pins:

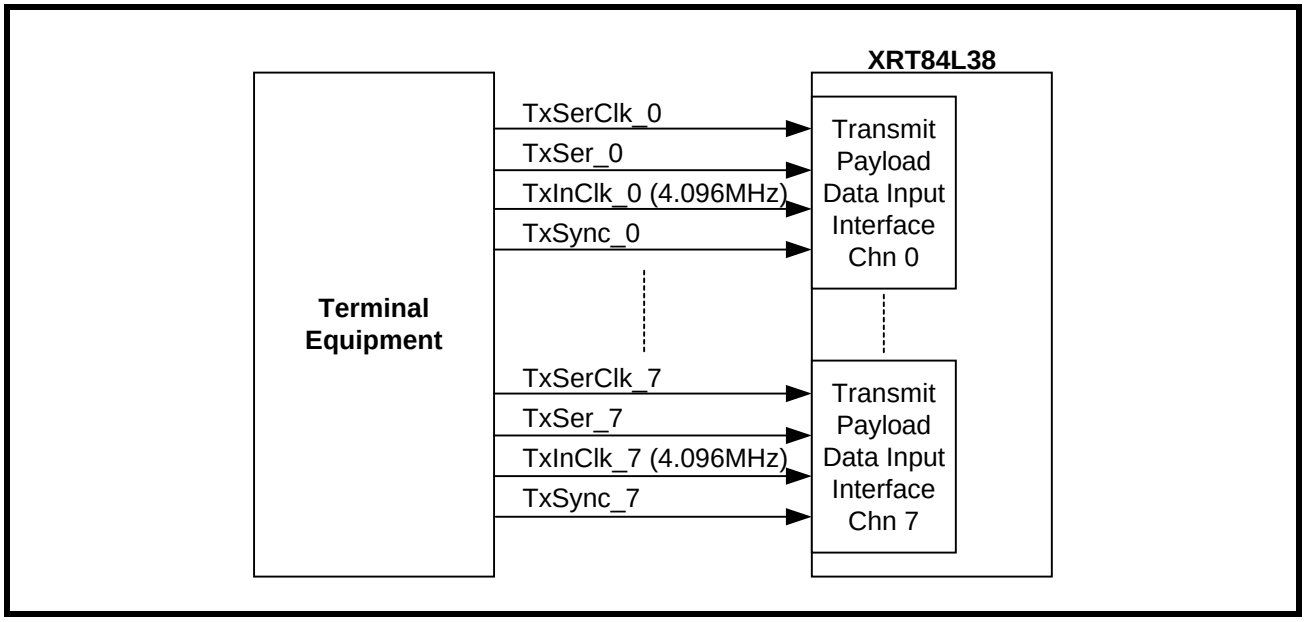
- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane interface is still accepting data through TxSer_n at an E1 equivalent data rate of 2.048Mbit/s. However, the local Terminal Equipment supplies a free-running 4.096MHz clock to the Transmit Input Clock pin of the framer. The local Terminal Equipment provides synchronized payload data at every other rising edge of the Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at every other falling edge of the clock.

Transmit Single-frame Synchronization input signal (TxSync_n) should pulse HIGH at the beginning of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of an E1 frame. It is responsibility of the local Terminal Equipment to align the Transmit Single-frame Synchronization signal with serial data stream going into the framer.

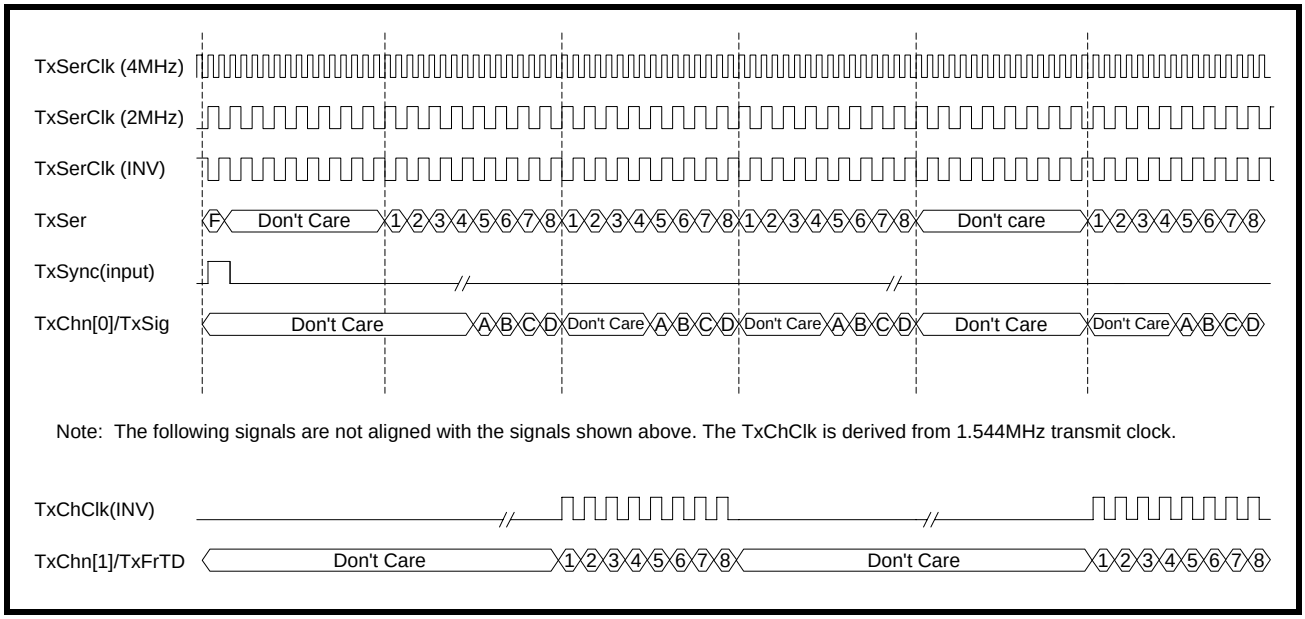
See Figure 71 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in 4.096Mbit/s mode.

FIGURE 71. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING 4.096MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at 4.096Mbit/s mode is shown in Figure 72.

FIGURE 72. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 4.096MBIT/S MODE



6.1.3.3 E1 Transmit Input Interface - 8.192 MHz

(This interface mode is the same as running at 2.048 MHz. The only difference is that the Transmit Input Clock runs four times faster at 8.192MHz)

When the Transmit Multiplex Enable bit is set to zero and the Transmit Interface Mode Select [1:0] bits are set to 11, the Transmit Back-plane interface of framer is running at a clock rate of 8.192MHz.

The interface consists of the following pins:

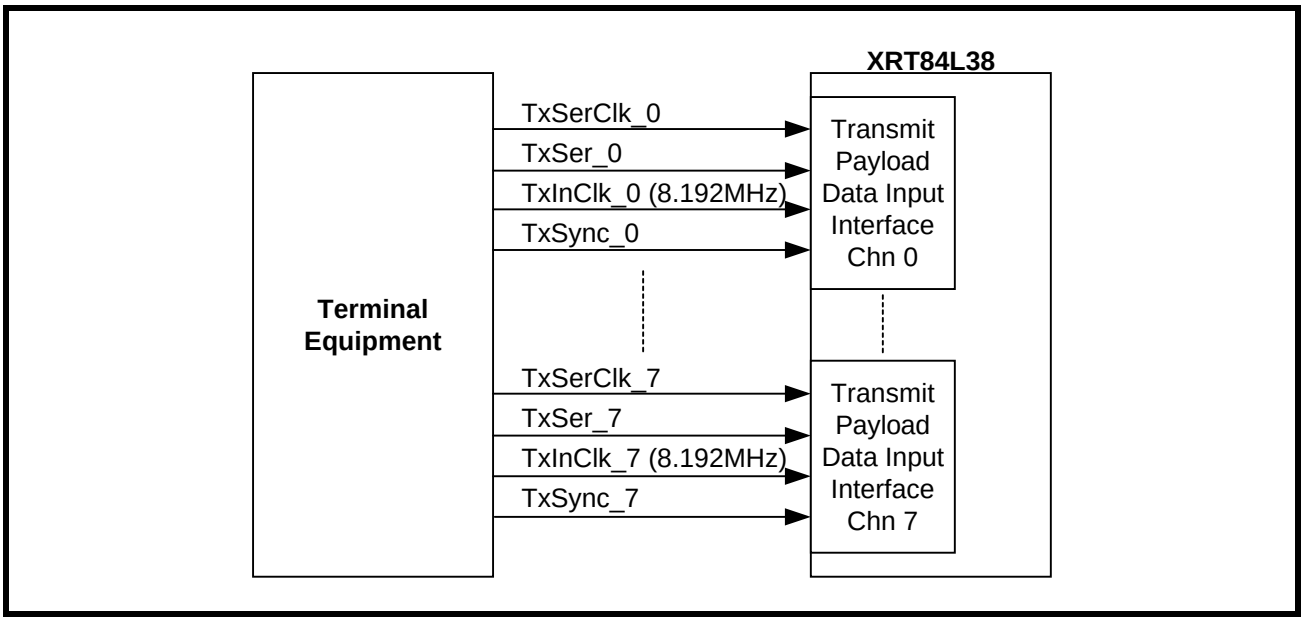
- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane interface is still accepting data through TxSer_n at an E1 equivalent data rate of 2.048Mbit/s. However, the local Terminal Equipment supplies a free-running 8.192MHz clock to the Transmit Input Clock pin of the framer. The local Terminal Equipment provides synchronized payload data at every other four rising edge of the Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at every other four falling edge of the clock.

The Transmit Single-frame Synchronization input signal (TxSync_n) should pulse HIGH at the beginning of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of an E1 frame. It is responsibility of the local Terminal Equipment to align the Transmit Single-frame Synchronization signal with serial data stream going into the framer.

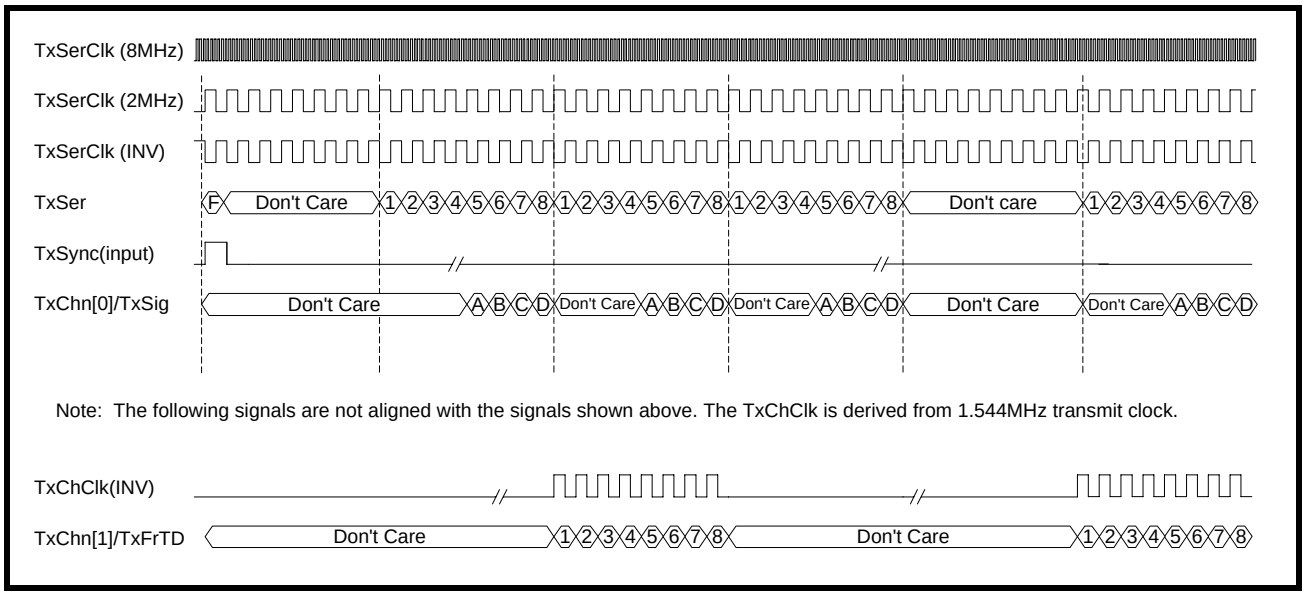
See Figure 73 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in 8.192Mbit/s mode.

FIGURE 73. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING 8.192MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at 8.192Mbit/s mode is shown in Figure 74.

FIGURE 74. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 8.192MBIT/S MODE



6.1.3.4 E1 Transmit Input Interface - Bit-Multiplexed 16.384Mbit/s

When the Transmit Multiplex Enable bit is set to one and the Transmit Interface Mode Select [1:0] bits are set to 01, the Transmit Back-plane interface of framer is running at a clock rate of 16.384MHz.

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane Interface is accepting data through TxSer_0 or TxSer_4 pins at 16.384Mbit/s. The local Terminal Equipment multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz is supplied to the Transmit Input Clock pin of Channel 0 and Channel 4 of the framer. The local Terminal Equipment provides multiplexed payload data at rising edge of this Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the clock.

The local Terminal Equipment maps four 2.048Mbit/s E1 data streams into this 16.384Mbit/s data stream as described below:

1. Payload data of four channels are repeated and grouped together in a bit-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the first payload bit of Timeslot 0 of Channel 1 and 2. The first payload bit of Timeslot 0 of Channel 3 is sent last.

After the first bits of Timeslot 0 of all four channels are sent, it comes the second bit of Timeslot 0 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	1_1	1_1	1_2	1_2	1_3	1_3

SECOND OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
2_0	2_0	2_1	2_1	2_2	2_2	2_3	2_3

X_Y: The Xth payload bit of Channel Y

2. The local Terminal Equipment also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream.

When the Terminal Equipment is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

FIFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	5_1	A_1	5_2	A_2	5_3	A_3

SIXTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
6_0	B_0	6_1	B_1	6_2	B_2	6_3	B_3

SEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
7_0	C_0	7_1	C_1	7_2	C_2	7_3	C_3

EIGHTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
8_0	D_0	8_1	D_1	8_2	D_2	8_3	D_3

X_Y: The Xth payload bit of Channel Y

A_Y: The signaling bit A of Channel Y

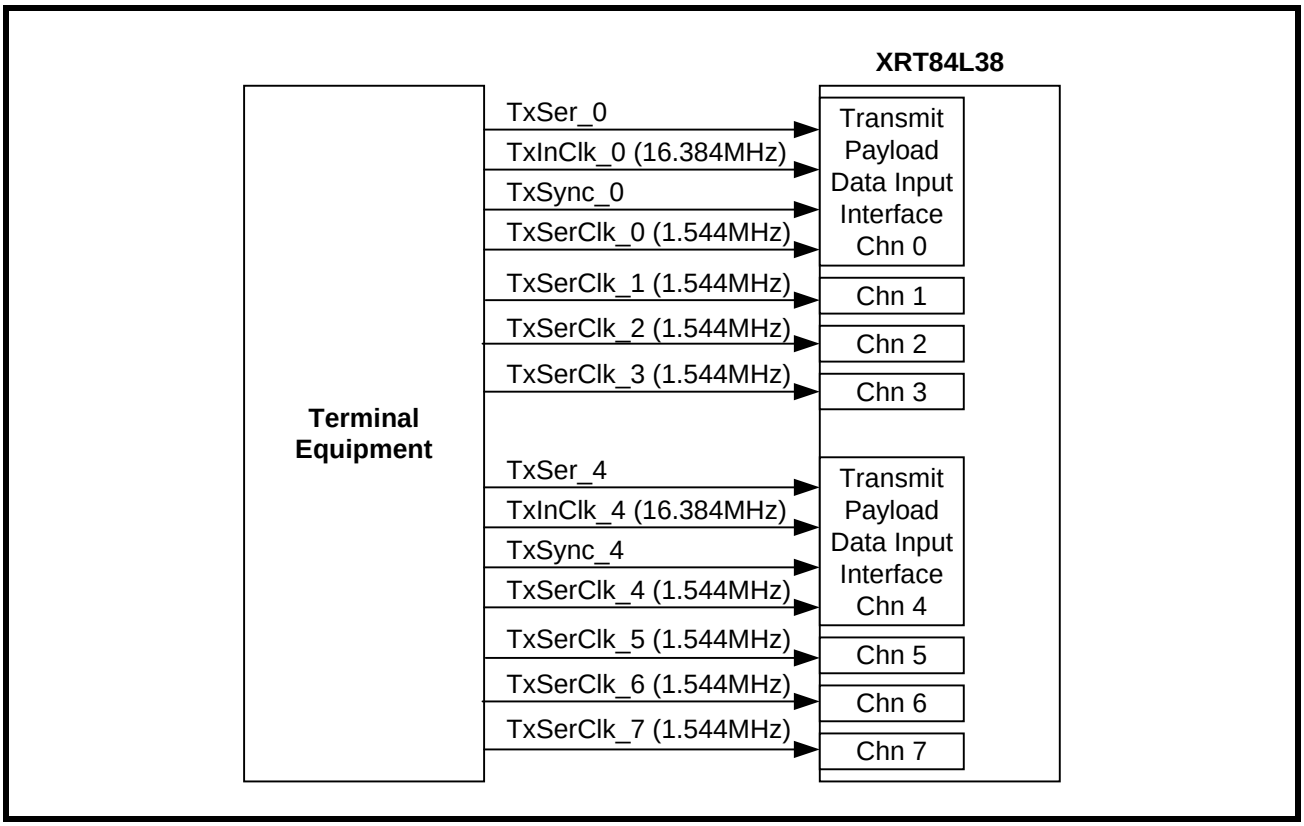
3. After the first octet of all four channels are sent, the local Terminal Equipment start sending the second octets following the same rules of Step 1 and 2.

The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH for one clock cycle at the first bit position of the data stream with data from Channel 0-3 multiplexed together. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH for one clock cycle at the first bit position of the data stream with data from Channel 4-7 multiplexed together. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of the multiplexed E1 frame. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT84L38 device and send to each individual channel. These data will be processed by each individual framer and send to LIU interface. The local Terminal Equipment provides a free-running 1.544MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

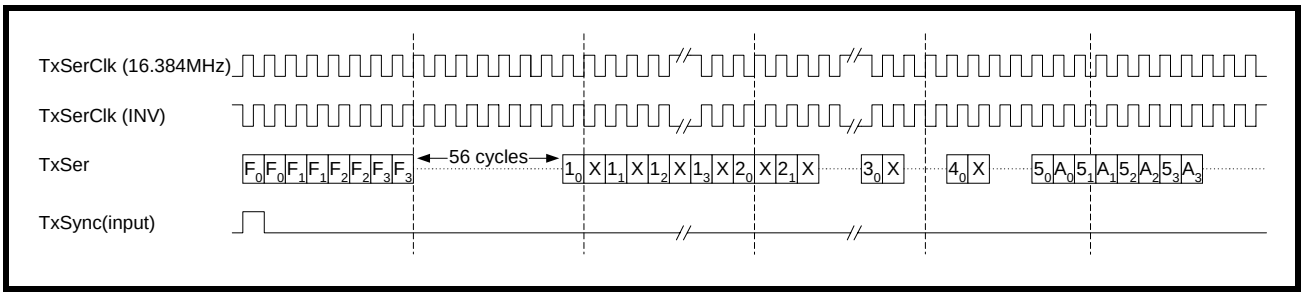
See Figure 75 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in Bit-multiplexed 16.384Mbit/s mode.

FIGURE 75. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 76 below when the framer is running at Bit-Multiplexed 16.384Mbit/s mode.

FIGURE 76. IMING SIGNAL WHEN THE FRAMER IS RUNNING AT BIT-MULTIPLEXED 16.384MBIT/S MODE



6.1.3.5 E1 Transmit Input Interface - HMVIP 16.384Mbit/s

When the Transmit Multiplex Enable bit is set to one and the Transmit Interface Mode Select [1:0] bits are set to 10, the Transmit Back-plane interface of framer is running at a clock rate of 16.384MHz.

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)

- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane Interface is accepting data through TxSer_0 or TxSer_4 pins at 16.384Mbit/s. The local Terminal Equipment multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz is supplied to the Transmit Input Clock pin of Channel 0 and Channel 4 of the framer. The local Terminal Equipment provides multiplexed payload data at rising edge of this Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the clock.

The local Terminal Equipment maps four 2.048Mbit/s E1 data streams into this 16.384Mbit/s data stream as described below:

1. Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0 and so on. After all the bits of Timeslot 0 of Channel 0 is sent repeatedly, the Terminal Equipment will start sending the payload bits of Timeslot 0 of Channel 1 and 2. The payload bits of Timeslot 0 of Channel 3 are sent the last.

After the payload bits of Timeslot 0 of all four channels are sent, it comes the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0

THIRD OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1

FIFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2

SEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3

X_Y: The Xth payload bit of Channel Y

2. The local Terminal Equipment also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream.

When the Terminal Equipment is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

SECOND OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	6_0	B_0	7_0	C_0	8_0	D_0

FOURTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_1	A_1	6_1	B_1	7_1	C_1	8_1	D_1

SIXTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_2	A_2	6_2	B_2	7_2	C_2	8_2	D_2

EIGHTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_3	A_3	6_3	B_3	7_3	C_3	8_3	D_3

X_Y: The Xth payload bit of Channel Y

A_Y: The signaling bit A of Channel Y

3. After the first octet of all four channels are sent, the local Terminal Equipment start sending the second octets following the same rules of Step 1 and 2.

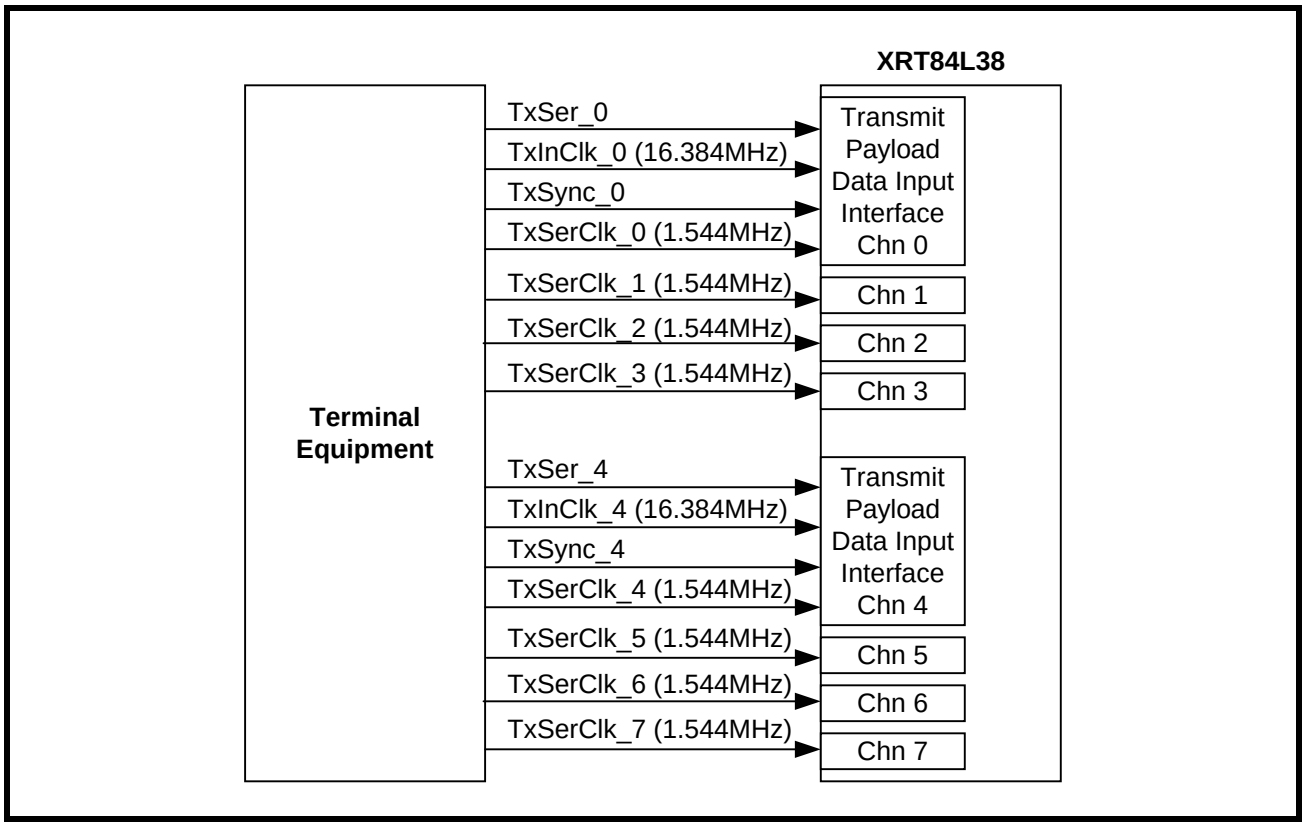
The Transmit Single-frame Synchronization signal should pulse HIGH for four clock cycles (the last two bit positions of the previous multiplexed frame and the first two bits of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH to identify the start of multiplexed data stream of Channel 4-7. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of the multiplexed E1 frame. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT84L38 device and send to each individual channel. These data will be processed by each individual framer and send to LIU interface. The local Terminal Equipment provides a free-running

2.048MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

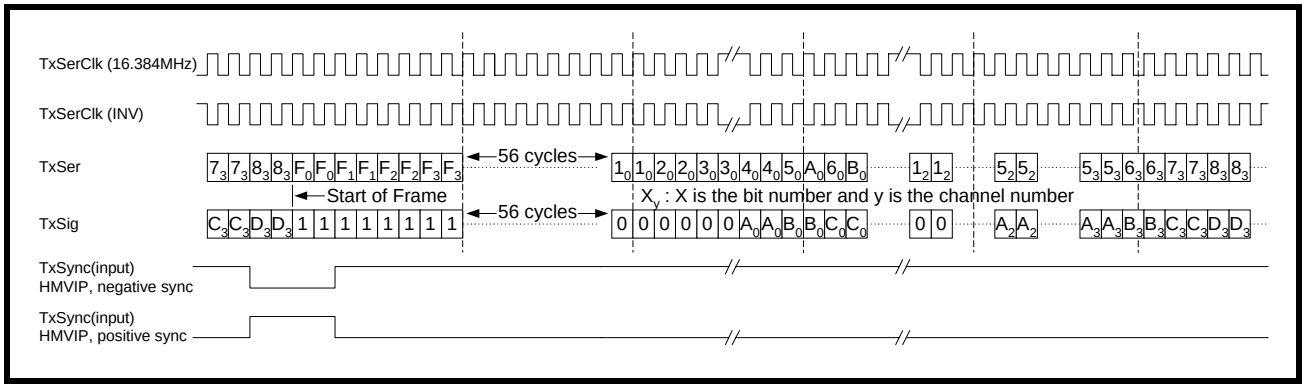
See Figure 77 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in HMVIP 16.384Mbit/s mode.

FIGURE 77. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 78 below when the framer is running at HMVIP 16.384Mbit/s mode.

FIGURE 78. TIMING SIGNAL WHEN THE FRAMER IS RUNNING AT HMVIP 16.384MBIT/S MODE



6.1.3.6 E1 Transmit Input Interface - H.100 16.384Mbit/s

When the Transmit Multiplex Enable bit is set to one and the Transmit Interface Mode Select [1:0] bits are set to 11, the Transmit Back-plane interface of framer is running at H.100 16.384Mbit/s mode.

(The HMVIP mode and the H.100 mode are essential the same except for the HIGH pulse position of the Transmit Single-frame Synchronization Signal)

The interface consists of the following pins:

- Data input (TxSer_n)
- Transmit Serial Clock Input signal (TxSerClk_n)
- Transmit Single-frame Synchronization Input signal (TxSync_n)
- Transmit Input Clock (TxInClk_n)
- Transmit Time-slot Indication clock (TxTSClk_n)
- Transmit Time Slot indicator bits (TxTSb[4:0]_n)

The Transmit Back-plane Interface is accepting data through TxSer_0 or TxSer_4 pins at 16.384Mbit/s. The local Terminal Equipment multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Transmit Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Transmit Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz is supplied to the Transmit Input Clock pin of Channel 0 and Channel 4 of the framer. The local Terminal Equipment provides multiplexed payload data at rising edge of this Transmit Input Clock. The Transmit High-speed Back-plane Interface of the framer then latches incoming serial data at falling edge of the clock.

The local Terminal Equipment maps four 2.048Mbit/s E1 data streams into this 16.384Mbit/s data stream as described below:

1. Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0 and so on. After all the bits of Timeslot 0 of Channel 0 is sent repeatedly, the Terminal Equipment will start sending the payload bits of Timeslot 0 of Channel 1 and 2. The payload bits of Timeslot 0 of Channel 3 are sent the last.

   After the payload bits of Timeslot 0 of all four channels are sent, it comes the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0

THIRD OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1

FIFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2

SEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3

X_Y: The Xth payload bit of Channel Y

2. The local Terminal Equipment also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream.

When the Terminal Equipment is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

SECOND OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	6_0	B_0	7_0	C_0	8_0	D_0

FOURTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_1	A_1	6_1	B_1	7_1	C_1	8_1	D_1

SIXTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_2	A_2	6_2	B_2	7_2	C_2	8_2	D_2

EIGHTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_3	A_3	6_3	B_3	7_3	C_3	8_3	D_3

X_Y: The Xth payload bit of Channel Y

A_Y: The signaling bit A of Channel Y

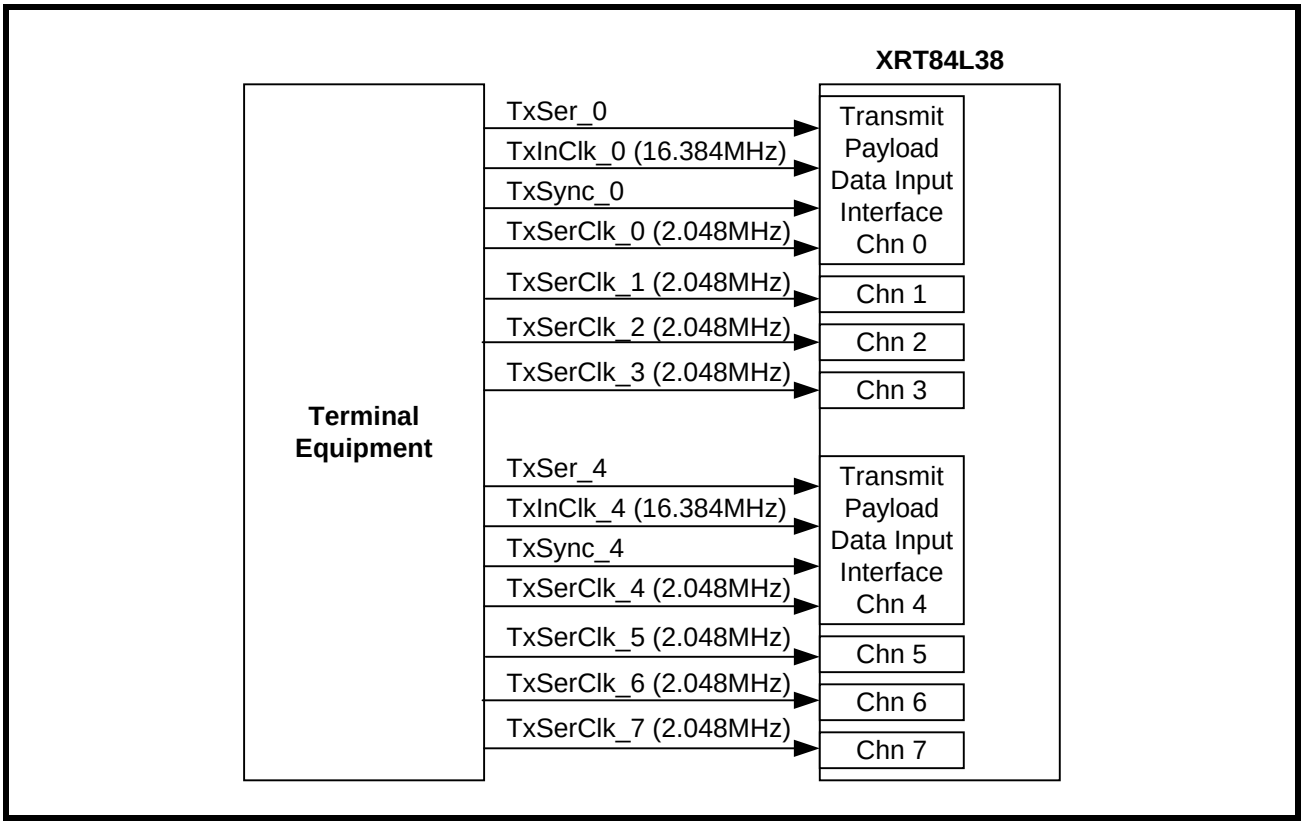
3. After the first octet of all four channels are sent, the local Terminal Equipment start sending the second octets following the same rules of Step 1 and 2.

The Transmit Single-frame Synchronization signal should pulse HIGH for two clock cycles (the last bit position of the previous multiplexed frame and the first bit position of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. The Transmit Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. The Transmit Single-frame Synchronization signal of Channel 4 pulses HIGH to identify the start of multiplexed data stream of Channel 4-7. By sampling the HIGH pulse on the Transmit Single-frame Synchronization signal, the framer can position the beginning of the multiplexed E1 frame. It is responsibility of the Terminal Equipment to align the multiplexed transmit serial data with the Transmit Single-frame Synchronization pulse.

Inside the framer, all the "don't care" bits will be stripped away. The framing bits, signaling and payload data are de-multiplexed inside the XRT84L38 device and send to each individual channel. These data will be processed by each individual framer and send to LIU interface. The local Terminal Equipment provides a free-running 2.048MHz clock to the Transmit Serial Input clock of each channel. The framer will use this clock to carry the processed payload and signaling data to the transmit section of the device.

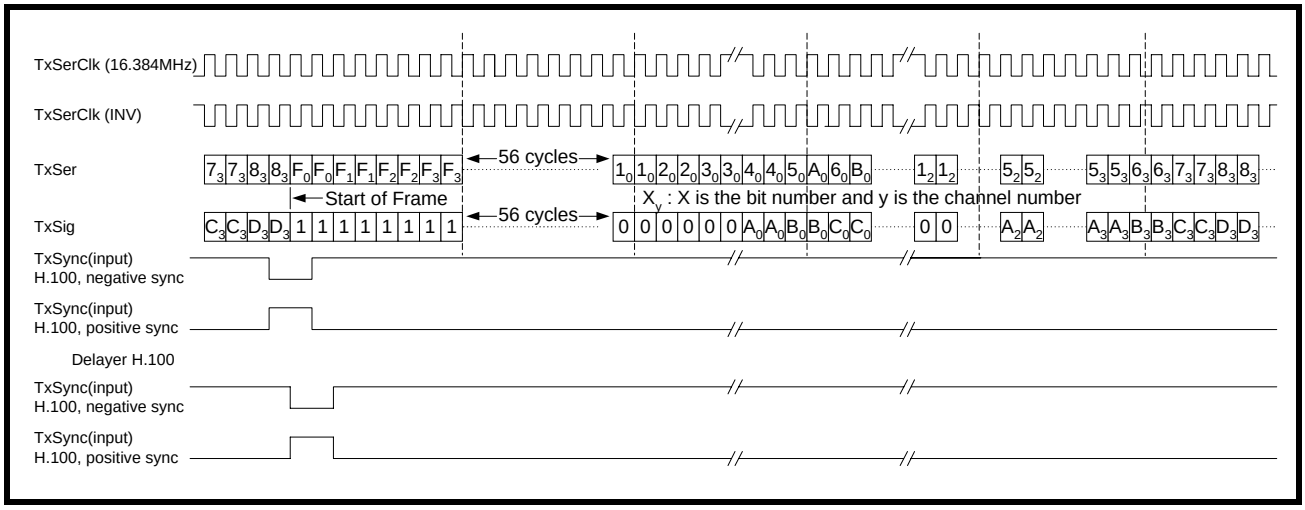
See Figure 79 below for how to interface the local Terminal Equipment with the Transmit Payload Data Input Interface block of the framer in HMVIP 16.384Mbit/s mode.

FIGURE 79. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 80 below when the framer is running at H.100 16.384Mbit/s mode.The E1 Receive Section

FIGURE 80. TIMING SIGNAL WHEN THE FRAMER IS RUNNING AT H.100 16.384MBIT/S MODE



6.2 THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK

6.2.1 Description of the Receive Payload Data Output Interface Block

Each of the eight framers within the XRT84L38 device includes a Receive Payload Data Output Interface block. The function of the block is to provide an interface to the Terminal Equipment (for example, a Central Office or switching equipment) that has data to receive from a "Far End" terminal over an DS1 or E1 transport medium.

The Payload Data Output Interface module (also known as the Back-plane Interface module) supports payload data to be taken from or presented to the system. In E1 mode, supported data rates are 1.544Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 12.352Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s. In E1 mode, supported data rates are XRT84V24 compatible 2.048Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s.

The Receive Payload Data Output Interface block supplies or accepts the following signals to the Terminal Equipment circuitry:

- Receive Serial Data Input (RxSer_n)
- Receive Serial Clock (RxSerClk_n)
- Receive Single-frame Synchronization Signal (RxSync_n)
- Receive Multi-frame Synchronization Signal (RxMSync_n)
- Receive Time-slot Indicator Clock (RxTSClk_n)
- Receive Time-slot Indication Bits (RxTSb[4:0]_n)

The Receive Serial Data is an output pin carrying payload, signaling and sometimes Data Link data supplied by XRT84L38 device to the local Terminal Equipment.

The Receive Serial Clock is an input or output signal used by the Receive Payload Data Input Interface block to send out serial data to the local Terminal Equipment. The Receive Clock Inversion bit of the Receive Interface Control Register (TICR) determines at which edge of the Receive Serial Clock would data transition on the Receive Serial Data pin occur.

The table below shows configurations of the Receive Clock Inversion bit of the Receive Interface Control Register (RICR).

RECEIVE INTERFACE CONTROL REGISTER (RICR) (INDIRECT ADDRESS = 0XN0H, 0X22H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Clock Inversion	R/W	0 - Serial data transition happens on rising edge of the Receive Serial Clock. 1 - Serial data transition happens on falling edge of the Receive Serial Clock.

Throughout the discussion of this datasheet, we assume that serial data transition happens on rising edge of the Receive Serial Clock unless stated otherwise.

The Receive Single-frame Synchronization signal is either input or output. When configure as input, it indicates beginning of an E1 frame. When configure as output, it indicates end of an E1 frame.

The Receive Multi-frame Synchronization signal is an output pin from XRT84L38 indicating end of an E1 multi-frame.

By connecting these signals with the local Terminal Equipment, the Receive Payload Data Output Interface routes received payload data from the Receive Framer Module to the local Terminal Equipment.

6.2.2 Brief Discussion of the Receive Payload Data Output Interface Block Operating at XRT84V24 Compatible 2.048Mbit/s mode

The incoming Receive Payload Data is taken into the framer from the LIU interface using the Recovered Receive Line Clock. The payload data is then routed through the Receive Farmer Module and presented to the Receive Payload Data Output Interface through the Receive Serial Data output pin (RxSer_n). This data is then clocked out using the Receive Serial Clock (RxSerClk_n).

There is a two-frame (512 bits) elastic buffer between the Receive Framer Module and the Receive Payload Data Output Interface. This buffer can be enabled or disabled via programming the Slip Buffer Enable [1:0] bits in Slip Buffer Control Register (SBCR).

The following table shows configurations of the Slip Buffer Enable [1:0] bits in Slip Buffer Control Register.

SLIP BUFFER CONTROL REGISTER (SBCR)(INDIRECT ADDRESS = 0XN0H, 0X16H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Slip Buffer Enable	R/W	00 - Slip Buffer is bypassed. The Receive Payload Data is passing from the Receive Framer Module to the Receive Payload Data Output Interface directly without routing through the Slip Buffer. The Receive Serial Clock signal (RxSerClk_n) is an output. 01 - The Elastic Store (Slip Buffer) is enabled. The Receive Payload Data is passing from the Receive Framer Module through the Slip Buffer to the Receive Payload Data Output Interface. The Receive Serial Clock signal (RxSerClk_n) is an input. 10 - The Slip Buffer acts as a FIFO. The FIFO Latency Register (FLR) determines the data latency. The Receive Payload Data is passing from the Receive Framer Module through the FIFO to the Receive Payload Data Output Interface. The Receive Serial Clock signal (RxSerClk_n) is an input. 11 - Slip Buffer is bypassed. The Receive Payload Data is passing from the Receive Framer Module to the Receive Payload Data Output Interface directly without routing through the Slip Buffer. The Receive Serial Clock signal (RxSerClk_n) is an output.

If the Slip Buffer is not in bypass mode, then the user has the option of either providing the Receive Single-Frame Synchronization pulse or getting the Receive Single-Frame Synchronization pulse on frame boundary at the RxSync_n pin. The Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register (SBCR) determines whether the Receive Single-Frame Synchronization signal is input or output. The table be-

low demonstrates settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register.

SLIP BUFFER CONTROL REGISTER (SBCR)(INDIRECT ADDRESS = 0XN0H, 0X16H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Slip Buffer Receive Synchronization Direction	R/W	0 - The Receive Single-Frame Synchronization signal (RxSync_n) is an output if the Slip Buffer is not in bypass mode. 1 - The Receive Single-Frame Synchronization signal (RxSync_n) is an input if the Slip Buffer is not in bypass mode.

If the Slip Buffer is in bypass mode, the Receive Payload Data is routed to the Receive Payload Data Output Interface from the Receive Framer Module directly. The Recovered Line Clock is used to carry the Receive Payload Data all the way from the LIU interface, to the Receive Framer Module and eventually output through the Receive Serial Data output pin. The Receive Serial Clock signal is therefore an output using the Recovered Receive Line Clock as timing source. The Receive Single-Frame Synchronization signal is also output in Slip Buffer bypass mode.

If the Slip Buffer is enabled, the Receive Payload Data is latched into the Elastic Store using the Recovered Receive Line Clock. The local Terminal Equipment supplies a free-running 2.048MHz clock to the Receive Serial Clock pin to latch the Receive Payload Data out from the Elastic Store. Since the Recovered Receive Line Clock and the Receive Serial Clock are coming from different timing sources, the Slip Buffer will gradually fill or empty. If the elastic buffer either fills or empties, a controlled slip will occur. If the buffer empties and a read occurs, then a full frame of data will be repeated and a status bit will be updated. If the buffer fills and a write comes, then a full frame of data will be deleted and another status bit will be set. A detailed description of the Elastic Buffer can be found in later sections. In this mode, the Receive Single-Frame Synchronization signal can be either input or output depending on the settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register.

If the Slip Buffer is put into a FIFO mode, it is acting like a standard First-In-First-Out storage. A fixed READ and WRITE latency is maintained in a programmable fashion controlled by the FIFO Latency Register (FIFOLR). The local Terminal Equipment supplies a 2.048MHz clock to the Receive Serial Clock pin to latch the Receive Payload Data out from the FIFO. However, it is the responsibility of the user to phase lock the input Receive Serial Clock to the Recovered Receive Line Clock to avoid either over-run or under-run of the FIFO. In this mode, the Receive Single-Frame Synchronization signal can be either input or output depending on the settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register.

The following table summaries the input or output nature of the Receive Serial Clock and Receive Single-Frame Synchronization signals for different Slip Buffer settings.

RECEIVE TIMING SOURCE	RXSERCLK_N	RXSYNC_N	
		Slip Buffer Synchronization Direction Bit = 0	Slip Buffer Synchronization Direction Bit = 1
Slip Buffer Bypassed	Output	Output	Output
Slip Buffer Enabled	Input	Output	Input
Slip Buffer Acts as FIFO	Input	Output	Input

The Receive Time-slot Indication Bits (RxTSb[4:0]_n) are multiplexed I/O pins. The functionality of these pins is governed by the value of Receive Fractional E1 Output Enable bit of the Receive Interface Control Register (RICR). The following table illustrates the configurations of the Receive Fractional E1 Input Enable bit.

RECEIVE INTERFACE CONTROL REGISTER (RICR) (INDIRECT ADDRESS = 0XN0H, 0X22H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Fractional E1 Output Enable	R/W	0 - The Receive Time-slot Indication bits (RxTSb[4:0] are outputting five-bit binary values of Time-slot number (0-31) being accepted and processed by the Receive Payload Data Output Interface block of the framer. The Receive Time-slot Indicator Clock signal (RxTSClk_n) is a 256KHz clock that pulses HIGH for one E1 bit period whenever the Receive Payload Data Output Interface block is accepting the LSB of each of the twenty-four time slots. 1 - The RxTSb[0]_n bit becomes the Receive Fractional E1 Output signal (RxFrTD_n) which carries Fractional E1 payload data from the framer. The RxTSb[1]_n bit becomes the Receive Signaling Data Output signal (RxSig_n) which is used to carry robbed-bit signaling data extracted from the inbound E1 frame. The RxTSb[2]_n bit serially outputs all five-bit binary values of the Time Slot number (0-31) being accepted and processed by the Receive Payload Data Output Interface block of the framer. The RxTSClk_n will output gaped fractional E1 clock that can be used by Terminal Equipment to latch in Fractional E1 payload data at rising edge of the clock. Or, The RxTSClk_n pin will be a clock enable signal to Receive Fractional E1 Output signal (RxFrTD_n) when the un-gaped Receive Serail Output Clock (RxSerClk_n) is used to latch in Fractional E1 Payload Data into the Terminal Equipment.

When configured to operate in normal condition (that is, when the Receive Fractional E1 Input Enable bit is equal to zero), these bits reflect the five-bit binary value of the Time Slot number (0-31) being outputted and processed by the Receive Payload Data Output Interface block of the framer. RxTSb[4] represents the MSB of the binary value and RxTSb[0] represents the LSB.

When the Receive Fractional E1 Output Enable bit is equal to one, the RxTSb[0]_n bit becomes the Receive Fractional E1 Output signal (RxFrTD_n). This output pin carries Fractional E1 Output data extracted by the framer from the incoming E1 data stream. The Fractional E1 Output Interface allows certain time-slots of E1 data to be routed to destinations other than the local Terminal Equipment. Function of the Fractional E1 Output signal will be discussed in details in later sections.

When the Receive Fractional E1 Output Enable bit is equal to one, the RxTSb[1]_n bit becomes the Receive Signaling Data Output signal (RxSig_n). These output pins can be used to carry robbed-bit signaling data extracted from the inbound E1 frame. Function of the Receive Signaling Data Output signal will be discussed in details in later sections.

When the Receive Fractional E1 Output Enable bit is equal to one, the RxTSb[2]_n bit serially outputs all five-bit binary values of the Time Slot number (0-31) being outputted and processed by the Receive Payload Data Output Interface block of the framer. MSB of the binary value is presented first and the LSB is presented last.

The RxTSb[3]_n and RxTSb[4}_n pins are not multiplexed.

The table below shows functionality of the RxTSb[2:0] bits when the Receive Fractional E1 Output bit is set to different values.

RECEIVE FRACTIONAL E1 OUTPUT BIT = 0		RECEIVE FRACTIONAL E1 OUTPUT BIT = 1	
RxTSb[0]	Output	RxFrTD	Output
RxTSb[1]	Output	RxSig	Output
RxTSb[2]	Output	RxTS	Output

The Receive Time-slot Indicator Clock signal (RxTSClk_n) is a multi-function output pin. When configured to operate in normal condition (that is, when the Receive Fractional E1 Input Enable bit is equal to zero), the RxTSClk_n is a 256KHz clock that pulses HIGH for one E1 bit period whenever the Receive Payload Data Output Interface block is outputting the LSB of each of the twenty-four time slots. The local Terminal Equipment should use this clock signal to sample the RxTSb[0] through RxTSb[4] bits and identify the time-slot being processed via the Receive Section of the framer.

When the Receive Fractional E1 Output Enable bit is equal to one, the RxTSClk_n will output gaped fractional E1 clock whenever Fractional E1 payload data is present at the RxFrTD_n pin. The local Terminal Equipment can latch in Fractional E1 payload data at falling edge of the clock. Otherwise, this pin will be a clock enable signal to Receive Fractional E1 output signal (RxFrTD_n) if the framer is configured accordingly. In this way, Fractional E1 payload data is clocked into the Terminal Equipment using un-gaped Receive Serial Output Clock (RxSerClk_n). A detailed discussion of the Fractional E1 Payload Data Output Interface can be found in later sections.

A detailed discussion of how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment with Slip Buffer enabled or disabled can be found in the later sections.

6.2.2.1 Connect the Receive Payload Data Output Interface block to the Local Terminal Equipment if the Slip Buffer is bypassed

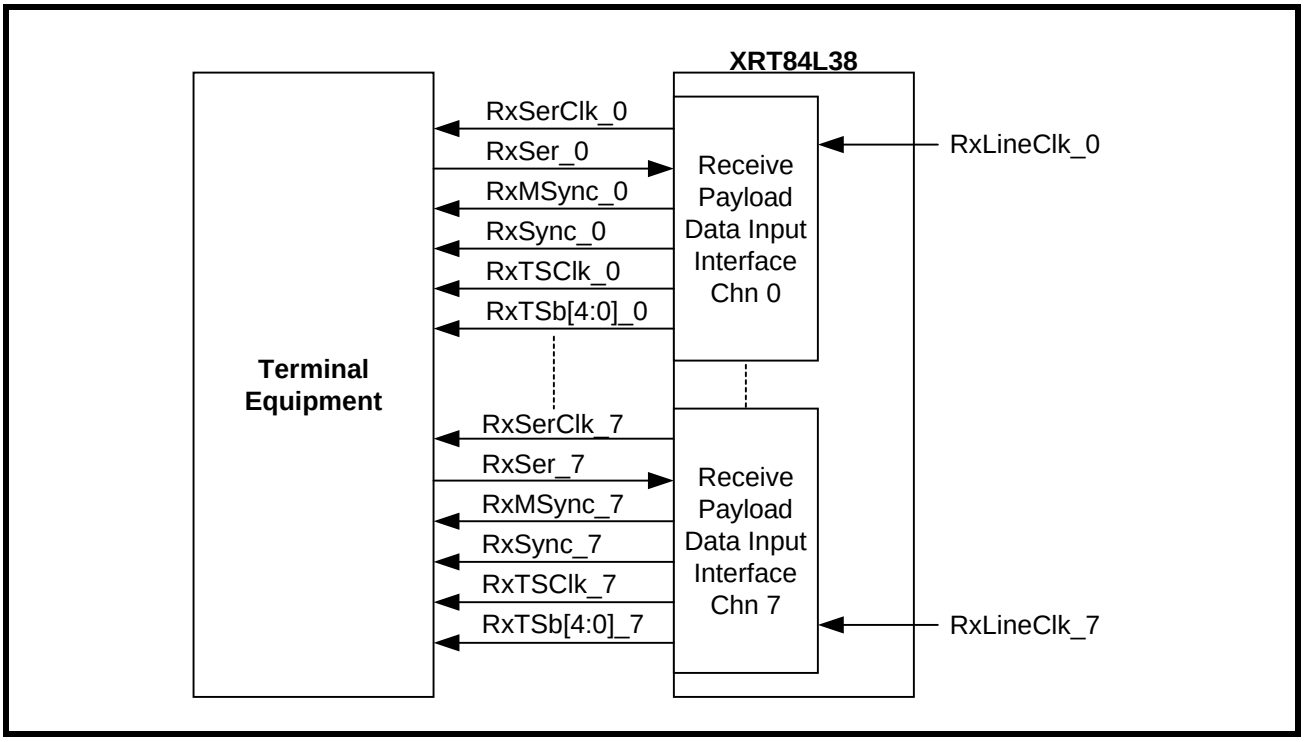
By setting the Slip Buffer Enable [1:0] bits of the Slip Buffer Control Register to 00 or 11, the Receive Framer Module routes the Receive Payload Data directly to the Receive Payload Data Output Interface without passing through the Elastic Buffer. The XRT84L38 device uses the Recovered Receive Line Clock internally to carry the Receive Payload Data directly across the whole chip. The Recovered Receive Line Clock is essentially become timing source of the Receive Serial Clock output.

If the Slip Buffer is bypassed, the Receive Single-frame Synchronization signal is automatically configured to be output signals. It should pulse HIGH for one E1 bit period (488ns) at the last bit position of each E1 frame. By triggering on the HIGH pulse on the Receive Single-frame Synchronization signal, the Terminal Equipment can identify the end of an E1 frame and should prepare to accept payload data of the next E1 frame from the framer.

The Receive Multi-frame Synchronization signal should pulse HIGH for one E1 bit period (488ns) at the last bit position of an E1 multi-frame. By triggering on the HIGH pulse on the Receive Multi-frame Synchronization signal, the framer can identify the end of an E1 super-frame and should prepare to accept payload data of the next E1 super-frame from the framer.

See Figure 81 for how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is bypassed and the Recovered Receive Line Clock is timing source of the Receive section.

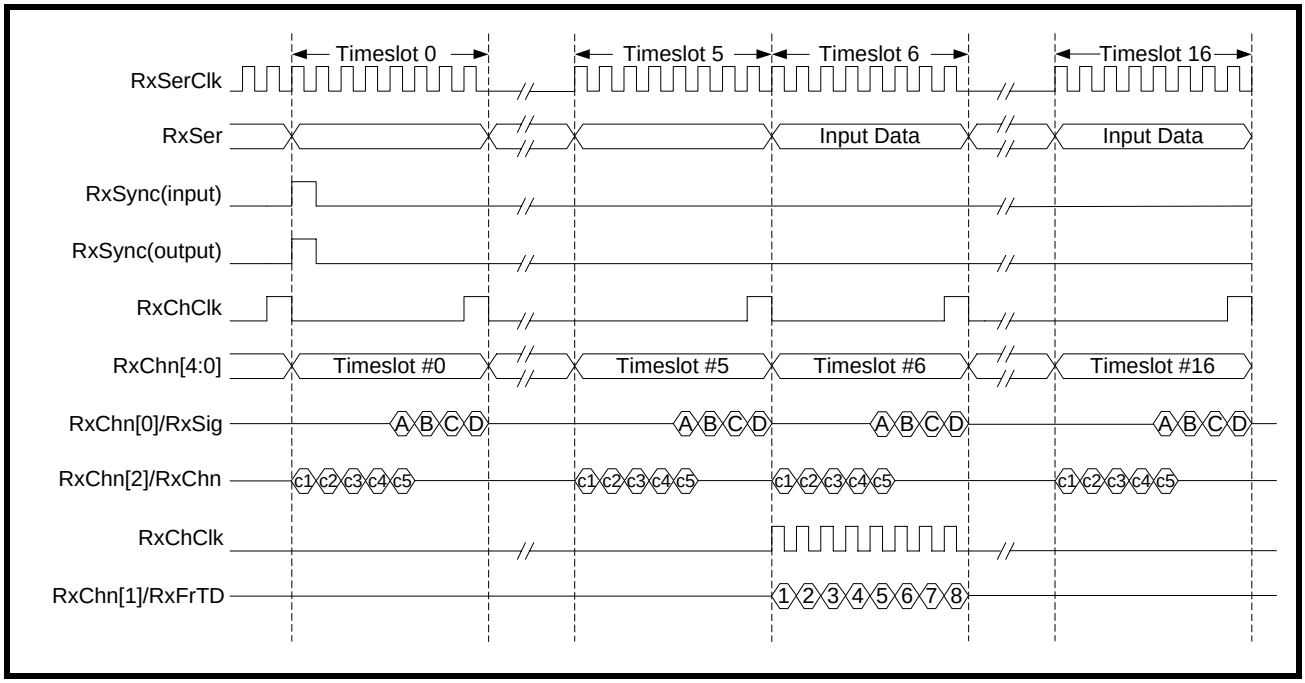
FIGURE 81. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT WITH SLIP BUFFER BYPASSED AND RECOVERED RECEIVE LINE CLOCK AS RECEIVE TIMING SOURCE



The following Figure 82 shows waveforms of the signals (RxSerClk_n, RxSer_n, RxSync_n, RxTSClk_n and RxTSb[4:0]_n) which connecting the Receive Payload Data Output Interface block to the local Terminal Equip-

ment when the Slip Buffer is bypassed and the Recovered Receive Line Clock is timing source of the Receive section.

FIGURE 82. WAVEFORMS OF THE SIGNALS CONNECTING THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WHEN THE SLIP BUFFER IS BYPASSED AND THE RECOVERED LINE CLOCK IS THE TIMING SOURCE OF THE RECEIVE SECTION



6.2.2.2 Connect the Receive Payload Data Output Interface block to the Local Terminal Equipment if the Slip Buffer is enabled

By setting the Slip Buffer Enable [1:0] bits of the Slip Buffer Control Register to 01, the framer includes the two-frame Elastic Buffer into its data path. The Receive Framer Module routes the Receive Payload Data to the Elastic Buffer first. The Receive Payload Data is then presented to the Receive Payload Data Output Interface. The XRT84L38 device uses the Recovered Receive Line Clock internally to clock in the Receive Payload Data into the Elastic Buffer. The Terminal Equipment should provide a 2.048MHz clock to the Receive Serial Clock input pin to latch data out from the Elastic Buffer.

The Recovered Receive Line Clock and the Receive Serial Clock are generated from two different timing sources. That is, the Recovered Receive Line Clock is originating from a remote site while Receive Serial Clock generating by a local oscillator. Any mismatch in frequencies of these two clocks will result in the Slip Buffer to gradually fill or deplete.

Overtime, the Elastic Buffer either fills or empties completely. Once that happened, a controlled slip by the XRT84L38 device will occur. The Receive Slip Buffer Slip bit of the Slip Buffer Status Register (SBSR) is set to 1.

If the buffer empties and a read occurs, then a full frame of data will be repeated and the Receive Slip Buffer Empty bit of the Slip Buffer Status Register (SBSR) will be forced HIGH. If the buffer fills and a write comes, then a full frame of data will be deleted and the Receive Slip Buffer Full bit of the Slip Buffer Status Register (SBSR) will be forced HIGH.

The following table demonstrates settings of the Receive Slip Buffer Slip bit, Receive Slip Buffer Empty bit and Receive Slip Buffer Full bit of the Slip Buffer Status Register.

SLIP BUFFER STATUS REGISTER (SBSR)(INDIRECT ADDRESS = 0XNAH, 0X08H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Slip Buffer Full	R/W	0 - The Receive Slip Buffer is not full. 1 - The Receive Slip Buffer is full and one frame of data is discarded.
1	Receive Slip Buffer Empty	R/W	0 - The Receive Slip Buffer is not empty. 1 - The Receive Slip Buffer is empty and one frame of data is repeated.
1	Receive Slip Buffer Slip	R/W	0 - The Receive Slip Buffer does not slip. 1 - The Receive Slip Buffer slips since either full or emptied.

In this mode, the Receive Single-Frame Synchronization signal can be either input or output depending on the settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register. When the Slip Buffer Receive Synchronization Direction bit is set to 0, the Receive Single-Frame Synchronization signal (RxSync_n) is an. When the Slip Buffer Receive Synchronization Direction bit is set to 1,the Receive Single-Frame Synchronization signal (RxSync_n) is an input.

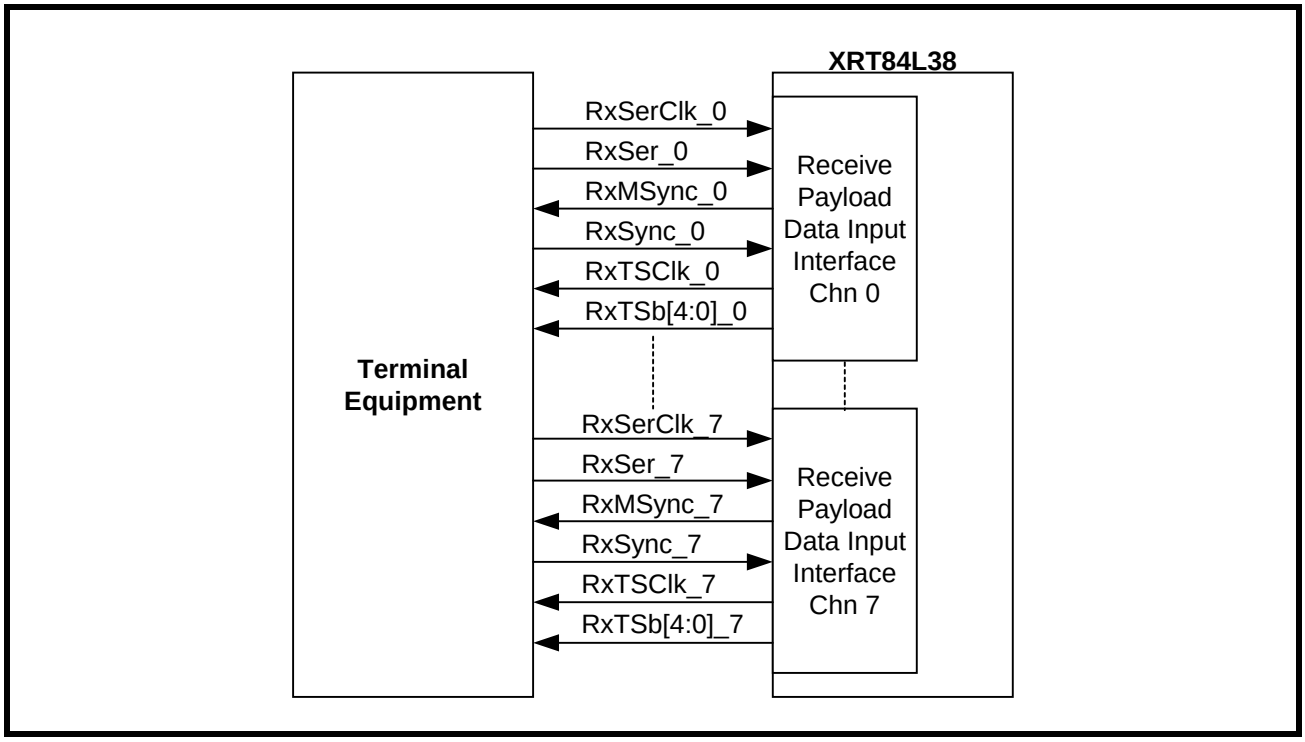
If the Receive Single-Frame Synchronization signal is an output, it should pulse HIGH for one E1 bit period (488ns) at the last bit position of each E1 frame. By triggering on the HIGH pulse on the Receive Single-frame Synchronization signal, the Terminal Equipment can identify the end of an E1 frame and should prepare to accept payload data of the next E1 frame from the framer.

If the Receive Single-Frame Synchronization signal is an input, it should pulse HIGH for one E1 bit period (488ns) at the first bit position (F-bit) of each E1 frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer should identity the beginning of an E1 frame and can send out data in a synchronized way. It is the responsibility of the local Terminal Equipment to align the start of an E1 frame with the Receive Single-Frame Synchronization pulse.

The Receive Multi-frame Synchronization signal should pulse HIGH for one E1 bit period (488ns) at the last bit position of Frame number one of an E1 multi-frame. By triggering on the HIGH pulse on the Receive Multi-frame Synchronization signal, the framer can identify the end of an E1 super-frame and should prepare to accept payload data of the next E1 super-frame from the framer.

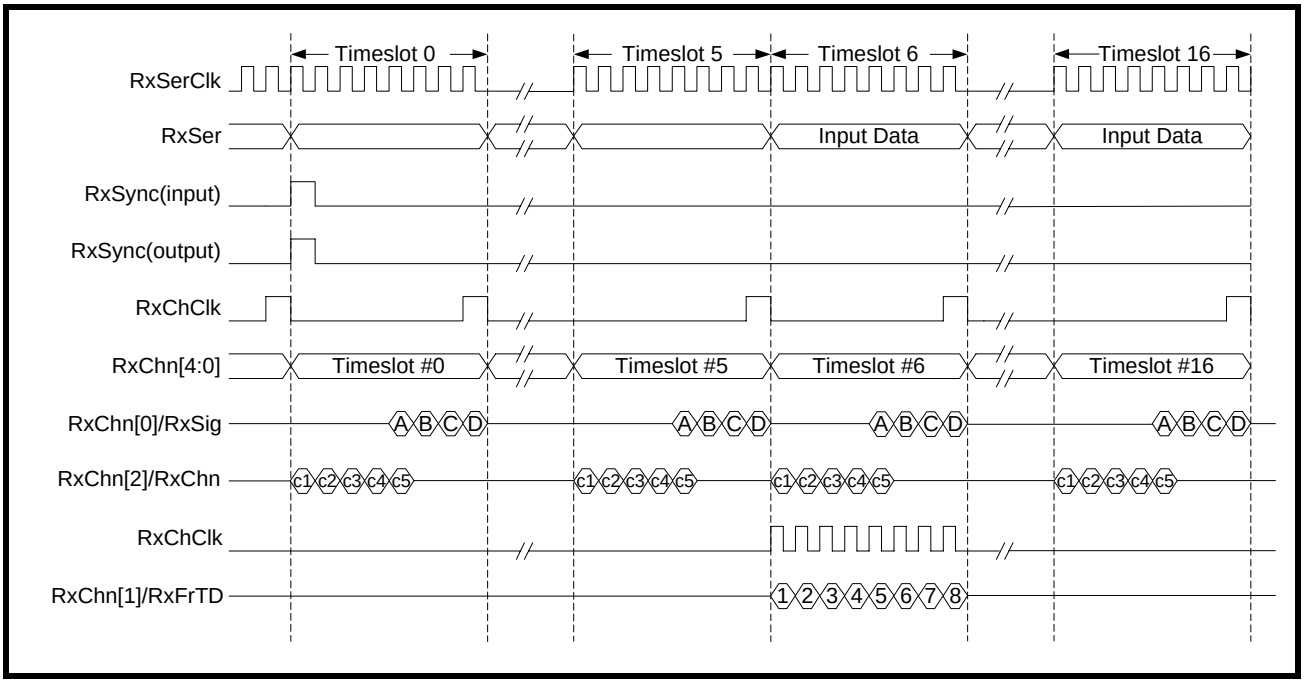
See Figure 83 for how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is enabled.

FIGURE 83. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT WITH SLIP BUFFER ENABLED OR ACTS AS FIFO



The following Figure 84 shows waveforms of the signals (RxSerClk_n, RxSer_n, RxSync_n, RxTSClk_n and RxTSb[4:0]_n) which connecting the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is enabled.

FIGURE 84. WAVEFORMS OF THE SIGNALS THAT CONNECT THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WHEN THE SLIP BUFFER IS ENABLED



6.2.2.3 Connect the Receive Payload Data Output Interface block to the Local Terminal Equipment if the Slip Buffer is configured as FIFO

By setting the Slip Buffer Enable [1:0] bits of the Slip Buffer Control Register to 10, the framer puts the Elastic Buffer into FIFO mode. Receive Framer Module routes the Receive Payload Data through the First-In-First-Out storage to the Receive Payload Data Output Interface. The XRT84L38 device uses the Recovered Receive Line Clock internally to clock in the Receive Payload Data into the FIFO. The Terminal Equipment should provide an external 2.048MHz clock to the Receive Serial Clock input pin to latch data out from the FIFO.

It is the responsibility of the user to phase lock the input Receive Serial Clock to the Recovered Receive Line Clock to avoid either over-run or under-run of the FIFO. The latency between writing a bit into the FIFO and reading the same bit from it (READ and WRITE latency) is actually depth of the FIFO, which is maintained in a programmable fashion controlled by the FIFO Latency Register (FIFOLR). The largest possible depth of the FIFO is thirty-two bytes or one E1 frame. The default depth of the FIFO when XRT84L38 first powered up is four bytes. The table below shows the FIFO Latency Register.

FIFO LATENCY REGISTER (FIFOL) (INDIRECT ADDRESS = 0XN0H, 0X17H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4-0	FIFO Latency	R/W	These bits determine depth of the FIFO in terms of bytes. The largest possible value is thirty-two bytes or one E1 frame.

In this mode, the Receive Single-Frame Synchronization signal can be either input or output depending on the settings of the Slip Buffer Receive Synchronization Direction bit of the Slip Buffer Control Register. When the Slip Buffer Receive Synchronization Direction bit is set to 0, the Receive Single-Frame Synchronization signal (RxSync_n) is an. When the Slip Buffer Receive Synchronization Direction bit is set to 1,the Receive Single-Frame Synchronization signal (RxSync_n) is an input.

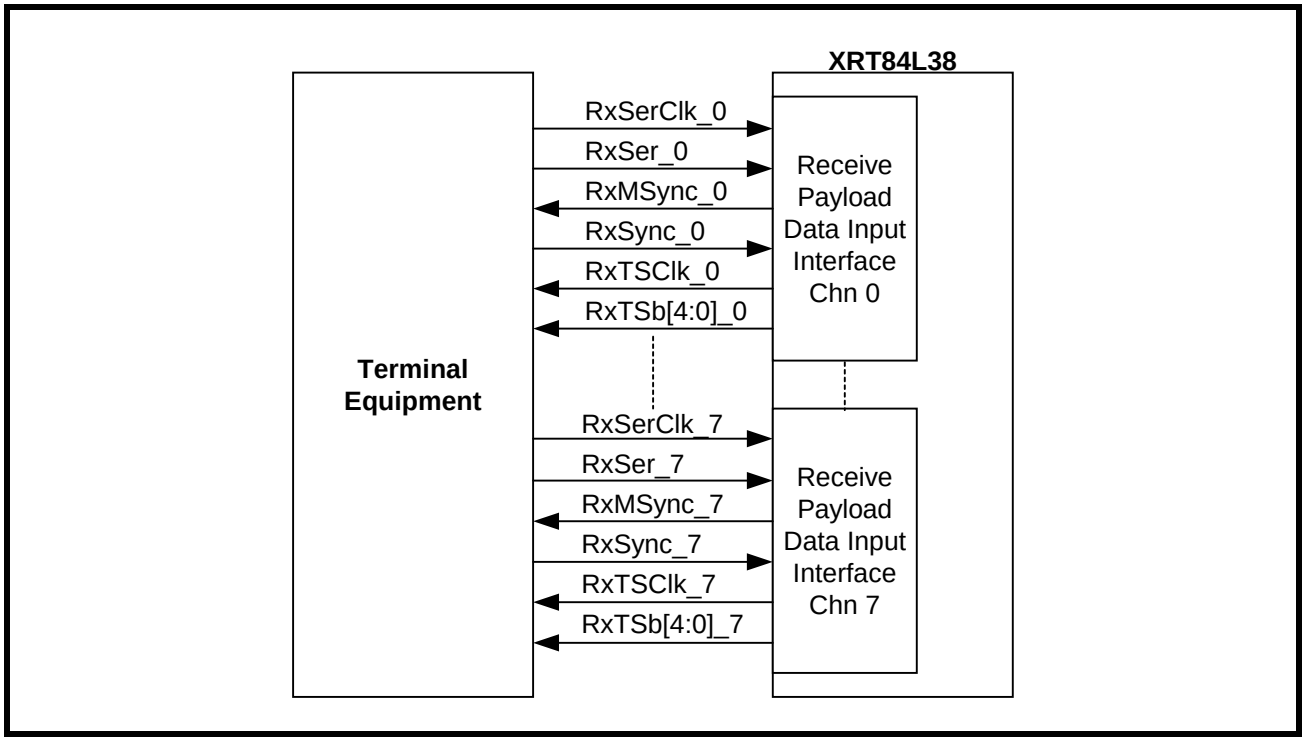
If the Receive Single-Frame Synchronization signal is an output, it should pulse HIGH for one E1 bit period (488ns) at the last bit position of each E1 frame. By triggering on the HIGH pulse on the Receive Single-frame Synchronization signal, the Terminal Equipment can identify the end of an E1 frame and should prepare to accept payload data of the next E1 frame from the framer.

If the Receive Single-Frame Synchronization signal is an input, it should pulse HIGH for one E1 bit period (488ns) at the first bit position (F-bit) of each E1 frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer should identity the beginning of an E1 frame and can send out data in a synchronized way. It is the responsibility of the local Terminal Equipment to align the start of an E1 frame with the Receive Single-Frame Synchronization pulse.

The Receive Multi-frame Synchronization signal should pulse HIGH for one E1 bit period (488ns) at the last bit position of Frame number one of an E1 multi-frame. By triggering on the HIGH pulse on the Receive Multi-frame Synchronization signal, the framer can identify the end of an E1 super-frame and should prepare to accept payload data of the next E1 super-frame from the framer.

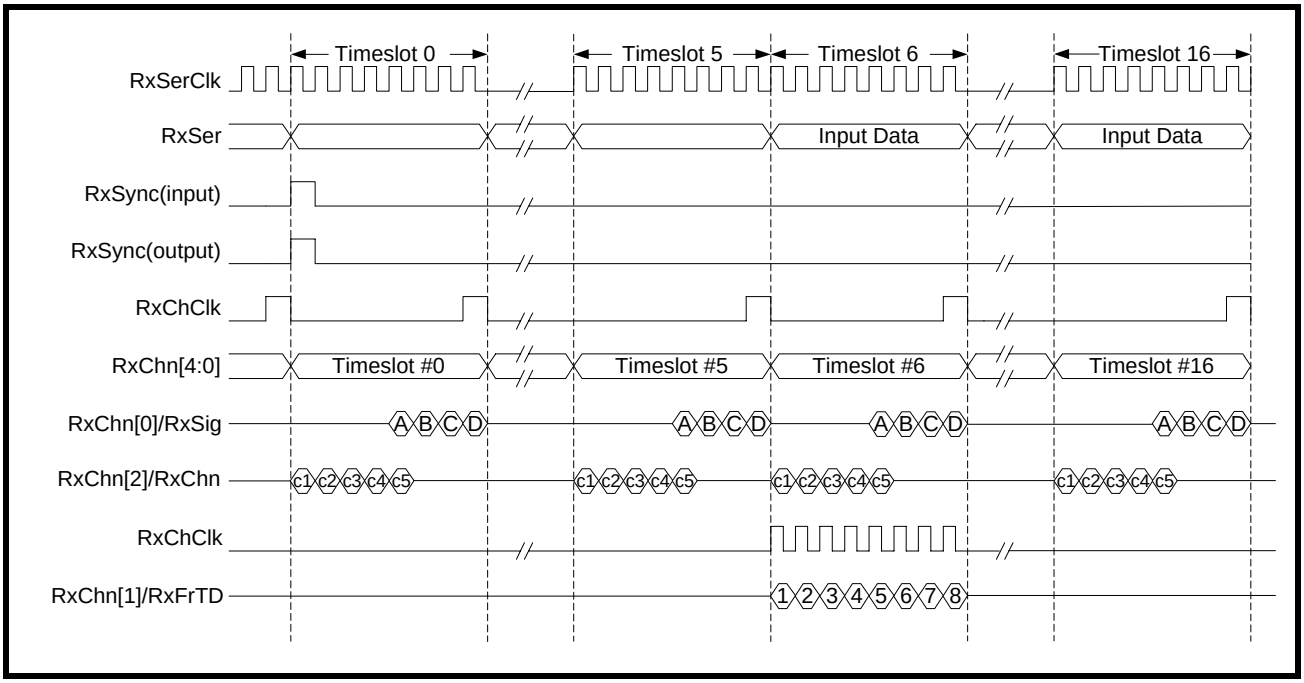
See Figure 85 for how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is acted as FIFO.

FIGURE 85. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT WITH SLIP BUFFER ENABLED OR ACTS AS FIFO



The following Figure 86 shows waveforms of the signals (RxSerClk_n, RxSer_n, RxSync_n, RxTSClk_n and RxTSb[4:0]_n) which connecting the Receive Payload Data Output Interface block to the local Terminal Equipment when the Slip Buffer is acted as FIFO.

FIGURE 86. WAVEFORMS OF THE SIGNALS THAT CONNECT THE RECEIVE PAYLOAD DATA OUTPUT INTERFACE BLOCK TO THE LOCAL TERMINAL EQUIPMENT WHEN THE SLIP BUFFER IS ACTED AS FIFO



6.2.3 High Speed Receive Back-plane Interface

The High-speed Back-plane Interface supports payload data to be taken from or presented to the local Terminal Equipment at different data rates. In E1 mode, supported High-speed data rates are MVIP 2.048Mbit/s, 4.096Mbit/s, 8.192Mbit/s, multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s or H.100 16.384Mbit/s. The Receive Multiplex Enable bit and the Receive Interface Mode Select [1:0] bits of the Receive Interface Control Register (RICR) determine the Receive Back-plane Interface data rate.

The following table shows configurations of the Receive Multiplex Enable bit and the Receive Interface Mode Select [1:0] bits of the Receive Interface Control Register (RICR).

RECEIVE INTERFACE CONTROL REGISTER (RICR) (INDIRECT ADDRESS = 0XN0H, 0X22H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Multiplex Enable	R/W	0 - The Receive Back-plane Interface block is configured to non-channel-multiplexed mode 1 - The Receive Back-plane Interface block is configured to channel-multiplexed mode
1-0	Receive Interface Mode Select	R/W	When combined with the Receive Multiplex Enable bit, these bits determine the Receive Back-plane Interface data rate.

The table below shows the combinations of Receive Multiplex Enable bit and Receive Interface Mode Select [1:0] bits and the resulting Receive Back-plane Interface data rates.

RECEIVE MULTIPLEX ENABLE BIT	RECEIVE INTERFACE MODE SELECT BIT 1	RECEIVE INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE
0	0	0	XRT84V24 Compatible 2.048Mbit/s
0	0	1	MVIP 2.048Mbit/s
0	1	0	4.096Mbit/s
0	1	1	8.192Mbit/s
1	0	0	-
1	0	1	Bit Multiplexed 16.384Mbit/s
1	1	0	HMVIP 16.384Mbit/s
1	1	1	H.100 16.384Mbit/s

When the Receive Multiplex Enable bit is set to zero, the framer is configured in non-channel-multiplexed mode. The possible data rates are XRT84V24 Compatible 2.048Mbit/s, MVIP 2.048Mbit/s, 4.096Mbit/s and 8.192Mbit/s. In non-channel-multiplexed mode, payload data of each channel are sending out from the Receive High-speed Back-plane Interface separately. Each channel uses its own Receive Serial Clock, Receive Serial Data, Receive Single-frame Synchronization signal and Receive Multi-frame Synchronization signal as interface between the framer and the Terminal Equipment. Section 2.1.1.1, 2.1.1.2 and 2.1.1.3 provide details on how to connect the Receive Payload Data Interface block with the local Terminal Equipment when the Back-plane interface data rate is 2.048Mbit/s.

When the Back-plane interface data rate is MVIP 2.048Mbit/s, 4.096Mbit/s and 8.192Mbit/s, the Receive Serial Clock, Receive Serial Data and Receive Single-frame Synchronization are all configured as inputs. The Receive Multi-frame Synchronization signal is still output. The Receive Serial Clock is configured as an input timing source for the High-speed Back-plane Interface with frequencies of 2.048 MHz, 4.096 MHz and 8.192 MHz respectively.

The table below summaries the clock frequencies of RxSerClk_n input when the framer is operating in non-multiplexed High-speed Back-plane mode.

RECEIVE MULTIPLEX ENABLE BIT = 0

RECEIVE INTERFACE MODE SELECT BIT 1	RECEIVE INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE	RXSERCLK
0	0	XRT84V24 Compatible 2.048Mbit/s	2.048MHz
0	1	MVIP 2.048Mbit/s	2.048 MHz
1	0	4.096Mbit/s	4.096 MHz
1	1	8.192Mbit/s	8.192 MHz

When the Receive Multiplex Enable bit is set to one, the framer is configured in channel-multiplexed mode. The possible data rates are bit-multiplexed 16.384Mbit/s, HMVIP 16.384Mbit/s and H.100 16.384Mbit/s. In channel-multiplexed mode, four channels share the Receive Serial Data, Receive Single-frame Synchronization signal and Receive Serial Clock of one channel as interface between the framer and the Terminal Equipment. The Receive Serial Clock runs at frequencies of 12.352 MHz or 16.384 MHz. It serves as the primary clock source for the High-speed Back-plane Interface.

Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4. The Re-

ceive Single-frame Synchronization signal of Channel 0 pulses HIGH at the beginning of the frame with data from Channel 0-3 multiplexed together. The Receive Single-frame Synchronization signal of Channel 4 pulses HIGH at the beginning of the frame with data from Channel 4-7 multiplexed together.

The table below summaries the clock frequencies of RxSerClk_n input when the framer is operating in multiplexed High-speed Back-plane mode.

RECEIVE MULTIPLEX ENABLE BIT = 1

RECEIVE INTERFACE MODE SELECT BIT 1	RECEIVE INTERFACE MODE SELECT BIT 0	BACK-PLANE INTERFACE DATA RATE	RXSERCLK
0	0	-	-
0	1	Bit-multiplexed 16.384Mbit/s	16.384 MHz
1	0	HMVIP 16.384Mbit/s	16.384 MHz
1	1	H.100 16.384Mbit/s	16.384 MHz

When the frame is running at High-speed Back-plane Interface mode other than the 2.048Mbit/s data rate, the Receive Single-frame Synchronization signal could pulse HIGH or LOW indicating boundaries of E1 frames. The Receive Synchronization Pulse Low bit of the Receive Interface Control Register (TICR) determines whether the Receive Single-frame Synchronization signal is HIGH active or LOW active.

The table below shows configurations of the Receive Synchronization Pulse LOW bit of the Receive Interface Control Register (RICR).

RECEIVE INTERFACE CONTROL REGISTER (RICR)(INDIRECT ADDRESS = 0XN0H, 0X22H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Synchronization Pulse LOW	R/W	0 - The Receive Single-frame Synchronization signal will pulse HIGH indicating the beginning of an E1 frame when the High-speed Back-plane Interface is running at a mode other than the 2.048Mbit/s. 1 - The Receive Single-frame Synchronization signal will pulse LOW indicating the beginning of an E1 frame when the High-speed Back-plane Interface is running at a mode other than the 2.048Mbit/s.

Throughout the discussion of this datasheet, we assume that the Receive Single-frame Synchronization signal pulses HIGH unless stated otherwise.

The following sections discuss details of how to operate the framer in different Back-plane interface speed mode and how to connect the Receive Payload Data Output Interface block to the local Terminal Equipment.

6.2.3.1 E1 Receive Input Interface - MVIP 2.048 MHz

When the Receive Multiplex Enable bit is set to zero and the Receive Interface Mode Select [1:0] bits are set to 01, the Receive Back-plane interface of framer is running at a data rate of 2.048Mbit/s.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

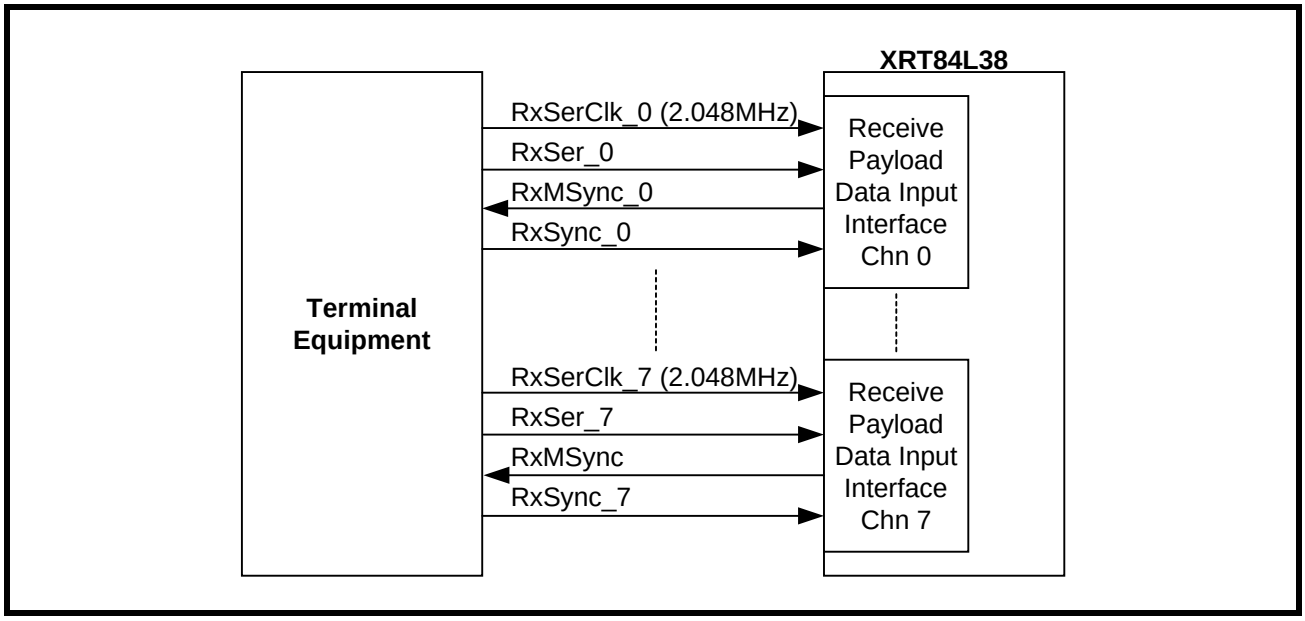
The Receive Back-plane interface is pumping out data through RxSer_n at an E1 equivalent data rate of 2.048Mbit/s. The local Terminal Equipment supplies a free-running 2.048MHz clock to the Receive Serial Clock

input. The Receive High-speed Back-plane Interface of the framer then sends out serial data at rising edge of the Receive Serial Clock. The local Terminal Equipment samples the serial data at falling edge of the clock.

The Receive Single-frame Synchronization input signal (RxSync_n) should pulse HIGH at the beginning of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer can identity the beginning of an E1 frame and start pumping payload data out.

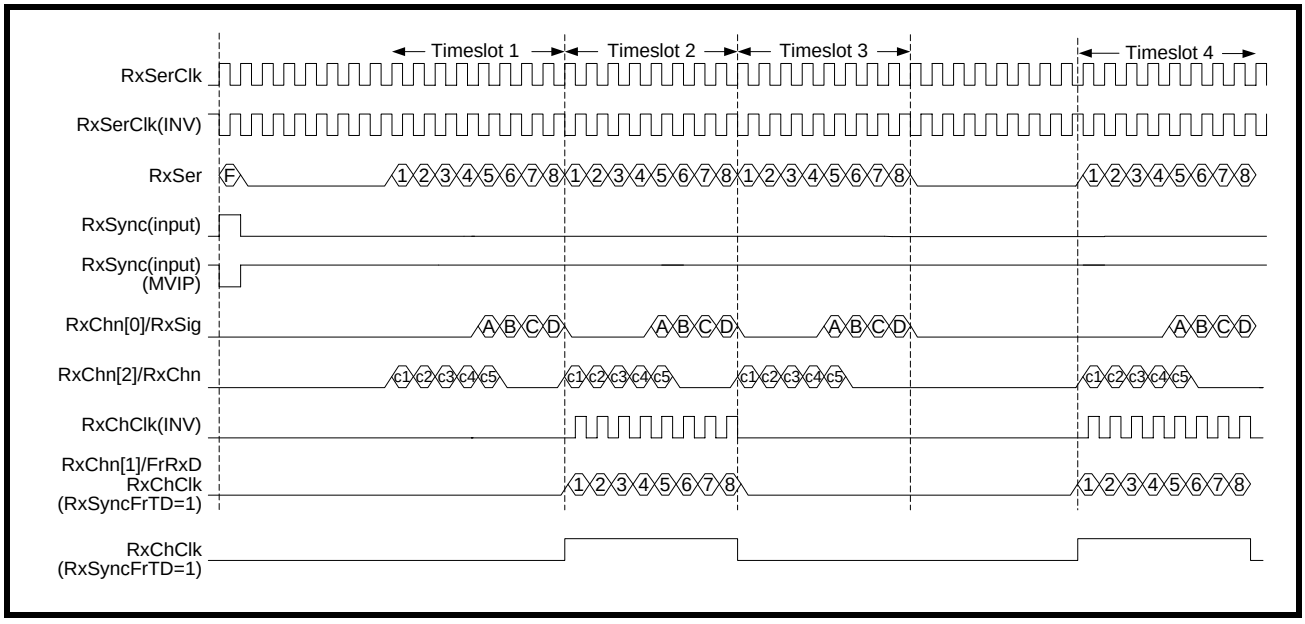
See Figure 87 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in MVIP 2.048Mbit/s mode.

FIGURE 87. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING MVIP 2.048MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at MVIP 2.048Mbit/s mode is shown in Figure 88.

FIGURE 88. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT MVIP 2.048MBIT/S



6.2.3.2 E1 Receive Input Interface - 4.096 MHz

(This interface mode is the same as running at 2.048 MHz. The only difference is that the Receive Serial Clock runs two times faster at 4.096 MHz)

When the Receive Multiplex Enable bit is set to zero and the Receive Interface Mode Select [1:0] bits are set to 10, the Receive Back-plane interface of framer is running at a clock rate of 4.096MHz.

The interface consists of the following pins:

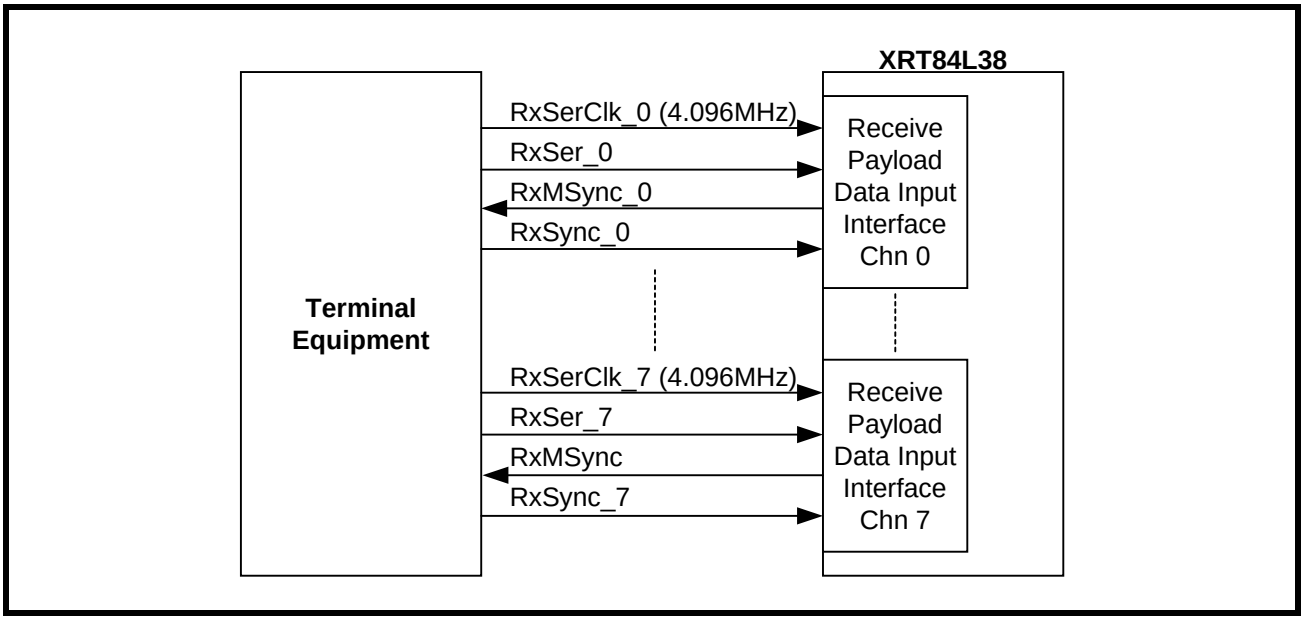
- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane interface is pumping out data through RxSer_n at an E1 equivalent data rate of 2.048Mbit/s. The local Terminal Equipment supplies a free-running 4.096MHz clock to the Receive Serial Clock input. The Receive High-speed Back-plane Interface of the framer then sends out serial data at every other rising edge of the Receive Serial Clock. The local Terminal Equipment samples the serial data at every other falling edge of the clock.

The Receive Single-frame Synchronization input signal (RxSync_n) should pulse HIGH at the beginning of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer can identity the beginning of an E1 frame and start pumping payload data out.

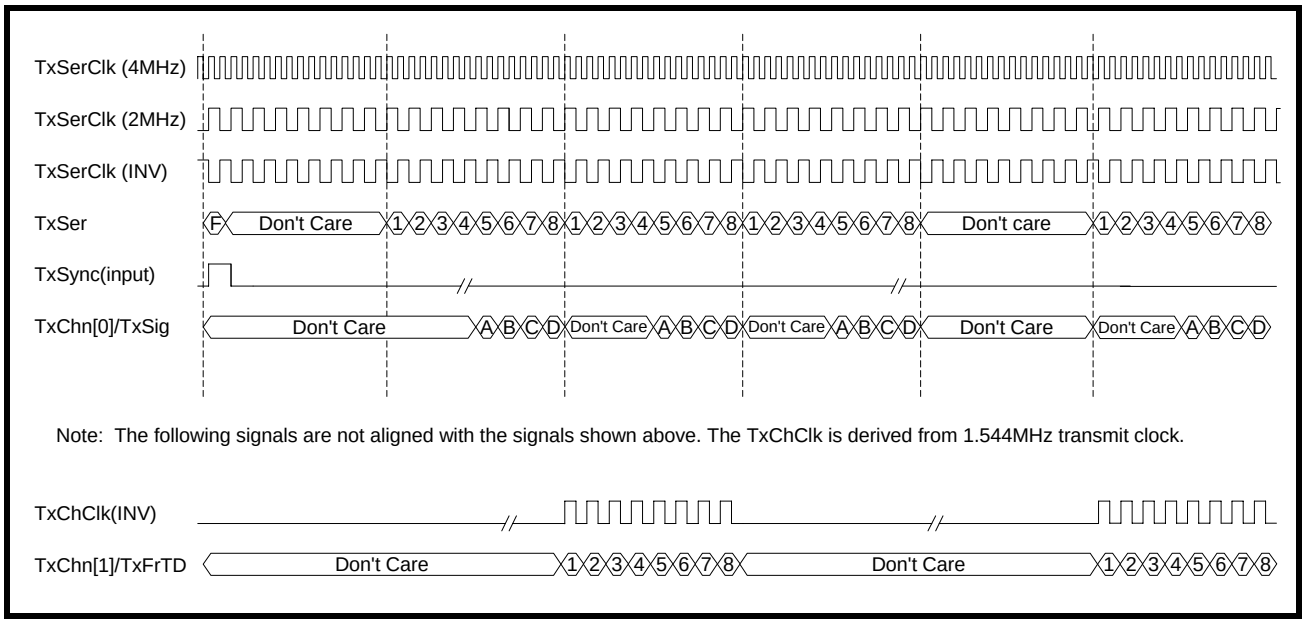
See Figure 89 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in 4.096Mbit/s mode.

FIGURE 89. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING 4.096MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at 4.096Mbit/s mode is shown in Figure 90.

FIGURE 90. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 4.096MBIT/S MODE



6.2.3.3 E1 Receive Input Interface - 8.192 MHz

(This interface mode is the same as running at 2.048 MHz. The only difference is that the Receive Serial Clock runs four times faster at 8.192MHz)

When the Receive Multiplex Enable bit is set to zero and the Receive Interface Mode Select [1:0] bits are set to 11, the Receive Back-plane interface of framer is running at a clock rate of 8.192MHz.

The interface consists of the following pins:

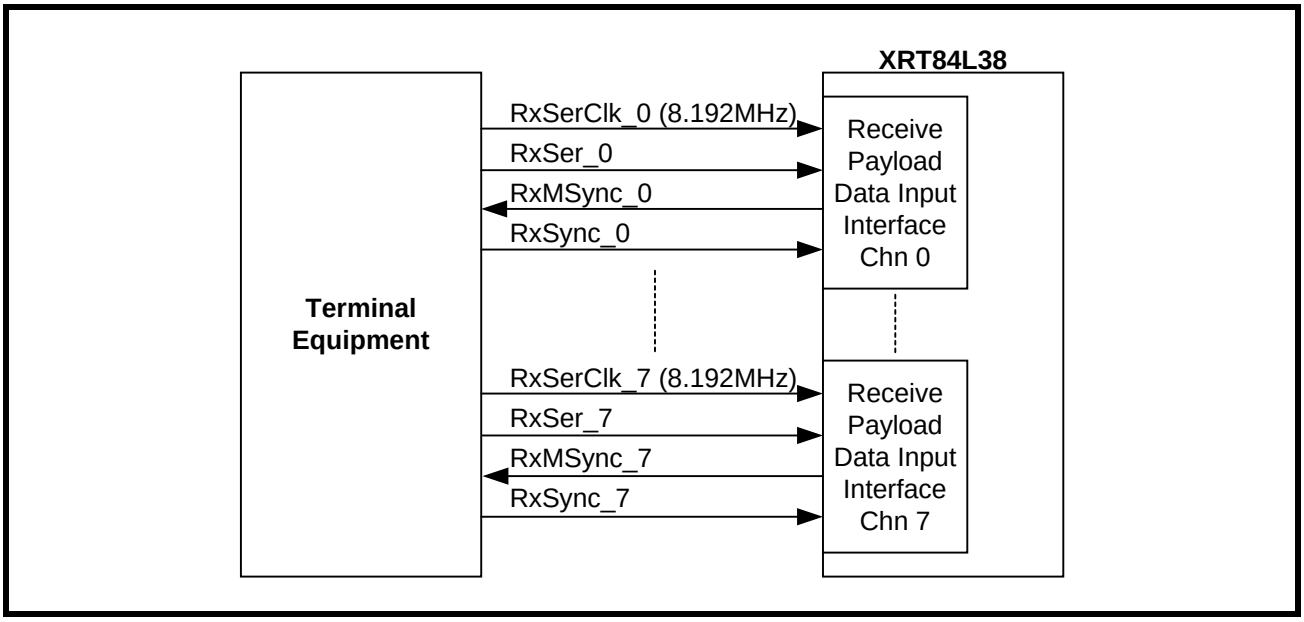
- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane interface is pumping out data through RxSer_n at an E1 equivalent data rate of 2.048Mbit/s. The local Terminal Equipment supplies a free-running 8.192MHz clock to the Receive Serial Clock input. The Receive High-speed Back-plane Interface of the framer then sends out serial data at every other four rising edge of the Receive Serial Clock. The local Terminal Equipment samples the serial data at every other four falling edge of the clock.

The Receive Single-frame Synchronization input signal (RxSync_n) should pulse HIGH at the beginning of the 256-bit frame indicating start of the frame. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the framer can identity the beginning of an E1 frame and start pumping payload data out.

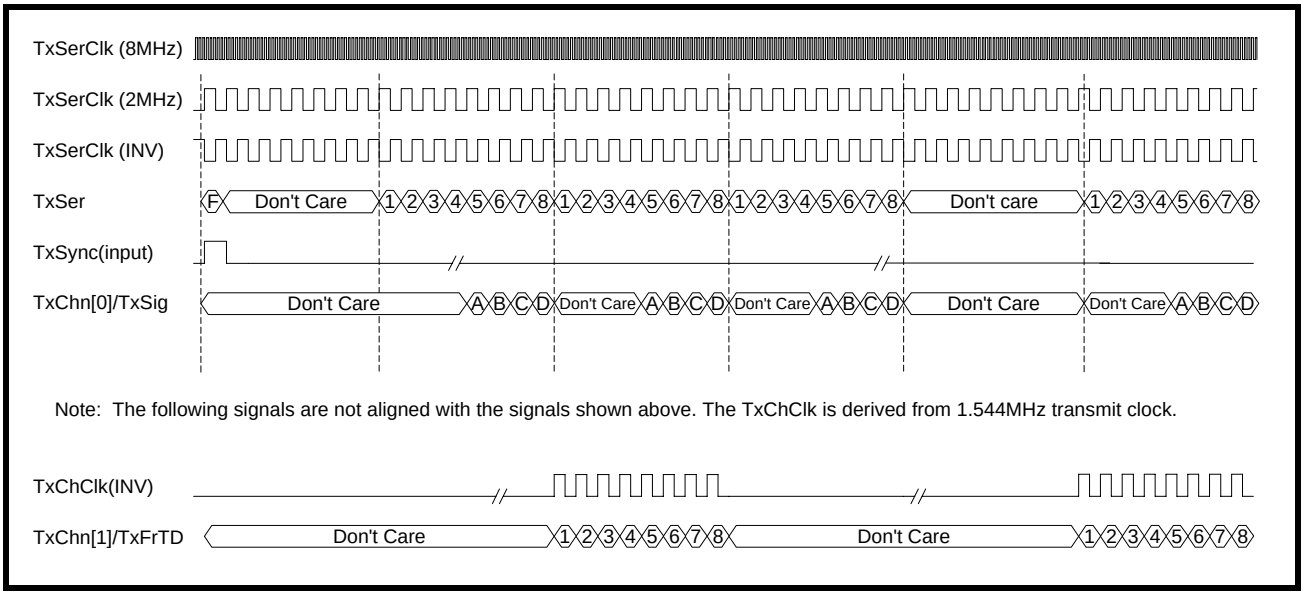
See Figure 91 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in 8.192Mbit/s mode.

FIGURE 91. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING 8.192MBIT/S DATA BUS



The timing diagram of input signals to the framer when running at 8.192Mbit/s mode is shown in Figure 92.

FIGURE 92. TIMING DIAGRAM OF INPUT SIGNALS TO THE FRAMER WHEN RUNNING AT 8.192MBIT/S MODE



6.2.3.4 E1 Receive Input Interface - Bit-Multiplexed 16.384Mbit/s

When the Receive Multiplex Enable bit is set to one and the Receive Interface Mode Select [1:0] bits are set to 01, the Receive Back-plane interface of framer is running at a clock rate of 16.384MHz.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)

- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane Interface is pumping out data through RxSer_0 or RxSer_4 pins at 16.384Mbit/s. It multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz are supplied to the Receive Serial Clock pin of Channel 0 and Channel 4 of the framer. The Receive High-speed Back-plane Interface of the farmer provides data at rising edge of this Receive Serial Clock. The local Terminal Equipment then latches incoming serial data at falling edge of the clock.

The Receive High-speed Back-plane Interface maps four 2.048Mbit/s E1 data streams into this 16.384Mbit/s data stream as described below:

1. Payload data of four channels are repeated and grouped together in a bit-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the first payload bit of Timeslot 0 of Channel 1 and 2. The first payload bit of Timeslot 0 of Channel 3 is sent last.

After the first bits of Timeslot 0 of all four channels are sent, it comes the second bit of Timeslot 0 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	1_1	1_1	1_2	1_2	1_3	1_3

SECOND OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
2_0	2_0	2_1	2_1	2_2	2_2	2_3	2_3

X_Y: The Xth payload bit of Channel Y

2. The Receive High-speed Back-plane Interface also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream.

When the Receive High-speed Back-plane Interface is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

FIFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	5_1	A_1	5_2	A_2	5_3	A_3

SIXTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
6_0	B_0	6_1	B_1	6_2	B_2	6_3	B_3

SEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
7_0	C_0	7_1	C_1	7_2	C_2	7_3	C_3

EIGHTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
8_0	D_0	8_1	D_1	8_2	D_2	8_3	D_3

X_Y: The Xth payload bit of Channel Y

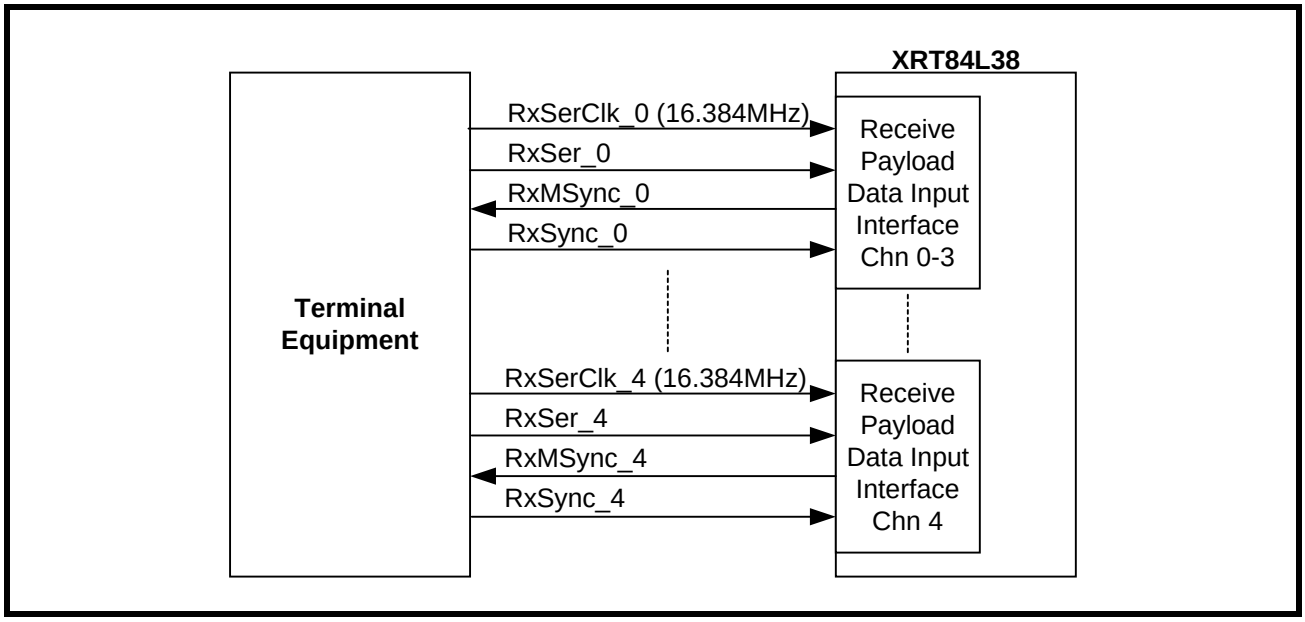
A_Y: The signaling bit A of Channel Y

3. After the first octets of all four channels are sent, the Receive High-speed Back-plane Interface will start sending the second octets following the same rules of Step 1 and 2.

The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH for one clock cycle at the first bit position of the data stream with data from Channel 0-3 multiplexed together. The Receive Single-frame Synchronization signal of Channel 4 pulses HIGH for one clock cycle at the first bit position of the data stream with data from Channel 4-7 multiplexed together. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the Receive High-speed Back-plane Interface of the framer can identify the beginning of a multiplexed frame and can start sending payload data of that frame.

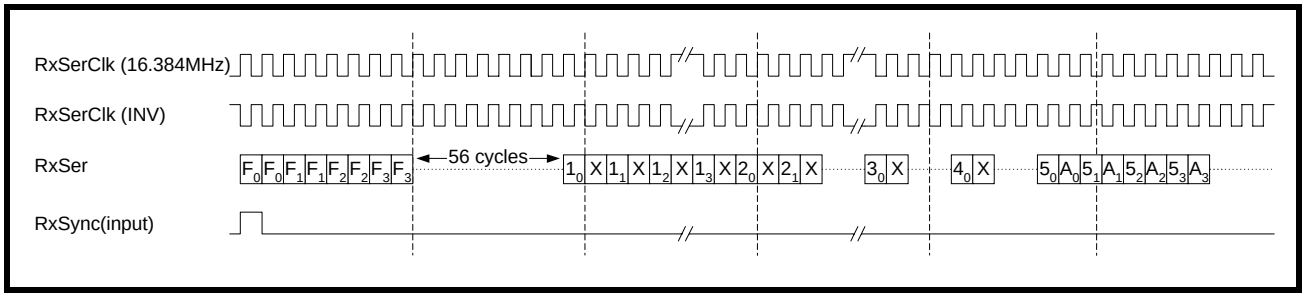
See Figure 93 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in Bit-multiplexed 16.384Mbit/s mode.

FIGURE 93. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING 16.384 MBIT/S DATA BUS



The Input signal timing is shown in Figure 94 below when the framer is running at Bit-Multiplexed 16.384Mbit/s mode.

FIGURE 94. TIMING SIGNAL WHEN THE FRAMER IS RUNNING AT BIT-MULTIPLEXED 16.384MBIT/S MODE



6.2.3.5 E1 Receive Input Interface - HMVIP 16.384Mbit/s

When the Receive Multiplex Enable bit is set to one and the Receive Interface Mode Select [1:0] bits are set to 10, the Receive Back-plane interface of framer is running at a clock rate of 16.384MHz.

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane Interface is pumping out data through RxSer_0 or RxSer_4 pins at 16.384Mbit/s. The Receive High-speed Back-plane Interface multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin

of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz are supplied to the Receive Serial Clock pin of Channel 0 and Channel 4 of the framer. The Receive High-speed Back-plane Interface of the farmer provides data at rising edge of this Receive Serial Clock. The local Terminal Equipment then latches incoming serial data at falling edge of the clock.

The Receive High-speed Back-plane Interface maps four 2.048Mbit/s E1 data streams into this 16.384Mbit/s data stream as described below:

1. Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0 and so on. After all the bits of Timeslot 0 of Channel 0 is sent repeatedly, the Terminal Equipment will start sending the payload bits of Timeslot 0 of Channel 1 and 2. The payload bits of Timeslot 0 of Channel 3 are sent the last.

After the payload bits of Timeslot 0 of all four channels are sent, it comes the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0

THIRD OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1

FIFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2

SEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3

X_Y: The Xth payload bit of Channel Y

2. The Receive High-speed Back-plane Interface also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream.

When the Receive High-speed Back-plane Interface is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

SECOND OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	6_0	B_0	7_0	C_0	8_0	D_0

FOURTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_1	A_1	6_1	B_1	7_1	C_1	8_1	D_1

SIXTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_2	A_2	6_2	B_2	7_2	C_2	8_2	D_2

EIGHTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_3	A_3	6_3	B_3	7_3	C_3	8_3	D_3

X_Y: The Xth payload bit of Channel Y

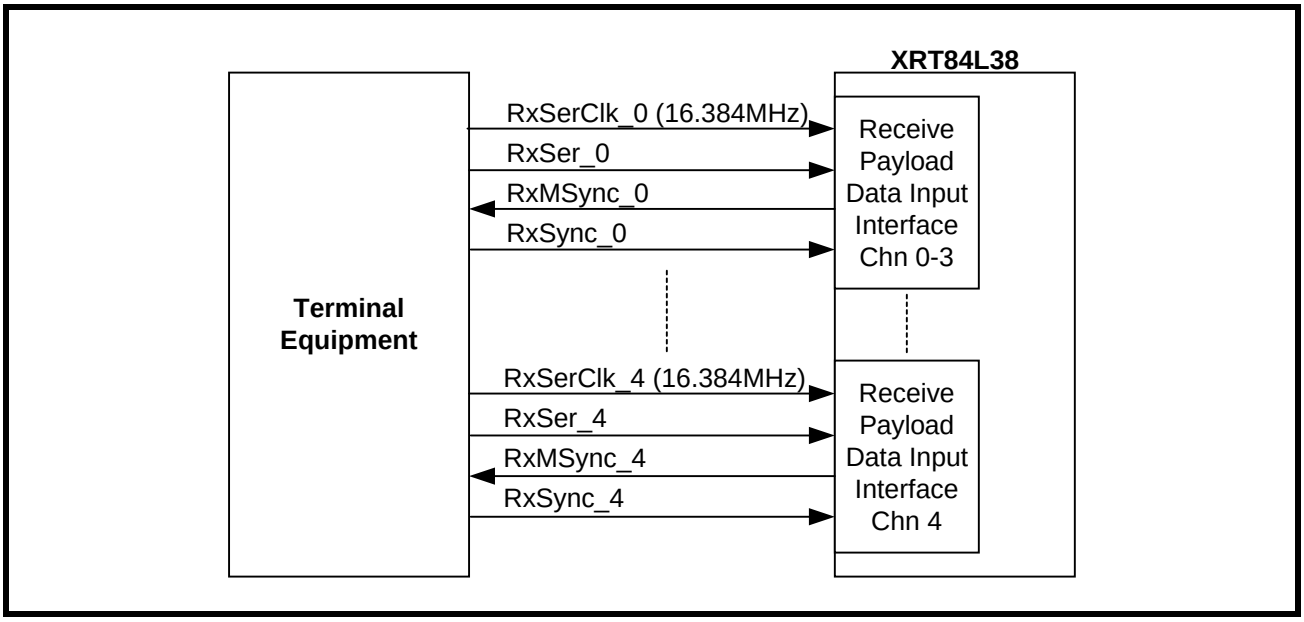
A_Y: The signaling bit A of Channel Y

3. After the first octets of all four channels are sent, the Receive High-speed Back-plane Interface will start sending the second octets following the same rules of Step 1 and 2.

The Receive Single-frame Synchronization signal should pulse HIGH for four clock cycles (the last two bit positions of the previous multiplexed frame and the first two bits of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the Receive High-speed Back-plane Interface of the framer can identify the beginning of a multiplexed frame and can start sending payload data of that frame.

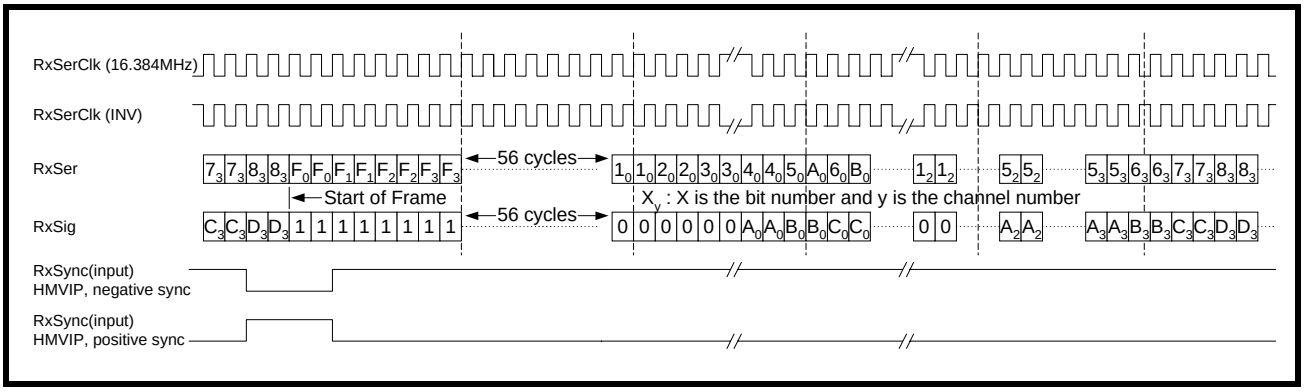
See Figure 95 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in HMVIP 16.384Mbit/s mode.

FIGURE 95. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 96 below when the framer is running at HMVIP 16.384Mbit/s mode.

FIGURE 96. TIMING SIGNAL WHEN THE FRAMER IS RUNNING AT HMVIP 16.384MBIT/S MODE



6.2.3.6 E1 Receive Input Interface - H.100 16.384Mbit/s

When the Receive Multiplex Enable bit is set to one and the Receive Interface Mode Select [1:0] bits are set to 11, the Receive Back-plane interface of framer is running at H.100 16.384Mbit/s mode.

(The HMVIP mode and the H.100 mode are essential the same except for the HIGH pulse position of the Receive Single-frame Synchronization Signal)

The interface consists of the following pins:

- Data input (RxSer_n)
- Receive Serial Clock Input signal (RxSerClk_n)
- Receive Single-frame Synchronization Input signal (RxSync_n)
- Receive Input Clock (RxInClk_n)
- Receive Time-slot Indication clock (RxTSClk_n)
- Receive Time Slot indicator bits (RxTSb[4:0]_n)

The Receive Back-plane Interface is pumping out data through RxSer_0 or RxSer_4 pins at 16.384Mbit/s. The Receive High-speed Back-plane Interface multiplexes payload and signaling data of every four channels into one data stream. Payload and signaling data of Channel 0-3 are multiplexed onto the Receive Serial Data pin of Channel 0. Payload and signaling data of Channel 4-7 are multiplexed onto the Receive Serial Data pin of Channel 4.

Free-running clocks of 16.384MHz are supplied to the Receive Serial Clock pin of Channel 0 and Channel 4 of the framer. The Receive High-speed Back-plane Interface of the farmer provides data at rising edge of this Receive Serial Clock. The local Terminal Equipment then latches incoming serial data at falling edge of the clock.

The Receive High-speed Back-plane Interface maps four 2.048Mbit/s E1 data streams into this 16.384Mbit/s data stream as described below:

1. Payload data of four channels are repeated and grouped together in a byte-interleaved way. The first payload bit of Timeslot 0 of Channel 0 is sent first, followed by the second payload bit of Timeslot 0 of Channel 0 and so on. After all the bits of Timeslot 0 of Channel 0 is sent repeatedly, the Receive High-speed Back-plane Interface will start sending the payload bits of Timeslot 0 of Channel 1 and 2. The payload bits of Timeslot 0 of Channel 3 are sent the last.

After the payload bits of Timeslot 0 of all four channels are sent, it comes the payload bits of Timeslot 1 of Channel 0 and so on. The table below demonstrates how payload bits of four channels are mapped into the 16.384Mbit/s data stream.

FIRST OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_0	1_0	2_0	2_0	3_0	3_0	4_0	4_0

THIRD OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_1	1_1	2_1	2_1	3_1	3_1	4_1	4_1

FIFTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_2	1_2	2_2	2_2	3_2	3_2	4_2	4_2

SEVENTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
1_3	1_3	2_3	2_3	3_3	3_3	4_3	4_3

X_Y: The Xth payload bit of Channel Y

2. The Receive High-speed Back-plane Interface also multiplexed signaling bits with payload bits and sent them together through the 16.384Mbit/s data stream.

When the Receive High-speed Back-plane Interface is sending the fifth payload bit of a particular channel, instead of sending it twice, it inserts the signaling bit A of that particular channel. Similarly, the sixth payload bit of a particular channels is followed by the signaling bit B of that channel; the seventh payload bit is followed by the signaling bit C; the eighth payload bit is followed by the signaling bit D.

The following table illustrates how payload bits and signaling bits are multiplexed together into the 16.384Mbit/s data stream.

SECOND OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_0	A_0	6_0	B_0	7_0	C_0	8_0	D_0

FOURTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_1	A_1	6_1	B_1	7_1	C_1	8_1	D_1

SIXTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_2	A_2	6_2	B_2	7_2	C_2	8_2	D_2

EIGHTH OCTET OF 16.384MBIT/S DATA STREAM

BIT 0	BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
5_3	A_3	6_3	B_3	7_3	C_3	8_3	D_3

X_Y: The Xth payload bit of Channel Y

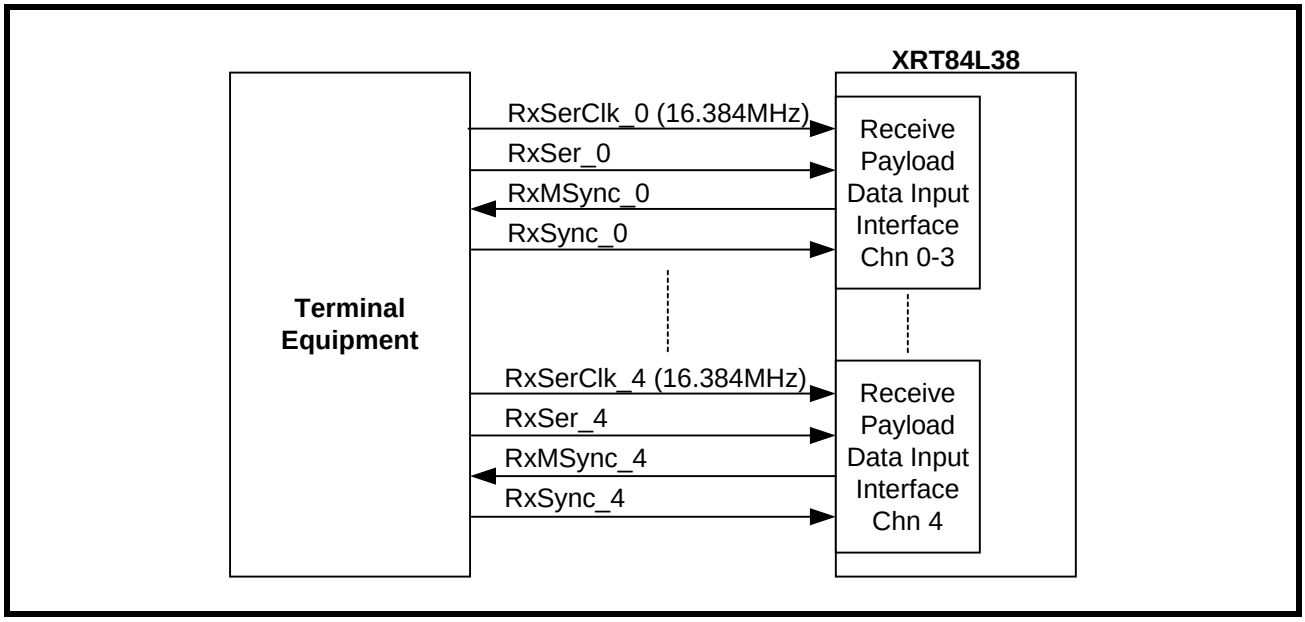
A_Y: The signaling bit A of Channel Y

3. After the first octets of all four channels are sent, the Receive High-speed Back-plane Interface will start sending the second octets following the same rules of Step 1 and 2.

The Receive Single-frame Synchronization signal should pulse HIGH for two clock cycles (the last bit position of the previous multiplexed frame and the first bit position of the next multiplexed frame) indicating frame boundary of the multiplexed data stream. The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. The Receive Single-frame Synchronization signal of Channel 0 pulses HIGH to identify the start of multiplexed data stream of Channel 0-3. By sampling the HIGH pulse of the Receive Single-frame Synchronization signal, the Receive High-speed Back-plane Interface of the framer can identify the beginning of a multiplexed frame and can start sending payload data of that frame.

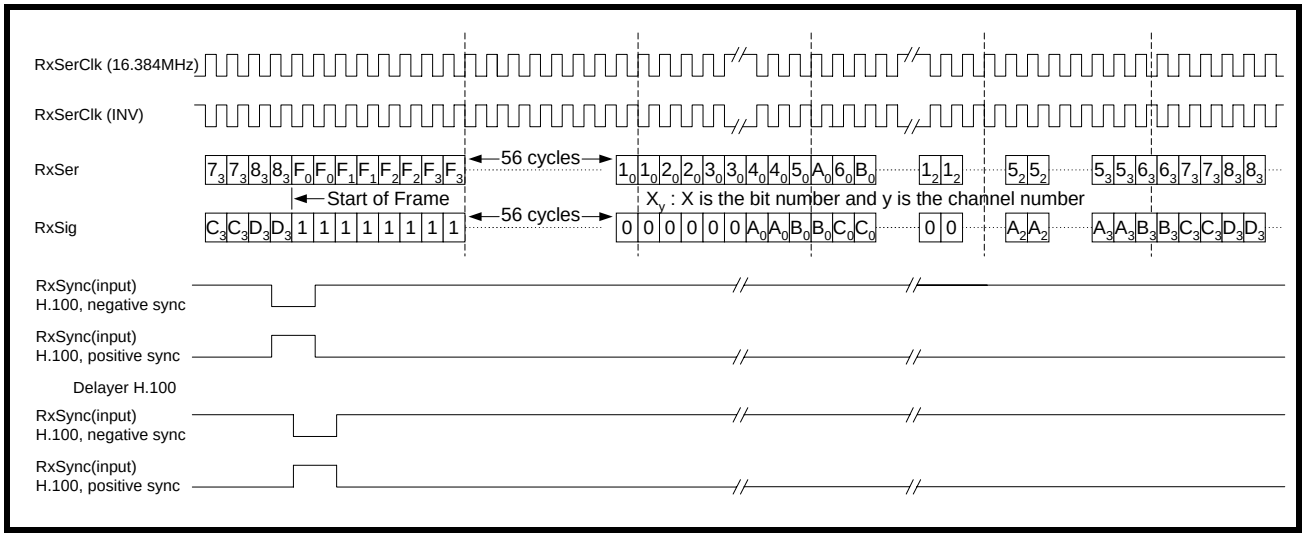
See Figure 97 below for how to interface the local Terminal Equipment with the Receive Payload Data Output Interface block of the framer in HMVIP 16.384Mbit/s mode.

FIGURE 97. INTERFACING XRT84L38 TO LOCAL TERMINAL EQUIPMENT USING 16.384MBIT/S DATA BUS



The Input signal timing is shown in Figure 98 below when the framer is running at H.100 16.384Mbit/s mode.

FIGURE 98. TIMING SIGNAL WHEN THE FRAMER IS RUNNING AT H.100 16.384MBIT/S MODE



7.0 DS1 OVERHEAD INTERFACE BLOCK

The XRT84L38 has the ability to extract or insert DS1 data link information from or into the following:

- Facility Data Link (FDL) bits in ESF framing format mode
- Signaling Framing (Fs) bits in SLC®96 and N framing format mode
- Remote Signaling (R) bits in T1DM framing format mode

The source and destination of these inserted and extracted data link bits would be from either the internal HDLC Controller or the external device accessible through DS1 Overhead Interface Block. The operation of the Transmit Overhead Input Interface Block and the Receive Overhead Output Interface Block will be discussed separately.

7.1 DS1 Transmit Overhead Input Interface Block

7.1.1 Description of the DS1 Transmit Overhead Input Interface Block

The DS1 Transmit Overhead Input Interface Block will allow an external device to be the provider of the Facility Data Link (FDL) bits in ESF framing format mode, Signaling Framing (Fs) bits in the SLC96 and N framing format mode and Remote Signaling (R) bit in T1DM framing format mode. This interface provides interface signals and required interface timing to shift in proper data link information at proper time.

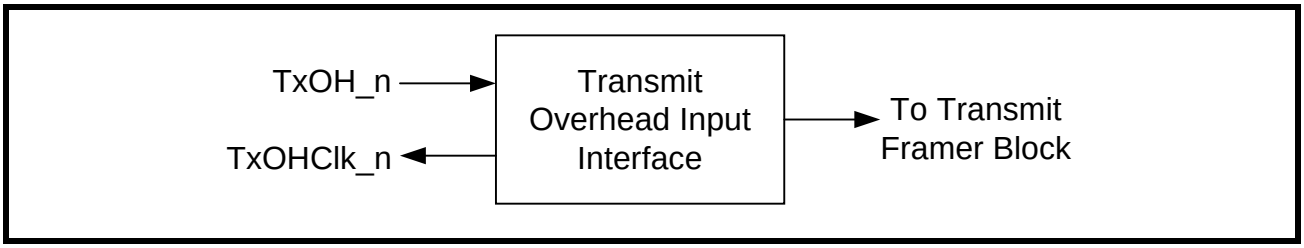
The Transmit Overhead Input Interface for a given Framer consists of two signals.

- TxOHClk_n: The Transmit Overhead Input Interface Clock Output signal
- TxOH_n: The Transmit Overhead Input Interface Input signal.

The Transmit Overhead Input Interface Clock Output pin (TxOHCLK_n) generates a rising clock edge for each data link bit position according to configuration of the framer. The Data Link equipment interfaced to the Transmit Overhead Input Interface block should update the data link bits on the TxOH_n line upon detection of the rising edge of TxOHClk_n. The Transmit Overhead Input Interface block will sample and latch the data link bits on the TxOH_n line on the falling edge of TxOHClk_n. The data link bits will be included and transmitted via the outgoing DS1 frames.

The figure below shows block diagram of the DS1 Transmit Overhead Input Interface of XRT84L38.

Figure 99. Block Diagram of the DS1 Transmit Overhead Input Interface of the XRT84L38



7.1.2 Configure the DS1 Transmit Overhead Input Interface module as source of the Facility Data Link (FDL) bits in ESF framing format mode

The FDL bits in ESF framing format mode can be inserted from:

- DS1 Transmit Overhead Input Interface Block
- DS1 Transmit HDLC Controller
- DS1 Transmit Serial Input Interface.

The Transmit Data Link Source Select bits of the Transmit Data Link Select Register (TDLSR) controls the insertion of data link bits into the FDL bits in ESF framing format mode. The table below shows configuration of the Transmit Data Link Source Select bits of the Transmit Data Link Select Register (TDLSR).

TRANSMIT DATA LINK SELECT REGISTER (TDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Data Link Source Select	R/W	00 - The Facility Data Link bits are inserted into the framer through either the LAPD controller or the SLCâ96 buffer. 01 - The Facility Data Link bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins. 10 - The Facility Data Link bits are inserted into the framer through the Transmit Overhead Input Interface via the TxOH_n pins. 11 - The Facility Data Link bits are forced to one by the framer.

If the Transmit Data Link Source Select bits of the Transmit Data Link Select Register are set to 10, the Transmit Overhead Input Interface Block becomes input source of the FDL bits.

The XRT84L38 allows the user to select bandwidth of the Facility Data Link Channel in ESF framing format mode. The FDL can be either a 4KHz or 2KHz data link channel. The Transmit Data Link Bandwidth Select bits of the Transmit Data Link Select Register (TDLSR) determine the bandwidth of FDL channel in ESF framing format mode.

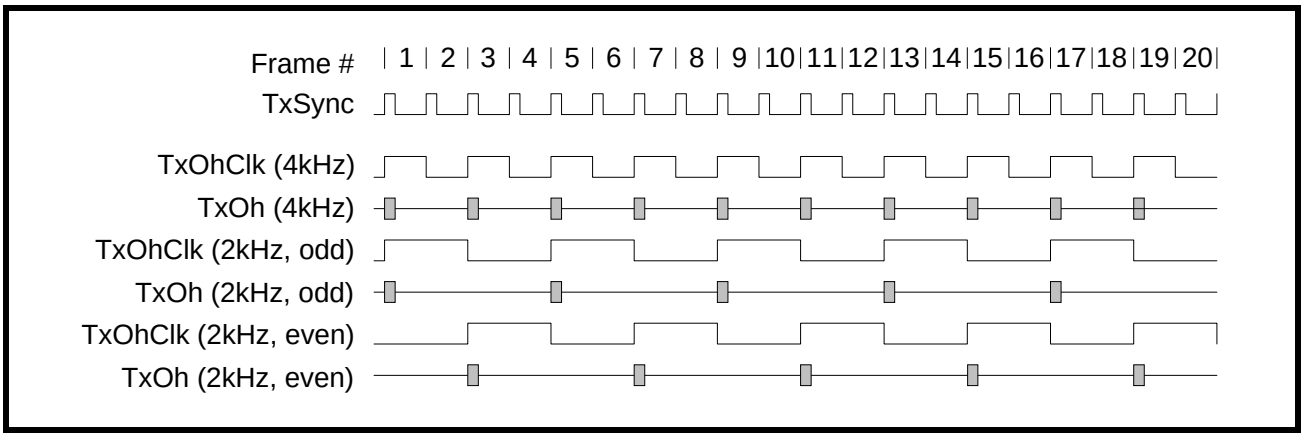
The table below shows configuration of the Transmit Data Link Bandwidth Select bits of the Transmit Data Link Select Register (TDLSR).)

TRANSMIT DATA LINK SELECT REGISTER (TDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	Transmit Data Link Bandwidth Select	R/W	00 - The Facility Data Link is a 4KHz channel. All available FDL bits (first bit of every other frame) are used as data link bits. 01 - The Facility Data Link is a 2KHz channel. Only the odd FDL bits (first bit of frame 1, 5, 9…) are used as data link bits. 10 - The Facility Data Link is a 2KHz channel. Only the even FDL bits (first bit of frame 3, 7, 11…) are used as data link bits.

Figure 100 below shows the timing diagram of the input and output signals associated with the DS1 Transmit Overhead Input Interface module in ESF framing format mode.

FIGURE 100. DS1 TRANSMIT OVERHEAD INPUT INTERFACE TIMING IN ESF FRAMING FORMAT MODE



7.1.3 Configure the DS1 Transmit Overhead Input Interface module as source of the Signaling Framing (Fs) bits in N or SLC®96 framing format mode

The Fs bits in SLC®96 and N framing format mode can be inserted from:

- DS1 Transmit Overhead Input Interface Block
- DS1 Transmit HDLC Controller
- DS1 Transmit Serial Input Interface.

The Transmit Data Link Source Select bits of the Transmit Data Link Select Register (TDLSR) controls the insertion of data link bits into the Fs bits in N or SLC®96 framing format mode. The table below shows configuration of the Transmit Data Link Source Select bits of the Transmit Data Link Select Register (TDLSR).

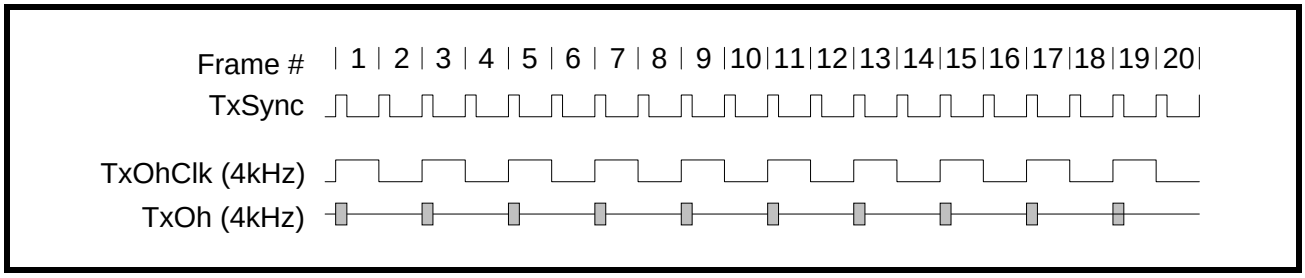
TRANSMIT DATA LINK SELECT REGISTER (TDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Data Link Source Select	R/W	00 - The Signaling Framing bits are inserted into the framer through either the LAPD controller or the SLCâ96 buffer. 01 - The Signaling Framing bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins. 10 - The Signaling Framing bits are inserted into the framer through the Transmit Overhead Input Interface via the TxOH_n pins. 11 - The Signaling Framing bits are forced to one by the framer.

If the Transmit Data Link Source Select bits of the Transmit Data Link Select Register are set to 10, the Transmit Overhead Input Interface Block becomes input source of the Fs bits.

Figure 101 below shows the timing diagram of the input and output signals associated with the DS1 Transmit Overhead Input Interface module in N or SLC®96 framing format mode.

FIGURE 101. DS1 TRANSMIT OVERHEAD INPUT TIMING IN N OR SLC®96 FRAMING FORMAT MODE



7.1.4 Configure the DS1 Transmit Overhead Input Interface module as source of the Remote Signaling (R) bits in T1DM framing format mode

The R bits in T1DM framing format mode can be inserted from:

- DS1 Transmit Overhead Input Interface Block
- DS1 Transmit HDLC Controller
- DS1 Transmit Serial Input Interface.

The Transmit Data Link Source Select bits of the Transmit Data Link Select Register (TDLSR) controls the insertion of data link bits into the R bits in T1DM framing format mode. The table below shows configuration of the Transmit Data Link Source Select bits of the Transmit Data Link Select Register (TDLSR).

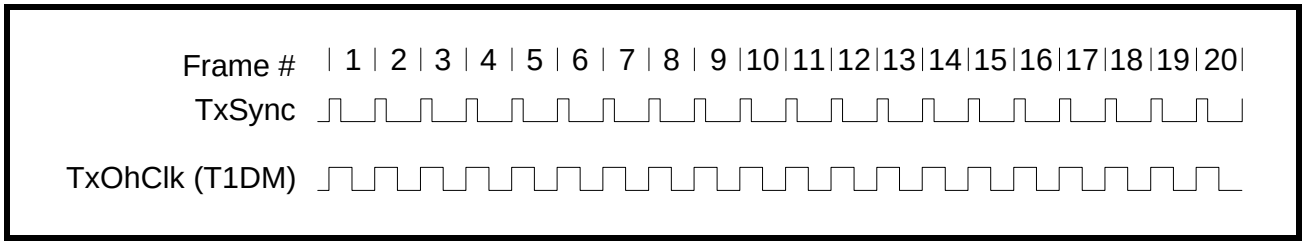
TRANSMIT DATA LINK SELECT REGISTER (TDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Data Link Source Select	R/W	00 - The Remote Signaling bits are inserted into the framer through either the LAPD controller or the SLCâ96 buffer. 01 - The Remote Signaling bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins. 10 - The Remote Signaling bits are inserted into the framer through the Transmit Overhead Input Interface via the TxOH_n pins. 11 - The Remote Signaling bits are forced to one by the framer.

If the Transmit Data Link Source Select bits of the Transmit Data Link Select Register are set to 10, the Transmit Overhead Input Interface Block becomes input source of the R bits. Since R bit presents in Timeslot 24 of every T1DM frame, therefore, bandwidth of T1DM data link channel is 8KHz.

Figure 102 below shows the timing diagram of the input and output signals associated with the DS1 Transmit Overhead Input Interface module in T1DM framing format mode.

FIGURE 102. DS1 TRANSMIT OVERHEAD INPUT INTERFACE MODULE IN T1DM FRAMING FORMAT MODE



7.2 DS1 Receive Overhead Output Interface Block

7.2.1 Description of the DS1 Receive Overhead Output Interface Block

The DS1 Receive Overhead Output Interface Block allows an external device to be the consumer of the Facility Data Link (FDL) bits in ESF framing format mode, Signaling Framing (Fs) bits in the SLC96 and N framing format mode and Remote Signaling (R) bit in T1DM framing format mode This interface provides interface signals and required interface timing to shift out proper data link information at proper time.

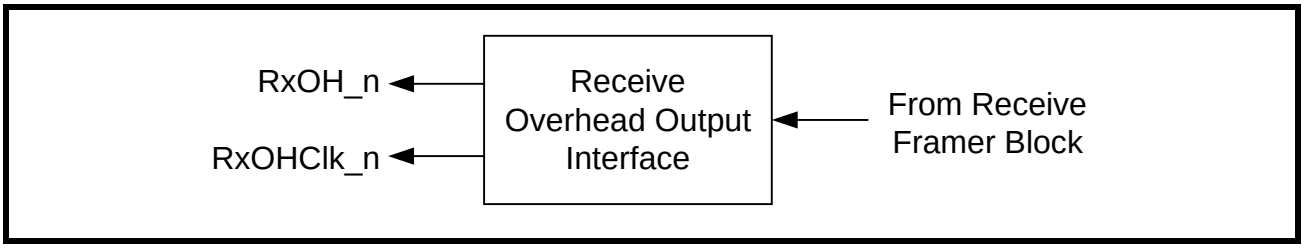
The Receive Overhead Output Interface for a given Framer consists of two signals.

- RxOHClk_n: The Receive Overhead Output Interface Clock Output signal
- RxOH_n: The Receive Overhead Output Interface Output signal.

The Receive Overhead Output Interface Clock Output pin (RxOHCLK_n) generates a rising clock edge for each data link bit position according to configuration of the framer. The data link bits extracted from the incoming T1 frames are outputted from the Receive Overhead Output Interface Output pin (RxOH_n) at the rising edge of RxOHClk_n. The Data Link equipment should sample and latch the data link bits at the falling edge of RxOHClk_n.

The figure below shows block diagram of the Receive Overhead Output Interface of XRT84L38.

Figure 103. Block Diagram of the DS1 Receive Overhead Output Interface of XRT84L38



7.2.2 Configure the DS1 Receive Overhead Output Interface module as destination of the Facility Data Link (FDL) bits in ESF framing format mode

The FDL bits in ESF framing format mode can be extracted to:

- DS1 Receive Overhead Output Interface Block
- DS1 Receive HDLC Controller
- DS1 Receive Serial Output Interface.

The Receive Data Link Source Select bits of the Receive Data Link Select Register (RDLSR) controls the extraction of FDL bits in ESF framing format mode. The table below shows configuration of the Receive Data Link Source Select bits of the Receive Data Link Select Register (RDLSR).

RECEIVE DATA LINK SELECT REGISTER (TDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Receive Data Link Destination Select	R/W	00 - The extracted Facility Data Link bits are stored in either the LAPD controller or the SLCâ96 buffer. At the same time, the extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 01 - The extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 10 - The extracted Facility Data Link bits are outputted from the framer through the Receive Overhead Output Interface via the RxOH_n pins. At the same time, the extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 11 - The Facility Data Link bits are forced to one by the framer.

If the Receive Data Link Source Select bits of the Receive Data Link Select Register are set to 10, the Receive Overhead Output Interface Block becomes Output source of the FDL bits.

The XRT84L38 allows the user to select bandwidth of the Facility Data Link Channel in ESF framing format mode. The FDL can be either a 4KHz or 2KHz data link channel. The Receive Data Link Bandwidth Select bits of the Receive Data Link Select Register (RDLSR) determine the bandwidth of FDL channel in ESF framing format mode.

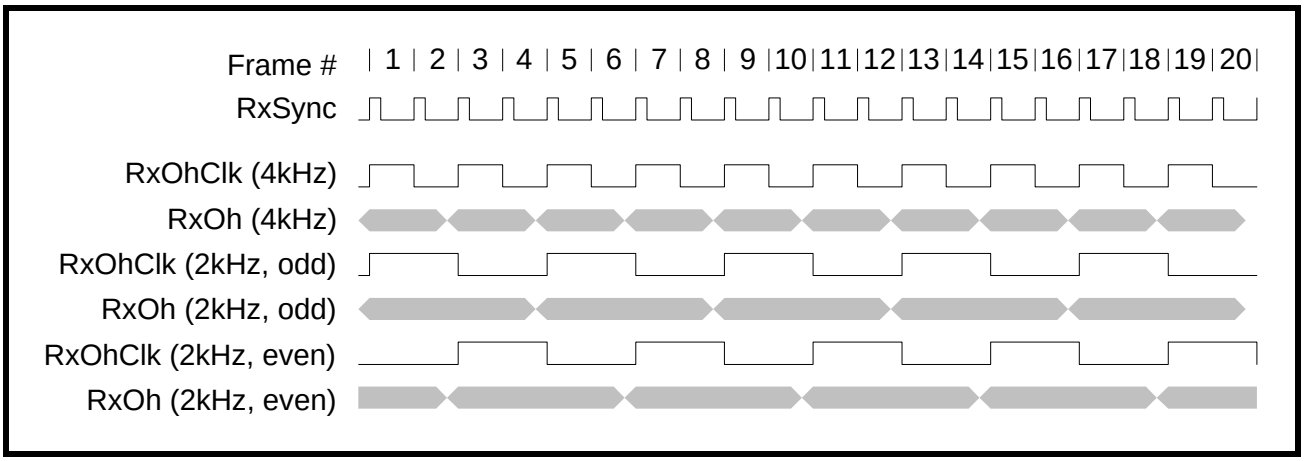
The table below shows configuration of the Receive Data Link Bandwidth Select bits of the Receive Data Link Select Register (TDLSR).

RECEIVE DATA LINK SELECT REGISTER (TDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	Receive Data Link Bandwidth Select	R/W	00 - The Facility Data Link is a 4KHz channel. All available FDL bits (first bit of every other frame) are used as data link bits. 01 - The Facility Data Link is a 2KHz channel. Only the odd FDL bits (first bit of frame 1, 5, 9…) are used as data link bits. 10 - The Facility Data Link is a 2KHz channel. Only the even FDL bits (first bit of frame 3, 7, 11…) are used as data link bits.

Figure 104 below shows the timing diagram of the Output and output signals associated with the DS1 Receive Overhead Output Interface module in ESF framing format mode.

FIGURE 104. DS1 RECEIVE OVERHEAD OUTPUT INTERFACE MODULE IN ESF FRAMING FORMAT MODE



7.2.3 Configure the DS1 Receive Overhead Output Interface module as destination of the Signaling Framing (Fs) bits in N or SLC®96 framing format mode

The Fs bits in SLC®96 and N framing format mode can be extracted to:

- DS1 Receive Overhead Output Interface Block
- DS1 Receive HDLC Controller
- DS1 Receive Serial Output Interface.

The Receive Data Link Source Select bits of the Receive Data Link Select Register (RDLSR) controls the destination of Fs bits in N or SLC®96 framing format mode. The table below shows configuration of the Receive Data Link Source Select bits of the Receive Data Link Select Register (RDLSR).

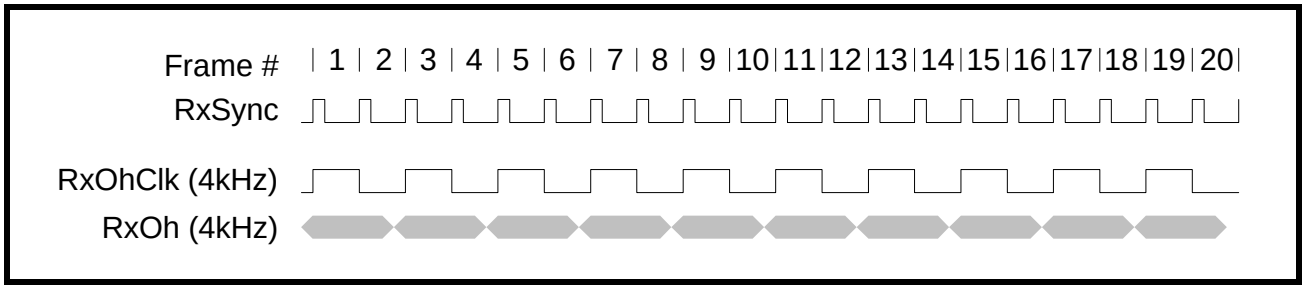
RECEIVE DATA LINK SELECT REGISTER (TDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Receive Data Link Source Select	R/W	00 - The extracted Facility Data Link bits are stored in either the LAPD controller or the SLCâ96 buffer. At the same time, the extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 01 - The extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 10 - The extracted Facility Data Link bits are outputted from the framer through the Receive Overhead Output Interface via the RxOH_n pins. At the same time, the extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 11 - The Facility Data Link bits are forced to one by the framer.

If the Receive Data Link Source Select bits of the Receive Data Link Select Register are set to 10, the Receive Overhead Output Interface Block outputs Fs bits extracted from the incoming T1 data stream.

Figure 105 below shows the timing diagram of the output signals associated with the DS1 Receive Overhead Output Interface module in N or SLC®96 framing format mode.

FIGURE 105. DS1 RECEIVE OVERHEAD OUTPUT INTERFACE TIMING IN N OR SLC®96 FRAMING FORMAT MODE



7.2.4 Configure the DS1 Receive Overhead Output Interface module as destination of the Remote Signaling (R) bits in T1DM framing format mode

The R bits in T1DM framing format mode can be extracted to:

- DS1 Receive Overhead Output Interface Block
- DS1 Receive HDLC Controller
- DS1 Receive Serial Output Interface.

The Receive Data Link Source Select bits of the Receive Data Link Select Register (RDLSR) controls the destination of R bits in T1DM framing format mode. The table below shows configuration of the Receive Data Link Source Select bits of the Receive Data Link Select Register (RDLSR).

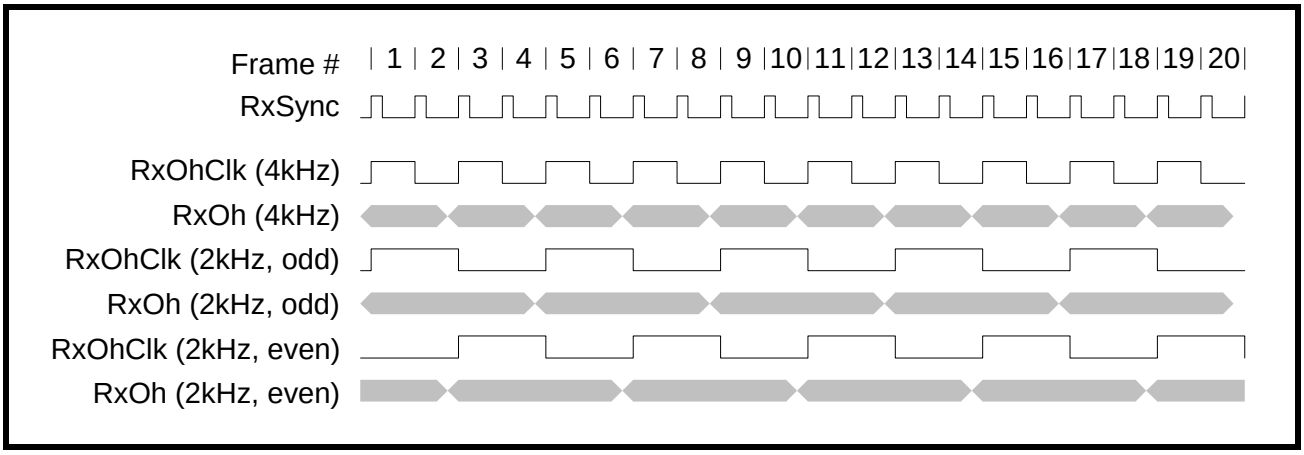
RECEIVE DATA LINK SELECT REGISTER (RDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Receive Data Link Source Select	R/W	00 - The extracted Facility Data Link bits are stored in either the LAPD controller or the SLC®96 buffer. At the same time, the extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 01 - The extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 10 - The extracted Facility Data Link bits are outputted from the framer through the Receive Overhead Output Interface via the RxOH_n pins. At the same time, the extracted Facility Data Link bits are outputted from the framer through the Receive Serial Data Output Interface via the RxSer_n pins. 11 - The Facility Data Link bits are forced to one by the framer.

If the Receive Data Link Source Select bits of the Receive Data Link Select Register are set to 10, the Receive Overhead Output Interface Block outputs the R bits extracted from the incoming T1 data stream. Since R bit presents in Timeslot 24 of every T1DM frame, therefore, bandwidth of T1DM data link channel is 8KHz.

Figure 106 below shows the timing diagram of the output signals associated with the DS1 Receive Overhead Output Interface module in T1DM framing format mode.

FIGURE 106. DS1 RECEIVE OVERHEAD OUTPUT INTERFACE TIMING IN T1DM FRAMING FORMAT MODE



8.0 E1 OVERHEAD INTERFACE BLOCK

The XRT84L38 has the ability to extract or insert E1 data link information from or into the E1 National bit sequence. The source and destination of these inserted and extracted data link bits would be from either the internal HDLC Controller or the external device accessible through E1 Overhead Interface Block. The operation of the Transmit Overhead Input Interface Block and the Receive Overhead Output Interface Block will be discussed separately.

8.1 E1 TRANSMIT OVERHEAD INPUT INTERFACE BLOCK

8.1.1 Description of the E1 Transmit Overhead Input Interface Block

The E1 Transmit Overhead Input Interface Block will allow an external device to be the provider of the E1 National bit sequence. This interface provides interface signals and required interface timing to shift in proper data link information at proper time.

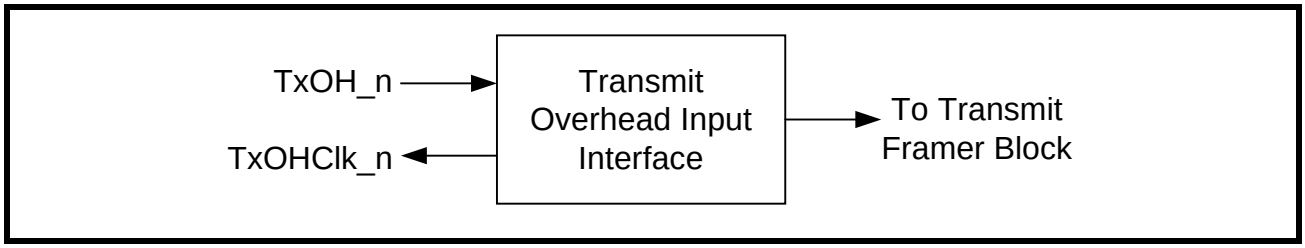
The Transmit Overhead Input Interface for a given Framer consists of two signals.

- TxOHClk_n: The Transmit Overhead Input Interface Clock Output signal
- TxOH_n: The Transmit Overhead Input Interface Input signal.

The Transmit Overhead Input Interface Clock Output pin (TxOHCLK_n) generates a rising clock edge for each National bit that is configured to carry Data Link information according to setting of the framer. The Data Link equipment interfaced to the Transmit Overhead Input Interface should update the data link bits on the TxOH_n line upon detection of the rising edge of TxOHClk_n. The Transmit Overhead Input Interface block will sample and latch the data link bits on the TxOH_n line on the falling edge of TxOHClk_n. The data link bits will be included in and transmitted via the outgoing E1 frames.

The figure below shows block diagram of the DS1 Transmit Overhead Input Interface of XRT84L38.

FIGURE 107. BLOCK DIAGRAM OF THE E1 TRANSMIT OVERHEAD INPUT INTERFACE OF XRT84L38



8.1.2 Configure the E1 Transmit Overhead Input Interface module as source of the National Bit Sequence in E1 framing format mode

The National Bit Sequence in E1 framing format mode can be inserted from:

- E1 Transmit Overhead Input Interface Block
- E1 Transmit HDLC Controller
- E1 Transmit Serial Input Interface

The purpose of the Transmit Overhead Input Interface is to permit Data Link equipment direct access to the Sa4 through Sa8 National bits that are to be transported via the outbound frames. The Transmit Data Link Source Select [1:0] bits, within the Synchronization MUX Register (SMR) determine source of the Sa4 through Sa8 National bits to be inserted into the outgoing E1 frames.

The table below shows configuration of the Transmit Data Link Source Select [1:0] bits of the Synchronization MUX Register (SMR).

SYNCHRONIZATION MUX REGISTER (SMR) (INDIRECT ADDRESS = 0XN0H, 0X09H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Transmit Data Link Source Select [1:0]	R/W	00 - The Sa4 through Sa8 National bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins. 01 - The Sa4 through Sa8 National bits are inserted into the framer through the Transmit LAPD Controller. 10 - The Sa4 through Sa8 National bits are inserted into the framer through the Transmit Overhead Input Interface via the TxOH_n pins. 11 - The Sa4 through Sa8 National bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins.

If the Transmit Data Link Source Select bits of the Transmit Data Link Select Register are set to 10, the Transmit Overhead Input Interface Block becomes input source of the FDL bits.

The XRT84L38 allows the user to decide on the following:

- How many of the National Bits will be used to carry the Data Link information bits
- Which of these National Bits will be used to carry the Data Link information bits.

The Transmit Sa Data Link Select bits of the Transmit Signaling and Data Link Select Register (TSDLSR) determine which ones of the National bits are configured as Data Link bits in E1 framing format mode. Depending upon the configuration of the Transmit Signaling and Data Link Select Register, either of the following cases may exists:

- None of the National bits are used to transport the Data Link information bits (That is, data link channel of XRT84L38 is inactive).
- Any combination of between 1 and all 5 of the National bits can be selected to transport the Data Link information bits.

The table below shows configuration of the Transmit Sa Data Link Select bits of the Transmit Signaling and Data Link Select Register (TSDLSR).

TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0AH)

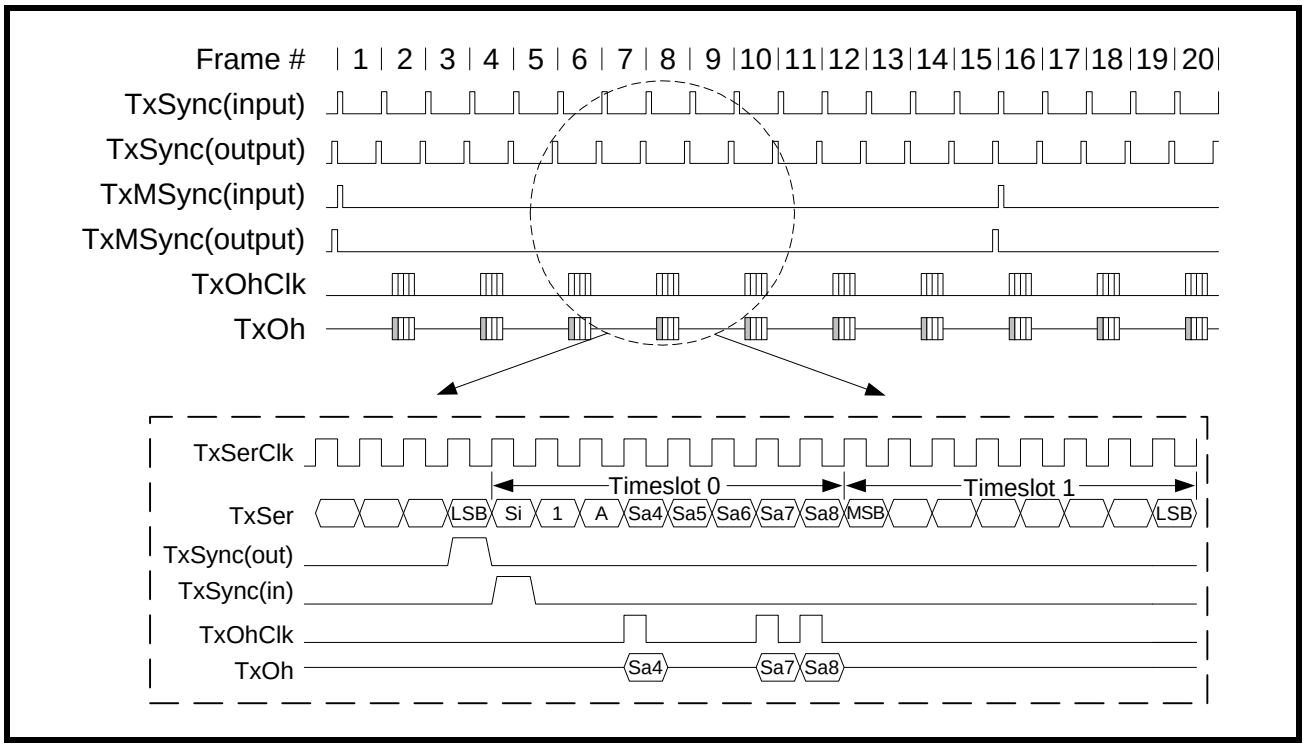
BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Transmit Sa8 Data Link Select	R/W	0 - Source of the Sa8 Nation bit is not from the data link interface. 1 - Source the Sa8 National bit from the data link interface.
6	Transmit Sa7 Data Link Select	R/W	0 - Source of the Sa7 Nation bit is not from the data link interface. 1 - Source the Sa7 National bit from the data link interface.
5	Transmit Sa6 Data Link Select	R/W	0 - Source of the Sa6 Nation bit is not from the data link interface. 1 - Source the Sa6 National bit from the data link interface.
4	Transmit Sa5 Data Link Select	R/W	0 - Source of the Sa5 Nation bit is not from the data link interface. 1 - Source the Sa5 National bit from the data link interface.
3	Transmit Sa4 Data Link Select	R/W	0 - Source of the Sa4 Nation bit is not from the data link interface. 1 - Source the Sa4 National bit from the data link interface.

For every Sa bit that is selected to carry Data Link information, the Transmit Overhead Input Interface will supply a clock pulse, via the TxOHClk_n output pin, such that:

- The Data Link equipment interfaced to the Transmit Overhead Input Interface should update the data on the TxOH_n line upon detection of the rising edge of TxOHClk_n.
- The Transmit Overhead Input Interface will sample and latch the data on the TxOH_n line on the falling edge of TxOHClk_n.

Figure 108 below shows the timing diagram of the input and output signals associated with the E1 Transmit Overhead Input Interface module in E1 framing format mode.

FIGURE 108. E1 TRANSMIT OVERHEAD INPUT INTERFACE TIMING



8.2 E1 RECEIVE OVERHEAD INTERFACE

8.2.1 Description of the E1 Receive Overhead Output Interface Block

The E1 Receive Overhead Output Interface Block will allow an external device to be the consumer of the E1 National bit sequence. This interface provides interface signals and required interface timing to shift out proper data link information at proper time.

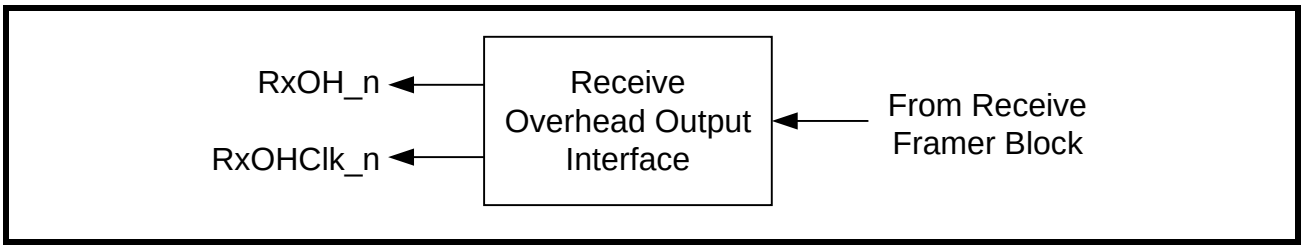
The Receive Overhead Output Interface for a given Framer consists of two signals.

- RxOHClk_n: The Receive Overhead Output Interface Clock Output signal
- RxOH_n: The Receive Overhead Output Interface Output signal.

The Receive Overhead Output Interface Clock Output pin (RxOHCLK_n) generates a rising clock edge for each National bit that is configured to carry Data Link information according to setting of the framer. The data link bits extracted from the incoming E1 frames are outputted from the Receive Overhead Output Interface Output pin (RxOH_n) before the rising edge of RxOHClk_n. The Data Link equipment should sample and latch the data link bits at the rising edge of RxOHClk_n.

The figure below shows block diagram of the Receive Overhead Output Interface of XRT84L38.

FIGURE 109. BLOCK DIAGRAM OF THE E1 RECEIVE OVERHEAD OUTPUT INTERFACE OF XRT84L38



8.2.2 Configure the E1 Receive Overhead Output Interface module as source of the National Bit Sequence in E1 framing format mode

The National Bit Sequence in E1 framing format mode can be extracted and directed to:

- E1 Receive Overhead Output Interface Block
- E1 Receive HDLC Controller
- E1 Receive Serial Output Interface

The purpose of the Receive Overhead Output Interface is to permit Data Link equipment to have direct access to the Sa4 through Sa8 National bits that are extracted from the incoming E1 frames. Independent of the availability of the E1 Receive HDLC Controller module, the XRT84L38 always output the received National bits through the Receive Overhead Output Interface block.

The XRT84L38 allows the user to decide on the following:

- How many of the National Bits is used to carry the Data Link information bits
- Which of these National Bits is used to carry the Data Link information bits.

The Receive Sa Data Link Select bits of the Receive Signaling and Data Link Select Register (TSDLSR) determine which ones of the National bits are configured as Data Link bits in E1 framing format mode. Depending upon the configuration of the Receive Signaling and Data Link Select Register, either of the following cases may exists:

- None of the received National bits are used to transport the Data Link information bits (That is, data link channel of XRT84L38 is inactive).
- Any combination of between 1 and all 5 of the received National bits are used to transport the Data Link information bits.

The table below shows configuration of the Receive Sa Data Link Select bits of the Receive Signaling and Data Link Select Register (RSDLSR).

RECEIVE SIGNALING AND DATA LINK SELECT REGISTER (RSDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0CH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Sa8 Data Link Select	R/W	0 - The received Sa8 Nation bit is not extracted to the data link interface. 1 - The received Sa8 Nation bit is extracted to the data link interface.
6	Receive Sa7 Data Link Select	R/W	0 - The received Sa7 Nation bit is not extracted to the data link interface. 1 - The received Sa7 Nation bit is extracted to the data link interface.
5	Receive Sa6 Data Link Select	R/W	0 - The received Sa6 Nation bit is not extracted to the data link interface. 1 - The received Sa6 Nation bit is extracted to the data link interface.
4	Receive Sa5 Data Link Select	R/W	0 - The received Sa5 Nation bit is not extracted to the data link interface. 1 - The received Sa5 Nation bit is extracted to the data link interface.

RECEIVE SIGNALING AND DATA LINK SELECT REGISTER (RSDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0CH)

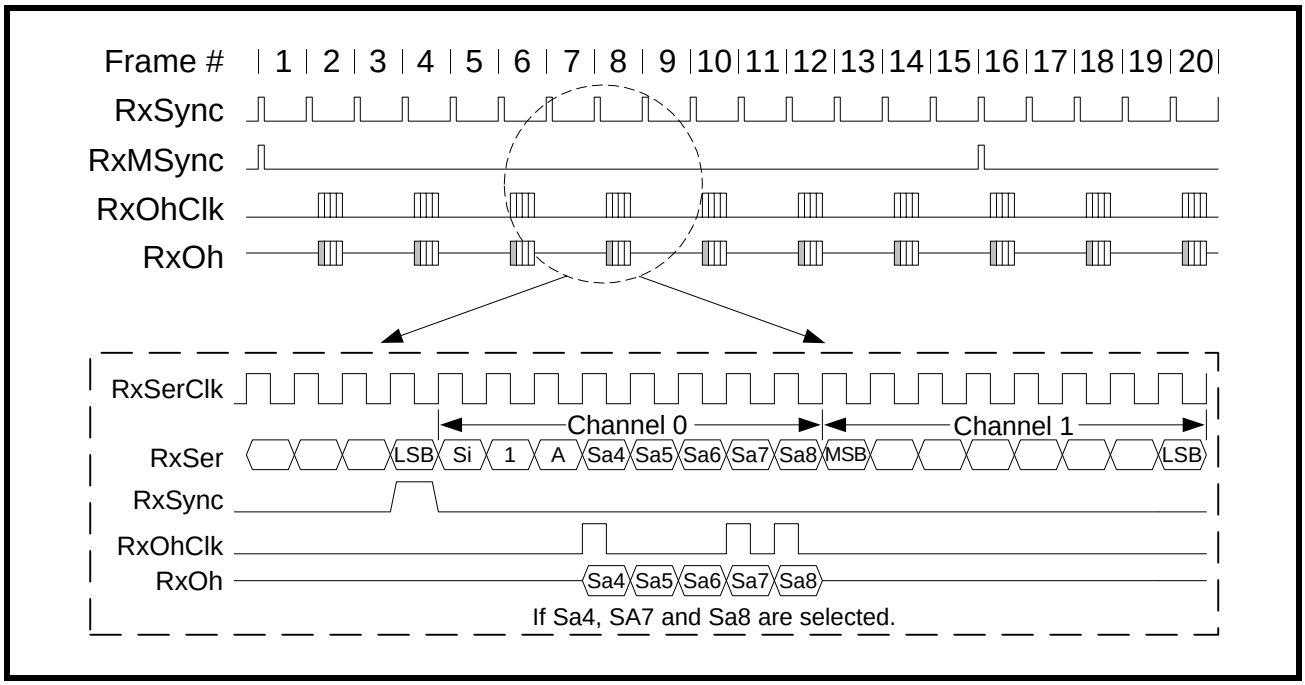
BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Sa4 Data Link Select	R/W	0 - The received Sa4 Nation bit is not extracted to the data link interface. 1 - The received Sa4 Nation bit is extracted to the data link interface.

For every received Sa bit that is determined to carry Data Link information, the Receive Overhead Output Interface will supply a clock pulse, via the RxOHClk_n output pin, such that:

- The Receive Overhead Output interface should update the data on the RxOH_n line before the rising edge of RxOHClk_n.
- The external Data Link equipment interfaced to the Receive Overhead Output Interface will sample and latch the data on the RxOH_n line on the rising edge of RxOHClk_n.

Figure 110 below shows the timing diagram of the output signals associated with the E1 Receive Overhead Output Interface module in E1 framing format mode.

FIGURE 110. E1 RECEIVE OVERHEAD OUTPUT INTERFACE TIMING



9.0 DS1 TRANSMIT FRAMER BLOCK

9.1 HOW TO CONFIGURE XRT84L38 TO OPERATE IN DS1 MODE

The XRT84L38 Octal T1/E1/J1 Framer supports DS1, J1 or E1 framing modes. Since J1 standard is very similar to DS1 standard with a few minor changes, the J1 framing mode is included as a sub-set of the DS1 framing mode. All eight framers within the XRT84L38 silicon can be individually configured to support DS1, J1 or E1 framing modes.

NOTE: *If transmitting section of one framer is configured to support either one of the framing modes, the receiving section is automatically configured to support the same framing modes.*

The T1/E1 Select bit of the Clock Select Register (CSR) controls which framing mode, that is, T1/J1 or E1, supported by the framer. The table below illustrates configurations of the T1/E1 Select bit of the Clock Select Register (CSR).

CLOCK SELECT REGISTER (CSR) (INDIRECT ADDRESS = 0XN0H, 0X00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	T1/E1 Select	R/W	0 - The XRT84L38 framer is running in E1 mode. 1 - The XRT84L38 framer is running in T1 mode.

Since J1 and DS1 are two very similar standards, to configure the framer to run in J1 mode, the user has to select DS1 mode by setting the T1/E1 Select bit of the Clock Select Register to 1 first.

The next step is to set the J1 CRC Calculation bit of the Framing Select Register (FSR). If this bit is set to 1, the XRT84L38 will do CRC-6 calculation in J1 mode. That is, the CRC-6 calculation is based on the actual values of all 4,632 bits in DS1 multi-frame including framing bits. If this bit is set to 0, the XRT84L38 will perform CRC-6 calculation in DS1 mode. That is, the CRC-6 calculation is done based on the actual values of 4,608 payload bits of a DS1 multi-frame and assumes that all the framing bits are one.

The table below shows configurations of the J1 CRC Calculation bit of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (INDIRECT ADDRESS = 0XN0H, 0X07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	J1 CRC Calculation	R/W	In J1 format, CRC-6 calculation is done based on the actual values of all payload bits as well as the framing bits. In DS1 format, CRC-6 calculation is done based on the payload bits only while assuming all the framing bits are one. 0 - The framer performs CRC-6 calculation in DS1 format. 1 - The framer performs CRC-6 calculation in J1 format. This feature permits the driver to comply with J1 standard.

The table below provides summary of how to select different operating modes for the XRT84L38 framer.

	T1/E1 SELECT BIT OF CSR	J1 CRC CALCULATION BIT OF FSR
T1	Set to 1	Set to 0
J1	Set to 1	Set to 1
E1	Set to 0	-

The purpose of the DS1 Transmit Framer block is to embed and encode user payload data into frames and to route this DS1 frame data to the Transmit DS1 LIU Interface block. Please note that the XRT84L38 has eight (8) individual DS1 Transmit Framer blocks. Hence, the following description applies to all eight of these individual Transmit DS1 Framer blocks.

The purpose of the DS1 Transmit Framer block is:

- To encode user data, inputted from the Terminal Equipment into a standard framing format.
- To provide individual data control and signaling conditioning of each DS0 channel.
- To support the transmission of HDLC messages, from the local transmitting terminal, to the remote receiving terminal.
- To transmit indications that the local receive framer has received error frames from the remote terminal.
- To transmit alarm condition indicators to the remote terminal.

The following sections discuss functionalities of the DS1 Transmit Framer block in details. We will also describe how to configure the XRT84L38 to transmit DS1 frames according to system requirement of users.

9.2 How to Configure the Framer to Transmit Data in Various DS1 Framing Formats

The XRT84L38 Octal T1/E1/J1 Framer supports the following DS1 framing formats:

- Super-Frame format (SF), also referred to as D4 framing
- Extended Super-Frame format (ESF)
- Non-signaling format (N)
- T1DM framing format
- SLCâ96 data link framing format, which use the Super-Frame (SF) framing structure

NOTE: *If the framer is configured to transmit DS1 frames according to one particular framing format, the receiving side of the framer is also configured to receive DS1 frames according to the same framing format. The user can set the Framing Format Select [2:0] bits of the Framing Select Register (FSR) to determine which DS1 framing format should XRT84L38 be configured to operate.*

The table below shows configurations of the Framing Format Select [2:0] bits of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (INDIRECT ADDRESS = 0XN0H, 0X07H)

Bit Number	Bit Name	Bit Type	Bit Description
2-0	T1 Framing Select	R/W	**T1 Framing Select:** These READ/WRITE bit-fields allow the user to select one of the five T1 framing formats supported by the framer. These framing formats include ESF, SLCâ96, SF, N and T1DM mode. **NOTE:** *Changing of framing format automatically forces the framer to perform re-synchronization.*

Framing Format	Bit 2	Bit 1	Bit 0
ESF	0	X	X
SLC®96	1	0	0
SF	1	0	1
N	1	1	0
T1DM	1	1	1

9.2.1 How to configure the framer to input framing alignment bits from different sources

In DS1 mode, different framing formats are distinguished by different patterns and functions of the framing alignment bit (first bit of a DS1 frame). The XRT84L38 can generate the framing alignment bits internally according to a particular framing format.

At the same time, the users can generate the framing alignment bits externally and insert them into the framer through the Transmit Serial Data Input Interface block via the TxSer_n pin. It is the user's responsibility to maintain the accuracy and integrity of the framing alignment bits. The user also has to make sure that the framing alignment bits are inserted into the framer at right position and right timing. However, this option is only available when the XRT84L38 is configured to run at a normal back-plane rate of 1.544Mbit/s.

The Framing Bit Source Select bit of the Synchronization MUX Register (SMR) controls source of the framing alignment bit. The table below shows configurations of the Framing Bit Source Select bit of the Synchronization MUX Register (SMR).

SYNCHRONIZATION MUX REGISTER (SMR) (INDIRECT ADDRESS = 0XN0H, 0X09H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	Framing Bit Source	R/W	**Framing Bit Source:** This READ/WRITE bit-field permits the user to determine where the framing alignment bits should be inserted. 0 - The framing alignment bits are generated and inserted by the framer internally. 1 - If the framer is operating in normal 1.544Mbit/s mode, the framing alignment bits are passed through from the Transmit Serial Data Input Interface block via the TxSer_n pin.

9.2.2 How to configure the framer to input CRC-6 bits from different sources

If the framer is configured to operate in Extended Super-frame Format, the framing bits of Frame number 2, 6, 10, 14, 18 and 22 of an ESF multi-frame are used as Cyclic Redundancy Check (CRC-6) code of the last ESF multi-frame. The CRC-6 bits are an indicator of the link quality and could be monitored by the user to establish error performance report.

The XRT84L38 can generate the CRC-6 bits internally by calculating the CRC check-sum of all the 4,632 bits in DS1 multi-frame while assuming the framing bits to be one.

At the same time, the users can generate the CRC-6 bits externally and insert them into the framer through the Transmit Serial Data Input Interface block via the TxSer_n pin. It is the user's responsibility to correctly compute the CRC-6 bits according to DS1 algorithm. Also, the user has to make sure that the CRC-6 bits are inserted into the framer at right position and right timing. However, this option is only available when the XRT84L38 is configured to run at a normal back-plane rate of 1.544Mbit/s.

The CRC-6 Source Select bit of the Synchronization MUX Register (SMR) controls from where to input CRC-6 bits into the framer. The table below shows configurations of the CRC-6 Source Select bit of the Synchronization MUX Register (SMR).

SYNCHRONIZATION MUX REGISTER (SMR) (INDIRECT ADDRESS = 0XN0H, 0X09H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	CRC-6 Source Select	R/W	**CRC-6 Source Select:** This READ/WRITE bit-field permits the user to determine where the CRC-6 bits should be inserted. 0 - The CRC-6 bits are generated and inserted by the framer internally. 1 - If the framer is operating in normal 1.544Mbit/s mode, the CRC-6 bits are generated by external equipment and passed through from the Transmit Serial Data Input Interface block via the TxSer_n pin.

9.3 How to Configure the Framer to Apply Data and Signaling Conditioning to DS1 Payload Data on a Per-Channel Basis

The XRT84L38 T1/J1/E1 Octal Framer provides individual control of each of the twenty-four DS0 channels. The user can apply data and signaling conditioning to raw DS1 payload data coming from the Terminal Equipment on a per-channel basis.

The XRT84L38 framer can apply the following changes to raw DS1 PCM data coming from the Terminal Equipment on a per-channel basis:

- All 8 bits of the input PCM data are inverted
- The even bits of the input PCM data are inverted
- The odd bits of the input PCM data are inverted
- The MSB of the input PCM data is inverted
- All input PCM data except the MSB are inverted

Configuration of the XRT84L38 framer to apply the above-mentioned changes to raw DS1 PCM data are controlled by the Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of each DS0 channel.

The XRT84L38 framer can also replace the incoming raw DS1 PCM data from the Terminal Equipment with pre-defined or user-defined codes. The XRT84L38 supports the following conditioning substitutions:

- BUSY code - an octet with hexadecimal value of 0x7F
- BUSY_TS code - an octet of pattern "111xxxxx" where "xxxxx" represents the timeslot number
- VACANT code - an octet with hexadecimal value of 0xFF
- A-law Digital Milliwatt code
- u-law Digital Milliwatt code
- IDLE code - an octet defined by the value stored in the User IDLE Code Register (UCR)
- MOOF code - MUX-Out-Of-Frame code with hexadecimal value of 0x1A
- PRBS code - an octet generated by the Pseudo-Random Bit Sequence (PRBS) Generator block of the framer

Once again, configuration of the XRT84L38 framer to replace raw DS1 PCM data with the above-mentioned coding schemes are controlled by the Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of each DS0 channel.

Finally, the XRT84L38 framer can configure any one or ones of the twenty-four DS0 channels to be D or E channels. D channel is used primarily for data link applications. E channel is used primarily for signaling for circuit switching with multiple access configurations.

The Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of each channel determine whether that particular channel is configured as D or E channel.

The table below illustrates configurations of the Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR).

TRANSMIT CHANNEL CONTROL REGISTER (TCCR) (INDIRECT ADDRESS = 0XN2H, 0X00H - 0X1FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-0	Transmit Conditioning Select	R/W	0000 - The input DS1 PCM data of this DS0 channel is unchanged. 0001 - All 8 bits of the input DS1 PCM data of this DS0 channel are inverted. 0010 - The even bits of the input DS1 PCM data of this DS0 channel are inverted. 0011 - The odd bits of the input DS1 PCM data of this DS0 channel are inverted. 0100 - The input DS1 PCM data of this DS0 channel are replaced by the octet stored in User IDLE Code Register (UCR). 0101 - The input DS1 PCM data of this DS0 channel are replaced by BUSY code (0x7F). 0110 - The input DS1 PCM data of this DS0 channel are replaced by VACANT code (0xFF). 0111 - The input DS1 PCM data of this DS0 channel are replaced by BUSY_TS code (111xxxxx). 1000 - The input DS1 PCM data of this DS0 channel are replaced by MUX-Out-Of-Frame (MOOF) code with value 0x1A. 1001 - The input DS1 PCM data of this DS0 channel are replaced by the A-law digital milliwatt pattern. 1010 - The input DS1 PCM data of this DS0 channel are replaced by the u-law digital milliwatt pattern. 1011 - The MSB bit of the input DS1 PCM data of this DS0 channel is inverted. 1100 - All bits of the input DS1 PCM data of this DS0 channel except MSB bit are inverted. 1101 - The input DS1 PCM data of this DS0 channel are replaced by PRBS pattern created by the internal PRBS Generator of XRT84L38 framer. 1110 - The input DS1 PCM data of this DS0 channel is unchanged. 1111 - This channel is configured as D or E timeslot.

9.3.1 How to apply User IDLE Code to the DS1 payload data

When the Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of a particular DS0 channel are set to 0100, input DS1 PCM data of this DS0 channel are replaced by the octet stored in User IDLE Code Register (UCR). The table below shows contents of the User IDLE Code Register.

USER IDLE CODE REGISTER (UCR) (INDIRECT ADDRESS = 0XN02H, 0X20H - 0X37H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	User IDLE Code	R/W	These READ/WRITE bit-fields permits the user store any value of IDLE code into the framer. When the Transmit Data Conditioning Select [3:0] bits of TCCR register of a particular DS0 channel are set to 0100, the input DS1 PCM data are replaced by contents of this register and sent to the Transmit LIU Interface.

Let us study the following example of applying the User IDLE Code.

In T1DM mode, the time slot 24 of a DS1 frame is used for synchronization and alarm. To generate the T1DM framing mode externally, the user can do the following:

- Write the T1DM synchronization word (0xBC) to the User IDLE Code Register of the time slot 24.
- Set the Transmit Data Conditioning Select [3:0] bits of the TCCR of channel 24 to "0100".

Upon doing the above, the payload data of channel 24 will be replaced by the T1DM synchronization code 0xBC.

9.4 How to Configure the XRT84L38 Framer to Apply Zero Code Suppression to DS1 Payload Data on a Per-Channel Basis

In order to guarantee adequate clock recovery from the received PCM data, a minimum "ones density" must be maintained. In the case of an all zero channel, that is, if all the incoming PCM data of a particular DS0 channel from the Terminal Equipment is zero, the raw PCM data is replaced by a certain pattern that no more than fifteen consecutive zeros will occur. It is known as zero code suppression.

The XRT84L38 framer supports three types of zero code suppression schemes:

- AT&T Bit 7 Stuffing - an old coding method that forces Bit 7 (the second LSB of a DS0 channel) to a 1 in an all zero channel.
- GTE Zero Code Suppression - Bit 8 (the LSB of a DS0 channel) is stuffed by 1 in non-signaling frame in an all zero channel. Otherwise, Bit 7 is stuffed by 1 in signaling frame if the signaling bit is zero.
- DDS Zero Code Suppression - an octet with hexadecimal value of 0x98 is used to replace the input data if it is all zero.

The Transmit Zero Code Suppression Select [1:0] bits of the Transmit Channel Control Register (TCCR) of a particular DS0 channel is used to select which type of zero code suppression scheme is used by the framer. The table below shows configurations of the Transmit Zero Code Suppression Select [1:0] bits of the Transmit Channel Control Register (TCCR).

TRANSMIT CHANNEL CONTROL REGISTER (TCCR) (INDIRECT ADDRESS = 0XN2H, 0X00H - 0X1FH)

Bit Number	Bit Name	Bit Type	Bit Description
5-4	Transmit Zero Code Suppression Select	R/W	00 - The input DS1 PCM data of this DS0 channel is unchanged. No zero code suppression is used. 01 - AT&T Bit 7 stuffing is used. 10 - GTE zero code suppression is used. 11 - DDS zero code suppression is used.

9.5 How to Configure the XRT84L38 Framer to Transmit Robbed-bit Signaling Information

The XRT84L38 T1/J1/E1 Octal Framer supports insertion of Robbed-bit Signaling information into the outgoing DS1 frame. It also supports extraction and substitution of Robbed-bit Signaling information from the incoming DS1 frame. The following section provides a brief overview of Robbed-bit Signaling in DS1 mode.

9.5.1 Brief Discussion of Robbed-bit Signaling in DS1 Framing Format

Signaling is required when dealing with voice and dial-up data services in DS1 applications. Traditionally, signaling is provided on a dial-up telephone line, across the talk-path. Bit robbing, or stealing the least significant bit (8th bit) in each of the twenty-four voice channels in the signaling frames allows enough bits to signal between the transmitting and receiving end. That is how the name Robbed-bit signaling comes from. These ends can be CPE to central office (CO) for switched services, or CPE to CPE for PBX-to-PBX connections.

Signaling is used to tell the receiver where the call or route is destined. The signal is sent through switches along the route to a distant end. Common types of signals are:

- On hook
- Off hook
- Dial tone

- Dialed digits
- Ringing cycle
- Busy tone

Robbed-bit Signaling is supported in three DS1 framing formats:

- Super-Frame (SF)
- SLC®96
- Extended Super-Frame (ESF)

In Super-Frame or SLC®96 framing mode, frame number 6 and frame number 12 are signaling frames. In channelized DS1 applications, these frames are used to contain the signaling information. In frame number 6 and 12, the least significant bit of all twenty-four timeslots is 'robbed' to carry call state information. The bit in frame 6 is called the A bit and the bit in frame 12 is called the B bit. The combination of A and B defines the state of the call for the particular timeslot that these two bits are located.

FRAME NUMBER	SIGNALING BIT
6	A
12	B

In Extended Super-Frame framing mode, frame number 6, 12, 18 and 24 are signaling frames. In these frames, the least significant bit of all twenty-four timeslots is 'robbed' to carry call state information. The bit in frame 6 is called the A bit, the bit in frame 12 is called the B bit, the bit in frame 18 is called the C bit and the bit in frame 24 is called the D bit. The combination of A, B, C and D defines the state of the call for the particular timeslot that these signaling bits are located.

FRAME NUMBER	SIGNALING BIT
6	A
12	B
18	C
24	D

9.5.2 Configure the framer to transmit Robbed-bit Signaling

The XRT84L38 framer supports transmission of Robbed-bit Signaling in ESF, SF and SLC®96 framing formats. Signaling bits can be inserted into the outgoing DS1 frame through the following:

- Signaling data is inserted from Transmit Signaling Control Registers (TSCR) of each timeslot
- Signaling data is inserted from TxSig_n pin
- Signaling data is embedded into the input PCM data coming from the Terminal Equipment

9.5.2.1 Insert Signaling Bits from TSCR Register

The four most significant bits of the Transmit Signaling Control Register (TSCR) of each timeslot can be used to store outgoing signaling data. The user can program these bits through microprocessor access. If the XRT84L38 framer is configure to insert signaling bits from TSCR registers, the DS1 Transmit Framer block will strip off the least significant bits of signaling frames and replace it with the signaling bit stored inside the TSCR registers. The insertion of signaling bit into PCM data is done on a per-channel basis. The most significant bit (Bit 7) of TSCR register is used to store Signaling bit A. Bit 6 is used to hold Signaling bit B. Bit 5 is used to hold Signaling bit C. Bit 4 is used to hold Signaling bit D.

In SF or SLCâ96 mode, the user can control the XRT84L38 framer to transmit no signaling (transparent), two-code signaling, or four-code signaling. Two-code signaling is done by substituting the least significant bit (LSB) of the specific channel in frame 6 and 12 with the content of the Signaling bit A of the specific TSCR register.

NOTE: *The user should make sure that Signaling bit A and Signaling bit B of the specific TSCR register have the same value.*

Four-code signaling is done by substituting the LSB of channel data in frame 6 with the Signaling bit A and the LSB of channel data in frame 12 with the Signaling bit B of the specific channel's TSCR register. If sixteen-code signaling is selected in SF format, only the Signaling bit A and Signaling bit B information are used.

In ESF mode, the user can control the XRT84L38 framer to transmit no signaling (transparent) by disable signaling insertion, two-code signaling, four-code signaling or sixteen code signaling. Two-code signaling is done by substituting the least significant bit (LSB) of the specific channel in frame 6, 12, 18 and 24 with the content of the Signaling bit A of the specific TSCR register.

NOTE: *The user should duplicate the contents of Signaling bit A of the specific TSCR register to Signaling bit B, C and D.*

Four-code signaling is done by substituting the LSB of channel data in frame 6 and frame 18 with the Signaling bit A and the LSB of channel data in frame 12 and frame 24 with the Signaling bit B of the specific channel's TSCR register.

NOTE: *The user should duplicate the contents of Signaling bit A of the specific TSCR register to Signaling bit C and duplicate the contents of Signaling bit B of the specific TSCR register to Signaling bit D.*

Sixteen-code signaling is implemented by substituting the LSB of channel data in frames 6, 12, 18, and 24 with the content of Signaling bit A, B, C, and D of TSCR register respectively.

In N mode, no robbed-bit signaling is allowed and the transmit data stream remains intact.

The table below shows the four most significant bits of the Transmit Signaling Control Register.

TRANSMIT SIGNALING CONTROL REGISTER (TSCR) (INDIRECT ADDRESS = 0XN2H, 0X40H - 0X57H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Signaling Bit A	R/W	This bit is used to store Signaling Bit A that is sent as the least significant bit of timeslot of frame number 6.
6	Signaling Bit B	R/W	This bit is used to store Signaling Bit B that is sent as the least significant bit of timeslot of frame number 12.
5	Signaling Bit C	R/W	This bit is used to store Signaling Bit C that is sent as the least significant bit of timeslot of frame number 18.
4	Signaling Bit D	R/W	This bit is used to store Signaling Bit D that is sent as the least significant bit of timeslot of frame number 24.

9.5.2.2 Insert Signaling Bits from TxSig_n Pin

The XRT84L38 framer can be configure to insert signaling bits provided by external equipment through the TxSig_n pins. This pin is a multiplexed I/O pin with two functions:

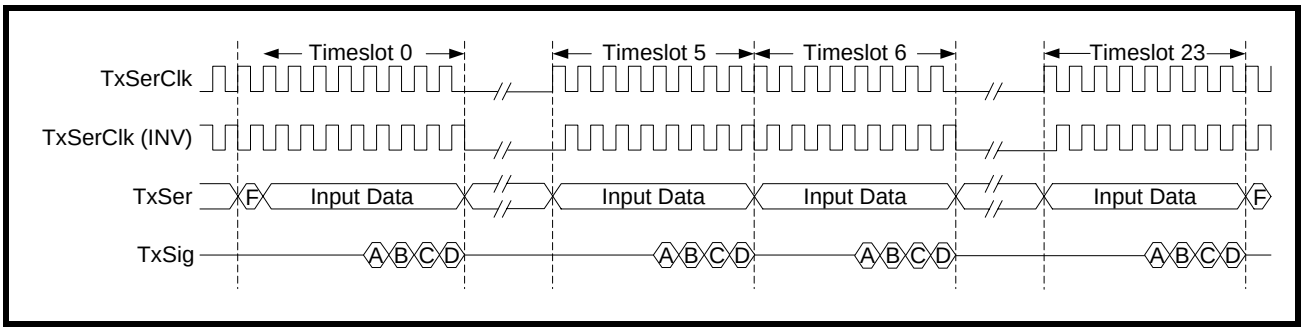
- TxTSb[0]_n - Transmit Timeslot Number Bit [0] Output pin
- TxSig_n - Transmit Signaling Input pin

When the Transmit Fractional DS1 bit of the Transmit Interface Control Register (TICR) is set to 0, this pin is configured as TxTSb[0]_n pin, it outputs bit 0 of the timeslot number of the DS1 PCM data that is transmitting.

When the Transmit Fractional DS1 bit of the Transmit Interface Control Register (TICR) is set to 1, this pin is configured as TxSig_n pin, it acts as an input source for the signaling bits to be transmitted in the outbound DS1 frames.

Figure 111 below is a timing diagram of the TxSig_n input pin. Please note that the Signaling Bit A of a certain timeslot coincides with Bit 5 of the PCM data; Signaling Bit B coincides with Bit 6 of the PCM data; Signaling Bit C coincides with Bit 7 of the PCM data and Signaling Bit D coincides with Bit 8 (LSB) of the PCM data.

FIGURE 111. TIMING DIAGRAM OF THE TXSIG_N INPUT



The table below shows configurations of the Transmit Fractional DS1 bit of the Transmit Interface Control Register (TICR).

TRANSMIT INTERFACE CONTROL REGISTER (TICR)(INDIRECT ADDRESS = 0XN0H, 0X20H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Transmit Fractional DS1	R/W	This READ/WRITE bit-field permits the user to determine which one of the two functions the multiplexed I/O pin of TxTSb[0]_n/TxSig_n is spotting. 0 - This pin is configured as TxTSb[0]_n pin, it outputs bit 0 of the timeslot number of the DS1 PCM data that is transmitting. 1 - This pin is configured as TxSig_n pin, it acts as an input source for the signaling bits to be transmitted in the outbound DS1 frames

9.5.2.3 Insert Signaling Data from TxSer_n Pin

Depends on applications, the Terminal Equipment can embed signaling information into the DS1 PCM data and then send the data to the XRT84L38 framer device. In this case, the user should configure the framer not to insert any signaling data. The input DS1 PCM data will then be directed to the Transmit LIU Interface without any modifications.

9.5.2.4 Enable Robbed-bit Signaling and Signaling Data Source Control

The Transmit Signaling Control Register (TSCR) of each channel selects source of signaling data to be inserted into the outgoing DS1 frame and enables robbed-bit signaling. As we mentioned before, the signaling data can be inserted from Transmit Signaling Control Registers (TSCR) of each timeslot, from the TxSig_n input pin or from the TxSer_n input pin.

The Transmit Signaling Data Source Select [1:0] bits of the Transmit Signaling Control Register (TSCR) determines from which sources the signaling data is inserted from. The table below shows configurations of the Transmit Signaling Data Source Select [1:0] bits of the Transmit Signaling Control Register (TSCR).

TRANSMIT SIGNALING CONTROL REGISTER (TSCR) (INDIRECT ADDRESS = 0XN2H, 0X40H - 0X57H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Signaling Source Select	R/W	00 - No signaling data is inserted into the input DS1 PCM data by the framer. However, the user can embed signaling data into DS1 PCM data before routing the PCM data into the framer. 01 - Signaling data is inserted into the input DS1 PCM data from TSCR register of each timeslot. 10 - Signaling data is inserted into the input DS1 PCM data from the TxSig_n input pin. 11 - No signaling data is inserted into the input DS1 PCM data by the framer. However, the user can embed signaling data into DS1 PCM data before routing the PCM data into the framer.

The Robbed-bit Signaling Enable bit of the Transmit Signaling Control Register (TSCR) determines whether Robbed-bit Signaling is available. The table below shows configurations of the Robbed-bit Signaling Enable bit of the Transmit Signaling Control Register (TSCR).

TRANSMIT SIGNALING CONTROL REGISTER (TSCR) (INDIRECT ADDRESS = 0XN2H, 0X40H - 0X57H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Robbed-bit Signaling Enable	R/W	0 - Robbed-bit Signaling is disabled. No signaling data will be inserted into the input PCM data no matter what the setting of the Transmit Signaling Source Select [1:0] bits is. 1 - Signaling data is enabled and inserted into the input DS1 PCM data according to setting of the Transmit Signaling Source Select [1:0] bits.

9.6 HOW TO CONFIGURE THE XRT84L38 FRAMER TO GENERATE AND TRANSMIT ALARMS AND ERROR INDICATIONS TO REMOTE TERMINAL

The XRT84L38 T1/J1/E1 Octal Framer can be configured to monitor quality of received DS1 frames. It can generate error indications if the local receive framer has received error frames from the remote terminal. If corresponding interrupt is enabled, the local microprocessor operation is interrupted by these error conditions. Upon microprocessor interruption, the user can intervene by looking into the error conditions.

At the same time, the user can configure the XRT84L38 framer to transmit alarms and error indications to remote terminal. Different alarms and error indications will be transmitted depending on the error condition. The section below gives a brief discussion of the error conditions and appropriate alarms that should be generated and transmitted by the XRT84L38 framer.

9.6.1 Brief discussion of alarms and error conditions

As defined in ANSI T1.231 specification, alarm conditions are created from defects. Defects are momentary impairments present on the DS1 trunk. If a defect is present for a sufficient amount of time (called the integration time), then the defect becomes an alarm. Once an alarm is declared, the alarm is present until after the defect clears for a sufficient period of time. The time it takes to clear an alarm is called the de-integration time.

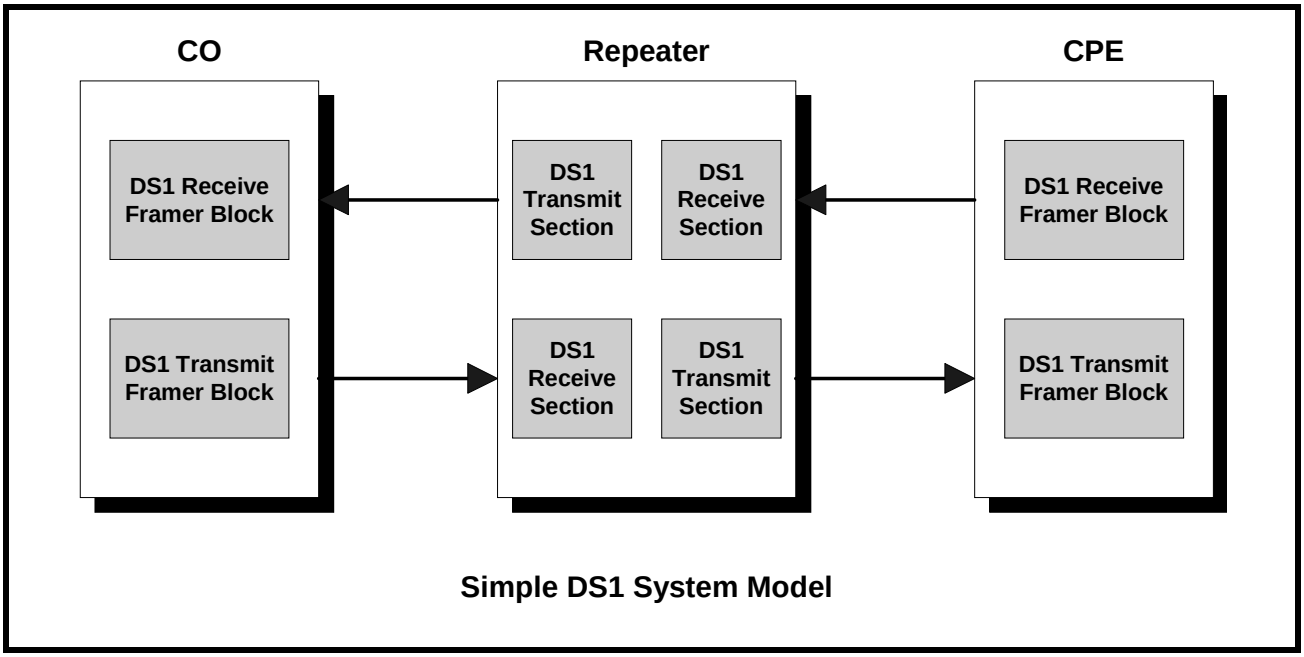
Alarms are used to detect and warn maintenance personnel of problems on the DS1 trunk. There are three types of alarms:

- Red alarm or Service Alarm Indication (SAI) Signal

- Blue alarm or Alarm Indication Signal (AIS)
- Yellow alarm or Remote Alarm Indication (RAI) Signal

To explain the error conditions and generation of different alarms, let us create a simple DS1 system model. In this model, a DS1 signal is sourced from the Central Office (CO) through a Repeater to the Customer Premises Equipment (CPE). At the same time, a DS1 signal is routed from the CPE to the Repeater and back to the Central Office. Figure 112 below shows the simple DS1 system model.

FIGURE 112. SIMPLE DIAGRAM OF DS1 SYSTEM MODEL



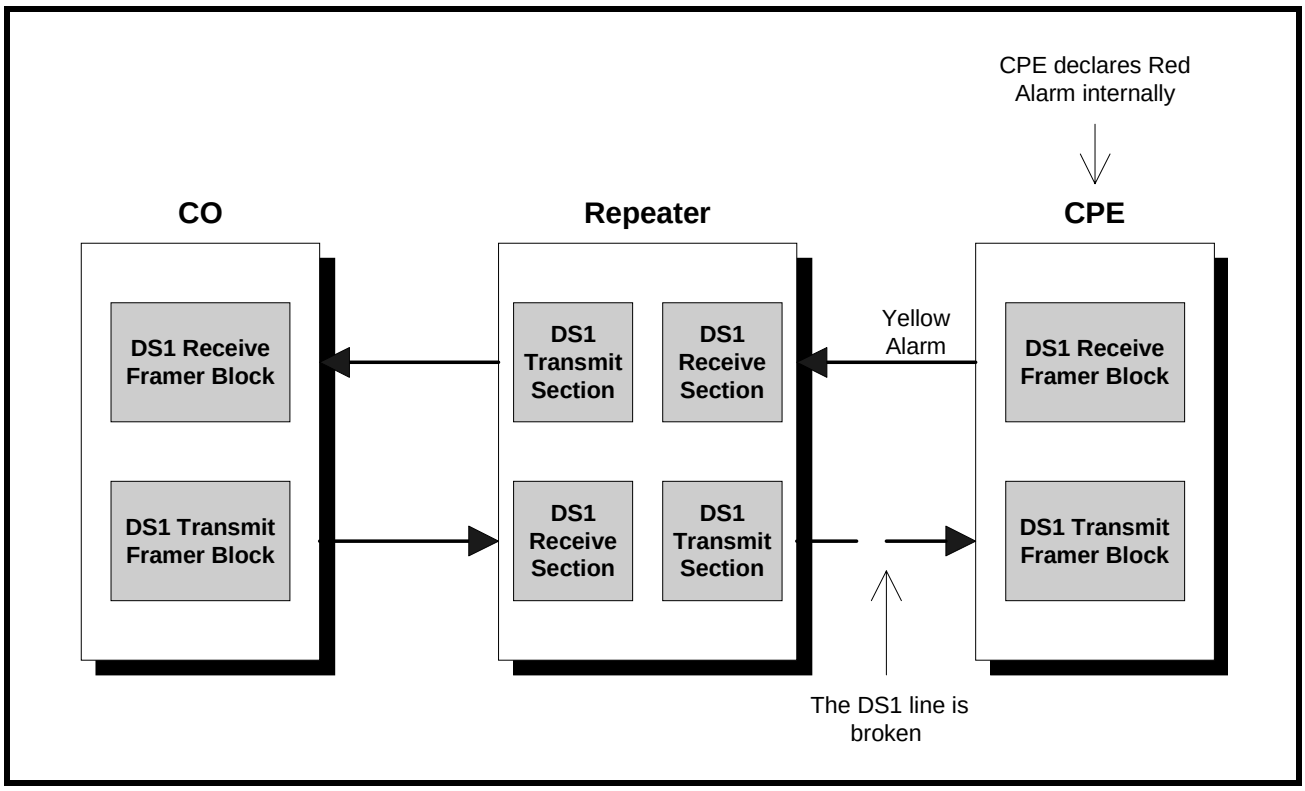
When the E1 system runs normally, that is, when there is no Loss of Signal (LOS) or Loss of Frame (LOF) detected in the line, no alarm will be generated. Sometimes, intermittent outburst of electrical noises on the line might result in Bipolar Violation or bit errors in the incoming signals, but these errors in general will not trigger the equipment to generate alarms. They will at most trigger the framer to generate interrupts which would cause the local microprocessor to create performance reports of the line.

Now, consider a case in which the E1 line from the Repeater to CPE is broken or interrupted, resulting in completely loss of incoming data or severely impaired signal quality. Upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the CPE will generate an internal Red Alarm, also known as the Service Alarm Indication. This alarm will normally trigger a microprocessor interrupt informing the user that an incoming signal failure is happening.

When the CPE is in the Red Alarm state, it will transmit the Yellow Alarm to the Repeater indicating the loss of an incoming signal or loss of frame synchronization. This Yellow Alarm informs the Repeater that there is a

problem further down the line and its transmission is not being received at the CPE. Figure ? below illustrates the scenario in which the E1 connection from the Repeater to CPE is broken.

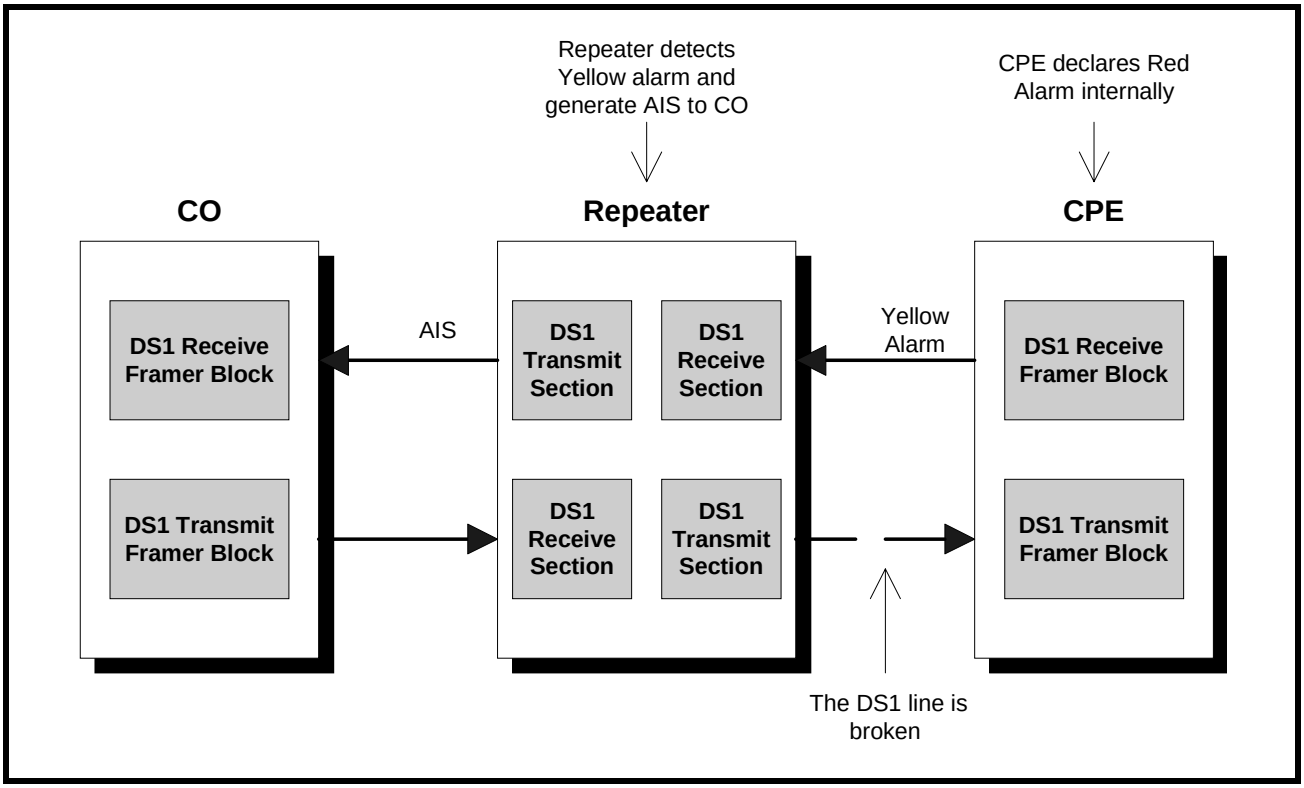
FIGURE 113. GENERATION OF YELLOW ALARM BY THE CPE UPON DETECTION OF LINE FAILURE



The Repeater, upon detection of Yellow Alarm originated from the CPE, will transmit a Blue Alarm, also known as Alarm Indication Signal (AIS) to the CO. Blue alarm is an all ones pattern indicating that the equipment is functioning but unable to offer service due to failures originated from remote side. It is sent such that the equipment downstream will not lose clock synchronization even though no meaningful data is received. Figure ? be-

low illustrates this scenario in which the Repeater is sending an AIS to CO upon detection of Yellow alarm originated from the CPE.

FIGURE 114. GENERATION OF AIS BY THE REPEATER UPON DETECTION OF YELLOW ALARM ORIGINATED BY THE CPE

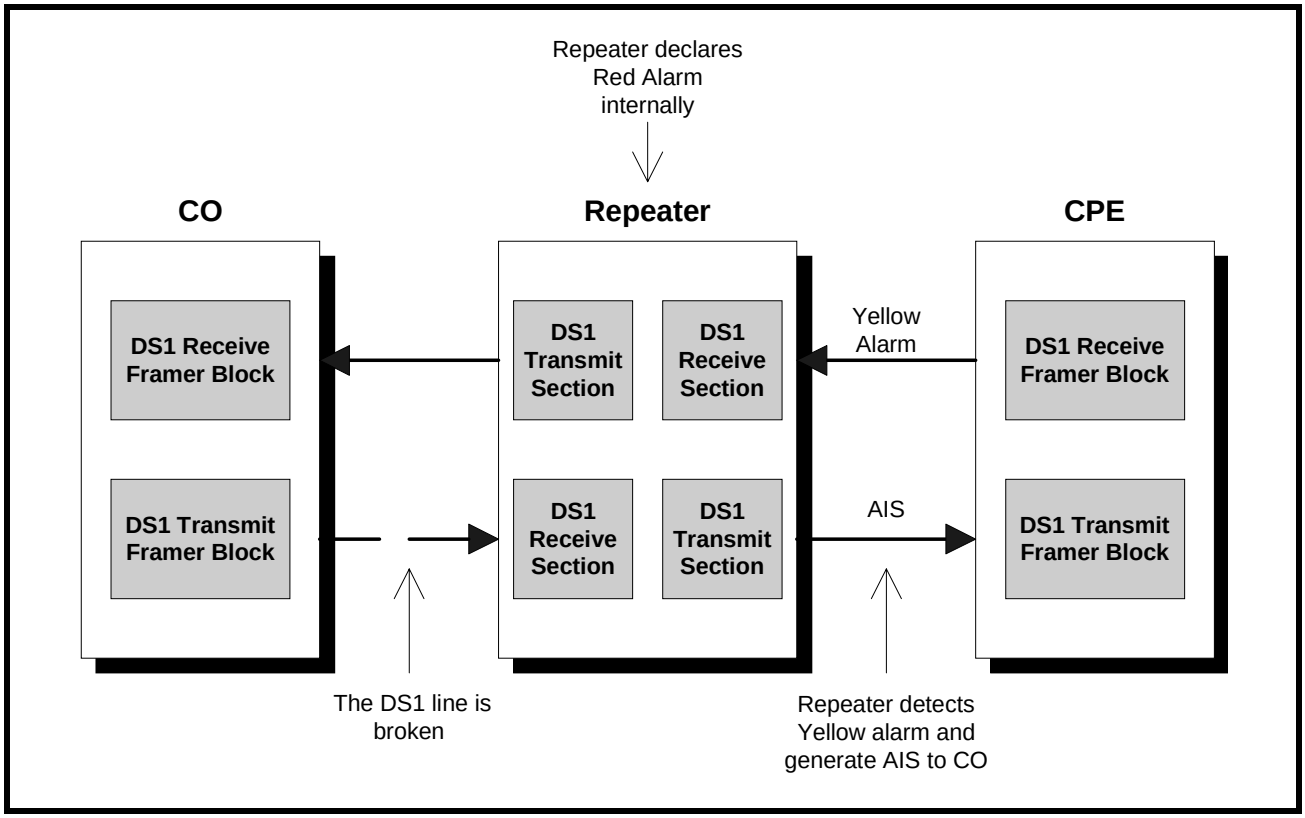


Now let us consider another scenario in which the DS1 line between CO and the Repeater is broken. Again, upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the Repeater will generate an internal Red Alarm. This alarm will normally trigger a microprocessor interrupt informing the user that an incoming signal failure is happening.

The Repeater will also send an all ones AIS pattern downstream to the CPE. The CPE uses the AIS signal to recover received clock and remain in synchronization with the system. Upon detecting the incoming AIS signal, the CPE will generate a Yellow Alarm to the Repeater to indicate the loss of incoming signal. Figure ? below il-

lustrates this scenario in which the Repeater is sending an AIS to the CPE and the CPE is sending a Yellow Alarm back to the Repeater.

FIGURE 115. GENERATION OF YELLOW ALARM BY THE CPE UPON DETECTION OF AIS ORIGINATED BY THE REPEATER



9.6.2 How to configure the framer to transmit AIS

As we discussed in the previous section, Alarm Indication Signal (AIS) or Blue Alarm is transmitted by the intermediate node to indicate that the equipment is still functioning but unable to offer services. It is an all ones (except for framing bits) pattern which can be used by the equipment further down the line to maintain clock recovery and timing synchronization.

The XRT84L38 framer can generate two types of AIS:

- Framed AIS
- Unframed AIS

Unframed AIS is an all ones pattern. If unframed AIS is sent, the equipment further down the line will be able to maintain timing synchronization and be able to recover clock from the received AIS signal. However, due to the lack of framing bits, the equipment farther down the line will not be able to maintain frame synchronization and will declare Loss of Frame (LOF).

On the other hand, the payload portion of a framed AIS pattern is all ones. However, a framed AIS pattern still has correct framing bits. Therefore, the equipment further down the line can still maintain frame synchronization as well as timing synchronization. In this case, no LOF or Red alarm will be declared.

The Transmit Alarm Indication Signal Select [1:0] bits of the Alarm Generation Register (AGR) enable the two types of AIS transmission that are supported by the XRT84L38 framer. The table below shows configurations of the Transmit Alarm Indication Signal Select [1:0] bits of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR)(INDIRECT ADDRESS = 0XN0H, 0X08H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Transmit AIS Select	R/W	These READ/WRITE bit-fields allows the user to choose which one of the two AIS pattern supported by the XRT84L38 framer will be transmitted. 00 - No AIS alarm is generated. 01 - Enable unframed AIS alarm of all ones pattern. 10 - Enable framed AIS alarm of all ones pattern except for framing bits. 11 - No AIS alarm is generated.

9.6.3 How to configure the framer to generate Red Alarm

Upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the Repeater will generate an internal Red Alarm when enabled. This alarm will normally trigger a microprocessor interrupt informing the user that an incoming signal failure is happening.

The Loss of Frame Declaration Enable bit of the Alarm Generation Register (AGR) enable the generation of Red Alarm. The table below shows configurations of the of Frame Declaration Enable bit of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR)(INDIRECT ADDRESS = 0XN0H, 0X08H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Loss of Frame Declaration Enable	R/W	This READ/WRITE bit-field permits the framer to declare Red Alarm in case of Loss of Frame Alignment (LOF). When receiver module of the framer detects Loss of Frame Alignment in the incoming data stream, it will generate a Red Alarm. The framer will also generate an RxLOFs interrupt to notify the microprocessor that an LOF condition is occurred. A Yellow Alarm is then returned to the remote transmitter to report that the local receiver detects LOF. 0 - Red Alarm declaration is disabled. 1 - Red Alarm declaration is enabled.

9.6.4 How to configure the framer to transmit Yellow Alarm

Upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the receiver will transmit the Yellow Alarm back to the source indicating the loss of an incoming signal. This Yellow Alarm informs the source that there is a problem further down the line and its transmission is not being received at the destination.

The XRT84L38 framer supports transmission of Yellow Alarm when running at the following framing formats:

- SF Mode
- ESF Mode
- N Mode
- T1DM Mode

Yellow alarm is transmitted in different forms for various framing formats. The Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register (AGR) enable transmission of different types of Yellow alarm that are supported by the XRT84L38 framer.

9.6.4.1 Transmit Yellow Alarm in SF Mode

In SF mode, the XRT84L38 supports transmission of Yellow Alarm in two ways. When the Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 01 or 11, the second MSB of all DS0 channels is transmitted as zero. This is Yellow Alarm for DS1 standard.

When the Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 10, the Framing bit of Frame 12 is transmitted as one. This is Yellow Alarm for J1 standard.

9.6.4.2 Transmit Yellow Alarm in ESF Mode

In ESF mode, the XRT84L38 transmits Yellow Alarm on the 4Kbit/s data link channel. The Facility Data Link bits are sent in the pattern of eight ones followed by eight zeros. The number of repetitions of this pattern depends on the duration of Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register. When these select bits are set to 01 or 11, the following scenario will happen:

1. If Bit 0 of Yellow Alarm Generation Select forms a pulse width shorter or equal to the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm is transmitted for 255 patterns.
2. If Bit 0 of Yellow Alarm Generation Select forms a pulse width longer than the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm continues until Bit 0 goes LOW.
3. A second pulse on Bit 0 of Yellow Alarm Generation Select during an alarm transmission resets the pattern counter. The framer will send another 255 patterns of the Yellow Alarm.

When these select bits are set to 10, Bit 1 of the Yellow Alarm Generation Select forms a pulse that controls the duration of Yellow Alarm transmission. The alarm continues until Bit 1 goes LOW.

When these select bits are set to 01, the following scenario will happen:

1. If Bit 0 of Yellow Alarm Generation Select forms a pulse width shorter or equal to the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm is transmitted for 255 patterns.
2. If Bit 0 of Yellow Alarm Generation Select forms a pulse width longer than the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm continues until Bit 0 goes LOW.
3. A second pulse on Bit 0 of Yellow Alarm Generation Select during an alarm transmission resets the pattern counter. The framer will send another 255 patterns of the Yellow Alarm.

9.6.4.3 Transmit Yellow Alarm in N Mode

In N mode, when the Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 01, 10 or 11, the second MSB of all DS0 channels is transmitted as zero.

9.6.4.4 Transmit Yellow Alarm in T1DM Mode

In T1DM mode, when the Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 01, 10 or 11, the Yellow Alarm bit (the third LSB of Timeslot 23) is set to zero.The table below shows configurations of the Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register (AGR).

)

ALARM GENERATION REGISTER (AGR)(INDIRECT ADDRESS = 0XN0H, 0X08H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	Yellow Alarm Generation Select	R/W	00 - Transmission of Yellow Alarm is disabled. 01 - The framer transmits Yellow Alarm by converting the second MSB of all outgoing twenty-four DS0 channel into zero. 10 - The framer transmits Yellow Alarm by sending the Super-frame Alignment Bit (Fs) of Frame 12 as one. 11 - The framer transmits Yellow Alarm by converting the second MSB of all outgoing twenty-four DS0 channel into zero. N Mode: 00 - Transmission of Yellow Alarm is disabled. 01, 10 or 11 - The framer transmits Yellow Alarm by converting the second MSB of all outgoing twenty-four DS0 channel into zero. ESF Mode: When the framer is in ESF mode, it transmits Yellow Alarm pattern of eight ones followed by eight zeros (1111_1111_0000_0000) through the 4Kbit/s data link bits. 00 - Transmission of Yellow Alarm is disabled. 01 - The following scenario will happen: **1.** If Bit 0 of Yellow Alarm Generation Select forms a pulse width shorter or equal to the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm is transmitted for 255 patterns. **2.** If Bit 0 of Yellow Alarm Generation Select forms a pulse width longer than the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm continues until Bit 0 goes LOW. **3.** A second pulse on Bit 0 of Yellow Alarm Generation Select during an alarm transmission resets the pattern counter. The framer will send another 255 patterns of the Yellow Alarm. 10 - Bit 1 of the Yellow Alarm Generation Select forms a pulse that controls the duration of Yellow Alarm transmission. The alarm continues until Bit 1 goes LOW. 11 - The following scenario will happen: **1.** If Bit 0 of Yellow Alarm Generation Select forms a pulse width shorter or equal to the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm is transmitted for 255 patterns. **2.** If Bit 0 of Yellow Alarm Generation Select forms a pulse width longer than the time required to transmit 255 patterns on the 4Kbit/s data link, the alarm continues until Bit 0 goes LOW. **3.** A second pulse on Bit 0 of Yellow Alarm Generation Select during an alarm transmission resets the pattern counter. The framer will send another 255 patterns of the Yellow Alarm. T1DM Mode: 00 - Transmission of Yellow Alarm is disabled. 01, 10 or 11 - The framer transmits Yellow Alarm by setting the Yellow Alarm bit (Y-bit) to zero.

10.0 DS1 RECEIVE FRAMER BLOCK

10.1 How to Configure XRT84L38 to Operate in DS1 Mode

The XRT84L38 Octal T1/E1/J1 Framer supports DS1, J1 or E1 framing modes. Since J1 standard is very similar to DS1 standard with a few minor changes, the J1 framing mode is included as a sub-set of the DS1 framing mode. All eight framers within the XRT84L38 silicon can be individually configured to support DS1, J1 or E1 framing modes.

NOTE: *If transmitting section of one framer is configured to support either one of the framing modes, the receiving section is automatically configured to support the same framing modes.*

The T1/E1 Select bit of the Clock Select Register (CSR) controls which framing mode supported by the framer. The table below illustrates configurations of the T1/E1 Select bit of the Clock Select Register (CSR).

CLOCK SELECT REGISTER (CSR) (INDIRECT ADDRESS = 0XN0H, 0X00H)

Bit Number	Bit Name	Bit Type	Bit Description
6	T1/E1 Select	R/W	0 - The XRT84L38 framer is running in E1 mode. 1 - The XRT84L38 framer is running in T1 mode.

Since J1 and DS1 are two very similar standards, to configure the framer to run in J1 mode, the user has to select DS1 mode by setting the T1/E1 Select bit of the Clock Select Register to 1 first.

The next step is to set the J1 CRC Calculation bit of the Framing Select Register (FSR). If this bit is set to 1, the XRT84L38 will do CRC-6 calculation in J1 mode. That is, the CRC-6 calculation is based on the actual values of all 4,632 bits in DS1 multi-frame including framing bits. If this bit is set to 0, the XRT84L38 will perform CRC-6 calculation in DS1 mode. That is, the CRC-6 calculation is done based on the actual values of 4,608 payload bits of a DS1 multi-frame and assumes that all the framing bits are one.

The table below shows configurations of the J1 CRC Calculation bit of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (INDIRECT ADDRESS = 0XN0H, 0X07H)

Bit Number	Bit Name	Bit Type	Bit Description
5	J1 CRC Calculation	R/W	In J1 format, CRC-6 calculation is done based on the actual values of all payload bits as well as the framing bits. In DS1 format, CRC-6 calculation is done based on the payload bits only while assuming all the framing bits are one. 0 - The framer will perform CRC-6 calculation in DS1 format. 1 - The framer will perform CRC-6 calculation in J1 format. This feature permits the driver to comply with J1 standard.

The table below provides summary of how to select different operating modes for the XRT84L38 framer.

	T1/E1 Select bit of CSR	J1 CRC Calculation bit of FSR
T1	Set to 1	Set to 0
J1	Set to 1	Set to 1
E1	Set to 0	-

The purpose of the DS1 Receive Framer block is to accept framed DS1 data from the Receive DS1 LIU Interface block. The Receive Framer block will identify frame boundary and establish framing alignment synchronization of the incoming DS1 frame. The Receive Framer Block will then decode and extract user payload data

from received frames Please note that the XRT84L38 has eight (8) individual DS1 Transmit Framer blocks. Hence, the following description applies to all eight of these individual Transmit DS1 Framer blocks.

The purpose of the DS1 Receive Framer block is:

- To identify frame boundary and establish framing alignment synchronization.
- To decode user data, inputted from the Receive DS1 LIU Interface block to the Terminal Equipment.
- To provide individual data control and signaling conditioning of each DS0 channel.
- To support the receiving and extraction of HDLC messages, from the remote receiving terminal.
- To detect error conditions and generate indications and interrupts to notify the user that the local receive framer has received error frames from the remote terminal.
- To receive and decode alarm condition indicators from the remote terminal.

The following sections discuss functionalities of the DS1 Receive Framer block in details.

10.2 How to Configure the Framer to Receive Data in Various DS1 Framing Formats

The XRT84L38 Octal T1/E1/J1 Framer supports the following DS1 framing formats:

- Super-Frame format (SF), also referred to as D4 framing
- Extended Super-Frame format (ESF)
- Non-signaling format (N)
- T1DM framing format
- SLC®96 data link framing format, which use the Super-Frame (SF) framing structure

Note: *If the framer is configured to receive DS1 frames according to one particular framing format, the transmitting side of the framer is also configured to transmit DS1 frames according to the same framing format.*

The user can set the Framing Format Select [2:0] bits of the Framing Select Register (FSR) to determine which DS1 framing format should XRT84L38 be configured to operate.

The table below shows configurations of the Framing Format Select [2:0] bits of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (INDIRECT ADDRESS = 0XN0H, 0X07H)

<table>
<tr><th>Bit Number</th><th>Bit Name</th><th>Bit Type</th><th>Bit Description</th></tr>
<tr><td>2-0</td><td>T1 Framing Select</td><td>R/W</td><td>These READ/WRITE bit-fields allow the user to select one of the five T1 framing formats supported by the framer. These framing formats include ESF, SLC®96, SF, N and T1DM mode.
<table>
<tr><th>Framing Format</th><th>Bit 2</th><th>Bit 1</th><th>Bit 0</th></tr>
<tr><td>ESF</td><td>0</td><td>X</td><td>X</td></tr>
<tr><td>SLC®96</td><td>1</td><td>0</td><td>0</td></tr>
<tr><td>SF</td><td>1</td><td>0</td><td>1</td></tr>
<tr><td>N</td><td>1</td><td>1</td><td>0</td></tr>
<tr><td>T1DM</td><td>1</td><td>1</td><td>1</td></tr>
</table>
Note: Changing of framing format will automatically force the framer to perform re-synchronization.</td></tr>
</table>

10.3 How to Configure the Framer to Apply Data and Signaling Conditioning to Received DS1 Payload Data on a Per-Channel Basis

The XRT84L38 T1/J1/E1 Octal Framer provides individual control of each of the twenty-four DS0 channels. The user can apply data and signaling conditioning to the received DS1 payload data coming from the DS1 LIU Receive Block on a per-channel basis.

The XRT84L38 framer can apply the following changes to the received DS1 payload data coming from the Terminal Equipment on a per-channel basis:

- All 8 bits of the received payload data are inverted
- The even bits of the received payload data are inverted
- The odd bits of the received payload data are inverted
- The MSB of the received payload data is inverted
- All received payload data except the MSB are inverted

Configurations of the XRT84L38 framer to apply the above-mentioned changes to the received DS1 PAYLOAD data are controlled by the Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of each DS0 channel.

The XRT84L38 framer can also replace the incoming DS1 payload data from the DS1 LIU Receive Block with pre-defined or user-defined codes. The XRT84L38 supports the following conditioning substitutions:

- BUSY code - an octet with hexadecimal value of 0x7F
- BUSY_TS code - an octet of pattern "111xxxxx" where "xxxxx" represents the timeslot number
- VACANT code - an octet with hexadecimal value of 0xFF
- A-law Digital Milliwatt code
- u-law Digital Milliwatt code
- IDLE code - an octet defined by the value stored in the User IDLE Code Register (UCR)
- MOOF code - MUX-Out-Of-Frame code with hexadecimal value of 0x1A
- PRBS code - an octet generated by the Pseudo-Random Bit Sequence (PRBS) Generator block of the framer

Once again, configuration of the XRT84L38 framer to replace the received DS1 payload data with the above-mentioned coding schemes are controlled by the Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of each DS0 channel.

Finally, the XRT84L38 framer can configure any one or ones of the twenty-four DS0 channels to be D or E channels. D channel is used primarily for data link applications. E channel is used primarily for signaling for circuit switching with multiple access configurations.

The Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of each channel determine whether that particular channel is configured as D or E channel.

The table below illustrates configurations of the Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR).

RECEIVE CHANNEL CONTROL REGISTER (RCCR) (INDIRECT ADDRESS = 0XN2H, 0X60H - 0X7FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-0	Receive Conditioning Select	R/W	0000 - The received DS1 payload data of this DS0 channel is unchanged. 0001 - All 8 bits of the input DS1 payload data of this DS0 channel are inverted. 0010 - The even bits of the input DS1 payload data of this DS0 channel are inverted. 0011 - The odd bits of the input DS1 payload data of this DS0 channel are inverted. 0100 - The input DS1 payload data of this DS0 channel are replaced by the octet stored in User IDLE Code Register (UCR). 0101 - The input DS1 payload data of this DS0 channel are replaced by BUSY code (0x7F). 0110 - The input DS1 payload data of this DS0 channel are replaced by VACANT code (0xFF). 0111 - The input DS1 payload data of this DS0 channel are replaced by BUSY_TS code (111xxxxx). 1000 - The input DS1 payload data of this DS0 channel are replaced by MUX-Out-Of-Frame (MOOF) code with value 0x1A. 1001 - The input DS1 payload data of this DS0 channel are replaced by the A-law digital milliwatt pattern. 1010 - The input DS1 payload data of this DS0 channel are replaced by the u-law digital milliwatt pattern. 1011 - The MSB bit of the input DS1 payload data of this DS0 channel is inverted. 1100 - All bits of the input DS1 payload data of this DS0 channel except MSB bit are inverted. 1101 - The input DS1 payload data of this DS0 channel are replaced by PRBS pattern created by the internal PRBS Generator of XRT84L38 framer. 1110 - The input DS1 payload data of this DS0 channel is unchanged. 1111 - This channel is configured as D or E timeslot.

When the Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of a particular DS0 channel are set to 0100, the received DS1 payload data of this DS0 channel are replaced by the octet stored in the Receive User IDLE Code Register (RUCR). The table below shows contents of the Receive User IDLE Code Register.

RECEIVE USER IDLE CODE REGISTER (UCR) (INDIRECT ADDRESS = 0XN02H, 0X80H - 0X97H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	User IDLE Code	R/W	These READ/WRITE bit-fields permits the user store any value of IDLE code into the framer. When the Receive Data Conditioning Select [3:0] bits of RCCR register of a particular DS0 channel are set to 0100, the received DS1 payload data are replaced by contents of this register and sent to the Terminal Equipment.

10.4 How to Configure the XRT84L38 Framer to Apply Zero Code Suppression to Received DS1 Payload Data on a Per-Channel Basis

In order to guarantee adequate clock recovery from the received PCM data, a minimum "ones density" must be maintained. In the case of an all zero channel, that is, if all the incoming PCM data of a particular DS0 channel from the Terminal Equipment is zero, the raw PCM data is replaced by a certain pattern that no more than fifteen consecutive zeros will occur. It is known as zero code suppression.

In the receive end, the user needs to know what type of zero code suppression scheme is applied on the receiving data. In this way, a correct decoding method or the reverse of zero code suppression can be done to extract the payload data from the DS1 LIU Receive Block.

The XRT84L38 framer supports three types of zero code suppression schemes:

- AT&T Bit 7 Stuffing - an old coding method that forces Bit 7 (the second LSB of a DS0 channel) to a 1 in an all zero channel.
- GTE Zero Code Suppression - Bit 8 (the LSB of a DS0 channel) is stuffed by 1 in non-signaling frame in an all zero channel. Otherwise, Bit 7 is stuffed by 1 in signaling frame if the signaling bit is zero.
- DDS Zero Code Suppression - an octet with hexadecimal value of 0x98 is used to replace the input data if it is all zero.

The Receive Zero Code Suppression Select [1:0] bits of the Receive Channel Control Register (RCCR) of a particular DS0 channel is used to select which type of zero code suppression scheme is applied to the received DS1 payload data. The table below shows configurations of the Receive Zero Code Suppression Select [1:0] bits of the Receive Channel Control Register (RCCR).

RECEIVE CHANNEL CONTROL REGISTER (RCCR) (INDIRECT ADDRESS = 0XN2H, 0X60H - 0X7FH)

Bit Number	Bit Name	Bit Type	Bit Description
5-4	Receive Zero Code Suppression Select	R/W	00 - The received DS1 PAYLOAD data of this DS0 channel is unchanged. No zero code suppression is used. 01 - AT&T Bit 7 stuffing is used. 10 - GTE zero code suppression is used. 11 - DDS zero code suppression is used.

10.5 How to Configure the XRT84L38 Framer to Extract Robbed-bit Signaling Information

The XRT84L38 T1/J1/E1 Octal Framer supports insertion of Robbed-bit Signaling information into the outgoing DS1 frame. It also supports extraction and substitution of Robbed-bit Signaling information from the incoming DS1 frame. The following section describes how does the XRT84L38 framer extract and substitute Robbed-bit Signaling in DS1 mode.

10.5.1 Configure the framer to receive and extract Robbed-bit Signaling

The XRT84L38 framer supports receiving and extraction of Robbed-bit Signaling in ESF, SF and SLC®96 framing formats. The Receive Signaling Extraction Control [1:0] bits of the Receive Signaling Control Register (RSCR) of each channel select either:

- No signaling extraction
- Two-code signaling
- Four-code signaling or
- Sixteen-code signaling

In SF or SLCâ96 mode, the Receive Signaling Extraction Control [1:0] bits can select no signaling (transparent), two-code signaling, or four-code signaling. Two-code signaling decoding is done by stripping the least significant bit (LSB) of the specific channel in frame 6 and 12 and stores it into the Signaling Bit A position of RSRA register array. Four-code signaling is done by stripping the LSB of channel data in frame 6 and the LSB of channel data in frame 12, and store them into Signaling Bit A and Signaling Bit B position of RSRA register

array respectively. If 16-code signaling is selected in SF format, only the Signaling bit A and Signaling Bit B positions are filled.

In ESF mode, the Receive Signaling Extraction Control [1:0] bits can select no signaling (transparent), two-code signaling, four-code, or sixteen-code signaling. Two-code signaling decoding is done by stripping the least significant bit (LSB) of the specific channel in frame 6, 12, 18 and 24 and stores it into the Signaling Bit A position of RSRA register array. Four-code signaling is done by stripping the LSB of channel data in frame 6 and frame 18 and the LSB of channel data in frame 12 and 24, and store them into Signaling Bit A and Signaling Bit B position of RSRA register array respectively. Sixteen-code signaling is implemented by stripping the LSB of channel data in frames 6, 12, 18, and 24 and stores them into the Signaling Bit A, Signaling Bit B, Signaling Bit C and Signaling Bit D position of RSRA register array respectively.

The table below shows configurations of the Receive Signaling Extraction Control [1:0] bits of the Receive Signaling Control Register.

RECEIVE SIGNALING CONTROL REGISTER (RSCR) (INDIRECT ADDRESS = 0XN2H, 0XA0H - 0XB7H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Signaling Extraction Control	R/W	00 - The XRT84L38 framer does not extract signaling information from incoming DS1 payload data. 01 - The XRT84L38 framer extracts sixteen-code signaling information from incoming DS1 payload data. 10 - The XRT84L38 framer extracts four-code signaling information from incoming DS1 payload data. 11 - The XRT84L38 framer extracts two-code signaling information from incoming DS1 payload data.

Upon receiving and extraction of signaling bits from the incoming DS1 frames, the XRT84L38 framer compares the signaling bits with the previously received ones. If there is a change of signaling data, a Signaling Update (SIG) interrupt request may be generated at the end of a DS1 multi-frame. The user can thus be notified of a Change of Signaling Data event.

To enable the Signaling Update interrupt, the Signaling Change Interrupt Enable bit of the Framer Interrupt Enable Register (FIER) has to be set. In addition, the T1/E1 Framer Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Signaling Change Interrupt Enable bit of the Framer Interrupt Enable Register.

FRAMER INTERRUPT ENABLE REGISTER (FIER) (INDIRECT ADDRESS = 0XNAH, 0X05H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Signaling Change Interrupt Enable	R/W	0 - The Signaling Update interrupt is disabled. 1 - The Signaling Update interrupt is enabled.

The table below shows configurations of the T1/E1 Framer Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	T1/E1 Framer Interrupt Enable	R/W	0 - Every interrupt generated by the Framer Interrupt Status Register (FISR) is disabled. 1 - Every interrupt generated by the Framer Interrupt Status Register (FISR) is enabled.

When these interrupt enable bits are set and the signaling information received is changed, the DS1 Receive Framer block will set the Signaling Updated status bit of the Framer Interrupt Status Register (FISR) to one. This status indicator is valid until the Framer Interrupt Status Register is read. Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Signaling Update status bits of the Framer Interrupt Status Register.

FRAMER INTERRUPT STATUS REGISTER (FISR) (INDIRECT ADDRESS = 0XNAH, 0X04H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Signaling Updated	RUR / WC	0 - There is no change of signaling information in the incoming DS1 payload data. 1 - There is change of signaling information in the incoming DS1 payload data.

Now, there is only one problem remains. Since there are twenty-four DS0 channels in DS1, how do we know signaling information of which channel is changed?

To solve this problem, the XRT84L38 provides three 8-bit Signaling Change Registers to indicate the channel(s) which signaling data change had occurred over the last DS1 multi-frame period. Each bit of the Signaling Change Registers represents one timeslot of the DS1 frame. If any particular bit is zero, it means there is no change of signaling data occurred in that particular timeslot over the last DS1 multi-frame period. If any particular bit is one, it means there is change of signaling data occurred over the last DS1 multi-frame period.

The table below shows configurations of the Signaling Change Registers.

SIGNALING CHANGE REGISTERS (SCR) (INDIRECT ADDRESS = 0XN0H, 0X0DH - 0X0FH)

LOCATION \ BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0XN0H - 0X0DH	CH 0	CH 1	CH 2	CH 3	CH 4	CH 5	CH 6	CH 7
0xn0H - 0x0EH	Ch 8	Ch 9	Ch 10	Ch 11	Ch 12	Ch 13	Ch 14	Ch 15
0xn0H - 0x0FH	Ch 16	Ch 17	Ch 18	Ch 19	Ch 20	Ch 21	Ch 22	Ch 23

By reading contents of the Signaling Update status bits of the Framer Interrupt Status Register and the Signaling Change Registers, the user can clearly identify which one(s) of the twenty-four DS0 channels has changed signaling information over the last multi-frame period.

Depending on configurations of the XRT84L38 framer, the signaling bits can be extracted from the incoming DS1 frame and direct to all or any one of the following destinations:

- Signaling data is stored to Receive Signaling Register Array (RSRA) of each channel
- Signaling data is sent to the Terminal Equipment through the Receive Signaling Output pin (RxSig_n)

- Signaling data is embedded into the output PCM data sending towards the Terminal Equipment through the Receive Serial Output pin (RxSer_n)

The follow sections discuss how to configure the XRT84L38 framer to extract signaling information bits and send them to different destinations.

10.5.1.1 Store Signaling Bits into RSRA Register Array

The four least significant bits of the Receive Signaling Register Array (RSRA) of each timeslot can be used to store received signaling data. The user can read these bits through microprocessor access. If the XRT84L38 framer is configure to extract signaling bits from incoming DS1 payload data, the DS1 Receive Framer block will strip off the least significant bits of signaling frames and store them into appropriate locations of the RSRA. The extraction of signaling bit from DS1 PCM data is done on a per-channel basis. The Bit 3 of RSRA register is used to hole Signaling bit A. Bit 2 is used to hold Signaling bit B. Bit 1 is used to hold Signaling bit C. Bit 0 is used to hold Signaling bit D.

The table below shows the four least significant bits of the Receive Signaling Register Array.

RECEIVE SIGNALING REGISTER ARRAY (RSRA) (INDIRECT ADDRESS = 0XN4H, 0X00H - 0X17H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Signaling Bit A	R/W	This bit is used to store Signaling Bit A that is received and extracted as the least significant bit of timeslot of frame number 6.
2	Signaling Bit B	R/W	This bit is used to store Signaling Bit B that is received and extracted as the least significant bit of timeslot of frame number 12.
1	Signaling Bit C	R/W	This bit is used to store Signaling Bit C that is received and extracted as the least significant bit of timeslot of frame number 18.
0	Signaling Bit D	R/W	This bit is used to store Signaling Bit D that is received and extracted as the least significant bit of timeslot of frame number 24.

10.5.1.2 Outputting Signaling Bits through RxSig_n Pin

The XRT84L38 framer can be configure to output extracted signaling bits to external equipment through the RxSig_n pins. This pin is a multiplexed I/O pin with two functions:

- RxTSb[0]_n - Receive Timeslot Number Bit [0] Output pin
- RxSig_n - Receive Signaling Output pin

When the Receive Fractional DS1 bit of the Receive Interface Control Register (TICR) is set to 0, this pin is configured as RxTSb[0]_n pin, it outputs bit 0 of the timeslot number of the DS1 PCM data that is receiving.

When the Receive Fractional DS1 bit of the Receive Interface Control Register (TICR) is set to 1, this pin is configured as RxSig_n pin, it acts as an output source for the signaling bits to be received in the inbound DS1 frames.

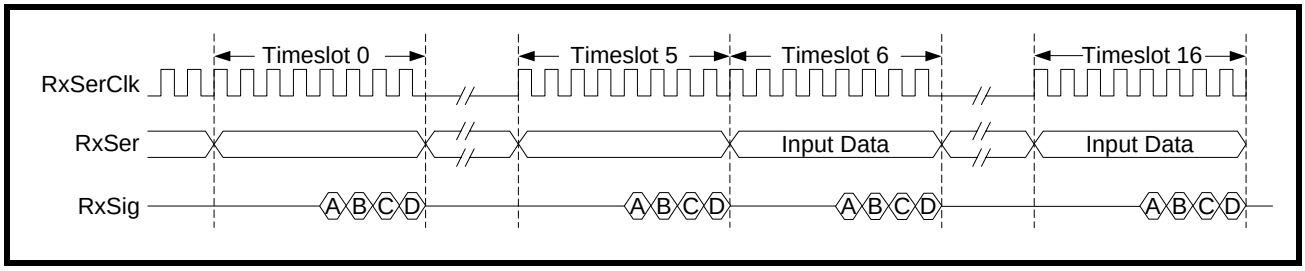
The table below shows configurations of the Receive Fractional DS1 bit of the Receive Interface Control Register (TICR).

RECEIVE INTERFACE CONTROL REGISTER (TICR) (INDIRECT ADDRESS = 0XN0H, 0X20H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Fractional DS1	R/W	This READ/WRITE bit-field permits the user to determine which one of the two functions the multiplexed I/O pin of RxTSb[0]_n/RxSig_n is spotting. 0 - This pin is configured as RxTSb[0]_n pin, it outputs bit 0 of the timeslot number of the DS1 PCM data that is receiving. 1 - This pin is configured as RxSig_n pin, it acts as an output source for the signaling bits to be received in the inbound DS1 frames

Figure 116 below is a timing diagram of the RxSig_n output pin. Please note that the Signaling Bit A of a certain timeslot coincides with Bit 3 of the Received serial output data; Signaling Bit B coincides with Bit 2 of the Received serial output data; Signaling Bit C coincides with Bit 1 of the Received serial output data and Signaling Bit D coincides with Bit 0 of the Received serial output data.

FIGURE 116. TIMING DIAGRAM OF THE RXSIG_N OUTPUT PIN



The Receive Signaling Output Enable bit of the Receive Signaling Control Register (RSCR) determines whether the extracted signaling bits will be sent through the Receive Signaling Output pin (RxSig_n) to external equipments. The table below shows configurations of the Receive Signaling Output Enable bit of the Receive Signaling Control Register.

RECEIVE SIGNALING CONTROL REGISTER (RSCR) (INDIRECT ADDRESS = 0XN2H, 0XA0H - 0XB7H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Signaling Output Enable	R/W	0 - The XRT84L38 framer will not send extracted signaling bits from the incoming DS1 payload data to external equipment through the Receive Signaling Output pin (RxSig_n). 1 - The XRT84L38 framer will send extracted signaling bits from the incoming DS1 payload data to external equipment through the Receive Signaling Output pin (RxSig_n).

10.5.1.3 Send Signaling Data through RxSer_n Pin

As mentioned in the above sections, signaling information embedded in the incoming DS1 PCM data can be sent to either the RSRA register array and/or sent through the Receive Signaling Output pin, at the same time, the signaling data will be directed to the Receive Serial Data Output pin together with other incoming DS1 payload data. The external equipment can thus still extract signaling data from the received DS1 payload data separately.

10.5.1.4 Signaling Data Substitution

After channel conditioning, the signaling conditioning can be optionally enabled by the RSCR registers. The actual signaling bits in each channel can be replaced either with all ones or with signaling bits stored in the Receive Substitution Signaling Register (RSSR). To enable signaling substitution, the Receive Signaling Substitu-

tion Enable bit of the Receive Signaling Control Register (RSCR) has to be set to one. The table below shows configuration of the Receive Signaling Substitution Enable bit of the Receive Signaling Control Register.

RECEIVE SIGNALING CONTROL REGISTER (RSCR) (INDIRECT ADDRESS = 0XN2H, 0XA0H - 0XB7H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Receive Signaling Substitution Enable	R/W	0 - Signaling Substitution is disabled. The XRT84L38 framer will not replace extracted signaling bits from the incoming DS1 payload data with all ones or with signaling bits stored in RSSR registers. 1 - Signaling Substitution is enabled. The XRT84L38 framer will replace extracted signaling bits from the incoming DS1 payload data with all ones or with signaling bits stored in RSSR registers.

As mentioned before, the actual signaling bits in each channel can be replaced either with all ones or with signaling bits stored in the Receive Substitution Signaling Register (RSSR). The table below shows configurations of the Receive Substitution Signaling Register.

RECEIVE SUBSTITUTION SIGNALING REGISTER (RSSR) (INDIRECT ADDRESS = 0XN02H, 0X80H - 0X97H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-4	Reserved	R/W	
3	SIG16-A SIG4-A SIG2-A		Sixteen-Code Signaling bit A Four-Code Signaling bit A Two-Code Signaling bit A
2	SIG16-B SIG4-B SIG2-A		Sixteen-Code Signaling bit B Four-Code Signaling bit B Two-Code Signaling bit A
1	SIG16-C SIG4-A SIG2-A		Sixteen-Code Signaling bit C Four-Code Signaling bit A Two-Code Signaling bit A
0	SIG16-D SIG4-B SIG2-A		Sixteen-Code Signaling bit D Four-Code Signaling bit B Two-Code Signaling bit A

In SF or SLC®96 mode, the Receive Signaling Substitution Control [1:0] bits can select all ones substitution, two-code signaling substitution, or four-code signaling substitution. The XRT84L38 framer can substitute received signaling bits with all ones. Two-code signaling substitution is done by substituting the least significant bit (LSB) of the specific channel in frame 6 and 12 with the content of the SIG2-A bit of the Receive Substitution Signaling Register (RSSR). Four-code signaling substitution is done by substituting the LSB of channel data in frame 6 with the SIG4-A bit and the LSB of channel data in frame 12 with the SIG4-B bit of the RSSR register. If 16-code signaling substitution is selected in SF format, only the SIG16-A bit and SIG16-B bit are used.

In ESF mode, the Receive Signaling Substitution Control [1:0] bits can select all ones substitution, two-code signaling substitution, four-code signaling substitution, or sixteen-code signaling. The XRT84L38 framer can substitute received signaling bits with all ones. Two-code signaling substitution is done by substituting the LSB of the specific channel in frame 6, 12, 18, and 24 with the content of the SIG2-A bit of the register. Four-code signaling substitution is done by substituting the LSB of channel data in frames 6 and 18 with the SIG4-A bit and the LSB of channel data in frames 12 and 24 with the SIG4-B bit of the RSSR register. Sixteen-code sig-

naling substitution is implemented by substituting the LSB of channel data in frames 6, 12, 18, and 24 with the content of SIG16-A, SIG16-B, SIG16-C, and SIG16-D bits of RSSR register respectively.

The table below shows configurations of the Receive Signaling Substitution Control [1:0] bits of the Receive Signaling Control Register.

RECEIVE SIGNALING CONTROL REGISTER (RSCR) (INDIRECT ADDRESS = 0XN2H, 0X40H - 0X57H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Receive Signaling Substitution Control	R/W	00 - The received signaling bits are replaced by all ones and send to the external equipment. 01 - Two-code signaling substitution is applied to the received signaling bits. The replaced signaling information is sent to the external equipment. 10 - Four-code signaling substitution is applied to the received signaling bits. The replaced signaling information is sent to the external equipment. 11 - Sixteen-code signaling substitution is applied to the received signaling bits. The replaced signaling information is sent to the external equipment. ***NOTE:*** *In SF mode, this option is disabled.*

10.6 HOW TO CONFIGURE THE FRAMER TO DETECT ALARMS AND ERROR CONDITIONS

The XRT84L38 T1/J1/E1 Octal Framer can be configured to monitor quality of received DS1 frames. It can generate error indicators if the local receive framer has received error frames from the remote terminal. If corresponding interrupt is enabled, the local microprocessor operation is interrupted by these error conditions. Upon microprocessor interruption, the user can intervene by looking into the error conditions.

At the same time, the user can configure the XRT84L38 framer to transmit alarms and error indications to remote terminal. Different alarms and error indications will be transmitted depending on the error condition.

The section below gives a brief discussion of the error conditions that can be detected by the XRT84L38 framer and error indications that will be generated.

10.6.1 How to configure the framer to detect AIS Alarm

As we discussed before, transmission of Alarm Indication Signal (AIS) or Blue Alarm by the intermediate node indicates that the equipment is still functioning but unable to offer services. It is an all ones (except for framing bits) pattern which can be used by the equipment further down the line to maintain clock recovery and timing synchronization.

The XRT84L38 framer can detect two types of AIS in DS1 mode:

- Framed AIS
- Unframed AIS

Unframed AIS is an all ones pattern. If unframed AIS is sent, the equipment further down the line will be able to maintain timing synchronization and be able to recover clock from the received AIS signal. However, due to the lack of framing bits, the equipment farther down the line will not be able to maintain frame synchronization and will declare Loss of Frame (LOF).

On the other hand, the payload portion of a framed AIS pattern is all ones. However, a framed AIS pattern still has correct framing bits. Therefore, the equipment further down the line can still maintain frame synchronization as well as timing synchronization. In this case, no LOF or Red alarm will be declared.

The Alarm indication logic within the Receive Framer block of the XRT84L38 framer monitors the incoming DS1 frames for AIS. AIS alarm condition are detected and declared according to the following procedure:

1. The incoming DS1 frames are monitored for AIS detection. AIS detection is defined as an unframed or framed pattern with less than three zeros in two consecutive frames.
2. An AIS detection counter within the Receive Framer block of the XRT84L38 counts the occurrences of AIS detection over a 6 ms interval. It will indicate a valid AIS flag when twenty-two or more of a possible twenty-four AIS are detected.

3. Each 6 ms interval with a valid AIS flag increments a flag counter which declares AIS alarm when 255 valid flags have been collected.

Therefore, AIS condition has to be persisted for 1.53 seconds before AIS alarm condition is declared by the XRT84L38 framer.

If there is no valid AIS flag over a 6ms interval, the Alarm indication logic will decrement the flag counter. The AIS alarm is removed when the counter reaches 0. That is, AIS alarm will be removed if over 1.53 seconds, there is no valid AIS flag.

The Alarm Indication Signal Detection Select [1:0] bits of the Alarm Generation Register (AGR) enable the two types of AIS detection that are supported by the XRT84L38 framer. The table below shows configurations of the Alarm Indication Signal Detection Select [1:0] bits of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR) (INDIRECT ADDRESS = 0XN0H, 0X08H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	AIS Detection Select	R/W	00 - AIS alarm detection is disabled.When this bit is set to 01:Detection of unframed AIS alarm of all ones pattern is enabled. 10 - AIS alarm detection is disabled.When this bit is set to 00:Detection of framed AIS alarm of all ones pattern except for framing bits is enabled.

If detection of unframed or framed AIS alarm is enabled by the user and if AIS is present in the incoming DS1 frame, the XRT84L38 framer can generate a Receive AIS State Change interrupt associated with the setting of Receive AIS State Change bit of the Alarm and Error Status Register to one.

To enable the Receive AIS State Change interrupt, the Receive AIS State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) have to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive AIS State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (INDIRECT ADDRESS = 0XNAH, 0X03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive AIS State Change Interrupt Enable	R/W	0 - The Receive AIS State Change interrupt is disabled. 1 - The Receive AIS State Change interrupt is enabled.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and AIS is present in the incoming DS1 frame, the XRT84L38 framer will declare AIS by doing the following:

- Set the read-only Receive AIS State bit of the Alarm and Error Status Register (AESR) to one indicating there is AIS alarm detected in the incoming DS1 frame.
- Set the Receive AIS State Change bit of the Alarm and Error Status Register to one indicating there is a change in state of AIS. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive AIS State Change status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (INDIRECT ADDRESS = 0XNAH, 0X02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive AIS State Change	RUR / WC	0 - There is no change of AIS state in the incoming DS1 payload data. 1 - There is change of AIS state in the incoming DS1 payload data.

The Receive AIS State bit of the Alarm and Error Status Register (AESR), on the other hand, is a read-only bit indicating there is AIS alarm detected in the incoming DS1 frame.

The table below shows the Receive AIS State status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (INDIRECT ADDRESS = 0XNAH, 0X02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Receive AIS State	R	0 - There is no AIS alarm condition detected in the incoming DS1 payload data. 1 - There is AIS alarm condition detected in the incoming DS1 payload data.

10.6.2 How to configure the framer to detect Red Alarm

The Alarm indication logic within the Receive Framer block of the XRT84L38 framer monitors the incoming DS1 frames for red alarm or Loss of Frame (LOF) condition. Red alarm condition are detected and declared according to the following procedure:

1. The red alarm is detected by monitoring the occurrence of Loss of Frame (LOF) over a 6 ms interval.
2. An LOF valid flag will be posted on the interval when one or more LOF occurred during the interval.
3. Each interval with a valid LOF flag increments a flag counter which declares RED alarm when 63 valid intervals have been accumulated.
4. An interval without valid LOF flag decrements the flag counter. The Red alarm is removed when the counter reaches zero.

If LOF condition is present in the incoming DS1 frame, the XRT84L38 framer can generate a Receive Red Alarm State Change interrupt associated with the setting of Receive Red Alarm State Change bit of the Alarm and Error Status Register to one.

To enable the Receive Red Alarm State Change interrupt, the Receive Red Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Red Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (INDIRECT ADDRESS = 0XNAH, 0X03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Red Alarm State Change Interrupt Enable	R/W	0 - The Receive Red Alarm State Change interrupt is disabled. No Receive Loss of Frame (RxLOF) interrupt will be generated upon detection of LOF condition. 1 - The Receive Red Alarm State Change interrupt is enabled. Receive Loss of Frame (RxLOF) interrupt will be generated upon detection of LOF condition.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and Red Alarm is present in the incoming DS1 frame, the XRT84L38 framer will declare Red Alarm by doing the following:

- Set the read-only Receive Red Alarm State bit of the Alarm and Error Status Register (AESR) to one indicating there is Red Alarm detected in the incoming DS1 frame.
- Set the Receive Red Alarm State Change bit of the Alarm and Error Status Register to one indicating there is a change in state of Red Alarm. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Red Alarm State Change status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (INDIRECT ADDRESS = 0XNAH, 0X02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Red Alarm State Change	RUR / WC	0 - There is no change of Red Alarm state in the incoming DS1 payload data. 1 - There is change of Red Alarm state in the incoming DS1 payload data.

The Receive Red Alarm State bit of the Alarm and Error Status Register (AESR), on the other hand, is a read-only bit indicating there is Red Alarm detected in the incoming DS1 frame.

The table below shows the Receive Red Alarm State status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (INDIRECT ADDRESS = 0XNAH, 0X02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Red Alarm State	R	0 - There is no Red Alarm condition detected in the incoming DS1 payload data. 1 - There is Red Alarm condition detected in the incoming DS1 payload data.

10.6.3 How to configure the framer to detect Yellow Alarm

The Alarm indication logic within the Receive Framer block of the XRT84L38 framer monitors the incoming DS1 frames for Yellow Alarm condition. The yellow alarm is detected and declared according to the following procedure:

1. Monitor the occurrence of Yellow Alarm pattern over a 6 ms interval. A YEL valid flag will be posted on the interval when Yellow Alarm pattern occurred during the interval.
2. Each interval with a valid YEL flag increments a flag counter which declares YEL alarm when 80 valid intervals have been accumulated.
3. An interval without valid YEL flag decrements the flag counter. The YEL alarm is removed when the counter reaches zero.

If Yellow Alarm condition is present in the incoming DS1 frame, the XRT84L38 framer can generate a Receive Yellow Alarm State Change interrupt associated with the setting of Receive Yellow Alarm State Change bit of the Alarm and Error Status Register to one.

To enable the Receive Yellow Alarm State Change interrupt, the Receive Yellow Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Yellow Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (INDIRECT ADDRESS = 0XNAH, 0X03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	Receive Yellow Alarm State Change Interrupt Enable	R/W	0 - The Receive Yellow Alarm State Change interrupt is disabled. Any state change of Receive Yellow Alarm will not generate an interrupt. 1 - The Receive Yellow Alarm State Change interrupt is enabled. Any state change of Receive Yellow Alarm will generate an interrupt.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and Yellow Alarm is present in the incoming DS1 frame, the XRT84L38 framer will declare Yellow Alarm by doing the following:

- Set the read-only Receive Yellow Alarm State bit of the Alarm and Error Status Register (AESR) to one indicating there is Yellow Alarm detected in the incoming DS1 frame.
- Set the Receive Yellow Alarm State Change bit of the Alarm and Error Status Register to one indicating there is a change in state of Yellow Alarm. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Yellow Alarm State Change status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR)(INDIRECT ADDRESS = 0XNAH, 0X02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	Receive Yellow Alarm State Change	RUR / WC	0 - There is no change of Yellow Alarm state in the incoming DS1 payload data. 1 - There is change of Yellow Alarm state in the incoming DS1 payload data.

The table below shows the Receive AIS State Change status bits of the Alarm and Error Status Register.

The Receive Yellow Alarm State bit of the Alarm and Error Status Register (AESR), on the other hand, is a read-only bit indicating there is Yellow Alarm detected in the incoming DS1 frame.

The table below shows the Receive Yellow Alarm State status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (INDIRECT ADDRESS = 0XNAH, 0X02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Yellow Alarm State	R	0 - There is no Yellow Alarm condition detected in the incoming DS1 payload data. 1 - There is Yellow Alarm condition detected in the incoming DS1 payload data.

10.6.4 How to configure the framer to detect Bipolar Violation

The line coding for the DS1 signal should be bipolar. That is, a binary "0" is transmitted as zero volts while a binary "1" is transmitted as either a positive or negative pulse, opposite in polarity to the previous pulse. A Bipolar Violation or BPV occurs when the alternate polarity rule is violated. The Alarm indication logic within the Receive Framer block of the XRT84L38 framer monitors the incoming DS1 frames for Bipolar Violations.

If a Bipolar Violation is present in the incoming DS1 frame, the XRT84L38 framer can generate a Receive Bipolar Violation interrupt associated with the setting of Receive Bipolar Violation bit of the Alarm and Error Status Register to one.

To enable the Receive Bipolar Violation interrupt, the Receive Bipolar Violation Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Bipolar Violation Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (INDIRECT ADDRESS = 0XNAH, 0X03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Bipolar Violation Interrupt Enable	R/W	0 - The Receive Bipolar Violation interrupt is disabled. Occurrence of one or more bipolar violations will not generate an interrupt. 1 - The Receive Bipolar Violation interrupt is enabled. Occurrence of one or more bipolar violations will generate an interrupt.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and one or more Bipolar Violations are present in the incoming DS1 frame, the XRT84L38 framer will declare Receive Bipolar Violation by doing the following:

- Set the Receive Bipolar Violation bit of the Alarm and Error Status Register to one indicating there are one or more Bipolar Violations. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Bipolar Violation status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (INDIRECT ADDRESS = 0XNAH, 0X02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Bipolar Violation State Change	RUR / WC	0 - There is no change of Bipolar Violation state in the incoming DS1 payload data. 1 - There is change of Bipolar Violation state in the incoming DS1 payload data.

10.6.5 How to configure the framer to detect Loss of Signal

A Loss of Signal or LOS occurs when neither RPOS nor RNEG inputs of the framer receives a high level input for 32 consecutive bit times. The Alarm indication logic within the Receive Framer block of the XRT84L38 framer monitors the incoming DS1 frames for Loss of Signal conditions. If used in conjunction with EXAR LIUs, for example, the XRT83L3x family, the XRT84L38 framer also declares LOS when the Receive LOS (RxLOS) input pin is pulled HIGH.

The removal of LOS condition is through detection of 12.5% ones over 32 consecutive bits. In the other words, XRT84L38 framer will remove LOS alarm when there is no 4 consecutive zeros received.

NOTE: *The implementation of LOS detection and removal only apply to B8ZS coded bipolar inputs.*

If Loss of Signal condition is present in the incoming DS1 frame, the XRT84L38 framer can generate a Receive Loss of Signal interrupt associated with the setting of Receive Loss of Signal bit of the Alarm and Error Status Register to one.

To enable the Receive Loss of Signal interrupt, the Receive Loss of Signal Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Loss of Signal Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (INDIRECT ADDRESS = 0XNAH, 0X03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Loss of Signal Interrupt Enable	R/W	0 - The Receive Loss of Signal interrupt is disabled. Occurrence of Loss of Signals will not generate an interrupt. 1 - The Receive Loss of Signal interrupt is enabled. Occurrence of Loss of Signals will generate an interrupt.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and one or more Loss of Signals are present in the incoming DS1 frame, the XRT84L38 framer will declare Receive Loss of Signal by doing the following:

- Set the Receive Loss of Signal bit of the Alarm and Error Status Register to one indicating there is one or more Loss of Signals. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Loss of Signal status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (INDIRECT ADDRESS = 0XNAH, 0X02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Loss of Signal State	RUR / WC	0 - There is no change of Loss of Signal state in the incoming DS1 payload data. 1 - There is change of Loss of Signal state in the incoming DS1 payload data.

11.0 E1 TRANSMIT FRAMER BLOCK

11.1 How to Configure XRT84L38 to Operate in E1 Mode

The XRT84L38 Octal T1/E1/J1 Framer supports DS1, J1 or E1 framing modes. Since J1 standard is very similar to DS1 standard with a few minor changes, the J1 framing mode is included as a sub-set of the DS1 framing mode. All eight framers within the XRT84L38 silicon can be individually configured to support DS1, J1 or E1 framing modes.

Note: *If transmitting section of one framer is configured to support either one of the framing modes, the receiving section is automatically configured to support the same framing modes.*

The T1/E1 Select bit of the Clock Select Register (CSR) controls which framing mode, that is, T1/J1 or E1, supported by the framer. The table below illustrates configurations of the T1/E1 Select bit of the Clock Select Register (CSR).

CLOCK SELECT REGISTER (CSR) (INDIRECT ADDRESS = 0XN0H, 0X00H)

Bit Number	Bit Name	Bit Type	Bit Description
6	T1/E1 Select	R/W	0 - The XRT84L38 framer is running in E1 mode. 1 - The XRT84L38 framer is running in T1 mode.

The purpose of the E1 Transmit Framer block is to embed and encode user payload data into frames and to route this E1 frame data to the Transmit E1 LIU Interface block. Please note that the XRT84L38 has eight (8) individual E1 Transmit Framer blocks. Hence, the following description applies to all eight of these individual Transmit E1 Framer blocks.

The purpose of the E1 Transmit Framer block is:

- To encode user data, inputted from the Terminal Equipment into a standard framing format.
- To provide individual data control and signaling conditioning of each DS0 channel.
- To support the transmission of HDLC messages, from the local transmitting terminal, to the remote receiving terminal.
- To transmit indications that the local receive framer has received error frames from the remote terminal.
- To transmit alarm condition indicators to the remote terminal.

The following sections discuss the functionalities of E1 Transmit Framer block in detail. We will also describe how to configure the XRT84L38 to transmit E1 frames according to system requirement of users.

11.2 How to Configure the Framer to Transmit and Receive Data in E1 Framing Format

The XRT84L38 Octal T1/E1/J1 Framer is designed to meet the requirement of ITU-T Recommendation G.704. The E1 framer supports the following:

- Frame Alignment Signal (FAS)
- CRC-4 Multi-frame

The ITU-T Recommendation G.704 also specifies two forms of signaling that can be supported by the E1 Transport medium:

- Channel Associated Signaling (CAS)
- Common Channel Signaling (CCS)

The XRT84L38 framer supports both CAS, CCS signaling format together with Clear Channel without signaling.

11.2.1 How to configure the framer to choose FAS searching algorithm

The XRT84L38 framer can use two algorithms to search for FAS pattern and thus declare FAS alignment synchronization. The FAS Selection bit of the Framing Select Register (FSR) allows the user to choose which one of the two algorithms for searching FAS frame alignment.

The table below shows configurations of the FAS Selection bit of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (INDIRECT ADDRESS = 0XN0H, 0X07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	FAS Selection bit	R/W	This Read/Write bit field allows the user to determine which algorithm is used for searching FAS frame alignment pattern. When an FAS alignment pattern is found and locked, the XRT84L38 will generate Receive Synchronization (RxSync_n) pulse. 0 - Algorithm 1 is selected for searching FAS frame alignment pattern. 1 - Algorithm 2 is selected for searching FAS frame alignment pattern.

11.2.2 How to configure the framer to enable CRC-4 Multi-frame alignment and select the locking criteria

The CRC-4 Selection [1:0] bits of the Framing Select Register (FSR) enable the framer to search for CRC-4 Multi-frame alignment and select the criteria for locking the CRC-4 Multi-frame alignment.

The table below shows configurations of the CRC-4 Selection [1:0] bit of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (INDIRECT ADDRESS = 0XN0H, 0X07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	CRC-4 Selection bit	R/W	Theses Read/Write bit fields allow the user to enable searching of CRC-4 Multi-frame alignment and determine what criteria are used for locking the CRC-4 Multi-frame alignment pattern. 00 - Searching of CRC-4 Multi-frame alignment is disabled. The XRT84L38 framer will not search for CRC-4 Multi-frame alignment and thus will not declare CRC-4 Multi-frame synchronization. No Receive CRC-4 Multi-frame Synchronization (RxCRCMsync_n) pulse will be generated by the framer. 01 - Searching of CRC-4 Multi-frame alignment is enabled. The XRT84L38 will search for and declare CRC-4 Multi-frame synchronization if:At least one valid CRC-4 Multi-frame alignment signal is observed within 8 ms. 10 - Searching of CRC-4 Multi-frame alignment is enabled. The XRT84L38 will search for and declare CRC-4 Multi-frame synchronization if:At least two valid CRC-4 Multi-frame alignment signals are observed within 8 ms. The time separating two CRC-4 Multi-frame alignment signals is multiple of 2 ms. 11 - Searching of CRC-4 Multi-frame alignment is enabled. The XRT84L38 will search for and declare CRC-4 Multi-frame synchronization if:At least three valid CRC-4 Multi-frame alignment signals are observed within 8 ms. The time separating two CRC-4 Multi-frame alignment signals is multiple of 2 ms.

11.2.3 How to configure the framer to enable CAS Multi-frame alignment

The XRT84L38 framer can use two algorithms to search for CAS Multi-frame alignment pattern. Upon detecting of CAS Multi-frame alignment pattern, the framer will declare CAS Multi-frame alignment synchronization and generate the Receive CAS Multi-frame synchronization pulse (RxCASMsync_n). The CAS Selection [1:0] bits of the Framing Select Register (FSR) enable the framer to search for CAS Multi-frame alignment.

The table below shows configurations of the CAS Selection [1:0] bit of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (INDIRECT ADDRESS = 0XN0H, 0X07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	CAS Selection bit	R/W	These Read/Write bit fields allow the user to enable searching of CAS Multi-frame alignment and determine which algorithm of the two are used for locking the CAS Multi-frame alignment pattern. 00 - Searching of CAS Multi-frame alignment is disabled. The XRT84L38 framer will not search for CAS Multi-frame alignment and thus will not declare CAS Multi-frame synchronization. No Receive CAS Multi-frame Synchronization (RxCRCMsync_n) pulse will be generated by the framer. 01 - Searching of CAS Multi-frame alignment is enabled. The XRT84L38 will search for and declare CAS Multi-frame synchronization using Algorithm 1. 10 - Searching of CAS Multi-frame alignment is enabled. The XRT84L38 will search for and declare CAS Multi-frame synchronization using Algorithm 2 (G.732). 11 - Searching of CAS Multi-frame alignment is disabled. The XRT84L38 framer will not search for CAS Multi-frame alignment and thus will not declare CAS Multi-frame synchronization. No Receive CAS Multi-frame Synchronization (RxCRCMsync_n) pulse will be generated by the framer.

11.2.4 How to configure the framer to input the framing alignment bits from different sources

In E1 mode, the Frame Alignment Signal (FAS) pattern of "0011011" contained in bit 2 to 8 of every other frame (called FAS frame) are used to identify the frame boundaries. In addition, bit 2 of the non-FAS frames is fixed to "1" to prevent simulation of the FAS frames.

In the non-FAS frames, bit 1 is used to transmit the 6-bit CRC-4 multi-frame alignment signal of "001011" and two E bits. The 6-bit CRC-4 multi-frame alignment signal is used to identify the CRC-4 multi-frame boundaries.

The A bit at bit 3 of non-FAS frame is used as remote yellow alarm indication. When the A bit is "0", it denotes undistributed operation of the framer. When the A bit is "1", it denotes yellow alarm condition.

The framing alignment bits include the FAS pattern, the CRC-4 multi-frame alignment bits and the A bit. Under default condition, the XRT84L38 can generate these framing alignment bits internally.

At the same time, the users can generate the framing alignment bits externally and insert them into the framer through the Transmit Serial Data Input Interface block via the TxSer_n pin. It is the user's responsibility to maintain the accuracy and integrity of the framing alignment bits. The user also has to make sure that the framing alignment bits are inserted into the framer at right position and right timing. However, this option is only available when the XRT84L38 is configured to run at a normal back-plane rate of 2.048Mbit/s in E1 mode.

The Framing Bit Source Select bit of the Synchronization MUX Register (SMR) controls source of the framing alignment bit. The table below shows configurations of the Framing Bit Source Select bit of the Synchronization MUX Register (SMR).

SYNCHRONIZATION MUX REGISTER (SMR) (INDIRECT ADDRESS = 0XN0H, 0X09H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	Framing Bit Source	R/W	This READ/WRITE bit-field permits the user to determine where the framing alignment bits should be inserted. 0 - The framing alignment bits are generated and inserted by the framer internally. 1 - If the framer is operating in normal 2.048Mbit/s mode, the framing alignment bits are passed through from the Transmit Serial Data Input Interface block via the TxSer_n pin.

11.2.5 How to configure the framer to input CRC-4 bits from different sources

Each E1 CRC-4 multi-frame is divided into two sub-multi-frames. Each sub-multi-frame consists of 8 E1 frames. If the framer is configured to operate in CRC-4 multi-frame format, bit 1 of the FAS frames are used as Cyclic Redundancy Check (CRC-4) code of the last CRC-4 sub- multi-frame. The CRC-4 bits are an indicator of the link quality and could be monitored by the user to establish error performance report.

The XRT84L38 can generate the CRC-4 bits internally by calculating the CRC check-sum of all the payload bits in each E1 sub-multi-frame.

At the same time, the users can generate the CRC-4 bits externally and insert them into the framer through the Transmit Serial Data Input Interface block via the TxSer_n pin. It is the user's responsibility to correctly compute the CRC-4 bits according to E1 algorithm. Also, the user has to make sure that the CRC-4 bits are inserted into the framer at right position and right timing. However, this option is only available when the XRT84L38 is configured to run at a normal back-plane rate of 2.048Mbit/s.

The CRC-4 Source Select bit of the Synchronization MUX Register (SMR) controls from where to input CRC-4 bits into the framer. The table below shows configurations of the CRC-4 Source Select bit of the Synchronization MUX Register (SMR).

SYNCHRONIZATION MUX REGISTER (SMR) (INDIRECT ADDRESS = 0XN0H, 0X09H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	CRC-4 Source Select	R/W	This READ/WRITE bit-field permits the user to determine where the CRC-4 bits should be inserted. 0 - The CRC-4 bits are generated and inserted by the framer internally. 1 - If the framer is operating in normal 2.048Mbit/s mode, the CRC-4 bits are generated by external equipment and passed through from the Transmit Serial Data Input Interface block via the TxSer_n pin.

11.2.6 How to configure the framer to input E bits from different sources

Each E1 CRC-4 multi-frame is divided into two sub-multi-frames. Each sub-multi-frame consists of 8 E1 frames, 4 of them are FAS frames and the other 4 are non-FAS frames. Of the second CRC-4 sub-multi-frame, bit 1 of the last 2 non-FAS frames is called E bit.

The E bits are used to indicate that the previous received sub-multi-frame is error-ed. When a sub-multi-frame is received, the framer calculated the CRC-4 bits of the received sub-multi-frame. The frame then compares the calculated CRC-4 bits with the received CRC-4 bits. If they are the same, the framer will set E bit to "1" and transmit it to the remote terminal. If the calculated CRC-4 bits and the receive CRC-4 bits are different, the

framer will set E bit to "0" and transmit it out. The first E bit indicates error of the first CRC-4 sub-multi-frame while the second E bit indicates error of the second CRC-4 sub-multi-frame.

The delay between the detection of an error-ed CRC-4 sub-multi-frame and the setting of the corresponding E bit that represents the error state should not be more than one second. If the E bits are not used, they should be set to "1".

NOTE: *The E bits will always be taken into account even if the sub-multi-frame which contains them is error-ed.*

Under default condition, the XRT84L38 generate the E bits internally by calculating the CRC check-sum of all the payload bits in each received E1 sub-multi-frame and compare them against the received CRC-4 bits.

At the same time, the users can force the E bits to either "0" or "1". Source of the E bits can also be the internal HDLC controller such that the E bits can be used to transmit data link message.

The E bit Source Select bit of the Synchronization MUX Register (SMR) controls from where to input E bits into the framer. The table below shows configurations of the E bit Source Select bit of the Synchronization MUX Register (SMR).

SYNCHRONIZATION MUX REGISTER (SMR) (INDIRECT ADDRESS = 0XN0H, 0X09H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-6	E bit Source Select	R/W	These READ/WRITE bit-fields permits the user to determine where the E bits should be inserted and what the E bits should be. 00 - The E bits are generated and inserted by the framer internally. 01 - The E bits are forced to be "0" and are inserted by the framer internally. 10 - The E bits are forced to be "1" and are inserted by the framer internally. 11 - Source of the E bits is HDLC controller of the framer. The E bits are used to carry data link messages.

11.3 HOW TO CONFIGURE THE FRAMER TO APPLY DATA AND SIGNALING CONDITIONING TO E1 PAYLOAD DATA ON A PER-CHANNEL BASIS

The XRT84L38 T1/J1/E1 Octal Framer provides individual control of each of the thirty two DS0 channels. The user can apply data and signaling conditioning to raw E1 payload data coming from the Terminal Equipment on a per-channel basis.

The XRT84L38 framer can apply the following changes to raw E1 PCM data coming from the Terminal Equipment on a per-channel basis:

- All 8 bits of the input PCM data are inverted
- The even bits of the input PCM data are inverted
- The odd bits of the input PCM data are inverted
- The MSB of the input PCM data is inverted
- All input PCM data except the MSB are inverted

Configuration of the XRT84L38 framer to apply the above-mentioned changes to raw E1 PCM data are controlled by the Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of each DS0 channel.

The XRT84L38 framer can also replace the incoming raw E1 PCM data from the Terminal Equipment with predefined or user-defined codes. The XRT84L38 supports the following conditioning substitutions:

- BUSY code - an octet with hexadecimal value of 0x7F
- BUSY_TS code - an octet of pattern "111xxxxx" where "xxxxx" represents the timeslot number
- VACANT code - an octet with hexadecimal value of 0xFF
- A-law Digital Milliwatt code

- u-law Digital Milliwatt code
- IDLE code - an octet defined by the value stored in the User IDLE Code Register (UCR)
- MOOF code - MUX-Out-Of-Frame code with hexadecimal value of 0x1A
- PRBS code - an octet generated by the Pseudo-Random Bit Sequence (PRBS) Generator block of the framer

Once again, configuration of the XRT84L38 framer to replace raw E1 PCM data with the above-mentioned coding schemes are controlled by the Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of each DS0 channel.

Finally, the XRT84L38 framer can configure any one or ones of the thirty two DS0 channels to be D or E channels. D channel is used primarily for data link applications. E channel is used primarily for signaling for circuit switching with multiple access configurations.

The Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of each channel determine whether that particular channel is configured as D or E channel.

The table below illustrates configurations of the Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR).

TRANSMIT CHANNEL CONTROL REGISTER (TCCR) (INDIRECT ADDRESS = 0XN2H, 0X00H - 0X1FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-0	Transmit Conditioning Select	R/W	0000 - The input E1 PCM data of this DS0 channel is unchanged. 0001 - All 8 bits of the input E1 PCM data of this DS0 channel are inverted. 0010 - The even bits of the input E1 PCM data of this DS0 channel are inverted. 0011 - The odd bits of the input E1 PCM data of this DS0 channel are inverted. 0100 - The input E1 PCM data of this DS0 channel are replaced by the octet stored in User IDLE Code Register (UCR). 0101 - The input E1 PCM data of this DS0 channel are replaced by BUSY code (0x7F). 0110 - The input E1 PCM data of this DS0 channel are replaced by VACANT code (0xFF). 0111 - The input E1 PCM data of this DS0 channel are replaced by BUSY_TS code (111xxxxx). 1000 - The input E1 PCM data of this DS0 channel are replaced by MUX-Out-Of-Frame (MOOF) code with value 0x1A. 1001 - The input E1 PCM data of this DS0 channel are replaced by the A-law digital milliwatt pattern. 1010 - The input E1 PCM data of this DS0 channel are replaced by the u-law digital milliwatt pattern. 1011 - The MSB bit of the input E1 PCM data of this DS0 channel is inverted. 1100 - All bits of the input E1 PCM data of this DS0 channel except MSB bit are inverted. 1101 - The input E1 PCM data of this DS0 channel are replaced by PRBS pattern created by the internal PRBS Generator of XRT84L38 framer. 1110 - The input E1 PCM data of this DS0 channel is unchanged. 1111 - This channel is configured as D or E timeslot.

When the Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of a particular DS0 channel are set to 0100, input E1 PCM data of this DS0 channel are replaced by the octet stored in User IDLE Code Register (UCR). The table below shows contents of the User IDLE Code Register.

USER IDLE CODE REGISTER (UCR) (INDIRECT ADDRESS = 0XN02H, 0X20H - 0X3FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	User IDLE Code	R/W	These READ/WRITE bit-fields permits the user store any value of IDLE code into the framer. When the Transmit Data Conditioning Select [3:0] bits of TCCR register of a particular DS0 channel are set to 0100, the input E1 PCM data are replaced by contents of this register and sent to the Transmit LIU Interface.

11.4 HOW TO CONFIGURE THE XRT84L38 FRAMER TO TRANSMIT SIGNALING INFORMATION

Each 256-bit E1 frame is divided into 32 octets or time slots numbered 0 to 31. Each time slot is a 64kbits/s channel carrying voice or data information. The time slot 0 is used for frame and multi-frame synchronization, CRC-4 error detection, yellow alarm transmission and data link transmission. The time slot 1 to time slot 15 and time slot 17 to time slot 31 are used to carry a PCM encoded voice band signal or data. The remaining 64kbits/s channel time slot 16 may be used for signaling. The XRT84L38 T1/J1/E1 Octal Framer supports the following signaling formats to interconnect to CEPT channelized service functions:

- Common Channel Signaling (CCS)
- Channel Associated Signaling (CAS)
- Primary Rate ISDN Message Oriented Signaling (ISDN-PRI)

The XRT84L38 T1/J1/E1 Octal Framer supports insertion of various types of signaling information into the timeslot 16 of an outgoing E1 frame. It also supports extraction and substitution of signaling information from the incoming E1 frame. The following section provides a brief overview of Common Channel Signaling, Channel Associated Signaling in E1 mode.

NOTE: *The time slot 16 can also be configured to carry PCM encoded voice or data if neither CCS nor CAS signaling is used. The XRT84L38 framer allows the user to choose which one of the CCS, CAS, ISDN-PRI message or PCM data to be carries on the time slot 16.*

11.4.1 Brief Discussion of Common Channel Signaling in E1 Framing Format

As the name referred, Common Channel Signaling is signaling information common to all thirty voice or data channels of an E1 trunk. The time slot 16 may be used to carry Common Channel Signaling data of up to a rate of 64kbits/s. The national bits of time slot 0 may also be used for Common Channel Signaling. Since there are five national bits of time slot 0 per every two E1 frames, the total bandwidth of the national bits is 20kbits/s. The Common Channel Signaling is essentially data link information that provides performance monitoring and transmission quality report.

11.4.2 Brief Discussion of Channel Associated Signaling in E1 Framing Format

Signaling is required when dealing with voice and dial-up data services in E1 applications. Traditionally, signaling is provided on a dial-up telephone line, across the talk-path. Signaling is used to tell the receiver where the call or route is destined. The signal is sent through switches along the route to a distant end. Common types of signals are:

- On hook
- Off hook
- Dial tone
- Dialed digits
- Ringing cycle
- Busy tone

A signal is consists of four bits namely A, B, C and D. These bits define the state of the call for a particular time slot. The time slot 16 octet of each E1 frame can carry CAS signals for two E1 voice or data channels. Therefore, sixteen E1 frames are needed to carry CAS signals for all 32 E1 channels. The sixteen E1 frames then forms a CAS Multi-frame.

The time slot 16 of Frame number 0 of an E1 CAS Multi-frame carries the pattern of "0000 XYXX". The time slot 16 of Frame number 1 carries signals of Channel 1 and Channel 17. The time slot 16 of Frame number 2 carries signals of Channel 2 and Channel 18, and so on. The following table shows the bit allocations of Channel Associated Signaling in E1 framing format.

TIME SLOT 16 OF FRAME 0		TIME SLOT 16 OF FRAME 1		TIME SLOT 16 OF FRAME 2		TIME SLOT 16 OF FRAME 3	
0000	XYXX	ABCD of Ch. 1	ABCD of Ch. 17	ABCD of Ch. 2	ABCD of Ch. 18	ABCD of Ch. 3	ABCD of Ch. 19

TIME SLOT 16 OF FRAME 4		TIME SLOT 16 OF FRAME 5		TIME SLOT 16 OF FRAME 6		TIME SLOT 16 OF FRAME 7	
ABCD of Ch. 4	ABCD of Ch. 20	ABCD of Ch. 5	ABCD of Ch. 21	ABCD of Ch. 6	ABCD of Ch. 22	ABCD of Ch. 7	ABCD of Ch. 23

TIME SLOT 16 OF FRAME 8		TIME SLOT 16 OF FRAME 9		TIME SLOT 16 OF FRAME 10		TIME SLOT 16 OF FRAME 11	
ABCD of Ch. 8	ABCD of Ch. 24	ABCD of Ch. 9	ABCD of Ch. 25	ABCD of Ch. 10	ABCD of Ch. 26	ABCD of Ch. 11	ABCD of Ch. 27

TIME SLOT 16 OF FRAME 12		TIME SLOT 16 OF FRAME 13		TIME SLOT 16 OF FRAME 14		TIME SLOT 16 OF FRAME 15	
ABCD of Ch. 12	ABCD of Ch. 28	ABCD of Ch. 13	ABCD of Ch. 29	ABCD of Ch. 14	ABCD of Ch. 30	ABCD of Ch. 15	ABCD of Ch. 31

The four zeros pattern is the multi-frame alignment signal that indicates the beginning of an E1 CAS Multi-frame. The XRT84L38 framer, upon detection of the four zeros pattern in the time slot 16, declares CAS multi-frame synchronization and would pulse the Receive CAS Multi-frame Synchronization pulse (RxCASMSync_n) HIGH for one clock period. The user, triggering on the Receive CAS Multi-frame Synchronization pulse, would thus identify the received CAS Multi-frame boundary.

The X in XYXX pattern located in the time slot 16 of Frame number 0 should be fixed to "1" and can be used to prevent mimicking of CAS Multi-frame alignment pattern.

The Y in XYXX pattern is used for alarm indication of time slot 16 to the remote terminal. If signals of time slot 16 is transmitted and received correctly, the Y bit is set to "0". In an alarm condition, the Y bit is set to "1". Therefore, Y bit is also known as CAS Multi-frame yellow alarm.

11.4.3 Configure the framer to transmit Channel Associated Signaling

The XRT84L38 framer supports transmission of Common Channel Signaling and Channel Associated Signaling according to ITU-T Recommendation G.704. As discussed briefly before, Channel Associated Signaling includes the signaling bits, the CAS Multi-frame Alignment pattern and the X and Y bits.

Signaling bits can be inserted into the outgoing E1 frame through the following:

- Signaling data is inserted from the Transmit Signaling Control Registers (TSCR) of each timeslot.
- Signaling data is inserted from TxSig_n pin.
- Signaling data is inserted from TxOH-n pin.

- Signaling data is embedded into the input PCM data coming from the Terminal Equipment.

The CAS Multi-frame alignment pattern of four zeros can be inserted into the outgoing E1 frame by using the following method:

- CAS Multi-frame alignment pattern is inserted from theTransmit Signaling Control Registers (TSCR).
- CAS Multi-frame alignment pattern is inserted from TxSig_n pin.
- CAS Multi-frame alignment pattern is inserted from TxOH-n pin.
- CAS Multi-frame alignment pattern is embedded into the input PCM data coming from the Terminal Equipment.

The CAS Multi-frame Yellow Alarm Y bit and the X bits can be inserted into the outgoing E1 frame by using the following method:

- The X and Y bits are inserted from the Transmit Signaling Control Register (TSCR).
- The X and Y bits are inserted from TxSig_n pin.
- The X and Y bits are inserted from TxOH-n pin.
- The X and Y bits are embedded into the input PCM data coming from the Terminal Equipment.
- The X bit is inserted from the Transmit Signaling Control Register (TSCR) and Y bit is generated by the XRT84L38 framer according to operating condition of the E1 link.

11.4.3.1 Insert Signaling Bits from TSCR Register

The four most significant bits of the Transmit Signaling Control Register (TSCR) of each time slot can be used to store outgoing signaling data. The user can program these bits through microprocessor access. If the XRT84L38 framer is configure to insert signaling bits from TSCR registers, the E1 Transmit Framer block will fill up the time slot 16 octet with the signaling bits stored inside the TSCR registers. The insertion of signaling bit into PCM data is done on a per-channel basis. The most significant bit (Bit 7) of TSCR register is used to store Signaling bit A. Bit 6 is used to hold Signaling bit B. Bit 5 is used to hold Signaling bit C. Bit 4 is used to hold Signaling bit D.

The table below shows the four most significant bits of the Transmit Signaling Control Register.

TRANSMIT SIGNALING CONTROL REGISTER (TSCR) (INDIRECT ADDRESS = 0XN2H, 0X40H - 0X5FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Signaling Bit A	R/W	This bit is used to store Signaling Bit A.
6	Signaling Bit B	R/W	This bit is used to store Signaling Bit B.
5	Signaling Bit C	R/W	This bit is used to store Signaling Bit C.
4	Signaling Bit D	R/W	This bit is used to store Signaling Bit D.

11.4.3.2 Insert Signaling Bits from TxSig_n Pin

The XRT84L38 framer can be configure to insert signaling bits provided by external equipment through the TxSig_n pins. This pin is a multiplexed I/O pin with two functions:

- TxTSb[0]_n - Transmit Timeslot Number Bit [0] Output pin
- TxSig_n - Transmit Signaling Input pin

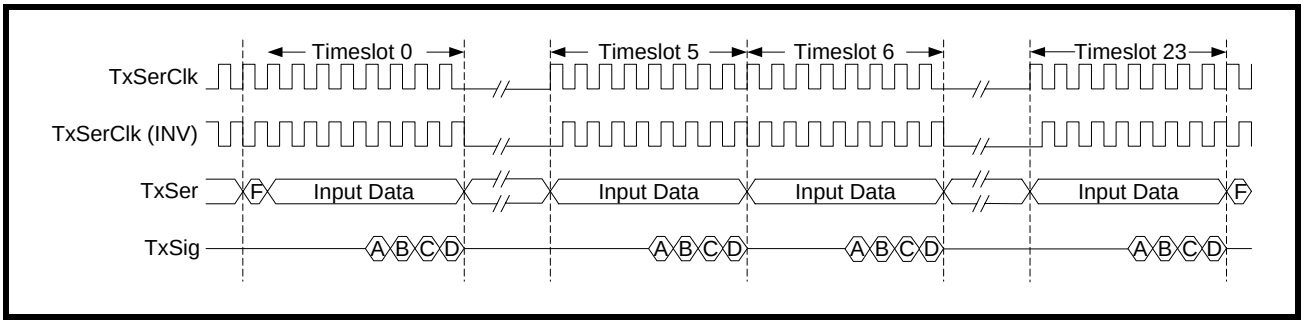
When the Transmit Fractional E1 bit of the Transmit Interface Control Register (TICR) is set to 0, this pin is configured as TxTSb[0]_n pin, it outputs bit 0 of the timeslot number of the E1 PCM data that is transmitting.

When the Transmit Fractional E1 bit of the Transmit Interface Control Register (TICR) is set to 1, this pin is configured as TxSig_n pin, it acts as an input source for the signaling bits to be transmitted in the outbound E1 frames.

Figure 117 below is a timing diagram of the TxSig_n input pin. Please note that the Signaling Bit A of a certain channel coincides with Bit 5 of the PCM data of that channel; Signaling Bit B coincides with Bit 6 of the PCM

data; Signaling Bit C coincides with Bit 7 of the PCM data and Signaling Bit D coincides with Bit 8 (LSB) of the PCM data.

FIGURE 117. TIMING DIAGRAM OF THE TXSIG_N INPUT



The table below shows configurations of the Transmit Fractional E1 bit of the Transmit Interface Control Register (TICR).

TRANSMIT INTERFACE CONTROL REGISTER (TICR) (INDIRECT ADDRESS = 0XN0H, 0X20H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Transmit Fractional E1	R/W	This READ/WRITE bit-field permits the user to determine which one of the two functions the multiplexed I/O pin of TxTSb[0]_n/TxSig_n is spotting. 0 - This pin is configured as TxTSb[0]_n pin, it outputs bit 0 of the timeslot number of the E1 PCM data that is transmitting. 1 - This pin is configured as TxSig_n pin, it acts as an input source for the signaling bits to be transmitted in the outbound E1 frames

11.4.3.3 Insert Signaling Bits from TxOH_n Pin

The XRT84L38 framer can be configure to insert signaling bits provided by external equipment through the Transmit Overhead TxOH_n input pins.

The TxOH_n pin can acts as an input source for the signaling bits to be transmitted in the outbound E1 frames. When this pin is chosen as the input source for the signaling bits, any data presents on this pin in time slot 16 would be taken into the framer directly. The time slot 16 octet of the outbound E1 frame will be replaced by data inputted from this pin in time slot 16.

Please note that the Signaling bit A of Channel 1-15 coincides with Bit 1 of the PCM data; Signaling bit B Channel 1-15 coincides with Bit 2 of the PCM data; Signaling bit C Channel 1-15 coincides with Bit 3 of the PCM; Signaling bit D Channel 1-15 coincides with Bit 4 of the PCM data.

Similarly, the Signaling bit A of Channel 17-31 coincides with Bit 5 of the PCM data; Signaling bit B Channel 17-31 coincides with Bit 6 of the PCM data; Signaling bit C Channel 17-31 coincides with Bit 7 of the PCM; Signaling bit D Channel 17-31 coincides with Bit 8 of the PCM data.

Figure 118 below is a timing diagram of the TxOH_n input pin.

FIGURE 118. TIMING DIAGRAM OF THE TXOH_N INPUT

11.4.3.4 Insert Signaling Data from TxSer_n Pin

Depends on applications, the Terminal Equipment can embed signaling information into the E1 PCM data and then send the data to the XRT84L38 framer device. In this case, the user should configure the framer not to insert any signaling data. The input E1 PCM data will then be directed to the Transmit LIU Interface without any modifications.

11.4.3.5 Enable Channel Associated Signaling and Signaling Data Source Control

The Transmit Signaling Control Register (TSCR) of each channel selects source of signaling data to be inserted into the outgoing E1 frame and enables Channel Associated signaling. As we mentioned before, the signaling data can be inserted from Transmit Signaling Control Registers (TSCR) of each timeslot, from the TxSig_n input pin, from the TxOH_n input pin or from the TxSer_n input pin. The Transmit Signaling Data Source Select [1:0] bits of the Transmit Signaling Control Register (TSCR) determines from which sources the signaling data is inserted from.

The table below shows configurations of the Transmit Signaling Data Source Select [1:0] bits of the Transmit Signaling Control Register (TSCR).

TRANSMIT SIGNALING CONTROL REGISTER (TSCR) (INDIRECT ADDRESS = 0XN2H, 0X40H - 0X57H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Signaling Source Select	R/W	00 - None of the signaling data, the CAS Multi-frame alignment pattern, the X bit or the CAS Multi-frame Yellow Alarm bit Y is inserted into the outgoing E1 PCM data by the framer. However, the user can embed the signaling data, the CAS Multi-frame alignment pattern, the X bit or the CAS Multi-frame Yellow Alarm bit Y into E1 PCM data before routing the PCM data into the framer. 01 - The signaling data, the CAS Multi-frame alignment pattern, the X bit or the CAS Multi-frame Yellow Alarm bit Y is inserted into the outgoing E1 PCM data from TSCR register of each timeslot. 10 - If the XRT84L38 framer is operating in E1 2.048Mbit/s mode and if the TxFR2048 bit of the Transmit Interface Control Register (TICR) is set to zero: The signaling data, the CAS Multi-frame alignment pattern, the X bit or the CAS Multi-frame Yellow Alarm bit Y is inserted into the outgoing E1 PCM data from the TxOH_n input pin. If the XRT84L38 framer is operating in E1 2.048Mbit/s mode and if the TxFR2048 bit of the Transmit Interface Control Register (TICR) is set to one: The signaling data, the CAS Multi-frame alignment pattern, the X bit or the CAS Multi-frame Yellow Alarm bit Y is inserted into the outgoing E1 PCM data from the TxSig_n input pin. 11 - No signaling data or the CAS Multi-frame alignment pattern is inserted into the input E1 PCM data by the framer. However, the user can embed signaling data into E1 PCM data before routing the PCM data into the framer. The X bit is inserted into the outgoing E1 PCM data from TSCR register. The CAS Multi-frame Yellow Alarm Y bit is generated by the XRT84L38 framer depends on operating condition of the E1 link.

11.5 HOW TO CONFIGURE THE XRT84L38 FRAMER TO GENERATE AND TRANSMIT ALARMS AND ERROR INDICATIONS TO REMOTE TERMINAL

The XRT84L38 T1/J1/E1 Octal Framer can be configured to monitor quality of received E1 frames. It can generate error indications if the local receive framer has received error frames from the remote terminal. If corresponding interrupt is enabled, the local microprocessor operation is interrupted by these error conditions. Upon microprocessor interruption, the user can intervene by looking into the error conditions.

At the same time, the user can configure the XRT84L38 framer to transmit alarms and error indications to remote terminal. Different alarms and error indications will be transmitted depending on the error condition. The section below gives a brief discussion of the error conditions and appropriate alarms that should be generated and transmitted by the XRT84L38 framer.

11.5.1 Brief discussion of alarms and error conditions

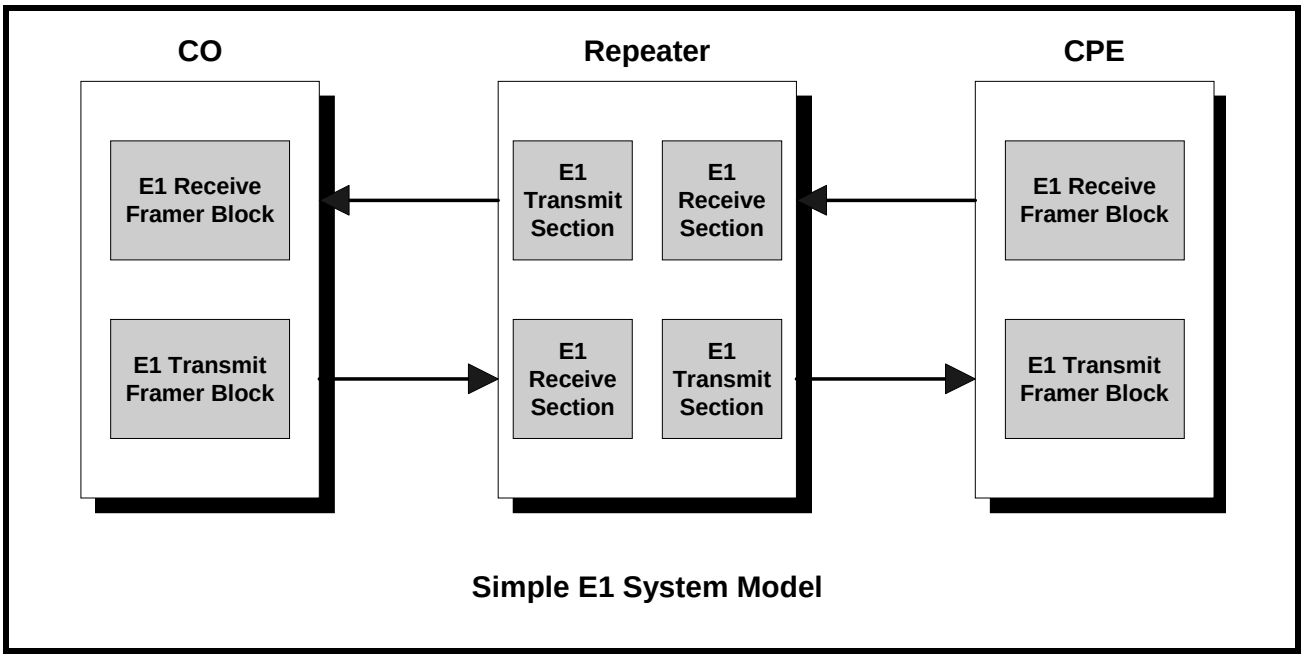
As defined in E1 specification, alarm conditions are created from defects. Defects are momentary impairments present on the E1 trunk. If a defect is present for a sufficient amount of time (called the integration time), then the defect becomes an alarm. Once an alarm is declared, the alarm is present until after the defect clears for a sufficient period of time. The time it takes to clear an alarm is called the de-integration time.

Alarms are used to detect and warn maintenance personnel of problems on the E1 trunk. There are three types of alarms:

- Red alarm or Service Alarm Indication (SAI) Signal
- Blue alarm or Alarm Indication Signal (AIS)
- Yellow alarm or Remote Alarm Indication (RAI) Signal

To explain the error conditions and generation of different alarms, let us create a simple E1 system model. In this model, an E1 signal is sourced from the Central Office (CO) through a Repeater to the Customer Premises Equipment (CPE). At the same time, an E1 signal is routed from the CPE to the Repeater and back to the Central Office. Figure 119 below shows the simple E1 system model.

FIGURE 119. SIMPLE DIAGRAM OF E1 SYSTEM MODEL



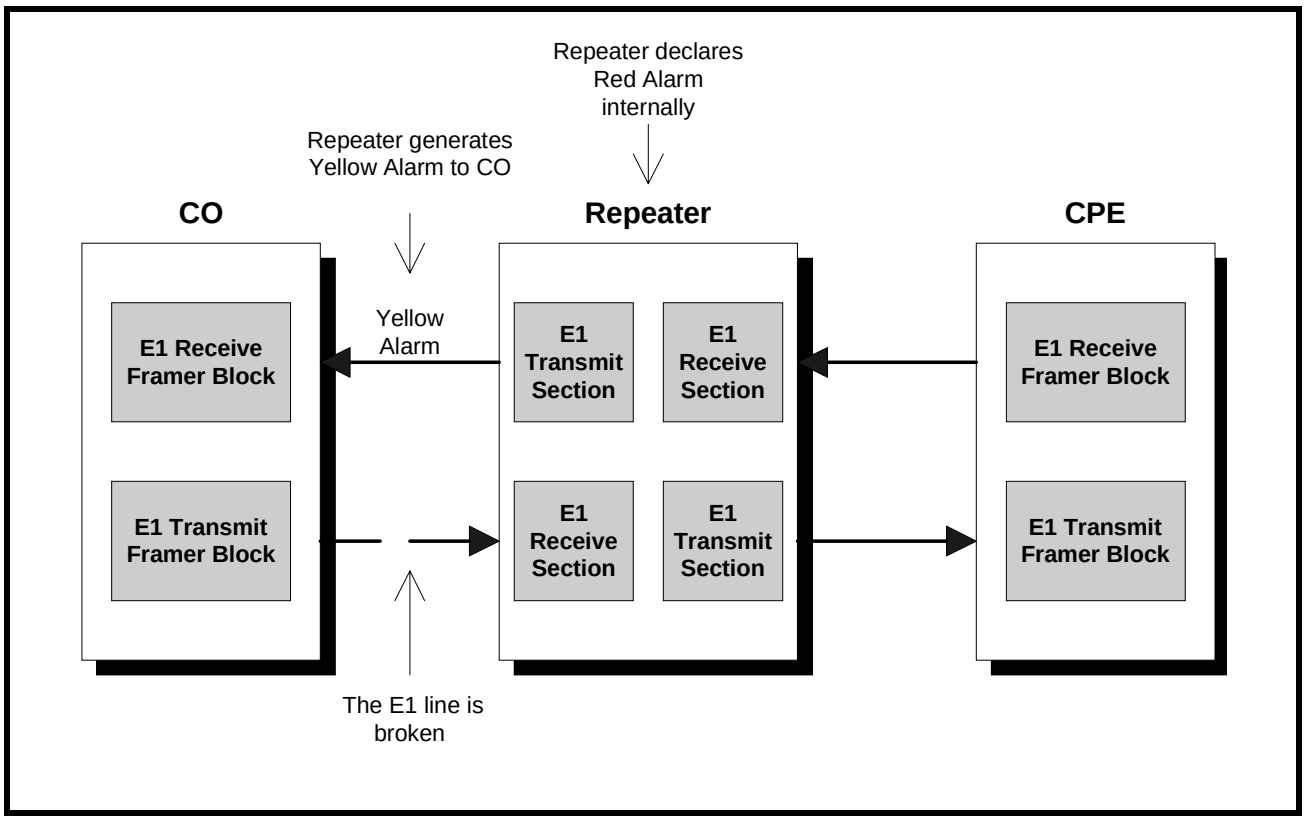
When the E1 system runs normally, that is, when there is no Loss of Signal (LOS) or Loss of Frame (LOF) detected in the line, no alarm will be generated. Sometimes, intermittent outburst of electrical noises on the line might result in Bipolar Violation or bit errors in the incoming signals, but these errors in general will not trigger the equipment to generate alarms. They will, depending on the system requirements, trigger the framer to generate interrupts that would cause the local microprocessor to create performance reports of the line.

Now, consider a case in which the E1 line from the CO to the Repeater is broken or interrupted, resulting in completely loss of incoming data or severely impaired signal quality. Upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the Repeater will generate an internal Red Alarm, also known as the Service Alarm Indication. This alarm will normally trigger a microprocessor interrupt informing the user that an incoming signal failure is happening.

When the Repeater is in the Red Alarm state, it will transmit the Yellow Alarm to the CO indicating the loss of an incoming signal or loss of frame synchronization. This Yellow Alarm informs the Repeater that there is a

problem further down the line and its transmission is not being received at the Repeater. Figure 120 below illustrates the scenario in which the E1 connection from the CO to the Repeater is broken.

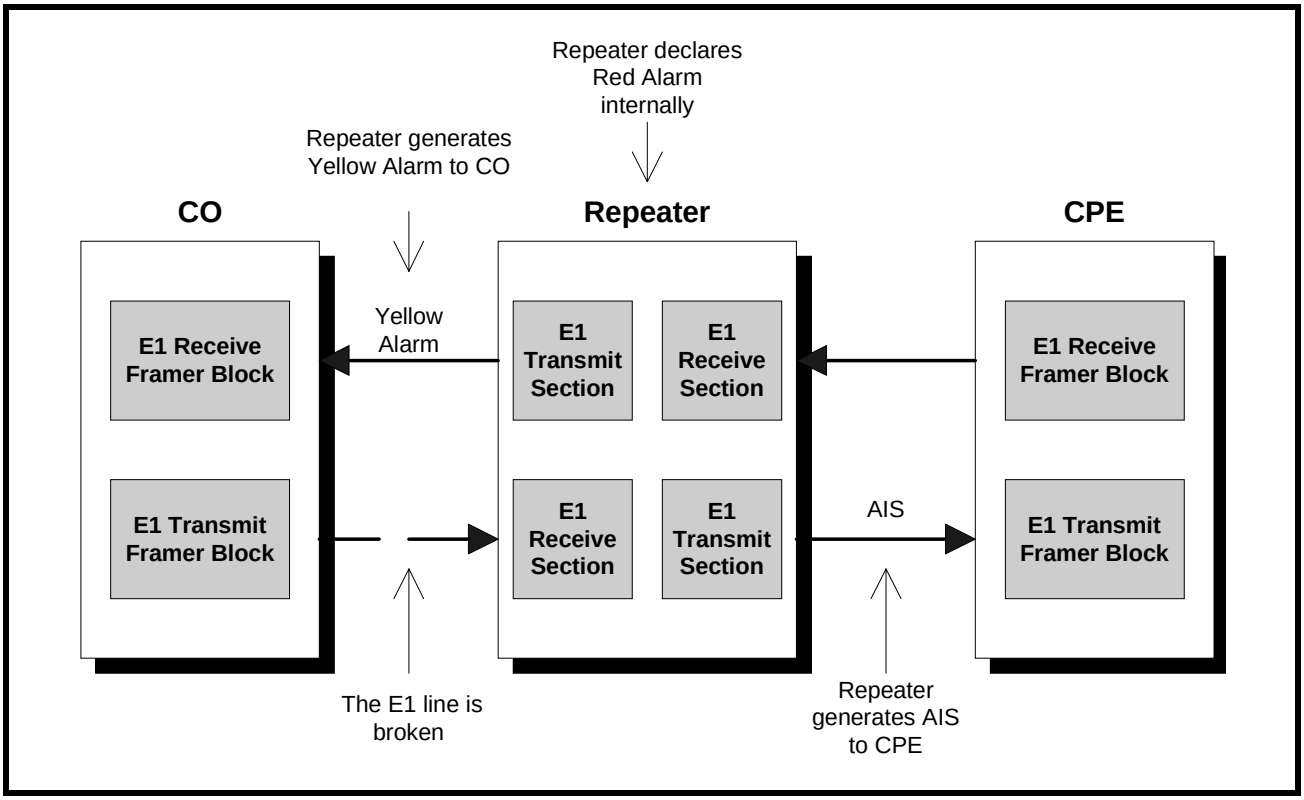
FIGURE 120. GENERATION OF YELLOW ALARM BY THE REPEATER UPON DETECTION OF LINE FAILURE



The Repeater will also transmit a Blue Alarm, also known as Alarm Indication Signal (AIS) to the CPE. Blue alarm is an all ones pattern indicating that the equipment is functioning but unable to offer service due to failures originated from remote side. It is sent such that the equipment downstream will not lose clock synchroni-

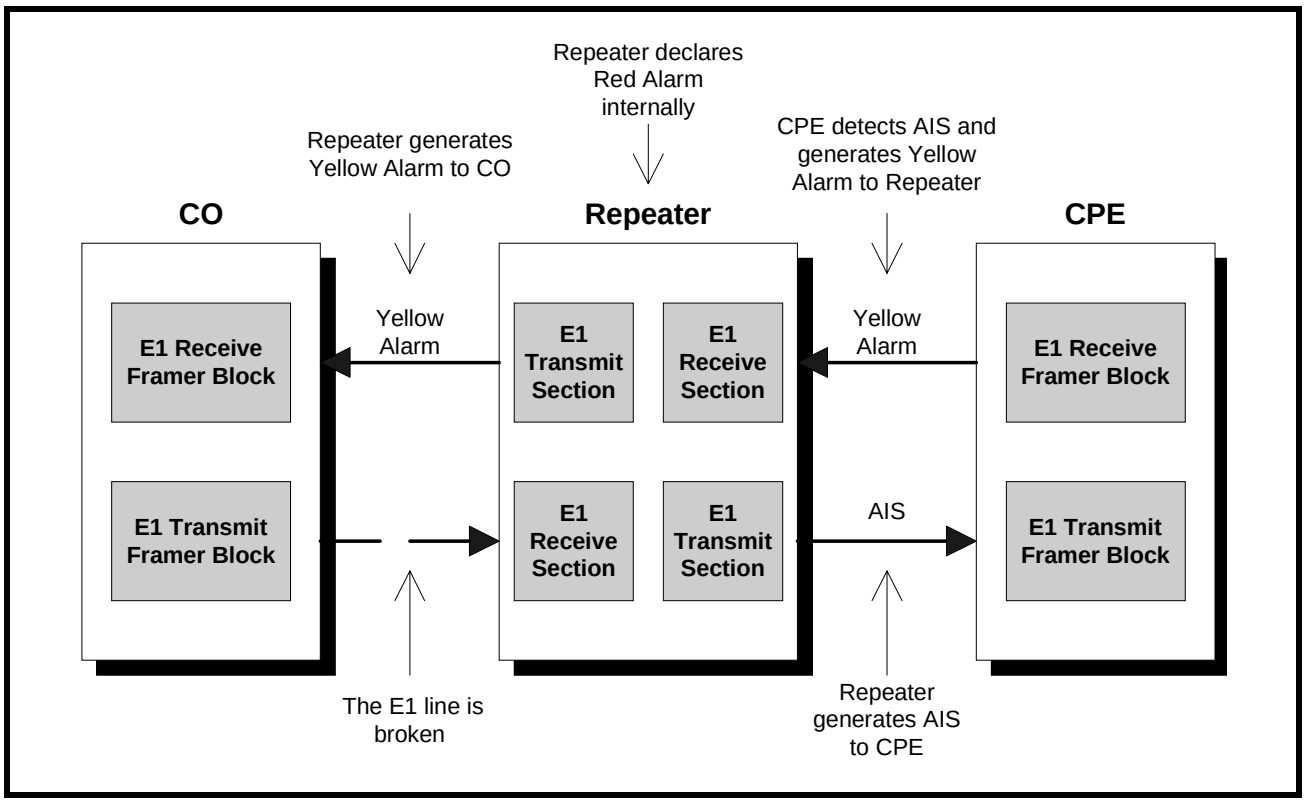
zation even though no meaningful data is received. Figure 121 below illustrates this scenario in which the Repeater is sending an AIS to the CPE upon detection of line failure from the CO.

FIGURE 121. GENERATION OF AIS BY THE REPEATER UPON DETECTION OF LINE FAILURE



Now, the CPE uses the AIS signal sent by the Repeater to recover received clock and remain in synchronization with the system. Upon detecting the incoming AIS signal, the CPE will generate a Yellow Alarm automatically to the Repeater to indicate the loss of incoming data. Figure 122 below illustrates this scenario in which the Repeater is sending an AIS to the CPE and the CPE is sending a Yellow Alarm back to the Repeater.

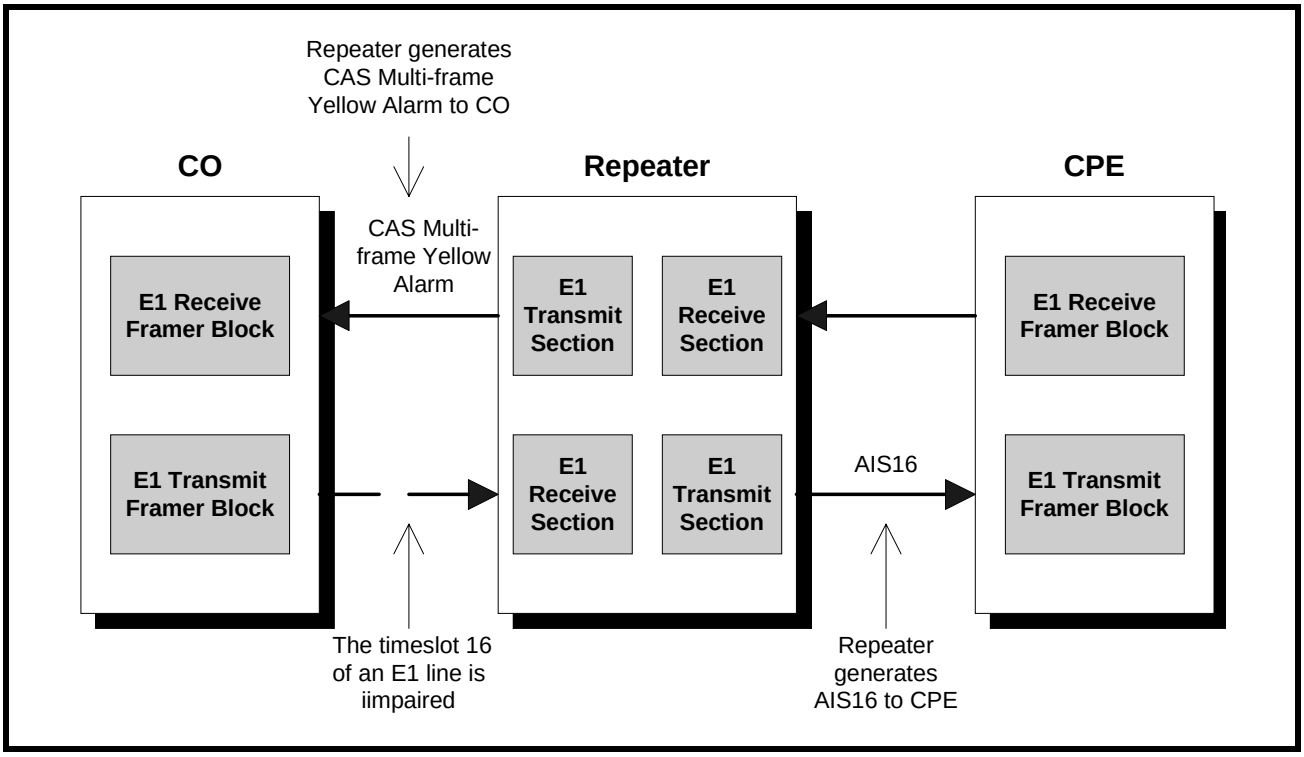
FIGURE 122. GENERATION OF YELLOW ALARM BY THE CPE UPON DETECTION OF AIS ORIGINATED BY THE REPEATER



Next, let us consider the scenario in which the signaling and data link channel (the time slot 16) of an E1 line between a far-end terminal (for example, the CO) and a near-end terminal (for example, the repeater) is impaired. In this case, the CAS signaling data received by the repeater is corrupted. The Repeater will then send an all ones pattern in time slot 16 (AIS16 pattern) downstream to the CPE. The repeater will also generate a CAS Multi-frame Yellow Alarm upstream to the CO to indicate the loss of CAS Multi-frame synchronization.

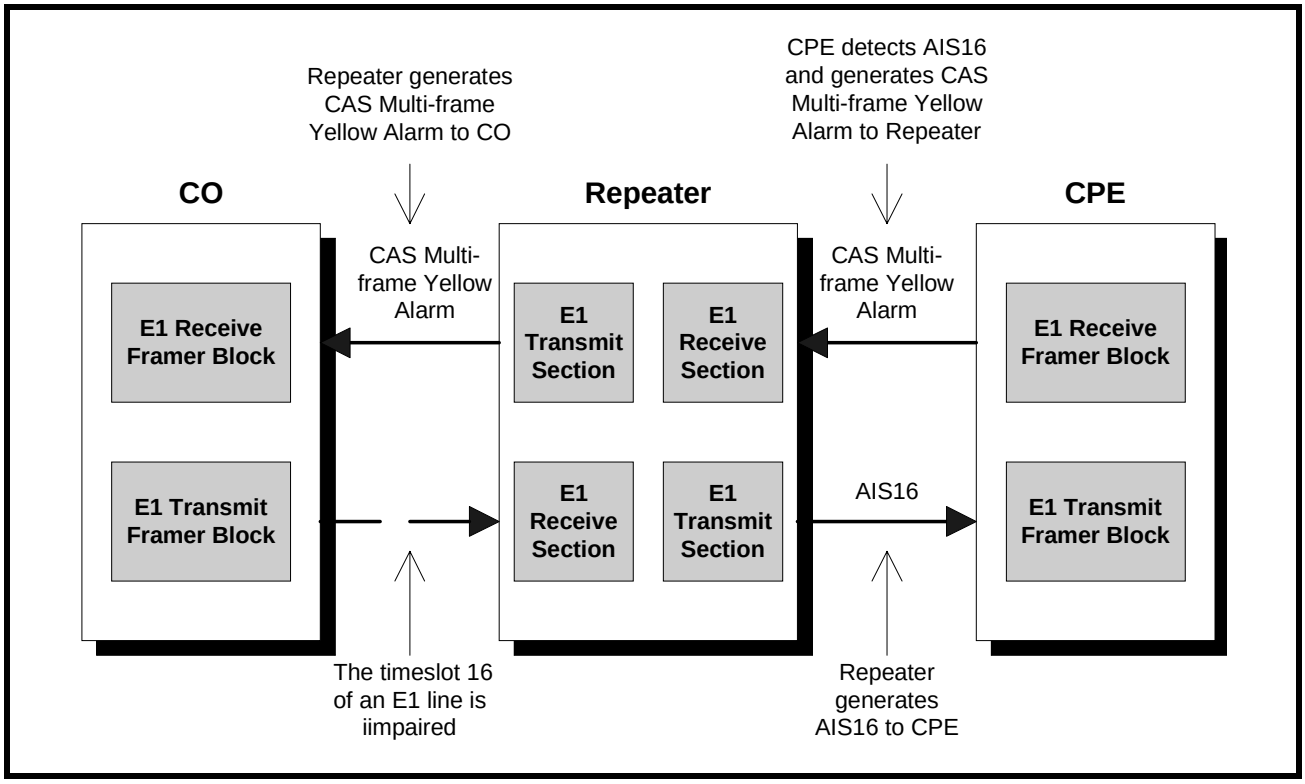
Figure 123 below illustrates this scenario in which the Repeater is sending an "AIS16" pattern to the CPE while sending a CAS Multi-frame Yellow Alarm to the CO.

FIGURE 123. GENERATION OF CAS MULTI-FRAME YELLOW ALARM AND AIS16 BY THE REPEATER



The CPE, upon detecting the incoming AIS16 signal, will generate a CAS Multi-frame Yellow Alarm to the Repeater to indicate the loss of CAS Multi-frame synchronization. Figure 124 below illustrates the CPE sending a CAS Multi-frame Yellow Alarm back to the Repeater

FIGURE 124. GENERATION OF CAS MULTI-FRAM YELLOW ALARM BY THE CPE UPON DETECTION OF "AIS16" PATTERN SENT BY THE REPEATER



In summary, AIS or Blue Alarm is sent by a piece of E1 equipment downstream indicating that the incoming signal from upstream is lost. Yellow Alarm is sent by a piece of E1 equipment upstream upon detection of Loss of Signal, Loss of Frame or when it is receiving AIS.

Similarly, an "AIS16" pattern is sent by a piece of E1 equipment downstream indicating that the incoming data link channel from upstream is damaged. The CAS Multi-frame Yellow Alarm is sent by a piece of E1 equipment upstream upon detection of Loss of CAS Multi-frame synchronization or when it is receiving an "AIS16" pattern.

11.5.2 How to configure the framer to transmit AIS

As we discussed in the previous section, Alarm Indication Signal (AIS) or Blue Alarm is transmitted by the intermediate node to indicate that the equipment is still functioning but unable to offer services. It is an all ones (except for framing bits) pattern which can be used by the equipment further down the line to maintain clock recovery and timing synchronization.

The XRT84L38 framer can generate three types of AIS when it is running in E1 format:

- Framed AIS
- Unframed AIS
- AIS16

Unframed AIS is an all ones pattern. If unframed AIS is sent, the equipment further down the line will be able to maintain timing synchronization and be able to recover clock from the received AIS signal. However, due to the lack of framing bits, the equipment farther down the line will not be able to maintain frame synchronization and will declare Loss of Frame (LOF).

On the other hand, the payload portion of a framed AIS pattern is all ones. However, a framed AIS pattern still has correct framing bits. Therefore, the equipment further down the line can still maintain frame synchronization as well as timing synchronization. In this case, no LOF or Red alarm will be declared.

"AIS16" is an AIS alarm that only supported in E1 framing format. It is an all ones pattern in time slot 16 of each E1 frame. As we mentioned before, time slot 16 is usually used for signaling and data link in E1, therefore, an "AIS16" alarm is transmitted by the intermediate node to indicate that the data link channel is having a problem. Since all the other thirty one time slots are still transmitting normal data (that is, framing information and PCM data), therefore, the equipment further down the line can still maintain frame synchronization, timing synchronization as well as receiving PCM data. In this case, no LOF or Red alarm will be declared by the equipments further down the line. However, a CAS Multi-frame Yellow Alarm will be sent by the equipment further down the line to indicate the loss of CAS Multi-frame alignment.

The Transmit Alarm Indication Signal Select [1:0] bits of the Alarm Generation Register (AGR) enable the three types of AIS transmission that are supported by the XRT84L38 framer. The table below shows configurations of the Transmit Alarm Indication Signal Select [1:0] bits of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR) (INDIRECT ADDRESS = 0XN0H, 0X08H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Transmit AIS Select	R/W	These READ/WRITE bit-fields allows the user to choose which one of the three AIS pattern supported by the XRT84L38 framer will be transmitted. 00 - No AIS alarm is generated. 01 - Enable unframed AIS alarm of all ones pattern. 11 - AIS16 pattern is generated. Only time slot 16 is carrying the all ones pattern. The other time slots still carry framing and PCM data. 11 - Enable framed AIS alarm of all ones pattern except for framing bits.

11.5.3 How to configure the framer to generate Red Alarm

Upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the Repeater will generate an internal Red Alarm when enabled. This alarm will normally trigger a microprocessor interrupt informing the user that an incoming signal failure is happening.

The Loss of Frame Declaration Enable bit of the Alarm Generation Register (AGR) enable the generation of Red Alarm. The table below shows configurations of the of Frame Declaration Enable bit of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR) (INDIRECT ADDRESS = 0XN0H, 0X08H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Loss of Frame Declaration Enable	R/W	This READ/WRITE bit-field permits the framer to declare Red Alarm in case of Loss of Frame Alignment (LOF). When receiver module of the framer detects Loss of Frame Alignment in the incoming data stream, it will generate a Red Alarm. The framer will also generate an RxLOFs interrupt to notify the microprocessor that an LOF condition is occurred. A Yellow Alarm is then returned to the remote transmitter to report that the local receiver detects LOF. 0 - Red Alarm declaration is disabled. 1 - Red Alarm declaration is enabled.

11.5.4 How to configure the framer to transmit Yellow Alarm

The XRT84L38 framer supports transmission of both Yellow Alarm and CAS Multi-frame Yellow Alarm in E1 mode.

Upon detection of Loss of Signal (LOS) or Loss of Frame (LOF) condition, the receiver will transmit the Yellow Alarm back to the source indicating the loss of an incoming signal. This Yellow Alarm informs the source that there is a problem further down the line and its transmission is not being received at the destination.

On the other hand, upon detection of Loss of CAS Multi-frame alignment pattern, the receiver section of the XRT84L38 framer will transmit a CAS Multi-frame Yellow Alarm back to the source indicating the Loss of CAS Multi-frame synchronization.

The Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register (AGR) enable transmission of different types of Yellow alarm that are supported by the XRT84L38 framer.

11.5.4.1 Transmit Yellow Alarm

The Yellow Alarm bits are located at bit 3 of time slot 0 of non-FAS frames. A logic one of this bit denotes the Yellow Alarm and a logic zero of this bit denotes normal operation. The XRT84L38 supports transmission of Yellow Alarm automatically or manually.

When the Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 01, the Yellow Alarm bit is transmitted by echoing the received FAS alignment pattern. If the correct FAS alignment is received, the Yellow Alarm bit is set to zero. If the FAS alignment pattern is missing or corrupted, the Yellow Alarm bit is set to one while Loss of Frame Synchronization is declared.

When the Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 10, the Yellow Alarm bit is transmitted as zero.

When the Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 11, the Yellow Alarm bit is transmitted as one.

11.5.4.2 Transmit CAS Multi-frame Yellow Alarm

Within the sixteen-frame CAS Multi-frame, the CAS Multi-frame Yellow Alarm bits are located at bit 6 of time slot 16 of frame number 0. A logic one of this bit denotes the CAS Multi-frame Yellow Alarm and a logic zero of this bit denotes normal operation. The XRT84L38 supports transmission of CAS Multi-frame Yellow Alarm automatically or manually.

When the CAS Multi-frame Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 01, the CAS Multi-frame Yellow Alarm bit is transmitted by echoing the received CAS Multi-frame alignment pattern (the four zeros pattern). If the correct CAS Multi-frame alignment is received, the CAS Multi-frame Yellow Alarm bit is set to zero. If the CAS Multi-frame alignment pattern is missing or corrupted, the CAS Multi-frame Yellow Alarm bit is set to one while Loss of CAS Multi-frame Synchronization is declared.

When the CAS Multi-frame Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 10, the CAS Multi-frame Yellow Alarm bit is transmitted as zero.

When the CAS Multi-frame Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register are set to 11, the CAS Multi-frame Yellow Alarm bit is transmitted as one.

The table below shows configurations of the Yellow Alarm Generation Select [1:0] bits of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR) (INDIRECT ADDRESS = 0XN0H, 0X08H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	Yellow Alarm Generation Select	R/W	These READ/WRITE bit-fields allows the user to choose how the XRT84L38 would generate Yellow Alarm and CAS Multi-frame Yellow Alarm. 00 - Transmission of Yellow Alarm and CAS Multi-frame Yellow Alarm is disabled. 01 - The Yellow Alarm bit is transmitted by echoing the received FAS alignment pattern. If the correct FAS alignment is received, the Yellow Alarm bit is set to zero. If the FAS alignment pattern is missing or corrupted, the Yellow Alarm bit is set to one. The CAS Multi-frame Yellow Alarm bit is transmitted by echoing the received CAS Multi-frame alignment pattern (the four zeros pattern). If the correct CAS Multi-frame alignment is received, the CAS Multi-frame Yellow Alarm bit is set to zero. If the CAS Multi-frame alignment pattern is missing or corrupted, the CAS Multi-frame Yellow Alarm bit is set to one. 10 - The Yellow Alarm and CAS Multi-frame Yellow Alarms are transmitted as zero. 11 - The Yellow Alarm and CAS Multi-frame Yellow Alarms are transmitted as one.

12.0 E1 RECEIVE FRAMER BLOCK

12.1 How to Configure XRT84L38 to Operate in E1 Mode

The XRT84L38 Octal T1/E1/J1 Framer supports DS1, J1 or E1 framing modes. Since J1 standard is very similar to DS1 standard with a few minor changes, the J1 framing mode is included as a sub-set of the DS1 framing mode. All eight framers within the XRT84L38 silicon can be individually configured to support DS1, J1 or E1 framing modes.

Note: *If transmitting section of one framer is configured to support either one of the framing modes, the receiving section is automatically configured to support the same framing modes.*

The T1/E1 Select bit of the Clock Select Register (CSR) controls which framing mode, that is, T1/J1 or E1, supported by the framer. The table below illustrates configurations of the T1/E1 Select bit of the Clock Select Register (CSR).

CLOCK SELECT REGISTER (CSR)(INDIRECT ADDRESS = 0XN0H, 0X00H)

Bit Number	Bit Name	Bit Type	Bit Description
6	T1/E1 Select	R/W	0 - The XRT84L38 framer is running in E1 mode. 1 - The XRT84L38 framer is running in T1 mode.

The purpose of the E1 Transmit Framer block is to embed and encode user payload data into frames and to route this E1 frame data to the Transmit E1 LIU Interface block. Please note that the XRT84L38 has eight (8) individual E1 Transmit Framer blocks. Hence, the following description applies to all eight of these individual Transmit E1 Framer blocks.

The purpose of the E1 Transmit Framer block is:

- To encode user data, inputted from the Terminal Equipment into a standard framing format.
- To provide individual data control and signaling conditioning of each DS0 channel.
- To support the transmission of HDLC messages, from the local transmitting terminal, to the remote receiving terminal.
- To transmit indications that the local receive framer has received error frames from the remote terminal.
- To transmit alarm condition indicators to the remote terminal.

The following sections discuss the functionalities of E1 Transmit Framer block in details. We will also describe how to configure the XRT84L38 to transmit E1 frames according to system requirement of users.

12.2 How to Configure the Framer to Receive Data in Various E1 Framing Formats

The XRT84L38 Octal T1/E1/J1 Framer is designed to meet the requirement of ITU-T Recommendation G.704. The E1 framer supports the following:

- Frame Alignment Signal (FAS)
- CRC-4 Multi-frame

The ITU-T Recommendation G.704 also specifies two forms of signaling that can be supported by the E1 Transport medium:

- Channel Associated Signaling (CAS)
- Common Channel Signaling (CCS)

The XRT84L38 framer supports both CAS, CCS signaling format together with Clear Channel without signaling.

12.2.1 How to configure the framer to choose FAS searching algorithm

The XRT84L38 framer can use two algorithms to search for FAS pattern and thus declare FAS alignment synchronization. The FAS Selection bit of the Framing Select Register (FSR) allows the user to choose which one of the two algorithms for searching FAS frame alignment.

The table below shows configurations of the FAS Selection bit of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (INDIRECT ADDRESS = 0XN0H, 0X07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	FAS Selection bit	R/W	This Read/Write bit field allows the user to determine which algorithm is used for searching FAS frame alignment pattern. When an FAS alignment pattern is found and locked, the XRT84L38 will generate Receive Synchronization (RxSync_n) pulse. 0 - Algorithm 1 is selected for searching FAS frame alignment pattern. 1 - Algorithm 2 is selected for searching FAS frame alignment pattern.

12.2.2 How to configure the framer to enable CRC-4 Multi-frame alignment and select the locking criteria

The CRC-4 Selection [1:0] bits of the Framing Select Register (FSR) enable the framer to search for CRC-4 Multi-frame alignment and select the criteria for locking the CRC-4 Multi-frame alignment.

The table below shows configurations of the CRC-4 Selection [1:0] bit of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (INDIRECT ADDRESS = 0XN0H, 0X07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	CRC-4 Selection bit	R/W	Theses Read/Write bit fields allow the user to enable searching of CRC-4 Multi-frame alignment and determine what criteria are used for locking the CRC-4 Multi-frame alignment pattern. 00 - Searching of CRC-4 Multi-frame alignment is disabled. The XRT84L38 framer will not search for CRC-4 Multi-frame alignment and thus will not declare CRC-4 Multi-frame synchronization. No Receive CRC-4 Multi-frame Synchronization (RxCRCMsync_n) pulse will be generated by the framer. 01 - Searching of CRC-4 Multi-frame alignment is enabled. The XRT84L38 will search for and declare CRC-4 Multi-frame synchronization if: At least one valid CRC-4 Multi-frame alignment signal is observed within 8 ms. 10 - Searching of CRC-4 Multi-frame alignment is enabled. The XRT84L38 will search for and declare CRC-4 Multi-frame synchronization if: At least two valid CRC-4 Multi-frame alignment signals are observed within 8 ms. The time separating two CRC-4 Multi-frame alignment signals is multiple of 2 ms. 11 - Searching of CRC-4 Multi-frame alignment is enabled. The XRT84L38 will search for and declare CRC-4 Multi-frame synchronization if: At least three valid CRC-4 Multi-frame alignment signals are observed within 8 ms. The time separating two CRC-4 Multi-frame alignment signals is multiple of 2 ms.

12.2.3 How to configure the framer to enable CAS Multi-frame alignment

The XRT84L38 framer can use two algorithms to search for CAS Multi-frame alignment pattern. Upon detecting of CAS Multi-frame alignment pattern, the framer will declare CAS Multi-frame alignment synchronization and generate the Receive CAS Multi-frame synchronization pulse (RxCASMsync_n). The CAS Selection [1:0] bits of the Framing Select Register (FSR) enable the framer to search for CAS Multi-frame alignment.

The table below shows configurations of the CAS Selection [1:0] bit of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (INDIRECT ADDRESS = 0XN0H, 0X07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5-4	CAS Selection bit	R/W	These Read/Write bit fields allow the user to enable searching of CAS Multi-frame alignment and determine which algorithm of the two are used for locking the CAS Multi-frame alignment pattern. 00 - Searching of CAS Multi-frame alignment is disabled. The XRT84L38 framer will not search for CAS Multi-frame alignment and thus will not declare CAS Multi-frame synchronization. No Receive CAS Multi-frame Synchronization (RxCRCMsync_n) pulse will be generated by the framer. 01 - Searching of CAS Multi-frame alignment is enabled. The XRT84L38 will search for and declare CAS Multi-frame synchronization using Algorithm 1. 10 - Searching of CAS Multi-frame alignment is enabled. The XRT84L38 will search for and declare CAS Multi-frame synchronization using Algorithm 2 (G.732). 11 - Searching of CAS Multi-frame alignment is disabled. The XRT84L38 framer will not search for CAS Multi-frame alignment and thus will not declare CAS Multi-frame synchronization. No Receive CAS Multi-frame Synchronization (RxCRCMsync_n) pulse will be generated by the framer.

12.3 HOW TO CONFIGURE THE FRAMER TO APPLY DATA AND SIGNALING CONDITIONING TO RECEIVED E1 PAYLOAD DATA ON A PER-CHANNEL BASIS

The XRT84L38 T1/J1/E1 Octal Framer provides individual control of each of the thirty two DS0 channels. The user can apply data and signaling conditioning to the received E1 payload data coming from the E1 LIU Receive Block on a per-channel basis.

The XRT84L38 framer can apply the following changes to the received E1 payload data coming from the Terminal Equipment on a per-channel basis:

- All 8 bits of the received payload data are inverted
- The even bits of the received payload data are inverted
- The odd bits of the received payload data are inverted
- The MSB of the received payload data is inverted
- All received payload data except the MSB are inverted

Configurations of the XRT84L38 framer to apply the above-mentioned changes to the received E1 PAYLOAD data are controlled by the Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of each DS0 channel.

The XRT84L38 framer can also replace the incoming E1 payload data from the E1 LIU Receive Block with predefined or user-defined codes. The XRT84L38 supports the following conditioning substitutions:

- BUSY code - an octet with hexadecimal value of 0x7F
- BUSY_TS code - an octet of pattern "111xxxxx" where "xxxxx" represents the timeslot number
- VACANT code - an octet with hexadecimal value of 0xFF
- A-law Digital Milliwatt code
- u-law Digital Milliwatt code
- IDLE code - an octet defined by the value stored in the User IDLE Code Register (UCR)
- MOOF code - MUX-Out-Of-Frame code with hexadecimal value of 0x1A

- PRBS code - an octet generated by the Pseudo-Random Bit Sequence (PRBS) Generator block of the framer

Once again, configuration of the XRT84L38 framer to replace the received E1 payload data with the above-mentioned coding schemes are controlled by the Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of each DS0 channel.

Finally, the XRT84L38 framer can configure any one or ones of the thirty two DS0 channels to be D or E channels. D channel is used primarily for data link applications. E channel is used primarily for signaling for circuit switching with multiple access configurations.

The Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of each channel determine whether that particular channel is configured as D or E channel.

The table below illustrates configurations of the Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR).

RECEIVE CHANNEL CONTROL REGISTER (RCCR) (INDIRECT ADDRESS = 0XN2H, 0X60H - 0X7FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-0	Receive Conditioning Select	R/W	0000 - The received E1 payload data of this DS0 channel is unchanged. 0001 - All 8 bits of the input E1 payload data of this DS0 channel are inverted. 0010 - The even bits of the input E1 payload data of this DS0 channel are inverted. 0011 - The odd bits of the input E1 payload data of this DS0 channel are inverted. 0100 - The input E1 payload data of this DS0 channel are replaced by the octet stored in User IDLE Code Register (UCR). 0101 - The input E1 payload data of this DS0 channel are replaced by BUSY code (0x7F). 0110 - The input E1 payload data of this DS0 channel are replaced by VACANT code (0xFF). 0111 - The input E1 payload data of this DS0 channel are replaced by BUSY_TS code (111xxxxx). 1000 - The input E1 payload data of this DS0 channel are replaced by MUX-Out-Of-Frame (MOOF) code with value 0x1A. 1001 - The input E1 payload data of this DS0 channel are replaced by the A-law digital milliwatt pattern. 1010 - The input E1 payload data of this DS0 channel are replaced by the u-law digital milliwatt pattern. 1011 - The MSB bit of the input E1 payload data of this DS0 channel is inverted. 1100 - All bits of the input E1 payload data of this DS0 channel except MSB bit are inverted. 1101 - The input E1 payload data of this DS0 channel are replaced by PRBS pattern created by the internal PRBS Generator of XRT84L38 framer. 1110 - The input E1 payload data of this DS0 channel is unchanged. 1111 - This channel is configured as D or E timeslot.

When the Receive Data Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of a particular DS0 channel are set to 0100, the received E1 payload data of this DS0 channel are replaced by the

octet stored in the Receive User IDLE Code Register (RUCR). The table below shows contents of the Receive User IDLE Code Register.

RECEIVE USER IDLE CODE REGISTER (UCR) (INDIRECT ADDRESS = 0XN02H, 0X80H - 0X97H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-0	User IDLE Code	R/W	These READ/WRITE bit-fields permits the user store any value of IDLE code into the framer. When the Receive Data Conditioning Select [3:0] bits of RCCR register of a particular DS0 channel are set to 0100, the received E1 payload data are replaced by contents of this register and sent to the Terminal Equipment.

12.4 How to Configure the XRT84L38 Framer to Extract Robbed-bit Signaling Information

The XRT84L38 T1/J1/E1 Octal Framer supports insertion of Robbed-bit Signaling information into the outgoing E1 frame. It also supports extraction and substitution of Robbed-bit Signaling information from the incoming E1 frame. The following section describes how does the XRT84L38 framer extract and substitute Robbed-bit Signaling in E1 mode.

12.4.1 Configure the framer to receive and extract Robbed-bit Signaling

The XRT84L38 framer supports receiving and extraction of CAS signaling. The Receive Signaling Extraction Control [1:0] bits of the Receive Signaling Control Register (RSCR) of each channel select either:

- No signaling extraction
- Two-code signaling
- Four-code signaling or
- Sixteen-code signaling

The table below shows configurations of the Receive Signaling Extraction Control [1:0] bits of the Receive Signaling Control Register.

RECEIVE SIGNALING CONTROL REGISTER (RSCR) (INDIRECT ADDRESS = 0XN2H, 0XA0H - 0XB7H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Signaling Extraction Control	R/W	00 - The XRT84L38 framer does not extract signaling information from incoming E1 payload data. 01 - The XRT84L38 framer extracts sixteen-code signaling information from incoming E1 payload data. 10 - The XRT84L38 framer extracts four-code signaling information from incoming E1 payload data. 11 - The XRT84L38 framer extracts two-code signaling information from incoming E1 payload data.

Upon receiving and extraction of signaling bits from the incoming E1 frames, the XRT84L38 framer compares the signaling bits with the previously received ones. If there is a change of signaling data, a Signaling Update (SIG) interrupt request may be generated at the end of an E1 multi-frame. The user can thus be notified of a Change of Signaling Data event.

To enable the Signaling Update interrupt, the Signaling Change Interrupt Enable bit of the Framer Interrupt Enable Register (FIER) has to be set. In addition, the T1/E1 Framer Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Signaling Change Interrupt Enable bit of the Framer Interrupt Enable Register.

FRAMER INTERRUPT ENABLE REGISTER (FIER) (INDIRECT ADDRESS = 0XNAH, 0X05H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Signaling Change Interrupt Enable	R/W	0 - The Signaling Update interrupt is disabled. 1 - The Signaling Update interrupt is enabled.

The table below shows configurations of the T1/E1 Framer Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	T1/E1 Framer Interrupt Enable	R/W	0 - Every interrupt generated by the Framer Interrupt Status Register (FISR) is disabled. 1 - Every interrupt generated by the Framer Interrupt Status Register (FISR) is enabled.

When these interrupt enable bits are set and the signaling information received is changed, the E1 Receive Framer block will set the Signaling Updated status bit of the Framer Interrupt Status Register (FISR) to one. This status indicator is valid until the Framer Interrupt Status Register is read. Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Signaling Update status bits of the Framer Interrupt Status Register.

FRAMER INTERRUPT STATUS REGISTER (FISR) (INDIRECT ADDRESS = 0XNAH, 0X04H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Signaling Updated	RUR / WC	0 - There is no change of signaling information in the incoming E1 payload data. 1 - There is change of signaling information in the incoming E1 payload data.

Now, there is only one problem remains. Since there are thirty two DS0 channels in E1, how do we know signaling information of which channel is changed?

To solve this problem, the XRT84L38 provides three 8-bit Signaling Change Registers to indicate the channel(s) which signaling data change had occurred over the last E1 multi-frame period. Each bit of the Signaling Change Registers represents one timeslot of the E1 frame. If any particular bit is zero, it means there is no change of signaling data occurred in that particular timeslot over the last E1 multi-frame period. If any particular bit is one, it means there is change of signaling data occurred over the last E1 multi-frame period.

The table below shows configurations of the Signaling Change Registers.

SIGNALING CHANGE REGISTERS (SCR) (INDIRECT ADDRESS = 0XN0H, 0X0DH - 0X10H)

LOCATION \ BIT	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0xn0H - 0x0DH	Ch 0	Ch 1	Ch 2	Ch 3	Ch 4	Ch 5	Ch 6	Ch 7
0xn0H - 0x0EH	Ch 8	Ch 9	Ch 10	Ch 11	Ch 12	Ch 13	Ch 14	Ch 15
0xn0H - 0x0FH	Ch 16	Ch 17	Ch 18	Ch 19	Ch 20	Ch 21	Ch 22	Ch 23
0xn0H - 0x0FH	Ch 24	Ch 25	Ch 26	Ch 27	Ch 28	Ch 29	Ch 30	Ch 31

By reading contents of the Signaling Update status bits of the Framer Interrupt Status Register and the Signaling Change Registers, the user can clearly identify which one(s) of the thirty-two DS0 channels has changed signaling information over the last multi-frame period.

Depending on configurations of the XRT84L38 framer, the signaling bits can be extracted from the incoming E1 frame and direct to all or any one of the following destinations:

- Signaling data is stored to Receive Signaling Register Array (RSRA) of each channel
- Signaling data is sent to the Terminal Equipment through the Receive Signaling Output pin (RxSig_n)
- Signaling data is sent to the Terminal Equipment through the Receive Overhead Output pin (RxOH_n)
- Signaling data is embedded into the output PCM data sending towards the Terminal Equipment through the Receive Serial Output pin (RxSer_n)

The follow sections discuss how to configure the XRT84L38 framer to extract signaling information bits and send them to different destinations.

12.4.1.1 Store Signaling Bits into RSRA Register Array

The four least significant bits of the Receive Signaling Register Array (RSRA) of each timeslot can be used to store received signaling data. The user can read these bits through microprocessor access. If the XRT84L38 framer is configure to extract signaling bits from incoming E1 payload data, the E1 Receive Framer block will strip off the CAS signaling bits from time slot 16 of the incoming E1 frames and store them into appropriate locations of the RSRA. The extraction of signaling bit from E1 PCM data is done on a per-channel basis. The Bit 3 of RSRA register is used to hole Signaling bit A. Bit 2 is used to hold Signaling bit B. Bit 1 is used to hold Signaling bit C. Bit 0 is used to hold Signaling bit D.

The table below shows the four least significant bits of the Receive Signaling Register Array.

RECEIVE SIGNALING REGISTER ARRAY (RSRA) (INDIRECT ADDRESS = 0XN4H, 0X00H - 0X1FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Signaling Bit A	R/W	This bit is used to store Signaling Bit A that is received and extracted.
2	Signaling Bit B	R/W	This bit is used to store Signaling Bit B that is received and extracted.
1	Signaling Bit C	R/W	This bit is used to store Signaling Bit C that is received and extracted.
0	Signaling Bit D	R/W	This bit is used to store Signaling Bit D that is received and extracted.

12.4.1.2 Outputting Signaling Bits through RxSig_n Pin

The XRT84L38 framer can be configure to output extracted signaling bits to external equipment through the RxSig_n pins. This pin is a multiplexed I/O pin with two functions:

- RxTSb[0]_n - Receive Timeslot Number Bit [0] Output pin
- RxSig_n - Receive Signaling Output pin

When the Receive Fractional E1 bit of the Receive Interface Control Register (RICR) is set to 0, this pin is configured as RxTSb[0]_n pin, it outputs bit 0 of the timeslot number of the E1 PCM data that is receiving.

When the Receive Fractional E1 bit of the Receive Interface Control Register (RICR) is set to 1, this pin is configured as RxSig_n pin, it acts as an output source for the signaling bits to be received in the inbound E1 frames.

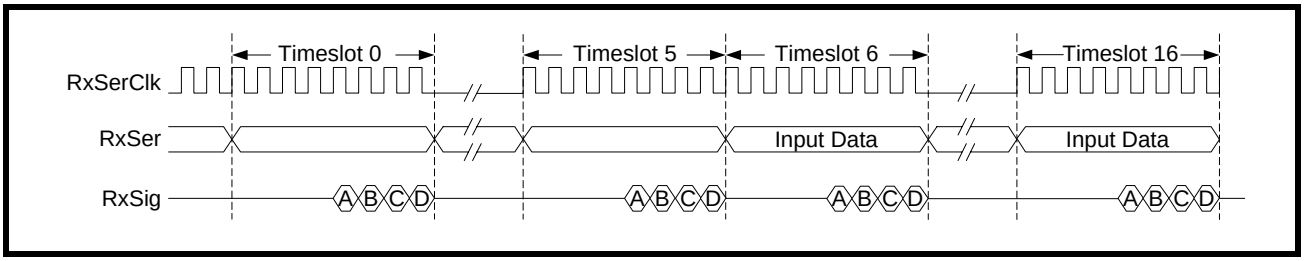
The table below shows configurations of the Receive Fractional E1 bit of the Receive Interface Control Register (RICR).

RECEIVE INTERFACE CONTROL REGISTER (RICR) (INDIRECT ADDRESS = 0XN0H, 0X20H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Fractional E1	R/W	This READ/WRITE bit-field permits the user to determine which one of the two functions the multiplexed I/O pin of RxTSb[0]_n/RxSig_n is spotting. 0 - This pin is configured as RxTSb[0]_n pin, it outputs bit 0 of the timeslot number of the E1 PCM data that is receiving. 1 - This pin is configured as RxSig_n pin, it acts as an output source for the signaling bits to be received in the inbound E1 frames

Figure 125 below is a timing diagram of the RxSig_n output pin. Please note that the Signaling Bit A of a certain timeslot coincides with Bit 3 of the Received serial output data; Signaling Bit B coincides with Bit 2 of the Received serial output data; Signaling Bit C coincides with Bit 1 of the Received serial output data and Signaling Bit D coincides with Bit 0 of the Received serial output data.

FIGURE 125. TIMING DIAGRAM OF RXSIG_N OUTPUT PIN



12.4.1.3 Outputting Signaling Bits from RxOH_n Pin

The XRT84L38 framer can be configure to output extracted signaling bits to external equipment through the Receive Overhead RxOH_n output pins.

The RxOH_n pin can acts as an output source for the signaling bits to be received in the inbound E1 frames. When this pin is chosen as the output source for the signaling bits, any data presents in time slot 16 of the incoming E1 frames would be presented onto the pin directly.

Please note that the Signaling bit A of Channel 1-15 coincides with Bit 1 of the PCM data; Signaling bit B Channel 1-15 coincides with Bit 2 of the PCM data; Signaling bit C Channel 1-15 coincides with Bit 3 of the PCM; Signaling bit D Channel 1-15 coincides with Bit 4 of the PCM data.

Similarly, the Signaling bit A of Channel 17-31 coincides with Bit 5 of the PCM data; Signaling bit B Channel 17-31 coincides with Bit 6 of the PCM data; Signaling bit C Channel 17-31 coincides with Bit 7 of the PCM; Signaling bit D Channel 17-31 coincides with Bit 8 of the PCM data.

Figure 126 below is a timing diagram of the RxOH_n output pin.

FIGURE 126. TIMING DIAGRAM OF THE RXOH_N OUTPUT PIN

(REDRAW) Figure ?: Timing diagram of the RxOH_n Output pin

The Receive Signaling Output Enable bit of the Receive Signaling Control Register (RSCR) determines whether the extracted signaling bits will be sent through the Receive Overhead Output pin (RxOH_n) to external equipments. The table below shows configurations of the Receive Overhead Output Enable bit of the Receive Signaling Control Register.

RECEIVE SIGNALING CONTROL REGISTER (RSCR) (INDIRECT ADDRESS = 0XN2H, 0XA0H - 0XBFH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Signaling Output Enable	R/W	0 - The XRT84L38 framer will not send extracted signaling bits from the incoming E1 payload data to external equipment through the Receive Overhead Output pin (RxOH_n). 1 - The XRT84L38 framer will send extracted signaling bits from the incoming E1 payload data to external equipment through the Receive Overhead Output pin (RxOH_n).

12.4.1.4 Send Signaling Data through RxSer_n Pin

As mentioned in the above sections, signaling information embedded in the incoming E1 PCM data can be sent to either the RSRA register array and/or sent through the Receive Signaling Output pin, at the same time, the signaling data will be directed to the Receive Serial Data Output pin together with other incoming E1 payload data. The external equipment can thus still extract signaling data from the received E1 payload data separately.

12.4.1.5 Signaling Data Substitution

After channel conditioning, the signaling conditioning can be optionally enabled by the RSCR registers. The actual signaling bits in each channel can be replaced either with all ones or with signaling bits stored in the Receive Substitution Signaling Register (RSSR). To enable signaling substitution, the Receive Signaling Substitution Enable bit of the Receive Signaling Control Register (RSCR) has to be set to one. The table below shows configuration of the Receive Signaling Substitution Enable bit of the Receive Signaling Control Register.

RECEIVE SIGNALING CONTROL REGISTER (RSCR) (INDIRECT ADDRESS = 0XN2H, 0XA0H - 0XBFH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Receive Signaling Substitution Enable	R/W	0 - Signaling Substitution is disabled. The XRT84L38 framer will not replace extracted signaling bits from the incoming E1 payload data with all ones or with signaling bits stored in RSSR registers. 1 - Signaling Substitution is enabled. The XRT84L38 framer will replace extracted signaling bits from the incoming E1 payload data with all ones or with signaling bits stored in RSSR registers.

As mentioned before, the actual signaling bits in each channel can be replaced either with all ones or with signaling bits stored in the Receive Substitution Signaling Register (RSSR). The table below shows configurations of the Receive Substitution Signaling Register.

RECEIVE SUBSTITUTION SIGNALING REGISTER (RSSR) (INDIRECT ADDRESS = 0XN02H, 0X80H - 0X9FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7-4	Reserved	R/W	

RECEIVE SUBSTITUTION SIGNALING REGISTER (RSSR) (INDIRECT ADDRESS = 0XN02H, 0X80H - 0X9FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	SIG16-A SIG4-A SIG2-A		Sixteen-Code Signaling bit A Four-Code Signaling bit A Two-Code Signaling bit A
2	SIG16-B SIG4-B SIG2-A		Sixteen-Code Signaling bit B Four-Code Signaling bit B Two-Code Signaling bit A
1	SIG16-C SIG4-A SIG2-A		Sixteen-Code Signaling bit C Four-Code Signaling bit A Two-Code Signaling bit A
0	SIG16-D SIG4-B SIG2-A		Sixteen-Code Signaling bit D Four-Code Signaling bit B Two-Code Signaling bit A

The Receive Signaling Substitution Control [1:0] bits can select all ones substitution, two-code signaling substitution, four-code signaling substitution, or sixteen-code signaling.

The XRT84L38 framer can substitute received signaling bits with all ones. Two-code signaling substitution is done by substituting all the four signaling bits with the content of the SIG2-A bit of the register. Four-code signaling substitution is done by substituting the first two signaling bits of the four with the SIG4-A bit and the last two signaling bits of the four with the SIG4-B bit of the RSSR register. Sixteen-code signaling substitution is implemented by substituting the four signaling bits with the content of SIG16-A, SIG16-B, SIG16-C, and SIG16-D bits of RSSR register respectively.

The table below shows configurations of the Receive Signaling Substitution Control [1:0] bits of the Receive Signaling Control Register.

RECEIVE SIGNALING CONTROL REGISTER (RSCR) (INDIRECT ADDRESS = 0XN2H, 0X40H - 0X5FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Receive Signaling Substitution Control	R/W	00 - The received signaling bits are replaced by all ones and send to the external equipment. 01 - Two-code signaling substitution is applied to the received signaling bits. The replaced signaling information is sent to the external equipment. 10 - Four-code signaling substitution is applied to the received signaling bits. The replaced signaling information is sent to the external equipment. 11 - Sixteen-code signaling substitution is applied to the received signaling bits. The replaced signaling information is sent to the external equipment.

12.5 How to Configure the Framer to Detect Alarms and Error Conditions

The XRT84L38 T1/J1/E1 Octal Framer can be configured to monitor quality of received E1 frames. It can generate error indicators if the local receive framer has received error frames from the remote terminal. If corresponding interrupt is enabled, the local microprocessor operation is interrupted by these error conditions. Upon microprocessor interruption, the user can intervene by looking into the error conditions.

At the same time, the user can configure the XRT84L38 framer to receive alarms and error indications to remote terminal. Different alarms and error indications will be received depending on the error condition.

The section below gives a brief discussion of the error conditions that can be detected by the XRT84L38 framer and error indications that will be generated.

12.5.1 How to configure the framer to detect AIS Alarm

Transmission of Alarm Indication Signal (AIS) or Blue Alarm by the intermediate node indicates that the equipment is still functioning but unable to offer services. It is an all ones (except for framing bits) pattern which can be used by the equipment further down the line to maintain clock recovery and timing synchronization.

The XRT84L38 framer can detect three types of AIS in E1 mode:

- Framed AIS
- Unframed AIS
- AIS16

Unframed AIS is an all ones pattern. If unframed AIS is sent, the equipment further down the line will be able to maintain timing synchronization and be able to recover clock from the received AIS signal. However, due to the lack of framing bits, the equipment farther down the line will not be able to maintain frame synchronization and will declare Loss of Frame (LOF).

On the other hand, the payload portion of a framed AIS pattern is all ones. However, a framed AIS pattern still has correct framing bits. Therefore, the equipment further down the line can still maintain frame synchronization as well as timing synchronization. In this case, no LOF or Red alarm will be declared.

"AIS16" is an AIS alarm that only supported in E1 framing format. It is an all ones pattern in time slot 16 of each E1 frame. As we mentioned before, time slot 16 is usually used for signaling and data link in E1, therefore, an "AIS16" alarm is transmitted by the intermediate node to indicate that the data link channel is having a problem. Since all the other thirty one time slots are still transmitting normal data (that is, framing information and PCM data), therefore, the equipment further down the line can still maintain frame synchronization, timing synchronization as well as receiving PCM data. In this case, no LOF or Red alarm will be declared by the equipments further down the line. However, a CAS Multi-frame Yellow Alarm will be sent by the equipment further down the line to indicate the loss of CAS Multi-frame alignment.

The Alarm indication logic within the Receive Framer block of the XRT84L38 framer monitors the incoming E1 frames for AIS (both framed and unframed) and AIS16 errors.

AIS alarm condition are detected and declared according to the following procedure:

1. The incoming E1 frames are monitored for AIS detection. AIS detection is defined as an unframed or framed pattern with less than three zeros in two consecutive frames. In the case of framed AIS, time slot 0 is excluded.
2. An AIS detection counter within the Receive Framer block of the XRT84L38 counts the occurrences of AIS detection over a 4 ms interval. It will indicate a valid AIS flag when thirteen or more of a possible sixteen AIS are detected.
3. Each 4 ms interval with a valid AIS flag increments a flag counter which declares AIS alarm when 25 valid flags have been collected.

Therefore, AIS condition has to be persisted for 104 ms before AIS alarm condition is declared by the XRT84L38 framer.

If there is no valid AIS flag over a 4ms interval, the Alarm indication logic will decrement the flag counter. The AIS alarm is removed when the counter reaches 0. That is, AIS alarm will be removed if in over 104 ms, there is no valid AIS flag.

AIS16 alarm condition are detected and declared according to the following procedure:

1. The incoming E1 frames are monitored for AIS16 detection. AIS16 detection is defined as two consecutive all ones time slot 16 bytes while CAS Multi-frame alignment pattern is missing or CAS Multi-frame is out of synchronization.
2. An AIS16 detection counter within the Receive Framer block of the XRT84L38 counts the occurrences of AIS16 detection.
3. Each valid AIS flag increments a flag counter which declares AIS alarm when 22 valid flags have been collected.

If there is no valid AIS16 flag, the Alarm indication logic will decrement the flag counter. The AIS16 alarm is removed when the counter reaches 0.

The Alarm Indication Signal Detection Select [1:0] bits of the Alarm Generation Register (AGR) enable the three types of AIS detection that are supported by the XRT84L38 framer. The table below shows configurations of the Alarm Indication Signal Detection Select [1:0] bits of the Alarm Generation Register (AGR).

ALARM GENERATION REGISTER (AGR) (INDIRECT ADDRESS = 0XN0H, 0X08H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	AIS Detection Select	R/W	00 - AIS alarm detection is disabled. 01 - Detection of unframed AIS alarm of all ones pattern is enabled. 10 - Detection of AIS16 alarm is enabled. 11 - Detection of framed AIS alarm of all ones pattern except for framing bits is enabled.

If detection of unframed or framed AIS alarm is enabled by the user and if AIS is present in the incoming E1 frame, the XRT84L38 framer can generate a Receive AIS State Change interrupt associated with the setting of Receive AIS State Change bit of the Alarm and Error Status Register to one.

To enable the Receive AIS State Change interrupt, the Receive AIS State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) have to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive AIS State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (INDIRECT ADDRESS = 0XNAH, 0X03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive AIS State Change Interrupt Enable	R/W	0 - The Receive AIS State Change interrupt is disabled. 1 - The Receive AIS State Change interrupt is enabled.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and AIS is present in the incoming E1 frame, the XRT84L38 framer will declare AIS by doing the following:

- Set the read-only Receive AIS State bit of the Alarm and Error Status Register (AESR) to one indicating there is AIS alarm detected in the incoming E1 frame.
- Set the Receive AIS State Change bit of the Alarm and Error Status Register to one indicating there is a change in state of AIS. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive AIS State Change status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (INDIRECT ADDRESS = 0XNAH, 0X02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive AIS State Change	RUR / WC	0 - There is no change of AIS state in the incoming E1 payload data. 1 - There is change of AIS state in the incoming E1 payload data.

The Receive AIS State bit of the Alarm and Error Status Register (AESR), on the other hand, is a read-only bit indicating there is AIS alarm detected in the incoming E1 frame.

The table below shows the Receive AIS State status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (INDIRECT ADDRESS = 0XNAH, 0X02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Receive AIS State	R	0 - There is no AIS alarm condition detected in the incoming E1 payload data. 1 - There is AIS alarm condition detected in the incoming E1 payload data.

12.5.2 How to configure the framer to detect Red Alarm

The Alarm indication logic within the Receive Framer block of the XRT84L38 framer monitors the incoming E1 frames for red alarm or Loss of Frame (LOF) condition. Red alarm condition are detected and declared according to the following procedure:

1. The red alarm is detected by monitoring the occurrence of Loss of Frame (LOF) over a 4 ms interval.
2. An LOF valid flag will be posted on the interval when one or more LOF occurred during the interval.
3. Each interval with a valid LOF flag increments a flag counter which declares RED alarm when 25 valid intervals have been accumulated.
4. An interval without valid LOF flag decrements the flag counter. The Red alarm is removed when the counter reaches zero.

If LOF condition is present in the incoming E1 frame, the XRT84L38 framer can generate a Receive Red Alarm State Change interrupt associated with the setting of Receive Red Alarm State Change bit of the Alarm and Error Status Register to one.

To enable the Receive Red Alarm State Change interrupt, the Receive Red Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Red Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (INDIRECT ADDRESS = 0XNAH, 0X03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Red Alarm State Change Interrupt Enable	R/W	0 - The Receive Red Alarm State Change interrupt is disabled. No Receive Loss of Frame (RxLOF) interrupt will be generated upon detection of LOF condition. 1 - The Receive Red Alarm State Change interrupt is enabled. Receive Loss of Frame (RxLOF) interrupt will be generated upon detection of LOF condition.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and Red Alarm is present in the incoming E1 frame, the XRT84L38 framer will declare Red Alarm by doing the following:

- Set the read-only Receive Red Alarm State bit of the Alarm and Error Status Register (AESR) to one indicating there is Red Alarm detected in the incoming E1 frame.
- Set the Receive Red Alarm State Change bit of the Alarm and Error Status Register to one indicating there is a change in state of Red Alarm. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Red Alarm State Change status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (INDIRECT ADDRESS = 0XNAH, 0X02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Receive Red Alarm State Change	RUR / WC	0 - There is no change of Red Alarm state in the incoming E1 payload data. 1 - There is change of Red Alarm state in the incoming E1 payload data.

The Receive Red Alarm State bit of the Alarm and Error Status Register (AESR), on the other hand, is a read-only bit indicating there is Red Alarm detected in the incoming E1 frame.

The table below shows the Receive Red Alarm State status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (INDIRECT ADDRESS = 0XNAH, 0X02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Red Alarm State	R	0 - There is no Red Alarm condition detected in the incoming E1 payload data. 1 - There is Red Alarm condition detected in the incoming E1 payload data.

12.5.3 How to configure the framer to detect Yellow Alarm

The Alarm indication logic within the Receive Framer block of the XRT84L38 framer monitors the incoming E1 frames for Yellow Alarm condition. The yellow alarm is detected and declared according to the following procedure:

1. Monitor the occurrence of Yellow Alarm pattern over a 4 ms interval. A YEL valid flag will be posted on the interval when Yellow Alarm pattern occurred during the interval.
2. Each interval with a valid YEL flag increments a flag counter which declares YEL alarm when 80 valid intervals have been accumulated.
3. An interval without valid YEL flag decrements the flag counter. The YEL alarm is removed when the counter reaches zero.

If Yellow Alarm condition is present in the incoming E1 frame, the XRT84L38 framer can generate a Receive Yellow Alarm State Change interrupt associated with the setting of Receive Yellow Alarm State Change bit of the Alarm and Error Status Register to one.

To enable the Receive Yellow Alarm State Change interrupt, the Receive Yellow Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Yellow Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (INDIRECT ADDRESS = 0XNAH, 0X03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	Receive Yellow Alarm State Change Interrupt Enable	R/W	0 - The Receive Yellow Alarm State Change interrupt is disabled. Any state change of Receive Yellow Alarm will not generate an interrupt. 1 - The Receive Yellow Alarm State Change interrupt is enabled. Any state change of Receive Yellow Alarm will generate an interrupt.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and Yellow Alarm is present in the incoming E1 frame, the XRT84L38 framer will declare Yellow Alarm by doing the following:

- Set the Receive Yellow Alarm State Change bit of the Alarm and Error Status Register to one indicating there is a change in state of Yellow Alarm. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Yellow Alarm State Change status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (INDIRECT ADDRESS = 0XNAH, 0X02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	Receive Yellow Alarm State Change	RUR / WC	0 - There is no change of Yellow Alarm state in the incoming E1 payload data. 1 - There is change of Yellow Alarm state in the incoming E1 payload data.

12.5.4 How to configure the framer to detect CAS Multi-frame Yellow Alarm

The Alarm indication logic within the Receive Framer block of the XRT84L38 framer monitors the incoming E1 frames for CAS Multi-frame Yellow Alarm condition. The CAS Multi-frame Yellow Alarm is detected and declared according to the following procedure:

1. Monitor the occurrence of CAS Multi-frame Yellow Alarm pattern over a 4 ms interval. An MYEL valid flag will be posted on the interval when CAS Multi-frame Yellow Alarm pattern occurred during the interval.
2. Each interval with a valid MYEL flag increments a flag counter which declares MYEL alarm when 80 valid intervals have been accumulated.
3. An interval without valid MYEL flag decrements the flag counter. The MYEL alarm is removed when the counter reaches zero.

If CAS Multi-frame Yellow Alarm condition is present in the incoming E1 frame, the XRT84L38 framer can generate a Receive CAS Multi-frame Yellow Alarm State Change interrupt associated with the setting of Receive CAS Multi-frame Yellow Alarm State Change bit of the Alarm and Error Status Register to one.

To enable the Receive CAS Multi-frame Yellow Alarm State Change interrupt, the Receive CAS Multi-frame Yellow Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive CAS Multi-frame Yellow Alarm State Change Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (INDIRECT ADDRESS = 0XNAH, 0X03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive CAS Multi-frame Yellow Alarm State Change Interrupt Enable	R/W	0 - The Receive CAS Multi-frame Yellow Alarm State Change interrupt is disabled. Any state change of Receive CAS Multi-frame Yellow Alarm will not generate an interrupt. 1 - The Receive CAS Multi-frame Yellow Alarm State Change interrupt is enabled. Any state change of Receive CAS Multi-frame Yellow Alarm will generate an interrupt.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and CAS Multi-frame Yellow Alarm is present in the incoming E1 frame, the XRT84L38 framer will declare CAS Multi-frame Yellow Alarm by doing the following:

- Set the Receive CAS Multi-frame Yellow Alarm State Change bit of the Alarm and Error Status Register to one indicating there is a change in state of CAS Multi-frame Yellow Alarm. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive CAS Multi-frame Yellow Alarm State Change status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (INDIRECT ADDRESS = 0XNAH, 0X02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive CAS Multi-frame Yellow Alarm State Change	RUR / WC	0 - There is no change of CAS Multi-frame Yellow Alarm state in the incoming E1 payload data. 1 - There is change of CAS Multi-frame Yellow Alarm state in the incoming E1 payload data.

12.5.5 How to configure the framer to detect Bipolar Violation

The line coding for the E1 signal should be bipolar. That is, a binary "0" is received as zero volts while a binary "1" is received as either a positive or negative pulse, opposite in polarity to the previous pulse. A Bipolar Violation or BPV occurs when the alternate polarity rule is violated. The Alarm indication logic within the Receive Framer block of the XRT84L38 framer monitors the incoming E1 frames for Bipolar Violations.

If a Bipolar Violation is present in the incoming E1 frame, the XRT84L38 framer can generate a Receive Bipolar Violation interrupt associated with the setting of Receive Bipolar Violation bit of the Alarm and Error Status Register to one.

To enable the Receive Bipolar Violation interrupt, the Receive Bipolar Violation Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Bipolar Violation Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (INDIRECT ADDRESS = 0XNAH, 0X03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Bipolar Violation Interrupt Enable	R/W	0 - The Receive Bipolar Violation interrupt is disabled. Occurrence of one or more bipolar violations will not generate an interrupt. 1 - The Receive Bipolar Violation interrupt is enabled. Occurrence of one or more bipolar violations will generate an interrupt.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and one or more Bipolar Violations are present in the incoming E1 frame, the XRT84L38 framer will declare Receive Bipolar Violation by doing the following:

- Set the Receive Bipolar Violation bit of the Alarm and Error Status Register to one indicating there are one or more Bipolar Violations. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Bipolar Violation status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (INDIRECT ADDRESS = 0XNAH, 0X02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	Receive Bipolar Violation State Change	RUR / WC	0 - There is no change of Bipolar Violation state in the incoming E1 payload data. 1 - There is change of Bipolar Violation state in the incoming E1 payload data.

12.5.6 How to configure the framer to detect Loss of Signal

A Loss of Signal or LOS occurs when neither RPOS nor RNEG inputs of the framer receives a high level input for 32 consecutive bit times. The Alarm indication logic within the Receive Framer block of the XRT84L38 framer monitors the incoming E1 frames for Loss of Signal conditions. If used in conjunction with EXAR LIUs, for example, the XRT83L3x family, the XRT84L38 framer also declares LOS when the Receive LOS (RxLOS) input pin is pulled HIGH.

The removal of LOS condition is through detection of 12.5% ones over 32 consecutive bits. In the other words, XRT84L38 framer will remove LOS alarm when there is no 4 consecutive zeros received.

NOTE: *The implementation of LOS detection and removal only apply to B8ZS coded bipolar inputs.*

If Loss of Signal condition is present in the incoming E1 frame, the XRT84L38 framer can generate a Receive Loss of Signal interrupt associated with the setting of Receive Loss of Signal bit of the Alarm and Error Status Register to one.

To enable the Receive Loss of Signal interrupt, the Receive Loss of Signal Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER) has to be set to one. In addition, the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Loss of Signal Interrupt Enable bit of the Alarm and Error Interrupt Enable Register (AEIER).

ALARM AND ERROR INTERRUPT ENABLE REGISTER (AEIER) (INDIRECT ADDRESS = 0XNAH, 0X03H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Loss of Signal Interrupt Enable	R/W	0 - The Receive Loss of Signal interrupt is disabled. Occurrence of Loss of Signals will not generate an interrupt. 1 - The Receive Loss of Signal interrupt is enabled. Occurrence of Loss of Signals will generate an interrupt.

The table below shows configurations of the Alarm and Error Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X01H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Alarm and Error Interrupt Enable	R/W	0 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is disabled. 1 - Every interrupt generated by the Alarm and Error Interrupt Status Register (AEISR) is enabled.

When these interrupt enable bits are set and one or more Loss of Signals are present in the incoming E1 frame, the XRT84L38 framer will declare Receive Loss of Signal by doing the following:

- ·Set the Receive Loss of Signal bit of the Alarm and Error Status Register to one indicating there is one or more Loss of Signals. This status indicator is valid until the Framer Interrupt Status Register is read.

Reading this register clears the associated interrupt if Reset-Upon-Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Loss of Signal status bits of the Alarm and Error Status Register.

ALARM AND ERROR STATUS REGISTER (AESR) (INDIRECT ADDRESS = 0XNAH, 0X02H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
4	Receive Loss of Signal State	RUR / WC	0 - There is no change of Loss of Signal state in the incoming E1 payload data. 1 - There is change of Loss of Signal state in the incoming E1 payload data.

13.0 DS1 HDLC CONTROLLER BLOCK

13.1 DS1 TRANSMIT HDLC CONTROLLER BLOCK

13.1.1 Description of the DS1 Transmit HDLC Controller Block

XRT84L38 allows user to insert data link information to outbound DS1 frames. The data link information in DS1raming format mode can be inserted from:

- DS1 Transmit Overhead Input Interface Block
- DS1 Transmit HDLC Controller
- DS1 Transmit Serial Input Interface

The Transmit Data Link Source Select [1:0] bits, within the Transmit Data Link Select Register (TSDLSR) determine source of the data link bits (Facility Data Link (FDL) bits in ESF framing format mode, Signaling Framing (Fs) bits in SLC®96 framing format mode and Remote Signaling (R) bits in T1DM framing format mode) to be inserted into the outgoing DS1 frames.

The table below shows configuration of the Transmit Data Link Source Select [1:0] bits of the Transmit Data Link Select Register (TSDLSR).

TRANSMIT DATA LINK SELECT REGISTER (TSDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Transmit Data Link Source Select [1:0]	R/W	00 - The data link bits are inserted into the framer through the Transmit HDLC Controller. 01 - The data link bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins. 10 - The data link bits are inserted into the framer through the Transmit Overhead Input Interface via the TxOH_n pins. 11 - The data link bits are forced into 1.

If the Transmit Data Link Source Select bits of the Transmit Data Link Select Register are set to 00, the Transmit HDLC Controller block becomes input source of the data link bits in outgoing DS1 frames.

Each of the eight framers within the XRT84L38 device contains a DS1 Transmit High-level Data Link Controller (HDLC) block. The function of this block is to provide a serial data link channel in DS1 mode through the following:

- Facility Data Link (FDL) bits in ESF framing format mode
- Signaling Framing (Fs) bits in SLC®96 framing format mode
- Remote Signaling (R) bits in T1DM framing format mode
- D or E signaling timeslot channel

Data link bits are automatically inserted into the Facility Data Link (FDL) bits in ESF framing format mode, Signaling Framing (Fs) bits in SLC®96 framing format mode and Remote Signaling (R) bits in T1DM framing format mode or forced to 1 by the framer. Additionally, XRT84L38 allows the user to define any one of ones of the twenty-four DS0 timeslots to be D or E channel. We will discuss how to configure XRT84L38 to transmit data link information through D or E channels in later section.

The DS1 Transmit HDLC Controller block contains three major functional modules associated with DS1 framing formats. They are the:

- SLC®96 Data Link Controller
- LAPD Controller
- Bit-Oriented Signaling Processor.

There are two 96-byte transmit message buffers in shared memory for each of the eight framers to transmit data link information. When one message buffer is filled up, the Transmit HDLC Controller automatically switches to the next message buffer to load data link messages. These two message buffers ping-pong among each other for data link message transmission.

The SLC®96 Enable bit and the LAPD Enable bit of the Data Link Control Register (DLCR) determines which one of the three functions is performed by the Transmit HDLC Controller block. The table below shows configuration of the SLC®96 Enable bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) INDIRECT ADDRESS = 0XN0H, 0X13H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	SLC®96 Enable	R/W	0 - In SLC®96 framing mode, the data link transmission is disabled. The framer transmits the regular SF framing bits. In ESF framing mode, the framer transmits regular ESF framing bits and Facility Data Link (FDL) bits. 1 - In SLC®96 framing mode, the data link transmission is enabled. In ESF framing mode, the framer transmits SLC®96-like message in the Facility Data Link bits.

The table below shows configuration of the LAPD Enable bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (INDIRECT ADDRESS = 0XN0H, 0X13H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	LAPD Enable	R/W	0 - The Transmit HDLC Controller will send out Bit-Oriented Signaling (BOS) message. 1 - The Transmit HDLC Controller will send out LAPD protocol or so-called Message-Oriented Signaling (MOS) message.

13.1.2 How to configure XRT84L38 to transmit data link information through D or E Channels

The XRT84L38 can configure any one or ones of the twenty-four DS0 channels to be D or E channels. D channel is used primarily for data link applications. E channel is used primarily for signaling for circuit switching with multiple access configurations.

The Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of each channel determine whether that particular channel is configured as D or E channel. These bits also determine what type of data or signaling conditioning is applied to each channel.

TRANSMIT CHANNEL CONTROL REGISTER (TCCR) (INDIRECT ADDRESS = 0XN2H, 0X00H - 0X1FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-0	Transmit Data Conditioning Select	R/W	1111 - This channel is configured as D or E timeslot.

If the Transmit Data Conditioning Select [3:0] bits of the Transmit Channel Control Register of a particular timeslot are set to 1111, that timeslot is configured as a D or E timeslot.

Any D or E timeslot can be configured to take data link information from the following sources:

- DS1 Transmit Overhead Output Interface Block
- DS1 Transmit HDLC Controller Block
- DS1 Transmit Serial Output Interface Block
- DS1 Transmit Fractional Input Interface Block

The Transmit D or E Channel Source Select [1:0] bits of the Transmit Data Link Select Register (TSDLSR) determines which one of the above-mentioned modules to be input sources of D or E timeslot. The table below

shows configuration of the Transmit D or E Channel Source Select [1:0] bits of the Transmit Data Link Select Register (TSDLSR).

TRANSMIT DATA LINK SELECT REGISTER (TSDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Transmit D or E Channel Source Select [1:0]	R/W	00 - The data link bits are inserted into the D or E channel through the Transmit Serial Data input Interface via the TxSer_n pins. 01 - The data link bits are inserted into the D or E channel through the Transmit HDLC Controller. 10 - The data link bits are inserted into the D or E channel through the Transmit Serial Data input Interface via the TxSer_n pins. 11 - The data link bits are inserted into the D or E channel through the Transmit Fractional T1 Input Interface via the TxFrT1_n pins.

For the Transmit HDLC Controller to be input source of D or E channel, the Transmit D or E Channel Source Select [1:0] bits of the Transmit Data Link Select Register has to be set to 01.

13.1.3 Transmit BOS (Bit Oriented Signaling) Processor

The Transmit BOS Processor handles transmission of BOS messages through the DS1 data link channel. It determines how many repetitions a certain BOS message will be transmitted. It also inserts BOS IDLE flag sequence and ABORT sequence to be transmitted on the data link channel. In the later sections, we will discuss BOS message format and how to transmit BOS message.

13.1.3.1 Description of BOS

Bit-Oriented Signaling message is a sixteen-bit pattern carries the form of:

(0d5d4d3d2d1d0011111111)

Where d5 is the MSB and d0 is the LSB. The rightmost "1" is transmitted first. Bit-Oriented Signaling message is classified into the following two groups:

- Priority Codeword Message
- Command and Response Information

Priority Codeword message is preemptive and has the highest priority among all data link information. Priority Codeword information indicates a condition that is affecting the quality of service and thus shall be transmitted until the condition no longer exists. The duration of transmission should not be less than one second. Priority codeword information may be interrupted by software for 100 milliseconds to send maintenance commands with a minimum interval of one second between interruptions. Yellow alarm (00000000 11111111) is the only priority message defined in standard.

Command and response information is transmitted to perform various functions. The BOS Processor send command and response message by transmitting a minimum of 10 repetitions of the appropriate codeword pattern. Command and response data transmission initiates action at the remote end, while the remote end will respond by sending Bit-Oriented response message to acknowledge the received commands. The activation and deactivation of line loop-back and payload loop-back functions are this type of signal.

13.1.3.2 How to configure the BOS Processor Block to transmit BOS

This section describes how to configure the BOS Processor Block to transmit BOS message in a step-by-step basis.

13.1.3.2.1 Step 1: Find out the next available transmit data link buffer

To transmit a bit-oriented signal, a repeating message is sent of the form (0d5d4d3d2d1d0011111111), where the "d5d4d3d2d1d0" represents a six-bit message. The user is recommended to read Transmit Data Link Byte Count Register for next available transmit data link buffer number.

The table below shows how content of the Buffer Enable bit of the Transmit Data Link Byte Count Register (TDLBCR) determines what the next available transmit data link buffer number is.

TRANSMIT DATA LINK BYTE COUNT REGISTER (TDLBCR) (INDIRECT ADDRESS = 0XN0H, 0X14H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Buffer Select	R	0 - The next available transmit data link buffer for sending out BOS or MOS message is Buffer 0. 1 - The next available transmit data link buffer for sending out BOS or MOS message is Buffer 1.

13.1.3.2.2 Step 2: Write BOS Message into transmit data link buffer

After finding out the next available transmit data link buffer, the user should write the eight bits message that are to be transmitted in the form (0d5d4d3d2d1d00) to the first location of the next available transmit data link buffer. The writing of these buffers is through the LAPD Buffer 0 indirect data registers and the LAPD Buffer1 indirect data registers. LAPD Buffer 0 and 1 indirect data registers have addresses 0xn6H and 0xn7H respectively. There is no indirect address register for transmit data link buffer 0 and 1.

A microcontroller WRITE access to the LAPD Buffer indirect data registers will access the transmit data link buffer and a microcontroller READ will access the receive data link buffers. The very first WRITE access to the LAPD Buffer indirect data register will always be direct to location 0 within the transmit data link buffer.

For example, if the BOS Message to be sent is (101011) and the next available transmit data link buffer of Channel n is 1. The user should write pattern (01010110) into transmit data link buffer 1 of Channel n. The following microprocessor access to the framer should be done:

WR n7H 56H

13.1.3.2.3 Step 3: Program BOS Message transmission repetitions

The user should program the value of message transmission repetitions into the Transmit Data Link Byte Count Register. The framer will transmit the BOS message the same number of times as was stored in the Transmit Data Link Byte Count Register (TDLBCR) before generating the Transmit End of Transfer (TxEOT) interrupts. If the value stored inside the Transmit Data Link Byte Count Register (TDLBCR) is set to 0, the message will be transmitted indefinitely and no Transmit End of Transfer interrupt will be generated.

The table below shows configurations of the Transmit Data Link Byte Count [6:0] bits the Transmit Data Link Byte Count Register (TDLBCR).

TRANSMIT DATA LINK BYTE COUNT REGISTER (TDLBCR) (INDIRECT ADDRESS = 0XN0H, 0X14H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6-0	Transmit Data Link Byte Count [6:0]	R/W	Value of these bits determines how many times a BOS message pattern will be transmitted by the framer before generating the Transmit End of Transfer (TxEOT) interrupt. ***NOTE:*** *If these bits are set to 0, the BOS message will be transmitted indefinitely and no Transmit End of Transfer interrupts will be generated.*

13.1.3.2.4 Step 4: Configure BOS Message transmission control bits

Configuration of the Data Link Control Register determines whether the BOS Processor will insert IDLE flag character or ABORT sequence to the data link channel. It also determines how the transition between MOS mode to BOS mode is done.

If the IDLE Insertion bit of the Data Link Control Register is set, repeated flags of value 0x7E are transmitted as soon as the current operation is finished (defined by the value in Transmit Data Link Byte Count Register).

However, if the Transmit Data Link Byte Count value is zero, the framer will not force a flag sequence on to the data link channel.

The table below shows configurations of the IDLE Insertion bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (INDIRECT ADDRESS = 0XN0H, 0X13H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	IDLE Insertion	R/W	0 - No flag sequence is sent on the data link channel. 1 - The framer forces a flag sequence of value 0x7E onto the data link channel.

If the ABORT bit of the Data Link Control Register is set, a BOS abort sequence (9 consecutive ones) is transmitted on the data link channel following by all-one transmission. In other words, all data link bits will be set to 1 after the transmission of the current message byte.

The table below shows configurations of the ABORT bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (INDIRECT ADDRESS = 0XN0H, 0X13H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	ABORT	R/W	0 - No ABORT sequence is sent on the data link channel. 1 - The framer forces an ABORT sequence of pattern (111111111) onto the data link channel. All data link bits will be set to 1 after sending the ABORT sequence.

Switching the data link channel from MOS mode to BOS mode while a message is being transmitted will interrupt the message after the octet in progress is transmitted. If the MOS ABORT bit of the Data Link Control Register is set, a MOS ABORT sequence (a zero followed by 7 ones) will be inserted before switching. Switching the data link from BOS to LAPD will not take place until the current operation completes if Transmit BOS byte count is not set to zero initially. If the Transmit BOS byte count value is set to zero, the transition from BOS mode to MOS mode will take place right after finishing the current message octet.

The table below shows configurations of the MOS ABORT bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (INDIRECT ADDRESS = 0XN0H, 0X13H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	MOS ABORT	R/W	0 - The framer forces an MOS ABORT sequence of one zero and seven ones (01111111) onto the data link channel during the transition from MOS mode to BOS mode. 1 - No MOS ABORT sequence is sent on the data link channel during the transition from MOS mode to BOS mode.

13.1.3.2.5 Step 5: Enable transmit BOS message interrupts

The BOS Processor can generate a couple of interrupts indicating the status of BOS message transmission to the microprocessor. These are the Transmit Start of Transfer (TxSOT) interrupt and the Transmit End of Transfer (TxEOT) interrupt.

To enable these interrupts, the Transmit Start of Transfer Enable bit and the Transmit End of Transfer Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Transmit Start of Transfer Enable bit and the Transmit End of Transfer Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (INDIRECT ADDRESS = 0XNAH, 0X07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Transmit Start of Transfer Enable	R/W	0 - The Transmit Start of Transfer interrupt is disabled. 1 - The Transmit Start of Transfer interrupt is enabled.
4	Transmit End of Transfer Enable	R/W	0 - The Transmit End of Transfer interrupt is disabled. 1 - The Transmit End of Transfer interrupt is enabled.

The table below shows configurations of the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	HDLC Controller Interrupt Enable	R/W	0 - Every interrupt generated by the HDLC Controller is disabled. 1 - Every interrupt generated by the HDLC Controller is enabled.

When these interrupt enable bits are set and the BOS message is transmitted to the data link channel, the BOS Processor changes the Transmit Start of Transfer and Transmit End of Transfer status bits of the Data Link Status Register (DLSR). These two status indicators are valid until the Data Link Status Register is read. Reading these register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Transmit Start of Transfer and Transmit End of Transfer status bits of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (INDIRECT ADDRESS = 0XNAH, 0X06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Transmit Start of Transfer	RUR / WC	0 - There is no data link message to be sent to the data link channel. 1 - The HDLC Controller will send a data link message to the data link channel.
4	Transmit End of Transfer	RUR / WC	0 - No data link message was sent to the data link channel. 1 - The HDLC Controller finished sending a data link message to the data link channel.

13.1.3.2.6 Step 6: BOS message transmission

A zero is then written into the LAPD enable bit of Data Link Control Register, which sets the transmitter to Bit-Oriented mode and kicks off the transmission process. The LAPD Controller latches these control bits of the Data Link Control Register and send a Transmit Start of Transfer interrupt (TxSOT) to the microprocessor to indicate that a BOS message will be send. After the required number of times of BOS message is sent, the LAPD Controller generates an Transmit End of Transfer interrupt (TxEOT) to the microprocessor to indicate that the BOS message transmission comes to an end.

The table below shows configurations of the LAPD Enable bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (INDIRECT ADDRESS = 0XN0H, 0X13H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	LAPD Enable	R/W	0 - The Transmit HDLC Controller will send out Bit-Oriented Signaling (BOS) message. 1 - The Transmit HDLC Controller will send out LAPD protocol or so-called Message-Oriented Signaling (MOS) message.

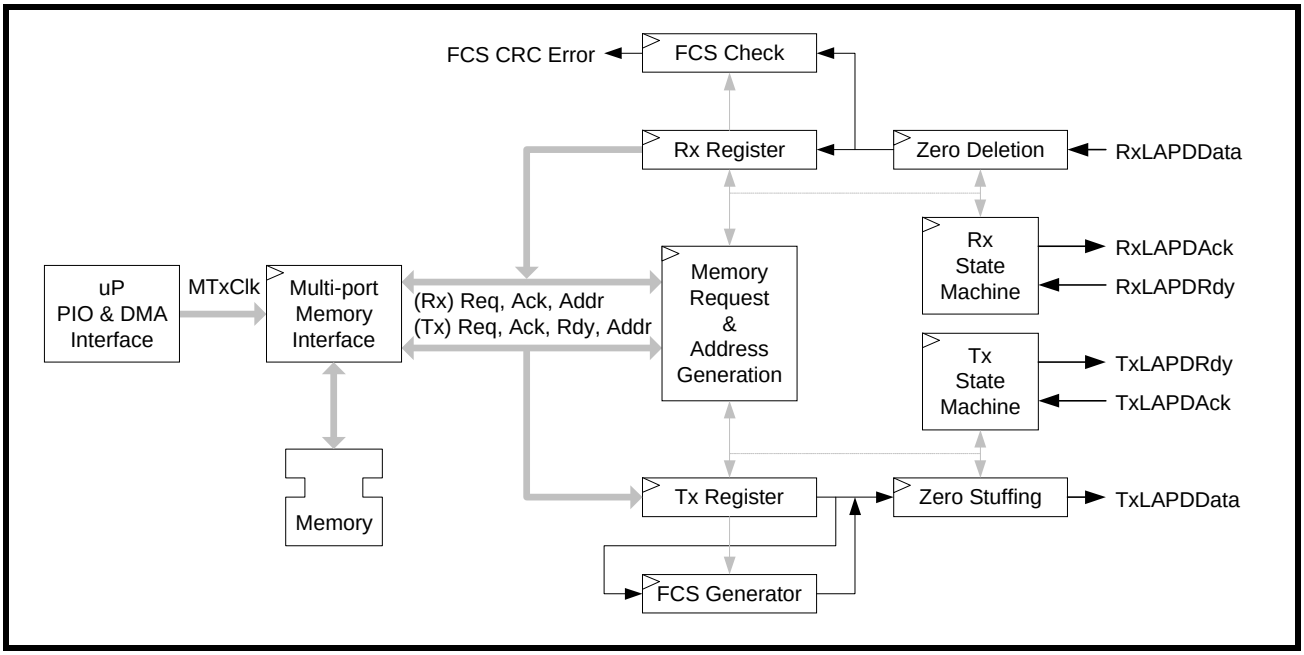
13.1.4 Transmit MOS (Message Oriented Signaling) or LAPD Controller

The Transmit LAPD controller implements the Message-Oriented protocol based on ITU Recommendation Q.921 Link Access Procedures on the D-channel (LAPD) type of protocol. It provides the following functions:

- Zero stuffing
- T1/E1 transmitter interface
- Transmit message buffer access
- Frame check sequence generation
- IDLE flag insertion
- ABORT sequence generation

Two 96-byte buffers in shared memory are allocated for LAPD transmitter to reduce the frequency of microprocessor interrupts and alleviate the response time requirement for microprocessor to handle each interrupt. There are no restrictions on the length of the message. However the 96-byte buffer is deep enough to hold one entire LAPD path or test signal identification message. Figure 127 depicts the block diagram of both transmit and receive LAPD controller.

FIGURE 127. LAPD CONTROLLER



In the later sections, we will briefly discuss MOS message format and how to configure the LAPD Controller to transmit MOS message.

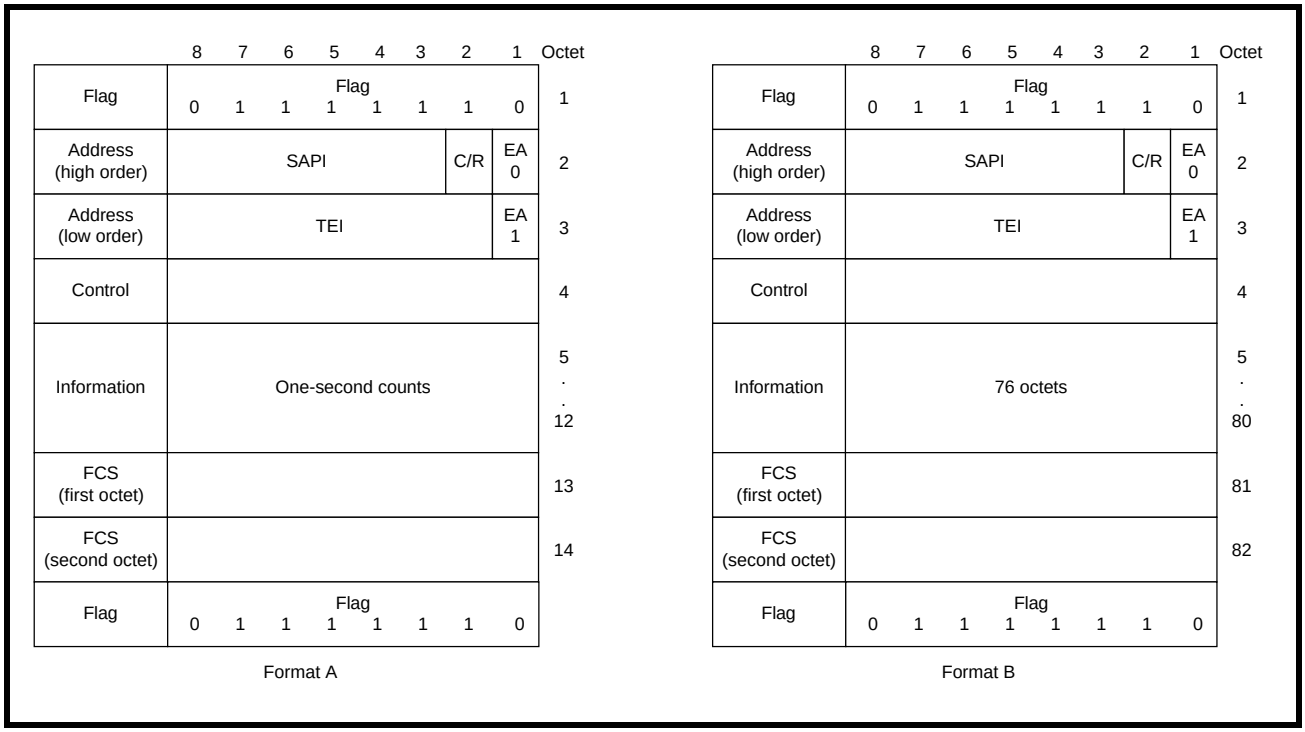
13.1.4.1 Discussion of MOS

Message-Oriented signals (MOS) sent by the transmit LAPD Controller are messages conforming to ITU Recommendation Q.921 LAPD protocol as defined below.

Two types of Message-Oriented signals are defined. One is a periodic performance report generated by the source or sink T1/E1 terminals as defined by ANSI T1.403. The other is a path or test signal identification message that may be optionally generated by a terminal or intermediate equipment on a T1/E1 circuit.

Message-oriented signals shall use the frame structure, field definitions and elements of procedure of the LAPD protocol defined in ITU recommendation Q.921 except the address field. Performance information is carried by Message-Oriented signal using LAPD protocol. The message structures of the periodic performance report and path or test signal identification message are shown in Figure 128 in format A and format B respectively.

FIGURE 128. LAPD FRAME STRUCTURE



13.1.4.1.1 Periodic Performance Report

The ANSI T1.403 standard requires that the status of the transmission quality be reported every one-second interval. The one-second timing may be derived from the DS1 signal or from a separate equally accurate (±32ppm) source. The phase of the one-second periods with respect to the occurrence of error events is arbitrary; that is, the one-second timing does not depend on the time of occurrence of any error event. A total of four seconds of information is transmitted so that recovery operations may be initiated in case an error corrupts a message.

Counts of events shall be accumulated in each contiguous one-second interval. At the end of each one-second interval, a modulo-4 counter shall be incremented, and the appropriate performance bits shall be set in bytes 5 and 6 in Format A. These octets and the octets that carry the performance bits of the preceding three one-second intervals form the periodic performance report.

The periodic performance report is made up of 14 bytes of data. Bytes 1 to 4, 13, and 14 are the message header and bytes 5 to 12 contain data regarding the four most-recent one-second intervals. The periodic performance report message uses the SAPI/TEI value of 14.

13.1.4.1.2 Transmission-Error Event

Occurrences of transmission-error events indicate the quality of transmission. The occurrences that shall be detected and reported are:

- CRC Error Event: A CRC-6 error event is the occurrence of a received CRC code that is not identical to the corresponding locally calculated code.
- Severely Errored Framing Event: A severely-errored-framing event is the occurrence of two or more framing-bit-pattern errors within a 3-ms period. Contiguous 3-ms intervals shall be examined. The 3-ms period may coincide with the ESF. The severely-errored-framing event, while similar in form to criteria for declaring a terminal has lost framing, is only designed as a performance indicator; existing terminal out-of-frame criteria will continue to serve as the basis for terminal alarms.
- Frame-Synchronization-Bit Error Event: A frame-synchronization-bit-error event is the occurrence of a received framing-bit-pattern not meeting the severely-errored-framing event criteria.
- Line-Code Violation event: A line-code violation event is a bipolar violation of the incoming data. A line-code violation event for an B8ZS-coded signal is the occurrence of a received excessive zeros (EXZ) or a bipolar violation that is not part of a zero-substitution code.
- Controlled Slip Event: A controlled-slip event is a replication, or deletion, of a T1 frame by the receiving terminal. A controlled slip may occur when there is a difference between the timing of a synchronous receiving terminal and the received signal.

13.1.4.1.3 Path and Test Signal Identification Message

The path identification message is used to identify the path between the source terminal and the sink terminal. The test signal identification message is used by test signal generating equipment. Both identification messages are made up of 82 bytes of data. Byte 1 to 4, 81 and 82 are the message header and bytes 5 to 80 contain six data elements. These messages use the SAPI/TEI value of 15 to differentiate themselves from the performance report message.

13.1.4.1.4 Frame Structure

The message structure of message-oriented signal is shown in Figure 1?2. Two format types are shown in the figure: format A for frames which are sending performance report message and format B for frames which containing a path or test signal identification message. The following abbreviations are used:

- SAPI: Service Access Point Identifier
- C/R: Command or Response
- EA: Extended Address
- TEI: Terminal Endpoint Identifier
- FCS: Frame Check Sequence

13.1.4.1.5 Flag Sequence

All frames shall start and end with the flag sequence consisting of one 0 bit followed by six contiguous 1 bits and one 0 bit. The flag preceding the address field is defined as the opening flag. The flag following the Frame Check Sequence (FCS) field is defined as the closing flag. The closing flag may also serve as the opening flag of the next frame, in some applications. However, all receivers must be able to accommodate receipt of one or more consecutive flags.

13.1.4.1.6 Address Field

The address field consists of two octets. A single octet address field is reserved for LAPB operation in order to allow a single LAPB data link connection to be multiplexed along with LAPD data link connections.

13.1.4.1.7 Address Field Extension bit (EA)

The address field range is extended by reserving bit 1 of the address field octets to indicate the final octet of the address field. The presence of a 1 in bit 1 of an address field octet signals that it is the final octet of the address field. The double octet address field for LAPD operation shall have bit 1 of the first octet set to a 0 and bit 1 of the second octet set to 1.

13.1.4.1.8 Command or Response bit (C/R)

The Command or Response bit identifies a frame as either a command or a response. The user side shall send commands with the C/R bit set to 0, and responses with the C/R bit set to 1. The network side shall do the opposite; That is, commands are sent with C/R bit set to 1, and responses are sent with C/R bit set to 0.

13.1.4.1.9 Service Access Point Identifier (SAPI)

The Service Access Point Identifier identifies a point at which data link layer services are preceded by a data link layer entity type to a layer 3 or management entity. Consequently, the SAPI specifies a data link layer entity type that should process a data link layer frame and also a layer 3 or management entity, which is to receive information carried by the data link layer frame. The SAPI allows 64 service access points to be specified, where bit 3 of the address field octet containing the SAPI is the least significant binary digit and bit 8 is the most significant. SAPI values are 14 and 15 for performance report message and path or test signal identification message respectively.

13.1.4.1.10 Terminal Endpoint Identifier (TEI)

The TEI sub-field allows 128 values where bit 2 of the address field octet containing the TEI is the least significant binary digit and bit 8 is the most significant binary digit. The TEI sub-field bit pattern 111 1111 (=127) is defined as the group TEI. The group TEI is assigned permanently to the broadcast data link connection associated with the addressed Service Access Point (SAP). TEI values other than 127 are used for the point-to-point data link connections associated with the addressed SAP. Non-automatic TEI values (0-63) are selected by the user, and their allocation is the responsibility of the user. The network automatically selects and allocates TEI values (64-126).

13.1.4.1.11 Control Field

The control field identifies the type of frame which will be either a command or response. The control field shall consist of one or two octets. Three types of control field formats are specified: 2-octet numbered information transfer (I format), 2-octet supervisory functions (S format), and single-octet unnumbered information transfers and control functions (U format). The control field for T1/E1 message is categorized as a single-octet unacknowledged information transfer having the value 0x03.

13.1.4.1.12 Frame Check Sequence (FCS) Field

The source of either the performance report or an identification message shall generate the frame check sequence. The FCS field shall be a 16-bit sequence. It shall be the ones complement of the sum (modulo 2) of:

- The remainder of xk (x15 + x14 + x13 + x12 + x11 + x10 + x9 + x8 + x7 + x6 + x5 + x4 + x3 + x2 + x + 1) divided (modulo 2) by the generator polynomial x16 + x12 + x5 + 1, where k is the number of bits in the frame existing between, but not including, the final bit of the opening flag and the first bit of the FCS, excluding bits inserted for transparency, and
- The remainder of the division (modulo 2) by the generator polynomial x16 + x12 + x5 + 1, of the product of x16 by the content of the frame existing between, but not including, the final bit of the opening flag and the first bit of the FCS, excluding bits inserted for transparency.

As a typical implementation at the transmitter, the initial content of the register of the device computing the remainder of the division is preset to all 1s and is then modified by division by the generator polynomial on the address, control and information fields; the ones complement of the resulting remainder is transmitted as the 16-bit FCS.

As a typical implementation at the receiver, the initial content of the register of the device computing the remainder is preset to all 1s. The final remainder, after multiplication by x16 and then division (modulo 2) by the generator polynomial x16 + x12 + x5 + 1 of the serial incoming protected bits and the FCS, will be 0001110100001111 (x15 through x0, respectively) in the absence of transmission errors.

13.1.4.1.13 Transparency (Zero Stuffing)

A transmitting data link layer entity shall examine the frame content between the opening and closing flag sequences, (address, control, information and FCS field) and shall insert a 0 bit after all sequences of five contiguous 1 bits (including the last five bits of the FCS) to ensure that an IDLE flag or an Abort sequence is not simulated within the frame. A receiving data link layer entity shall examine the frame contents between the opening and closing flag sequences and shall discard any 0 bit which directly follows five contiguous 1 bits.

13.1.4.2 How to configure the Transmit HDLC Controller Block to transmit MOS

This section describes how to configure the LAPD Controller Block to transmit MOS message in a step-by-step basis.

13.1.4.2.1 Step 1: Find out the next available transmit data link buffer

To transmit MOS message, the user is recommended to read Transmit Data Link Byte Count Register for next available transmit buffer number.

The table below shows how contents of the Buffer Enable bit of the Transmit Data Link Byte Count Register (TDLBCR) determines what the next available transmit buffer number is.

TRANSMIT DATA LINK BYTE COUNT REGISTER (TDLBCR) (INDIRECT ADDRESS = 0XN0H, 0X14H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Buffer Select	R	0 - The next available transmit buffer for sending out BOS or MOS message is Buffer 0. 1 - The next available transmit buffer for sending out BOS or MOS message is Buffer 1.

13.1.4.2.2 Step 2: Write MOS Message into transmit data link buffer

After finding out the next available transmit buffer, the user should write the entire message data to the available transmit data link buffer via PIO or DMA access. The writing of these buffers is through the LAPD Buffer 0 indirect data registers and the LAPD Buffer1 indirect data registers. LAPD Buffer 0 and 1 indirect data registers have addresses 0xn6H and 0xn7H respectively. There is no indirect address register for transmit data link buffer 0 and 1.

A microcontroller WRITE access to the LAPD Buffer indirect data registers will access the transmit data link buffer and a microcontroller READ will access the receive data link buffers. The very first WRITE access to the LAPD Buffer indirect data register will always be direct to location 0 within the transmit data link buffer. The next WRITE access to the LAPD Buffer indirect data register will be direct to location 1 within the transmit data link buffer and so on, until all 96 bytes of the transmit buffer is filled.

For example, if the first byte of the MOS message to be sent is (01010110) and the next available transmit data link buffer of Channel n is 1. The user should write pattern (01010110) into transmit data link buffer 1 of Channel n. The following microprocessor access to the framer should be done:

WR n7H 56H

The first byte of MOS message is written into location 0 of the transmit data link buffer. If the next byte of the MOS message is (10100101), the user should perform another microprocessor WRITE access:

WR n7H A5H

The second byte of MOS message is written into location 1 of the transmit data link buffer. The WRITE access should be repeated until the entire block of MOS message is written into the transmit buffer or the transmit buffer is completely filled.

13.1.4.2.3 Step 3: Program the Transmit Data Link Byte Count Register

The user should program byte count of the MOS message into the Transmit Data Link Byte Count Register after the whole block of data is present in the buffer memory.

The table below shows configurations of the Transmit Data Link Byte Count [6:0] bits the Transmit Data Link Byte Count Register (TDLBCR).

TRANSMIT DATA LINK BYTE COUNT REGISTER (TDLBCR) (INDIRECT ADDRESS = 0XN0H, 0X14H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6-0	Transmit Data Link Byte Count [6:0]	R/W	Value of these bits determines length of the MOS message pattern to be transmitted by the framer before generating the Transmit End of Transfer (TxEOT) interrupt.

13.1.4.2.4 Step 4: Configure MOS Message transmission control bits

Configuration of the Data Link Control Register determines whether the LAPD Controller will insert IDLE flag character, FCS or ABORT sequence to the data link channel. It also determines how the transition between MOS mode to BOS mode is done.

If the IDLE Insertion bit of the Data Link Control Register is set, repeated flags of value 0x7E are transmitted as soon as the current operation is finished (defined by the value in Transmit Data Link Byte Count Register). The IDLE bit must be set to 1 at the last block of transfer to enable FCS and flag insertion for message completion.

The table below shows configurations of the IDLE Insertion bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (INDIRECT ADDRESS = 0XN0H, 0X13H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	IDLE Insertion	R/W	0 - No flag sequence is sent on the data link channel. 1 - The framer forces a flag sequence of value 0x7E onto the data link channel.

NOTE: *If the entire message is longer than 96-byte in length or more than one full block of message has to be transmitted, the IDLE Insertion bit should not be set to one until the last block of message has to be sent.*

If the FCS Insertion bit of the Data Link Control Register (DLCR) is set to high, the LAPD Controller will calculate and insert the frame check sequence to the last block of the transmitted message.

The table below shows configurations of the FCS Insertion bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (INDIRECT ADDRESS = 0XN0H, 0X13H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	FCS Insertion	R/W	0 - No FCS will be inserted into the last block of the transmitted MOS message. 1 - The LAPD Controller will calculate and insert the FCS into the last block of the transmitted MOS message.

If the FCS is not enabled at the end of a message, the controller will return to sending IDLE flags immediately after the last octet is transmitted. This permits the use of a programmable FCS, which may be used for diagnostic tests or other test applications.

To abort a transmitting message, the LAPD Controller sets the ABORT bit in Data Link Control Register to 1. This bit is cleared after the LAPD transmitter finishes sending the message octet in progress. The transmitter then transmit an ABORT sequence of one zero followed by seven ones (01111111) before goes to idle if the IDLE bit is set. The transmitter will keep transmitting IDLE flag characters until it is instructed otherwise.

The table below shows configurations of the ABORT bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (INDIRECT ADDRESS = 0XN0H, 0X13H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	ABORT	R/W	0 - No ABORT sequence is sent on the data link channel. 1 - The framer forces an ABORT sequence of pattern (111111 10) onto the data link channel. IDLE flag pattern will be transmitted after the ABORT sequence is sent.

Switching the data link channel from MOS mode to BOS mode while a message is being transmitted will interrupt the message after the octet in progress is transmitted. If the MOS ABORT bit of the Data Link Control Register is set, a MOS ABORT sequence (a zero followed by 7 ones) will be inserted before switching. Switching the data link from BOS to LAPD will not take place until the current operation completes if Transmit BOS byte count is not set to zero initially. If the Transmit BOS byte count value is set to zero, the transition from BOS mode to MOS mode will take place right after finishing the current message octet.

The table below shows configurations of the MOS ABORT bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (INDIRECT ADDRESS = 0XN0H, 0X13H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	MOS ABORT	R/W	0 - The framer forces an MOS ABORT sequence of one zero and seven ones [0111 1111] onto the data link channel during the transition from MOS mode to BOS mode. 1 - No MOS ABORT sequence is sent on the data link channel during the transition from MOS mode to BOS mode.

13.1.4.2.5 Step 5: Enable transmit MOS message interrupts

The LAPD Controller can generate a couple of interrupts indicating the status of MOS message transmission to the microprocessor. These are the Transmit Start of Transfer (TxSOT) interrupt and the Transmit End of Transfer (TxEOT) interrupt.

To enable these interrupts, the Transmit Start of Transfer Enable bit and the Transmit End of Transfer Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Transmit Start of Transfer Enable bit and the Transmit End of Transfer Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (INDIRECT ADDRESS = 0XNAH, 0X07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Transmit Start of Transfer Enable	R/W	0 - The Transmit Start of Transfer interrupt is disabled. 1 - The Transmit Start of Transfer interrupt is enabled.
4	Transmit End of Transfer Enable	R/W	0 - The Transmit End of Transfer interrupt is disabled. 1 - The Transmit End of Transfer interrupt is enabled.

The table below shows configurations of the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	HDLC Controller Interrupt Enable	R/W	0 - Every interrupt generated by the HDLC Controller is disabled. 1 - Every interrupt generated by the HDLC Controller is enabled.

When these interrupt enable bits are set and the MOS message is transmitted to the data link channel, the LAPD Controller changes the Transmit Start of Transfer and Transmit End of Transfer status bits of the Data Link Status Register (DLSR). These two status indicators are valid until the Data Link Status Register is read. Reading these register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Transmit Start of Transfer and Transmit End of Transfer status bits of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (INDIRECT ADDRESS = 0XNAH, 0X06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Transmit Start of Transfer	RUR / WC	0 - There is no data link message to be sent to the data link channel. 1 - The HDLC Controller will send a data link message to the data link channel.
4	Transmit End of Transfer	RUR / WC	0 - No data link message was sent to the data link channel. 1 - The HDLC Controller finished sending a data link message to the data link channel.

13.1.4.2.6 Step 6: MOS message transmission

A one is then written into the LAPD enable bit of Data Link Control Register, which sets the transmitter to Message-Oriented mode and kicks off the transmission process. The LAPD controller latches these control bits of the Data Link Control Register and send a Transmit Start of Transfer interrupt (TxSOT) to the microprocessor to indicate that an MOS message will be send.

The LAPD transmitter will then transmit the open flag character (01111110) in the data link bit position first followed by the entire message. If the message is longer than 96 bytes or more than one full block of data are to be transmitted, the alternating buffer usage approach will provide more adequate time to allow the writing of the message in the Ping-Pong buffers without overwriting good data in the transmitting buffer or repeating data because it was written too late. User must fill in data fast enough in Ping-Pong buffer concatenation scenario to avoid automatic flag insertion between two blocks of data that will cause far-end FCS errors.

After the entire MOS message is sent, the LAPD Controller generates the Transmit End of Transfer (TxEOT) interrupt to the microprocessor indicating that the MOS message transmission is over.

The table below shows configurations of the LAPD Enable bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (INDIRECT ADDRESS = 0XN0H, 0X13H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	LAPD Enable	R/W	0 - The Transmit HDLC Controller will send out Bit-Oriented Signaling (BOS) message. 1 - The Transmit HDLC Controller will send out LAPD protocol or so-called Message-Oriented Signaling (MOS) message.

13.1.5 Transmit SLCâ96 Data link Controller

The SLC®96 T1 format is invented by AT&T and is used between the Digital Switch and a SLC®96 formatted remote terminal. The purpose of the SLC®96 product is to provide standard telephone service or Plain Old Telephone Service (POTS) in areas of high subscriber density but back-haul the traffic over T1 facilities.

To support the SLC®96 formatted remote terminal equipment, which is likely in an underground location, the T1s needed methods to:

- Indicate equipment failures of the equipment to maintenance personal
- Indicate failures of the POTS lines
- Test the POTS lines
- Provide redundancy on the T1s

The SLC®96 framing format is a D4 Super-frame (SF) format with specialized data link information bits. These data link information bits take the position of the Super-frame Alignment (Fs) bit positions. These bits consist of:

- Concentrator bits (C, bit position 1 to 11)
- First Spoiler bits (FS, bit position 12 to 14)
- Maintenance bits (M, bit position 15 to 17)
- Alarm bits (A, bit position 18 to 19)
- Protection Line Switch bits (S, bit position 20 to 23)
- Second Spoiler bit (SS, bit position 24)
- Resynchronization pattern (000111000111)

In SLCâ96 mode, six six-bit data will generate one 9-ms frame of the SLCâ96 message format. The format of the data link message is given in BELLCORE TR-TSY-000008. To select this mode, the Framing Select bits of

the Framing Select Register (FSR) must be set to binary number 100. The table below shows configuration of the Framing Select bits of the Framing Select Register (FSR).

FRAMING SELECT REGISTER (FSR) (INDIRECT ADDRESS = 0XN0H, 0X07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2-0	T1 Framing Select	R/W	**T1 Framing Select:** These READ/WRITE bit-fields allow the user to select one of the five T1 framing formats supported by the framer. These framing formats include ESF, SLC®96, SF, N and T1DM mode. **NOTE:** *Changing of framing format will automatically force the framer to RESYNC.*

Framing Format	Bit 2	Bit 1	Bit 0
ESF	0	X	X
SLC®96	1	0	0
SF	1	0	1
N	1	1	0
T1DM	1	1	1

When SLC®96 mode is enabled, the Fs bit is replaced by the data link message read from memory at the beginning of each D4 super-frame. The XRT84L38 allocates two 6-byte buffers to provide the SLC®96 Data Link Controller an alternating access mechanism for information transmission. The bit ordering and usage is shown in the following table; and the LSB is sent first. Note that these registers are memory-based storage and they need to be initialized.

TRANSMIT SLC®96 MESSAGE REGISTERS

BITBYTE	5	4	3	2	1	0
1	0	1	1	1	0	0
2	C1	1	1	1	0	0
3	C7	C6	C5	C4	C3	C2
4	1	0	C11	C10	C9	C8
5	A2	A1	M3	M2	M1	0
6	0	1	S4	S3	S2	S1

Each register is read out of memory once every six SF super-frames. The memory holding these registers owns a shared memory structure that is used by multiple devices. These include DS1 transmit module, DS1 receive module, Transmit LAPD Controller, Transmit SLCâ96 Data Link controller, Bit-Oriented Signaling Processor, Receive LAPD Controller, Receive SLCâ96 Data Link Controller, Receive Bit-Oriented Signaling Processor and microprocessor interface module.

13.1.5.1 How to configure the SLC®96 Data Link Controller to transmit SLC®96 Data Link Messages

This section describes how to configure the SLC®96 Data Link Controller to transmit SLC®96 Data Link message in a step-by-step basis.

13.1.5.1.1 Step 1: Find out the next available transmit data link buffer

To transmit SLC®96 Data Link message, the user is recommended to read Transmit Data Link Byte Count Register for next available transmit buffer number.

The table below shows how contents of the Buffer Enable bit of the Transmit Data Link Byte Count Register (TDLBCR) determines what the next available transmit buffer number is.

TRANSMIT DATA LINK BYTE COUNT REGISTER (TDLBCR) (INDIRECT ADDRESS = 0XN0H, 0X14H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Buffer Select	R	0 - The next available transmit buffer for sending out BOS or MOS message is Buffer 0. 1 - The next available transmit buffer for sending out BOS or MOS message is Buffer 1.

13.1.5.1.2 Step 2: Write SLC®96 Data Link Message into transmit data link buffer

After finding out the next available transmit buffer, the user should write the entire message data to the available transmit data link buffer via PIO or DMA access. The writing of these buffers is through the LAPD Buffer 0 indirect data registers and the LAPD Buffer1 indirect data registers. LAPD Buffer 0 and 1 indirect data registers have addresses 0xn6H and 0xn7H respectively. There is no indirect address register for transmit data link buffer 0 and 1.

A microcontroller WRITE access to the LAPD Buffer indirect data registers will access the transmit data link buffer and a microcontroller READ will access the receive data link buffers. The very first WRITE access to the LAPD Buffer indirect data register will always be direct to location 0 within the transmit data link buffer. The next WRITE access to the LAPD Buffer indirect data register will be direct to location 1 within the transmit data link buffer and so on, until all 96 bytes of the transmit buffer is filled.

For example, if the first byte of the SLC®96 Data Link message to be sent is (101011) and the next available transmit data link buffer of Channel n is 1. The user should write pattern (00101011) into transmit data link buffer 1 of Channel n. The following microprocessor access to the framer should be done:

WR n7H 2BH

The first byte of the SLC®96 Data Link message is written into location 0 of the transmit data link buffer. If the next byte of the data link message is (101001), the user should perform another microprocessor WRITE access of pattern (00101001):

WR n7H 29H

The second byte of data link message is written into location 1 of the transmit data link buffer. The WRITE access should be repeated until all six bytes of SLC®96 Data Link message is written into the transmit buffer or the transmit buffer is completely filled.

13.1.5.1.3 Step 3: Enable transmit data link message interrupt

The SLC®96 Data Link Controller can generate the Transmit Start of Transfer (TxSOT) interrupt indicating the status of data link message transmission to the microprocessor. To enable this interrupt, the Transmit Start of Transfer Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Transmit Start of Transfer Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (INDIRECT ADDRESS = 0XNAH, 0X07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Transmit Start of Transfer Enable	R/W	0 - The Transmit Start of Transfer interrupt is disabled. 1 - The Transmit Start of Transfer interrupt is enabled.

The table below shows configurations of the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	HDLC Controller Interrupt Enable	R/W	0 - Every interrupt generated by the HDLC Controller is disabled. 1 - Every interrupt generated by the HDLC Controller is enabled.

When this interrupt enable bit is set and the SLC®96 Data Link message is transmitted to the data link channel, the SLC®96 Data Link Controller changes the Transmit Start of Transfer status bits of the Data Link Status Register (DLSR). This status indicator is valid until the Data Link Status Register is read. Reading this register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Transmit Start of Transfer and Transmit End of Transfer status bits of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (INDIRECT ADDRESS = 0XNAH, 0X06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6	Transmit Start of Transfer	RUR / WC	0 - There is no data link message to be sent to the data link channel. 1 - The SLC®96 Data Link Controller will send SLC®96 data link message to the data link channel.

13.1.5.1.4 Step 4: Program the Data Link Control Register to activate SLC®96 Data Link Transmission

The SLC®96 Enable bit and the LAPD Enable bit of the Data Link Control Register (DLCR) determines which one of the three functions is performed by the Transmit HDLC Controller block. The table below shows configuration of the SLC®96 Enable bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (INDIRECT ADDRESS = 0XN0H, 0X13H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	SLC®96 Enable	R/W	0 - In SLC®96 framing mode, the data link transmission is disabled. The framer transmits the regular SF framing bits. In ESF framing mode, the framer transmits regular ESF framing bits and Facility Data Link (FDL) bits. 1 - In SLC®96 framing mode, the data link transmission is enabled. In ESF framing mode, the framer transmits SLC®96-like message in the Facility Data Link bits.

The table below shows configuration of the LAPD Enable bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (INDIRECT ADDRESS = 0XN0H, 0X13H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	LAPD Enable	R/W	0 - The Transmit HDLC Controller will send out Bit-Oriented Signaling (BOS) message. 1 - The Transmit HDLC Controller will send out LAPD protocol or so-called Message-Oriented Signaling (MOS) message.

To enable SLC®96 data link transmission, the user has to set both of the SLC®96 Enable bit and the LAPD Enable bit of the Data Link Control Register to 1.

Without inputting new message, the data link controller will loop on the same message over and over again. To force the data link to output all ones is done by setting the ABORT bit in Data Link Control Register to 1. This operation takes place after the current message finishes transmitting. The table below shows configurations of the ABORT bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (INDIRECT ADDRESS = 0XN0H, 0X13H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	ABORT	R/W	0 - No ABORT sequence is sent on the data link channel. 1 - The framer forces an ABORT sequence of pattern (111111 10) onto the data link channel.

Setting the SLCâ96 bit low will switch the data link back to transfer normal framing bits after the current message transmit completes.

13.2 DS1 RECEIVE HDLC CONTROLLER BLOCK

13.2.1 Description of the DS1 Receive HDLC Controller Block

XRT84L38 allows user to extract data link information from incoming DS1 frames. The data link information in DS1raming format mode can be extracted to the following:

- DS1 Receive Overhead Output Interface Block
- DS1 Receive HDLC Controller
- DS1 Receive Serial Output Interface

The Receive Data Link Source Select [1:0] bits, within the Receive Data Link Select Register (RSDLSR) determine destinations of the data link bits (Facility Data Link (FDL) bits in ESF framing format mode, Signaling Framing (Fs) bits in SLC®96 framing format mode and Remote Signaling (R) bits in T1DM framing format mode) extracted from the incoming DS1 frames.

The table below shows configuration of the Receive Data Link Source Select [1:0] bits of the Receive Data Link Select Register (RSDLSR).

RECEIVE DATA LINK SELECT REGISTER (RSDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0CH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1-0	Receive Data Link Source Select [1:0]	R/W	00 - The data link bits extracted from the incoming DS1 frame are sent to the Receive HDLC Controller. 01 - The data link bits extracted from the incoming DS1 frame are sent to the Receive Serial Data Output Interface via the RxSer_n pins. 10 - The data link bits extracted from the incoming DS1 frame are sent to the Receive Overhead Output Interface via the RxOH_n pins. 11 - The data link bits are forced into 1.

If the Receive Data Link Source Select bits of the Receive Data Link Select Register are set to 00, the Receive HDLC Controller block becomes output destination of the data link bits in incoming DS1 frames.

Each of the eight framers within the XRT84L38 device contains a DS1 Receive High-level Data Link Controller (HDLC) block. The function of this block is to establish a serial data link channel in DS1 mode through the following:

- Facility Data Link (FDL) bits in ESF framing format mode
- Signaling Framing (Fs) bits in SLC®96 framing format mode
- Remote Signaling (R) bits in T1DM framing format mode
- D or E signaling timeslot channel

Data link bits are automatically inserted into the Facility Data Link (FDL) bits in ESF framing format mode, Signaling Framing (Fs) bits in SLC®96 framing format mode and Remote Signaling (R) bits in T1DM framing format mode or forced to 1 by the framer. Additionally, XRT84L38 allows the user to define any one of ones of the twenty-four DS0 timeslots to be D or E channel. We will discuss how to configure XRT84L38 to Receive data link information through D or E channels in later section.

The DS1 Receive HDLC Controller block contains three major functional modules associated with DS1 framing formats. They are the:

- SLC®96 Data Link Controller
- LAPD Controller
- Bit-Oriented Signaling Processor.

There are two 96-byte receive message buffer in shared memory for each of the eight framers to receive data link information. When one message buffer is filled up, the DS1 Receive HDLC Controller automatically switches to the next message buffer to store data link messages. These two message buffers ping-pong among each other for data link message storage.

The SLC®96 Enable bit and the Message Type bit of the Data Link Status Register (DLSR) determines which one of the three messages is received and processed by the Receive HDLC Controller block.

The table below shows configuration of the SLC®96 Enable bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (INDIRECT ADDRESS = 0XN0H, 0X13H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	SLC®96 Enable	R/W	0 - In SLC®96 framing mode, the data link transmission is disabled. The framer receives the regular SF framing bits. In ESF framing mode, the framer receives regular ESF framing bits and Facility Data Link (FDL) bits. 1 - In SLC®96 framing mode, the data link transmission is enabled. In ESF framing mode, the framer receives SLC®96-like message in the Facility Data Link bits.

The table below shows configuration of the Message Type bit of the Data Link Status Register (DLSR).

DATA LINK STATUS REGISTER (DLSR) (INDIRECT ADDRESS = 0XNAH, 0X06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Message Type	RUR / WC	0 - The Receive HDLC Controller receives and processes Bit-Oriented Signaling (BOS) message. 1 - The Receive HDLC Controller receives and processes LAPD protocol or Message-Oriented Signaling (MOS) message.

13.2.2 How to configure XRT84L38 to Receive data link information through D or E Channels

The XRT84L38 can configure any one or ones of the twenty-four DS0 channels to be D or E channels. D channel is used primarily for data link applications. E channel is used primarily for signaling for circuit switching with multiple access configurations.

The Receive Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of each channel determine whether that particular channel is configured as D or E channel. These bits also determine what type of data or signaling conditioning is applied to each channel.

RECEIVE CHANNEL CONTROL REGISTER (RCCR) (INDIRECT ADDRESS = 0XN2H, 0X60H - 0X7FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-0	Receive Conditioning Select	R/W	1111 - This channel is configured as D or E timeslot.

If the Receive Conditioning Select [3:0] bits of the Receive Channel Control Register of a particular timeslot are set to 1111, that timeslot is configured as a D or E timeslot.

Any D or E timeslot can be configured to direct data link information to the following destinations:

- DS1 Receive Overhead Output Interface Block
- DS1 Receive HDLC Controller Block
- DS1 Receive Serial Output Interface Block
- DS1 Receive Fractional Output Interface Block

The Receive D or E Channel Source Select [1:0] bits of the Receive Data Link Select Register (RSDLSR) determines which one of the above-mentioned modules to be output destinations of D or E timeslot. The table be-

low shows configuration of the Receive D or E Channel Source Select [1:0] bits of the Receive Data Link Select Register (RSDLSR).

RECEIVE DATA LINK SELECT REGISTER (RSDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0CH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Receive D or E Channel Source Select [1:0]	R/W	00 - The data link bits extracted form the D or E channel of incoming DS1 frame are inserted into the Receive Serial Data Output Interface via the RxSer_n pins. 01 - The data link bits extracted form the D or E channel of incoming DS1 frame are inserted into the Receive HDLC Controller. 10 - The data link bits extracted form the D or E channel of incoming DS1 frame are inserted into the Receive Fractional T1 Output Interface via the RxFrT1_n pins. 11 - The data link bits extracted form the D or E channel of incoming DS1 frame are inserted into the Receive Serial Data Output Interface via the RxSer_n pins.

For the Receive HDLC Controller to be output destination of D or E channel, the Receive D or E Channel Source Select [1:0] bits of the Receive Data Link Select Register has to be set to 01.

13.2.3 Receive BOS (Bit Oriented Signaling) Processor

The Receive BOS Processor handles receiving and processing of BOS messages through the DS1 data link channel. It generates Receive End of Transfer (RxEOT) interrupt each time a BOS message is received and stores the BOS message into the receive message buffer. In the later section, we will discuss how to configure the BOS Processor Block to receive BOS message.

13.2.3.1 How to configure the BOS Processor Block to receive BOS

This section describes how to configure the BOS Processor Block to receive BOS message and how to read out the BOS message. The operation of the receive BOS Processor is interrupt-driven. When a BOS message is received, message octet is written to the next receive data link message buffer opposite to that last used. The receive BOS Processor generates interrupts to the microprocessor notifying it that a BOS message is received. The BOS message can then be extracted from the appropriate receive data link buffer.

13.2.3.1.1 Step 1: Enable receive BOS message interrupts

The BOS Processor can generate a couple of interrupts indicating the status of BOS message received to the microprocessor. These are the Receive Start of Transfer (RxSOT) interrupt and the Receive End of Transfer (RxEOT) interrupt.

To enable these interrupts, the Receive Start of Transfer Enable bit and the Receive End of Transfer Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Start of Transfer Enable bit and the Receive End of Transfer Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (INDIRECT ADDRESS = 0XNAH, 0X07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Start of Transfer Enable	R/W	0 - The Receive Start of Transfer interrupt is disabled. 1 - The Receive Start of Transfer interrupt is enabled.
3	Receive End of Transfer Enable	R/W	0 - The Receive End of Transfer interrupt is disabled. 1 - The Receive End of Transfer interrupt is enabled.

The table below shows configurations of the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	HDLC Controller Interrupt Enable	R/W	0 - Every interrupt generated by the HDLC Controller is disabled. 1 - Every interrupt generated by the HDLC Controller is enabled.

When these interrupt enable bits are set and the BOS message is received in the data link channel, the BOS Processor changes the Receive Start of Transfer and Receive End of Transfer status bits of the Data Link Status Register (DLSR). These two status indicators are valid until the Data Link Status Register is read. Reading these register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Start of Transfer and Receive End of Transfer status bits of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (INDIRECT ADDRESS = 0XNAH, 0X06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Start of Transfer	RUR / WC	0 - There is no data link message in the data link channel. 1 - The HDLC Controller began to receive a data link message in the data link channel.
3	Receive End of Transfer	RUR / WC	0 - No data link message was present in the data link channel. 1 - The HDLC Controller finished receiving a data link message in the data link channel.

The BOS Processor can also generate interrupts when either the BOS ABORT sequence (nine consecutive ones) or the IDLE flag character (hexadecimal value of 0x7EH) is received in the data link channel to the microprocessor. These are the Receive ABORT Sequence (RxABORT) interrupt and the Receive IDLE Flag Sequence (RxIDLE) interrupt.

To enable these interrupts, the Receive ABORT Sequence Enable bit and the Receive IDLE Flag Sequence Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive ABORT Sequence Enable bit and the Receive IDLE Flag Sequence Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (INDIRECT ADDRESS = 0XNAH, 0X07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive ABORT Sequence Enable	R/W	0 - The Receive ABORT Sequence interrupt is disabled. 1 - The Receive ABORT Sequence interrupt is enabled.
0	Receive IDLE Flag Sequence Enable	R/W	0 - The Receive IDLE Flag Sequence interrupt is disabled. 1 - The Receive IDLE Flag Sequence interrupt is enabled.

When these interrupt enable bits are set and the BOS ABORT sequence or IDLE Flag Sequence is received in the data link channel, the BOS Processor changes the Receive ABORT Sequence and Receive IDLE Flag Sequence status bits of the Data Link Status Register (DLSR). These two status indicators are valid until the Data

Link Status Register is read. Reading these register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive ABORT Sequence and Receive IDLE Flag Sequence status bits of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (INDIRECT ADDRESS = 0XNAH, 0X06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive ABORT Sequence	RUR / WC	0 - There is no BOS ABORT sequence received in the data link channel. 1 - The HDLC Controller receives BOS ABORT sequence in the data link channel.
0	Receive IDLE Flag Sequence	RUR / WC	0 - The message received in the data link channel is BOS message. 1 - The message received in the data link channel is MOS message.

13.2.3.1.2 Step 2: Find out the next available receive data link buffer

To transmit a bit-oriented signal, a repeating message is sent of the form (0d5d4d3d2d1d0011111111), where the "d5d4d3d2d1d0" represents a six-bit message. When receiving a BOS message, the received message octet is written to the next available receive data link buffer in the form of (0d5d4d3d2d1d00). The user is recommended to read Receive Data Link Byte Count Register for next available receive data link buffer number.

The table below shows how contents of the Receive Buffer Pointer bit of the Receive Data Link Byte Count Register (RDLBCR) determines what the next available receive data link buffer number is.

RECEIVE DATA LINK BYTE COUNT REGISTER (RDLBCR) (INDIRECT ADDRESS = 0XN0H, 0X15H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Buffer Pointer	R	0 - The next available receive data link buffer for reading out BOS or MOS message is Buffer 0. 1 - The next available receive data link buffer for reading out BOS or MOS message is Buffer 1.

13.2.3.1.3 Step 3: Program BOS Message receiving repetitions

The user should program the value of message receiving repetitions into the Receive Data Link Byte Count Register. The framer will receive the BOS message the same number of times as was stored in the Receive Data Link Byte Count Register (RDLBCR) before generating the Receive End of Transfer (RxEOT) interrupts. If the value stored inside the Receive Data Link Byte Count Register (RDLBCR) is set to 0, the message will be received indefinitely and no Receive End of Transfer interrupt will be generated.

The table below shows configurations of the Receive Data Link Byte Count [6:0] bits the Receive Data Link Byte Count Register (RDLBCR).

RECEIVE DATA LINK BYTE COUNT REGISTER (RDLBCR) (INDIRECT ADDRESS = 0XN0H, 0X15H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6-0	Receive Data Link Byte Count [6:0]	R/W	Value of these bits determines how many times a BOS message pattern will be received by the framer before generating the Receive End of Transfer (TxEOT) interrupt. ***NOTE:*** *If these bits are set to 0, the BOS message will be received indefinitely and no Receive End of Transfer interrupts will be generated.*

13.2.3.1.4 Step 4: Read BOS Message from receive data link buffer

Upon detection of the Receive End of Transfer (RxEOT) interrupt, the user should read the Message Type bit of the Data Link Status Register (DLSR) to find out what is the type of message received.

The table below shows how contents of the Message Type bit of the Data Link Status Register (DLSR) determines what the type of message received in the data link channel is.

DATA LINK STATUS REGISTER (DLSR) (INDIRECT ADDRESS = 0XNAH, 0X06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Message Type	RUR / WC	0 - There is no BOS ABORT sequence received in the data link channel. 1 - The HDLC Controller receives BOS ABORT sequence in the data link channel.

After determined that the received message is a BOS one, the use should read eight bits message from the first location of the next available receive data link buffer. The reading of these buffers is through the LAPD Buffer 0 indirect data registers and the LAPD Buffer1 indirect data registers. LAPD Buffer 0 and 1 indirect data registers have addresses 0xn6H and 0xn7H respectively. There is no indirect address register for receive data link buffer 0 and 1.

A microcontroller WRITE access to the LAPD Buffer indirect data registers will access the receive data link buffer and a microcontroller READ will access the receive data link buffers. The very first READ access to the LAPD Buffer indirect data register will always be direct to location 0 within the receive data link buffer.

For example, if the BOS Message to received is (101011) and the next available receive data link buffer of Channel n is 1. The user should be able to read pattern (01010110) from receive data link buffer 1 of Channel n. The following microprocessor access to the framer should be done:

RD n7H

The result of the READ access should be 0x56H.

13.2.4 Receive LAPD Controller

The receive LAPD controller implements the Message-Oriented protocol based on ITU Recommendation Q.921 Link Access Procedures on the D-channel (LAPD) type of protocol. It provides the following functions:

- Zero deletion
- Pattern recognition for IDLE flag detection
- Pattern recognition for ABORT sequence detection
- Frame check sequence verification
- T1 receiver interface
- Receive data link message buffer access

Two 96-byte buffers in shared memory are allocated for receive LAPD Controller to reduce the frequency of microprocessor interrupts and alleviate the response time requirement for microprocessor to handle each inter-

rupt. There are no restrictions on the length of the message received. However, the 96-byte buffer is deep enough to hold one entire LAPD path or test signal identification message.

The following section discuss how to configure the receive LAPD Controller to receive and extract MOS messages.

13.2.4.1 How to configure the Receive HDLC Controller Block to receive MOS message

This section describes how to configure the LAPD Controller Block to receive and extract MOS message in a step-by-step basis.

The operation of the receive LAPD Controller is interrupt-driven. When an MOS message is receiving, message octets are written to the next receive data link message buffer opposite to that last used. Each time the receiving data link message buffer is filled, a RxEOT interrupt is issued if it is enabled. This process continues until an ABORT sequence is received or an IDLE flag is received.

An interrupt is issued when one of the following conditions occurs and the corresponding interrupt enable bit is set.

- The RxSOT is set when the beginning of a data link message is received (the first non-flag message).
- The RxEOT is set when the end of a data link block is received.
- The RxIDLE is set if an IDLE flag sequence (b01111110) is received on the data link after either an ABORT sequence is received or a complete message is received.
- The RxABORT is set when an ABORT sequence is received.
- The FCS_ERR is issued when an erroneous frame check sequence is detected at the end of a message or an idle flag is received that is not octet aligned.

13.2.4.1.1 Step 1: Enable receive MOS message interrupts

The receive LAPD Controller can generate a couple of interrupts indicating the status of MOS message received to the microprocessor. These are the Receive Start of Transfer (RxSOT) interrupt and the Receive End of Transfer (RxEOT) interrupt.

To enable these interrupts, the Receive Start of Transfer Enable bit and the Receive End of Transfer Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Start of Transfer Enable bit and the Receive End of Transfer Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (INDIRECT ADDRESS = 0XNAH, 0X07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Start of Transfer Enable	R/W	0 - The Receive Start of Transfer interrupt is disabled. 1 - The Receive Start of Transfer interrupt is enabled.
3	Receive End of Transfer Enable	R/W	0 - The Receive End of Transfer interrupt is disabled. 1 - The Receive End of Transfer interrupt is enabled.

The table below shows configurations of the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	HDLC Controller Interrupt Enable	R/W	0 - Every interrupt generated by the HDLC Controller is disabled. 1 - Every interrupt generated by the HDLC Controller is enabled.

When these interrupt enable bits are set and the MOS message is received in the data link channel, the LAPD Controller changes the Receive Start of Transfer and Receive End of Transfer status bits of the Data Link Status Register (DLSR). These two status indicators are valid until the Data Link Status Register is read. Reading these register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Start of Transfer and Receive End of Transfer status bits of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (INDIRECT ADDRESS = 0XNAH, 0X06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Start of Transfer	RUR / WC	0 - There is no data link message in the data link channel. 1 - The HDLC Controller began to receive a data link message in the data link channel.
3	Receive End of Transfer	RUR / WC	0 - No data link message was present in the data link channel. 1 - The HDLC Controller finished receiving a data link message in the data link channel.

The LAPD Controller can also generate interrupts when either the MOS ABORT sequence (seven consecutive ones) or the IDLE flag character (hexadecimal value of 0x7EH) is received in the data link channel to the microprocessor. These are the Receive ABORT Sequence (RxABORT) interrupt and the Receive IDLE Flag Sequence (RxIDLE) interrupt.

To enable these interrupts, the Receive ABORT Sequence Enable bit and the Receive IDLE Flag Sequence Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive ABORT Sequence Enable bit and the Receive IDLE Flag Sequence Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (INDIRECT ADDRESS = 0XNAH, 0X07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive ABORT Sequence Enable	R/W	0 - The Receive ABORT Sequence interrupt is disabled. 1 - The Receive ABORT Sequence interrupt is enabled.
0	Receive IDLE Flag Sequence Enable	R/W	0 - The Receive IDLE Flag Sequence interrupt is disabled. 1 - The Receive IDLE Flag Sequence interrupt is enabled.

When these interrupt enable bits are set and the MOS ABORT sequence or IDLE Flag Sequence is received in the data link channel, the LAPD Controller changes the Receive ABORT Sequence and Receive IDLE Flag Sequence status bits of the Data Link Status Register (DLSR). These two status indicators are valid until the Data Link Status Register is read. Reading these register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive ABORT Sequence and Receive IDLE Flag Sequence status bits of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (INDIRECT ADDRESS = 0XNAH, 0X06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive ABORT Sequence	RUR / WC	0 - There is no BOS ABORT sequence received in the data link channel. 1 - The HDLC Controller receives MOS ABORT sequence in the data link channel.
0	Receive IDLE Flag Sequence	RUR / WC	0 - The message received in the data link channel is BOS message. 1 - The message received in the data link channel is MOS message.

Finally, the LAPD Controller generates Frame Check Sequence Error (FCS_ERR) interrupt when an erroneous frame check sequence is detected at the end of a message or an IDLE flag is received that is not octet aligned.

To enable this interrupt, the Frame Check Sequence Error Detection Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Frame Check Sequence Error Detection Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (INDIRECT ADDRESS = 0XNAH, 0X07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Frame Check Sequence Error Detection Enable	R/W	0 - The Frame Check Sequence Error Detection interrupt is disabled. 1 - The Frame Check Sequence Error Detection interrupt is enabled.

When the Frame Check Sequence Error Detection interrupt enable bits is set and an erroneous frame check sequence is detected at the end of a message, the LAPD Controller changes the Frame Check Sequence Error Detection status bits of the Data Link Status Register (DLSR). This status indicator is valid until the Data Link Status Register is read. Reading this register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset this status indicator.

The table below shows the Frame Check Sequence Error Detection status bits of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (INDIRECT ADDRESS = 0XNAH, 0X06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2	Frame Check Sequence Error Detection	RUR / WC	0 - There is no FCS error detected in the data link channel. 1 - The HDLC Controller receives an erroneous FCS in the data link channel.

13.2.4.1.2 Step 2: Find out the next available receive data link buffer

When the LAPD Controller is receiving MOS message, the received message octets are written to the next available receive data link buffer. The user is recommended to read Receive Data Link Byte Count Register for next available receive data link buffer number.

The table below shows how contents of the Receive Buffer Pointer bit of the Receive Data Link Byte Count Register (RDLBCR) determines what the next available receive data link buffer number is.

RECEIVE DATA LINK BYTE COUNT REGISTER (RDLBCR) (INDIRECT ADDRESS = 0XN0H, 0X15H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Buffer Pointer	R	0 - The next available receive data link buffer for reading out BOS or MOS message is Buffer 0. 1 - The next available receive data link buffer for reading out BOS or MOS message is Buffer 1.

13.2.4.1.3 Step 3: Reading the Receive Data Link Byte Count Register

The user should read the length of MOS message from the Receive Data Link Byte Count Register. The receive LAPD Controller increments the Receive Data Link Byte Count Register value when each octet of MOS message is received. After the Receive End of Transfer (RxEOT) interrupt is generated, the Receive Data Link Byte Count Register should contain the length of entire MOS message.

The table below shows configurations of the Receive Data Link Byte Count [6:0] bits of the Receive Data Link Byte Count Register (RDLBCR).

RECEIVE DATA LINK BYTE COUNT REGISTER (RDLBCR) (INDIRECT ADDRESS = 0XN0H, 0X15H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
6-0	Receive Data Link Byte Count [6:0]	R	Value of these bits determines how many times a BOS message pattern will be received by the framer before generating the Receive End of Transfer (TxEOT) interrupt.

13.2.4.1.4 Step 4: Read MOS Message from receive data link buffer

Upon detection of the Receive End of Transfer (RxEOT) interrupt, the user should read the Message Type bit of the Data Link Status Register (DLSR) to find out what is the type of message received.

The table below shows how contents of the Message Type bit of the Data Link Status Register (DLSR) determines what the type of message received in the data link channel is.

DATA LINK STATUS REGISTER (DLSR) (INDIRECT ADDRESS = 0XNAH, 0X06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Message Type	RUR / WC	0 - Message received in the data link channel is BOS. 1 - Message received in the data link channel is MOS.

After determined that the received message is an MOS one, the use should read the entire message from the available receive data link buffer. The reading of these buffers is through the LAPD Buffer 0 indirect data registers and the LAPD Buffer1 indirect data registers. LAPD Buffer 0 and 1 indirect data registers have addresses 0xn6H and 0xn7H respectively. There is no indirect address register for receive data link buffer 0 and 1.

A microcontroller WRITE access to the LAPD Buffer indirect data registers will access the receive data link buffer and a microcontroller READ will access the receive data link buffers. The very first READ access to the LAPD Buffer indirect data register will always be direct to location 0 within the receive data link buffer.

For example, if the first octet of the MOS Message received is (10101100) and the next available receive data link buffer of Channel n is 1. The user should be able to read pattern (01010110) from receive data link buffer 1 of Channel n. The following microprocessor access to the framer should be done:

RD n7H

The result of the READ access should be 0xACH.

13.2.5 Receive SLCâ96 Data link Controller

This section describes how to configure the Receive SLC®96 Data Link Controller block to receive SLC®96 Data Link message and how to read out the message from the receive data link message buffer. The operation of the Receive SLC®96 Data Link Controller is interrupt-driven. When a 36-bit SLC®96 Data Link message is received, message octet is written to the next receive data link message buffer opposite to that last used. The receive SLC®96 Data Link Controller generates interrupts to the microprocessor notifying it that a message is received. The data link message can then be extracted from the appropriate receive data link buffer.

In order to enable this mode of operation, the framing mode must be set to SLC®96. The XRT84L38 allocates two 6-byte buffers to provide SLC®96 Data Link Controller an alternating access mechanism for information received. The bit ordering and usage is shown in the following table. The bits 7 and 6 are forced to 0 by the SLC®96 Data Link Controller.

RECEIVE SLC®96 MESSAGE REGISTERS

BITBYTE	7	6	5	4	3	2	1	0
1/7	0	0	0	1	1	1	0	0
2/8	0	0	C1	1	1	1	0	0
3/9	0	0	C7	C6	C5	C4	C3	C2
4/10	0	0	1	0	C11	C10	C9	C8
5/11	0	0	A2	A1	M3	M2	M1	0
6/12	0	0	0	1	S4	S3	S2	S1

13.2.5.1 How to configure the SLC®96 Data Link Controller to receive SLC®96 Data Link Messages

This section describes how to configure the SLC®96 Data Link Controller to receive SLC®96 Data Link message in a step-by-step basis.

The operation of the receive SLC®96 Data Link Controller is interrupt-driven. When an SLC®96 Data Link message is receiving, message octets are written to the next receive data link message buffer opposite to that last used. Every time the SLC®96 Data Link controller receives a 36-bit SLC®96 data link message, an RxEOT interrupt is issued if it is enabled. This process continues until an ABORT sequence is received.

An interrupt is issued when one of the following conditions occurs and the corresponding interrupt enable bit is set.

- The RxSOT is set when the beginning of a data link message is received.
- The RxEOT is set when the end of a data link block is received.
- The RxABORT is set when an ABORT sequence is received.

13.2.5.1.1 Step 1: Enable receive SLC®96 Data Link message interrupts

The receive SLC®96 Data Link Controller can generate a couple of interrupts indicating the status of SLC®96 message received to the microprocessor. These are the Receive Start of Transfer (RxSOT) interrupt and the Receive End of Transfer (RxEOT) interrupt.

To enable these interrupts, the Receive Start of Transfer Enable bit and the Receive End of Transfer Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive Start of Transfer Enable bit and the Receive End of Transfer Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (INDIRECT ADDRESS = 0XNAH, 0X07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Start of Transfer Enable	R/W	0 - The Receive Start of Transfer interrupt is disabled. 1 - The Receive Start of Transfer interrupt is enabled.
3	Receive End of Transfer Enable	R/W	0 - The Receive End of Transfer interrupt is disabled. 1 - The Receive End of Transfer interrupt is enabled.

The table below shows configurations of the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register.

BLOCK INTERRUPT ENABLE REGISTER (BIER) (INDIRECT ADDRESS = 0XNAH, 0X00H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3	HDLC Controller Interrupt Enable	R/W	0 - Every interrupt generated by the HDLC Controller is disabled. 1 - Every interrupt generated by the HDLC Controller is enabled.

When these interrupt enable bits are set and the SLC®96 message is received in the data link channel, the SLC®96 Data Link Controller changes the Receive Start of Transfer and Receive End of Transfer status bits of the Data Link Status Register (DLSR). These two status indicators are valid until the Data Link Status Register is read. Reading these register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive Start of Transfer and Receive End of Transfer status bits of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (INDIRECT ADDRESS = 0XNAH, 0X06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
5	Receive Start of Transfer	RUR / WC	0 - There is no data link message in the data link channel. 1 - The SLC®96 Data Link Controller began to receive a data link message in the data link channel.
3	Receive End of Transfer	RUR / WC	0 - No data link message was present in the data link channel. 1 - The SLC®96 Data Link Controller finished receiving a data link message in the data link channel.

The SLC®96 Data Link Controller can also generate interrupts when the ABORT sequence is received in the data link channel to the microprocessor. This is the Receive ABORT Sequence (RxABORT).

To enable this interrupt, the Receive ABORT Sequence Enable bit of the Data Link Interrupt Enable Register (DLIER) have to be set. In addition, the HDLC Controller Interrupt Enable bit of the Block Interrupt Enable Register (BIER) needs to be one.

The table below shows configurations of the Receive ABORT Sequence Enable bit and the Receive IDLE Flag Sequence Enable bit of the Data Link Interrupt Enable Register.

DATA LINK INTERRUPT ENABLE REGISTER (DLIER) (INDIRECT ADDRESS = 0XNAH, 0X07H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive ABORT Sequence Enable	R/W	0 - The Receive ABORT Sequence interrupt is disabled. 1 - The Receive ABORT Sequence interrupt is enabled.

When these interrupt enable bits are set and the SLC®96 ABORT sequence is received in the data link channel, the SLC®96 Data Link Controller changes the Receive ABORT Sequence status bit of the Data Link Status Register (DLSR). This status indicator is valid until the Data Link Status Register is read. Reading the register clears the associated interrupt if Reset Upon Read is selected in Interrupt Control Register (ICR). Otherwise, a write-to-clear operation by the microprocessor is required to reset these status indicators.

The table below shows the Receive ABORT Sequence status bit of the Data Link Status Register.

DATA LINK STATUS REGISTER (DLSR) (INDIRECT ADDRESS = 0XNAH, 0X06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
1	Receive ABORT Sequence	RUR / WC	0 - There is no BOS ABORT sequence received in the data link channel. 1 - The SLC®96 Data Link Controller receives ABORT sequence in the data link channel.

13.2.5.1.2 Step 2: Find out the next available receive data link buffer

When the SLC®96 Data Link Controller is receiving SLC®96 message, the received message octets are written to the next available receive data link buffer. The user is recommended to read Receive Data Link Byte Count Register for next available receive data link buffer number.

The table below shows how contents of the Receive Buffer Pointer bit of the Receive Data Link Byte Count Register (RDLBCR) determines what the next available receive data link buffer number is.

RECEIVE DATA LINK BYTE COUNT REGISTER (RDLBCR) (INDIRECT ADDRESS = 0XN0H, 0X15H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Buffer Pointer	R	0 - The next available receive data link buffer for reading out data link message is Buffer 0. 1 - The next available receive data link buffer for reading out data link message is Buffer 1.

13.2.5.1.3 Step 3: Read SLC®96 Data LInk Message from receive data link buffer

Upon detection of the Receive End of Transfer (RxEOT) interrupt, the use should read the entire SLC®96 Data Link message from the available receive data link buffer. The reading of these buffers is through the LAPD Buffer 0 indirect data registers and the LAPD Buffer1 indirect data registers. LAPD Buffer 0 and 1 indirect data registers have addresses 0xn6H and 0xn7H respectively. There is no indirect address register for receive data link buffer 0 and 1.

A microcontroller WRITE access to the LAPD Buffer indirect data registers will access the receive data link buffer and a microcontroller READ will access the receive data link buffers. The very first READ access to the LAPD Buffer indirect data register will always be direct to location 0 within the receive data link buffer.

For example, if the first octet of the SLC®96 Message received is (00101011) and the next available receive data link buffer of Channel n is 1. The user should be able to read pattern (00101011) from receive data link buffer 1 of Channel n. The following microprocessor access to the framer should be done:

RD n7H

The result of the READ access should be 0x2BH.

14.0 E1 HDLC CONTROLLER BLOCK

14.1 E1 TRANSMIT HDLC CONTROLLER BLOCK

14.1.1 Description of the E1 Transmit HDLC Controller Block

XRT84L38 allows user to insert data link information to outbound E1 frames. The data link information in E1 framing format mode can be inserted from:

- E1 Transmit Overhead Input Interface Block
- E1 Transmit HDLC Controller
- E1 Transmit Serial Input Interface

The Transmit Data Link Source Select [1:0] bits, within the Synchronization MUX Register (SMR) determine source of the data link bits to be inserted into the outgoing E1 frames.

The table below shows configuration of the Transmit Data Link Source Select [1:0] bits of the Synchronization MUX Register (SMR).

SYNCHRONIZATION MUX REGISTER (SMR) (INDIRECT ADDRESS = 0XN0H, 0X09H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-2	Transmit Data Link Source Select [1:0]	R/W	00 - The data link bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins. 01 - The data link bits are inserted into the framer through the Transmit HDLC Controller. 10 - The data link bits are inserted into the framer through the Transmit Overhead Input Interface via the TxOH_n pins. 11 - The data link bits are inserted into the framer through the Transmit Serial Data input Interface via the TxSer_n pins.

If the Transmit Data Link Source Select bits of the Transmit Data Link Select Register are set to 01, the Transmit HDLC Controller block becomes input source of the data link bits in outgoing E1 frames.

Each of the eight framers within the XRT84L38 device contains an E1 Transmit High-level Data Link Controller (HDLC) block. The function of this block is to provide a serial data link channel in E1 mode through the following:

- The National bits (Sa4 through Sa8) of Timeslot 0 of non-FAS frame
- Timeslot 16 octet when the framer is in Common Channel Signaling mode
- D or E signaling timeslot channel

We will discuss how to configure XRT84L38 to transmit data link information through each of these data link channels in later sections.

The E1 Transmit HDLC Controller block contains two major functional modules associated with E1 framing formats. They are the LAPD Controller and the Bit-Oriented Signaling Processor.

There are two 96-byte transmit message buffers in shared memory for each of the eight framers to transmit data link information. When one message buffer is filled up, the Transmit HDLC Controller automatically switches to the next message buffer to load data link messages. These two message buffers ping-pong among each other for data link message transmission.

The LAPD Enable bit of the Data Link Control Register (DLCR) determines whether the Transmit HDLC Controller block should perform as the LAPD Controller or the BOS Processor.

The table below shows configuration of the LAPD Enable bit of the Data Link Control Register (DLCR).

DATA LINK CONTROL REGISTER (DLCR) (INDIRECT ADDRESS = 0XN0H, 0X13H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
0	LAPD Enable	R/W	0 - The Transmit HDLC Controller will send out Bit-Oriented Signaling (BOS) message. 1 - The Transmit HDLC Controller will send out LAPD protocol or so-called Message-Oriented Signaling (MOS) message.

14.1.2 How to configure XRT84L38 to transmit data link information through the National bits (Sa4 through Sa8)

As mentioned in previous section, the National bits (Sa4 through Sa8) of Timeslot 0 of non-FAS frame can be used to transmit data link information in E1 mode.

The XRT84L38 allows the user to decide on the following:

- Whether the National bits will be used to carry the data link information bits.
- How many of the National Bits will be used to carry the Data Link information bits.
- Which of these National Bits will be used to carry the Data Link information bits.

The Transmit Signaling and Data Link Control [2:0] bits of the Transmit Signaling and Data Link Select Register (TSDLSR) determines if the National bits will be used to carry data link information. The table below shows configuration of the Transmit Signaling and Data Link Control [2:0] bits of the Transmit Signaling and Data Link Select Register (TSDLSR).

TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2-0	Transmit Signaling and Data Link Select	R/W	000 - The data link interface is source of the Sa4 through Sa8 Nation bits. 001 - The data link interface is source of the Sa4 through Sa8 Nation bits. 010 - The Sa4 through Sa8 Nation bits are forced to 1. 011 - The Sa4 through Sa8 Nation bits are forced to 1. 1xx - The Sa4 through Sa8 Nation bits are forced to 1.

If the Transmit Signaling and Data Link Select [2:0] bits of the Transmit Signaling and Data Link Select Register is set to 000 or 001, the data link interface becomes source of the Sa4 through Sa8 National bits.

The Transmit Sa Data Link Select bits of the Transmit Signaling and Data Link Select Register (TSDLSR) determine which ones of the National bits are configured as Data Link bits in E1 framing format mode. Depending upon the configuration of the Transmit Signaling and Data Link Select Register, either of the following cases may exists:

- None of the National bits are used to transport the Data Link information bits (That is, data link channel of XRT84L38 is inactive).
- Any combination of between 1 and all 5 of the National bits can be selected to transport the Data Link information bits.

The table below shows configuration of the Transmit Sa Data Link Select bits of the Transmit Signaling and Data Link Select Register (TSDLSR).

TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Transmit Sa8 Data Link Select	R/W	0 - Source of the Sa8 Nation bit is not from the data link interface. 1 - Source the Sa8 National bit from the data link interface.
6	Transmit Sa7 Data Link Select	R/W	0 - Source of the Sa7 Nation bit is not from the data link interface. 1 - Source the Sa7 National bit from the data link interface.
5	Transmit Sa6 Data Link Select	R/W	0 - Source of the Sa6 Nation bit is not from the data link interface. 1 - Source the Sa6 National bit from the data link interface.
4	Transmit Sa5 Data Link Select	R/W	0 - Source of the Sa5 Nation bit is not from the data link interface. 1 - Source the Sa5 National bit from the data link interface.
3	Transmit Sa4 Data Link Select	R/W	0 - Source of the Sa4 Nation bit is not from the data link interface. 1 - Source the Sa4 National bit from the data link interface.

14.1.3 How to configure XRT84L38 to transmit data link information through Timeslot 16 octet

In E1 mode, Timeslot 16 octet can be configured to transmit the following:

- Channel Associated Signaling (CAS) bits A, B, C and D
- Common Channel Signaling (CCS) bits

The Common Channel Signaling (CCS) messages are actually data link information applicable to all thirty-two timeslots of an E1 frame, thus the name Common Channel Signaling. The Transmit Signaling and Data Link Control [2:0] bits of the Transmit Signaling and Data Link Select Register (TSDLSR) determine if Timeslot octet will be used to carry data link information or CAS signals. The table below shows configuration of the Transmit Signaling and Data Link Control [2:0] bits of the Transmit Signaling and Data Link Select Register (TSDLSR).

TRANSMIT SIGNALING AND DATA LINK SELECT REGISTER (TSDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0AH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2-0	Transmit Signaling and Data Link Select	R/W	000 - Timeslot 16 octet is taken directly from the Transmit Serial Input Interface through the TxSer_n pin. 001 - Timeslot 16 octet is taken directly from the Transmit Overhead Input Interface through the TxOH_n pin or the Transmit Signaling Control Register of Timeslot 16. 010 - Timeslot 16 octet is taken directly from the Transmit Serial Input Interface through the TxSer_n pin. 011 - Timeslot 16 octet is taken directly from the Transmit Overhead Input Interface through the TxOH_n pin or the Transmit Signaling Control Register of Timeslot 16. 1xx - Timeslot 16 octet is taken from the data link interface.

If the Transmit Signaling and Data Link Select [2:0] bits of the Transmit Signaling and Data Link Select Register are set to 1xx, the data link interface becomes source of the Timeslot 16 octet.

14.1.4 How to configure XRT84L38 to transmit data link information through D or E Channels

The XRT84L38 can configure any one or ones of the thirty-two E1 channels to be D or E channels except for Channel number 0. D channel is used primarily for data link applications. E channel is used primarily for signaling for circuit switching with multiple access configurations.

The Transmit Conditioning Select [3:0] bits of the Transmit Channel Control Register (TCCR) of each channel determine whether that particular channel is configured as D or E channel. These bits also determine what type of data or signaling conditioning is applied to each channel.

TRANSMIT CHANNEL CONTROL REGISTER (TCCR) (INDIRECT ADDRESS = 0XN2H, 0X00H - 0X1FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-0	Transmit Conditioning Select	R/W	1111 - This channel is configured as D or E timeslot.

If the Transmit Conditioning Select [3:0] bits of the Transmit Channel Control Register of a particular timeslot are set to 1111, that timeslot is configured as a D or E timeslot.

NOTE: *Timeslot 0 can never be configured as D or E timeslot.*

14.1.5 Transmit BOS (Bit Oriented Signaling) Processor

The Transmit BOS Processor handles transmission of BOS messages through the E1 data link channel. It determines how many repetitions a certain BOS message will be transmitted. It also inserts BOS IDLE flag sequence and ABORT sequence to be transmitted on the data link channel. Please see Section ? for descriptions of BOS message format and how to transmit BOS message.

14.1.6 Transmit MOS (Message Oriented Signaling) or LAPD Controller

The Transmit LAPD controller implements the Message-Oriented protocol based on ITU Recommendation Q.921 Link Access Procedures on the D-channel (LAPD) type of protocol. It provides the following functions:

- Zero stuffing
- T1/E1 transmitter interface
- Transmit message buffer access
- Frame check sequence generation
- IDLE flag insertion
- ABORT sequence generation

Two 96-byte buffers in shared memory are allocated for LAPD transmitter to reduce the frequency of microprocessor interrupts and alleviate the response time requirement for microprocessor to handle each interrupt. There are no restrictions on the length of the message. However the 96-byte buffer is deep enough to hold one entire LAPD path or test signal identification message. Please see Section ? for descriptions of MOS message format and how to configure the LAPD Controller to transmit MOS message.

14.2 E1 RECEIVE HDLC CONTROLLER BLOCK

14.2.1 Description of the E1 Receive HDLC Controller Block

XRT84L38 detects and extracts data link information from incoming E1 frames. The data link information in E1 framing format mode can be extracted to:

- E1 Receive Overhead Output Interface Block
- E1 Receive HDLC Controller
- E1 Receive Serial Output Interface

The extracted data link information is routed to the E1 Receive Overhead Output Interface and the E1 Receive Serial Output Interface no matter whether the E1 Receive HDLC Controller module is activated or not.

Each of the eight framers within the XRT84L38 device contains an E1 Receive High-level Data Link Controller (HDLC) block. The function of this block is to establish a serial data link channel in E1 mode through the following:

- The National bits (Sa4 through Sa8) of Timeslot 0 of non-FAS frame
- Timeslot 16 octet when the framer is in Common Channel Signaling mode
- D or E signaling timeslot channel

We will discuss how to configure XRT84L38 to transmit data link information through each of these data link channels in later sections.

The E1 Transmit HDLC Controller block contains two major functional modules associated with E1 framing formats. They are the LAPD Controller and the Bit-Oriented Signaling Processor.

There are two 96-byte receive message buffer in shared memory for each of the eight framers to receive data link information. When one message buffer is filled up, the E1 Receive HDLC Controller automatically switches to the next message buffer to store data link messages. These two message buffers ping-pong among each other for data link message storage.

The Message Type bit of the Data Link Status Register (DLSR) determines which one of the three messages is received and processed by the Receive HDLC Controller block.

The table below shows configuration of the Message Type bit of the Data Link Status Register (DLSR).

DATA LINK STATUS REGISTER (DLSR) (INDIRECT ADDRESS = 0XNAH, 0X06H)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Message Type	RUR / WC	0 - The Receive HDLC Controller receives and processes Bit-Oriented Signaling (BOS) message. 1 - The Receive HDLC Controller receives and processes LAPD protocol or Message-Oriented Signaling (MOS) message.

14.2.2 How to configure XRT84L38 to receive data link information through the National bits (Sa4 through Sa8)

As mentioned in previous section, the National bits (Sa4 through Sa8) of Timeslot 0 of non-FAS frame can be used to receive data link information in E1 mode.

The XRT84L38 allows the user to decide on the following:

- Whether the National bits will be used to carry the data link information bits.
- How many of the National Bits will be used to carry the Data Link information bits.
- Which of these National Bits will be used to carry the Data Link information bits.

The Receive Signaling and Data Link Control [2:0] bits of the Receive Signaling and Data Link Select Register (RSDLSR) determines if the National bits will be used to carry data link information. The table below shows configuration of the Receive Signaling and Data Link Control [2:0] bits of the Receive Signaling and Data Link Select Register (RSDLSR).

RECEIVE SIGNALING AND DATA LINK SELECT REGISTER (RSDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0CH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2-0	Receive Signaling and Data Link Select	R/W	000 - The data link interface is destination of the Sa4 through Sa8 Nation bits. 001 - The data link interface is destination of the Sa4 through Sa8 Nation bits. 010 - The Sa4 through Sa8 Nation bits are forced to 1. 011 - The Sa4 through Sa8 Nation bits are forced to 1. 1xx - The Sa4 through Sa8 Nation bits are forced to 1.

If the Receive Signaling and Data Link Select [2:0] bits of the Receive Signaling and Data Link Select Register are set to 000 or 001, the data link interface becomes destination of the Sa4 through Sa8 National bits.

The Receive Sa Data Link Select bits of the Receive Signaling and Data Link Select Register (RSDLSR) determine which ones of the National bits are configured as Data Link bits in E1 framing format mode. Depending upon the configuration of the Receive Signaling and Data Link Select Register, either of the following cases may exists:

- None of the National bits are used to transport the Data Link information bits (That is, data link channel of XRT84L38 is inactive).
- Any combination of between 1 and all 5 of the National bits can be selected to transport the Data Link information bits.

The table below shows configuration of the Receive Sa Data Link Select bits of the Receive Signaling and Data Link Select Register (RSDLSR).

RECEIVE SIGNALING AND DATA LINK SELECT REGISTER (RSDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0CH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
7	Receive Sa8 Data Link Select	R/W	0 - Destination of the Sa8 Nation bit is not the data link interface. 1 - Destination of the Sa8 National bit is the data link interface.
6	Receive Sa7 Data Link Select	R/W	0 - Destination of the Sa7 Nation bit is not the data link interface. 1 - Destination of the Sa7 National bit is the data link interface.
5	Receive Sa6 Data Link Select	R/W	0 - Destination of the Sa6 Nation bit is not the data link interface. 1 - Destination of the Sa6 National bit is the data link interface.
4	Receive Sa5 Data Link Select	R/W	0 - Destination of the Sa5 Nation bit is not the data link interface. 1 - Destination of the Sa5 National bit is the data link interface.
3	Receive Sa4 Data Link Select	R/W	0 - Destination of the Sa4 Nation bit is not the data link interface. 1 - Destination of the Sa4 National bit is the data link interface.

14.2.3 How to configure XRT84L38 to receive data link information through Timeslot 16 octet

In E1 mode, Timeslot 16 octet can be configured to receive the following:

- Channel Associated Signaling (CAS) bits A, B, C and D
- Common Channel Signaling (CCS) bits

The Common Channel Signaling (CCS) messages are actually data link information applicable to all thirty-two timeslots of an E1 frame, thus the name Common Channel Signaling. The Receive Signaling and Data Link Control [2:0] bits of the Receive Signaling and Data Link Select Register (RSDLSR) determine if Timeslot octet

will be used to carry data link information or CAS signals. The table below shows configuration of the Receive Signaling and Data Link Control [2:0] bits of the Receive Signaling and Data Link Select Register (RSDLSR).

RECEIVE SIGNALING AND DATA LINK SELECT REGISTER (RSDLSR) (INDIRECT ADDRESS = 0XN0H, 0X0CH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
2-0	Receive Signaling and Data Link Select	R/W	000 - Timeslot 16 octet is extracted directly to the Receive Serial Output Interface through the RxSer_n pin. 001 - Timeslot 16 octet is extracted directly to the Receive Overhead Output Interface through the RxOH_n pin or the Receive Signaling Control Register of Timeslot 16. 010 - Timeslot 16 octet is extracted directly to the Receive Serial Output Interface through the RxSer_n pin. 011 - Timeslot 16 octet is extracted directly to the Receive Overhead Output Interface through the RxOH_n pin or the Receive Signaling Control Register of Timeslot 16. 1xx - Timeslot 16 octet is extracted to the data link interface.

If the Receive Signaling and Data Link Select [2:0] bits of the Receive Signaling and Data Link Select Register are set to 1xx, the data link interface becomes destination of the Timeslot 16 octet.

14.2.4 How to configure XRT84L38 to receive data link information through D or E Channels

The XRT84L38 can configure any one or ones of the thirty-two E1 channels to be D or E channels except for Channel number 0. D channel is used primarily for data link applications. E channel is used primarily for signaling for circuit switching with multiple access configurations.

The Receive Conditioning Select [3:0] bits of the Receive Channel Control Register (RCCR) of each channel determine whether that particular channel is configured as D or E channel. These bits also determine what type of data or signaling conditioning is applied to each channel.

RECEIVE CHANNEL CONTROL REGISTER (RCCR) (INDIRECT ADDRESS = 0XN2H, 0X60H - 0X7FH)

BIT NUMBER	BIT NAME	BIT TYPE	BIT DESCRIPTION
3-0	Receive Conditioning Select	R/W	1111 - This channel is configured as D or E timeslot.

If the Receive Conditioning Select [3:0] bits of the Receive Channel Control Register of a particular timeslot are set to 1111, that timeslot is configured as a D or E timeslot.

NOTE: *Timeslot 0 can never be configured as D or E timeslot.*

14.2.5 Receive BOS (Bit Oriented Signaling) Processor

The Receive BOS Processor handles receiving and processing of BOS messages through the E1 data link channel. It generates Receive End of Transfer (RxEOT) interrupt each time a BOS message is received and stores the BOS message into the receive message buffer. Please see Section ? for how to configure the BOS Processor Block to receive BOS message.

14.2.6 Receive LAPD Controller

The receive LAPD controller implements the Message-Oriented protocol based on ITU Recommendation Q.921 Link Access Procedures on the D-channel (LAPD) type of protocol. It provides the following functions:

- Zero deletion
- Pattern recognition for IDLE flag detection
- Pattern recognition for ABORT sequence detection

- Frame check sequence verification
- T1 receiver interface
- Receive data link message buffer access

Two 96-byte buffers in shared memory are allocated for receive LAPD Controller to reduce the frequency of microprocessor interrupts and alleviate the response time requirement for microprocessor to handle each interrupt. There are no restrictions on the length of the message received. However, the 96-byte buffer is deep enough to hold one entire LAPD path or test signal identification message.

Please see Section ? for how to configure the receive LAPD Controller to receive and extract MOS messages.

15.0 TRANSMIT LIU INTERFACE

The purpose of the Transmit LIU Interface is to take the outbound frame data from the Transmit Framer block and to do the following:

- To encode the outbound frame data into any one of the following formats
- Single-Rail (e.g., a binary data stream)
- Dual-Rail, AMI Line Code
- Dual Rail, HDB3 Line Code
- To output this encoded data to an LIU device via the TxPOS, TxNEG and TxLineClk output pins.

16.0 RECEIVE LIU INTERFACE

The purpose of the Receive LIU Interface is to receive either single-rail or dual-rail data from an LIU IC and to do the following:

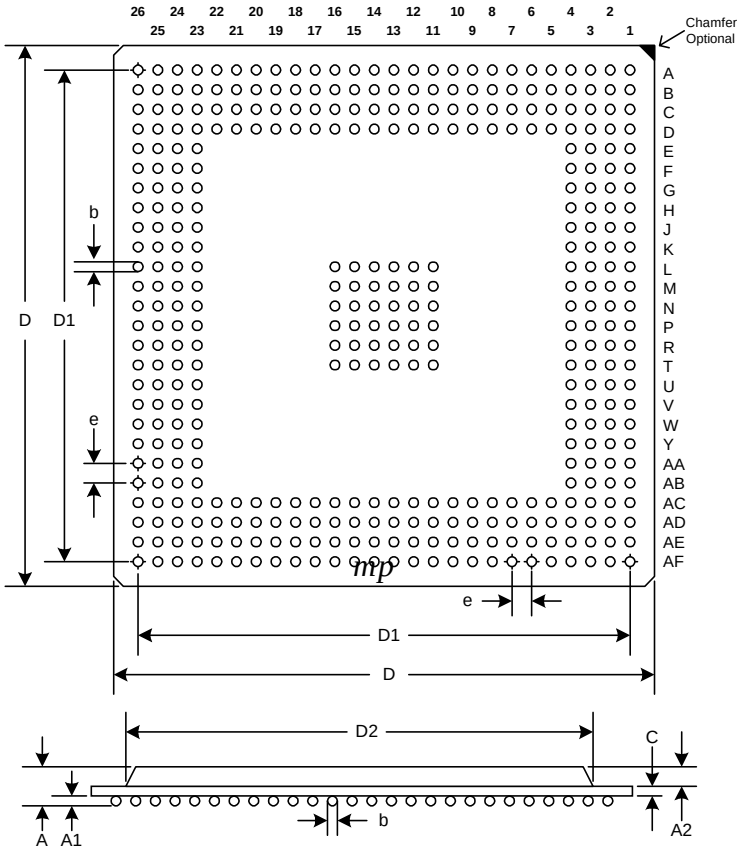
- Decode this incoming data from the single-rail, AMI or HDB3 line code and convert it into a binary data stream
- Route this binary data stream to the Receive Framer Block
- Detect and Declare the Loss of Signal Condition.

ORDERING INFORMATION

PART NUMBER	PACKAGE	OPERATING TEMPERATURE RANGE
XRT84L38	388 Pin Plastic Ball Grid Array	-40^{0}C to +85^{0}C

PACKAGE DIMENSIONS

388 Pin Plastic Ball Grid Array
(35 x 35 mm PBGA)
Rev. 1.0 (Bottom View)



Symbol	Inches MIN	Inches MAX	Millimeters MIN	Millimeters MAX
A	0.075	0.106	1.90	2.70
A1	0.020	0.028	0.50	0.70
A2	0.039	0.051	1.00	1.30
b	0.024	0.035	0.60	0.90
C	0.016	0.028	0.40	0.70
D	1.370	1.386	34.80	35.20
D1	1.250BSC		31.75BSC	
D2	1.177	1.185	29.90	30.10
e	0.050BSC		1.27BSC	

Note: The control dimension is the millimeter column

REVISIONS

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NOTICE