

## N-Channel 40-V (D-S), 175°C MOSFET

**PRODUCT SUMMARY**

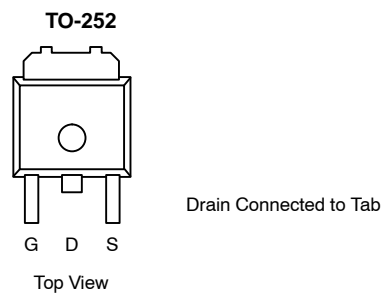
$V_{(BR)DSS}$ (V)	$r_{DS(on)}$ ( $\Omega$ )	$I_D$ (A) <sup>c</sup>	$Q_g$ (Typ)
40	0.006 @ $V_{GS} = 10$ V	109	95

**FEATURES**

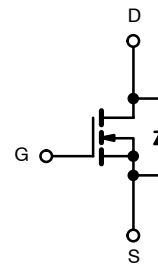
- TrenchFET® Power MOSFETS
- 175°C Junction Temperature
- High Threshold Voltage At High Temperature

**APPLICATIONS**

- Automotive Such As:
  - High-Side Switch
  - Motor Drives
  - 12-V Battery



Ordering Information: SUD50N04-06H—E3


**ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$  UNLESS OTHERWISE NOTED)**

Parameter		Symbol	Limit	Unit
Drain-Source Voltage		$V_{DS}$	40	V
Gate-Source Voltage		$V_{GS}$	$\pm 20$	
Continuous Drain Current ( $T_J = 175^\circ\text{C}$ )	$T_C = 25^\circ\text{C}$	$I_D$	109 <sup>c</sup>	A
	$T_C = 100^\circ\text{C}$		77 <sup>c</sup>	
Pulsed Drain Current		$I_{DM}$	100	
Avalanche Current (Single Pulse)		$I_{AS}$	50	
Repetitive Avalanche Energy (Single Pulse) <sup>a</sup>	$L = 0.1$ mH	$E_{AS}$	125	mJ
Power Dissipation	$T_C = 25^\circ\text{C}$	$P_D$	136	W
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	-55 to 175	$^\circ\text{C}$

**THERMAL RESISTANCE RATINGS**

Parameter		Symbol	Typical	Maximum	Unit
Junction-to-Ambient <sup>b</sup>	$t \leq 10$ sec	$R_{thJA}$	15	18	$^\circ\text{C/W}$
	Steady State		40	50	
Junction-to-Case		$R_{thJC}$	0.85	1.1	

## Notes:

- Duty cycle  $\leq 1\%$ .
- Surface mounted on 1" FR4 board.
- Based on maximum allowable Junction Temperature. Package limitation current is 50 A.

**SPECIFICATIONS (T<sub>J</sub> = 25 °C UNLESS OTHERWISE NOTED)**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
<b>Static</b>						
Drain-Source Breakdown Voltage	V <sub>(BR)DSS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 250 μA	40			V
Gate Threshold Voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>DS</sub> = 250 μA	3.4		5.0	
Gate-Body Leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V			1	μA
		V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 125 °C			50	
		V <sub>DS</sub> = 40 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 175 °C			150	
On-State Drain Current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> = 5 V, V <sub>GS</sub> = 10 V	50			A
Drain-Source On-State Resistance <sup>a</sup>	r <sub>DS(on)</sub>	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A		0.0049	0.006	Ω
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 125 °C			0.009	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 175 °C			0.012	
Forward Transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = 15 V, I <sub>D</sub> = 15 A	20	50		S
<b>Dynamic<sup>b</sup></b>						
Input Capacitance	C <sub>iss</sub>	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 25 V, f = 1 MHz		6700		pF
Output Capacitance	C <sub>oss</sub>			600		
Reverse Transfer Capacitance	C <sub>rss</sub>			320		
Total Gate Charge <sup>c</sup>	Q <sub>g</sub>	V <sub>DS</sub> = 20 V, V <sub>GS</sub> = 10 V, I <sub>D</sub> = 50 A		95		nC
Gate-Source Charge <sup>c</sup>	Q <sub>gs</sub>			37		
Gate-Drain Charge <sup>c</sup>	Q <sub>gd</sub>			21		
Gate Resistance	R <sub>g</sub>	f = 1.0 MHz		1.7		Ω
Turn-On Delay Time <sup>c</sup>	t <sub>d(on)</sub>	V <sub>DD</sub> = 20 V, R <sub>L</sub> = 0.4 Ω I <sub>D</sub> = 50 A, V <sub>GEN</sub> = 10 V, R <sub>g</sub> = 2.5 Ω		20	30	ns
Rise Time <sup>c</sup>	t <sub>r</sub>			95	145	
Turn-Off Delay Time <sup>c</sup>	t <sub>d(off)</sub>			50	75	
Fall Time <sup>c</sup>	t <sub>f</sub>			12	20	
<b>Source-Drain Ciode Ratings and Characteristics (T<sub>C</sub> = 25 °C)<sup>b</sup></b>						
Continuous Current	I <sub>s</sub>				50	A
Pulsed Current	I <sub>SM</sub>				100	
Forward Voltage <sup>a</sup>	V <sub>SD</sub>	I <sub>F</sub> = 30 A, V <sub>GS</sub> = 0 V		0.90	1.50	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 30 A, di/dt = 100 A/μs		40	60	ns

## Notes:

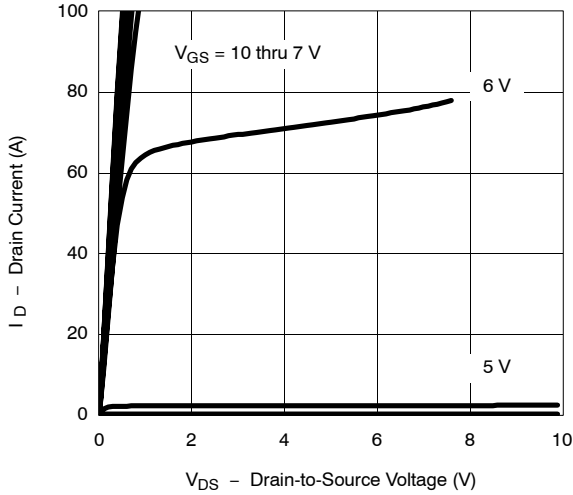
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.
- Guaranteed by design, not subject to production testing.
- Independent of operating temperature.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

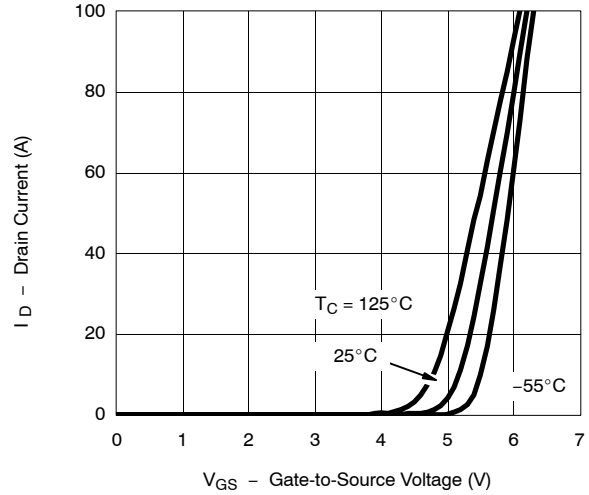


**TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)**

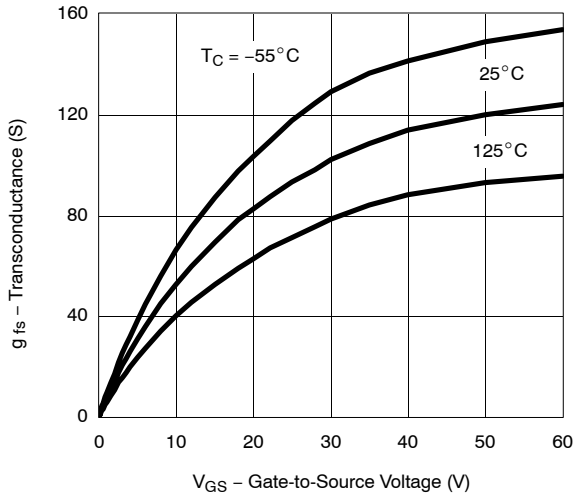
**Output Characteristics**



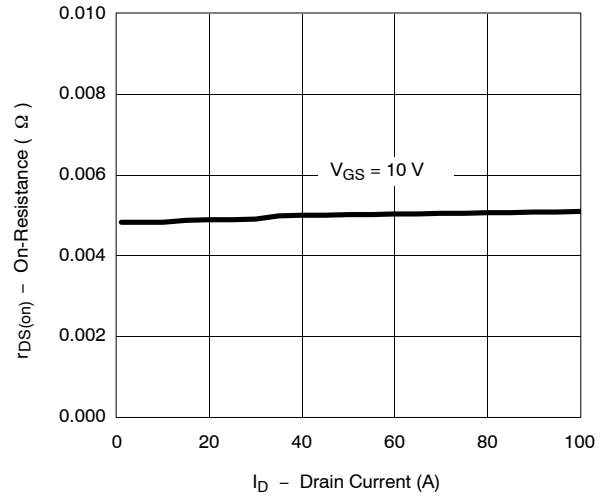
**Transfer Characteristics**



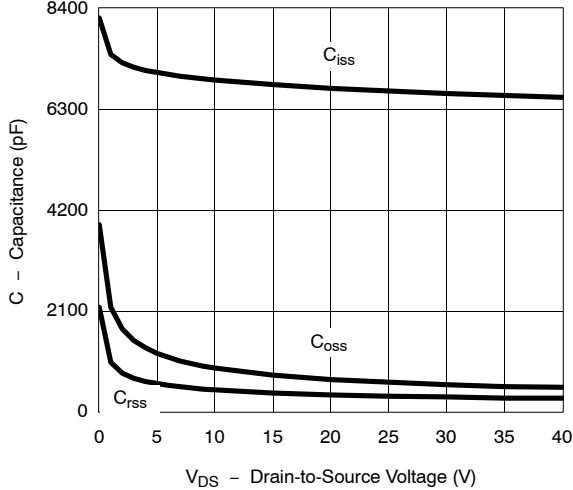
**Transconductance**



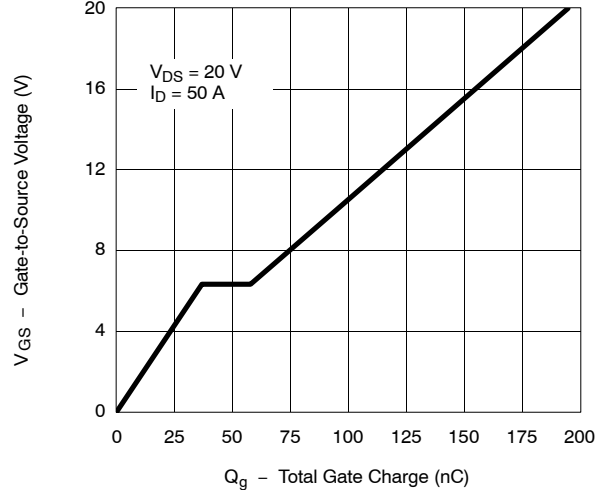
**On-Resistance vs. Drain Current**



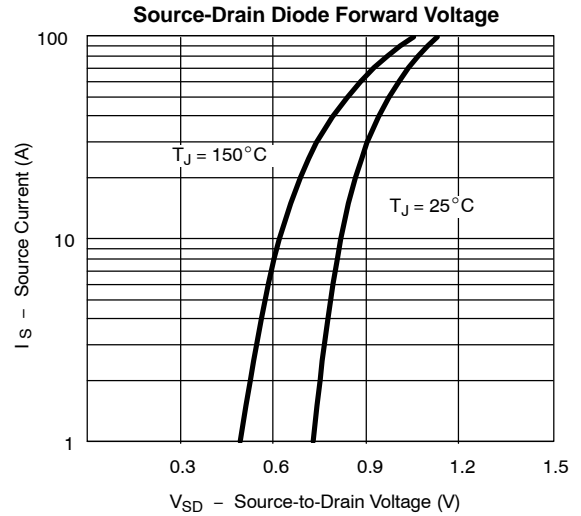
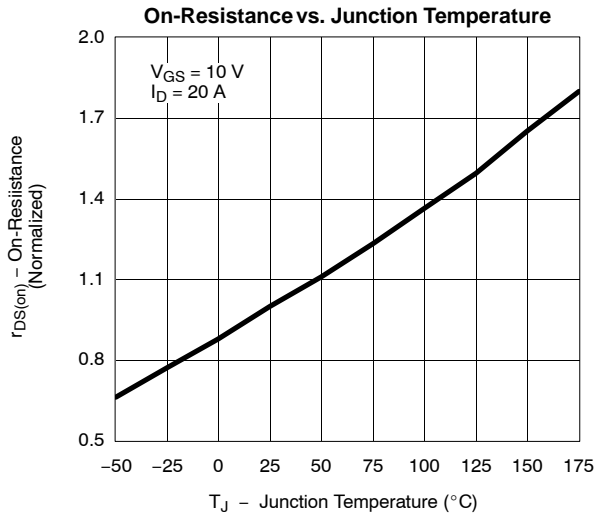
**Capacitance**



**Gate Charge**



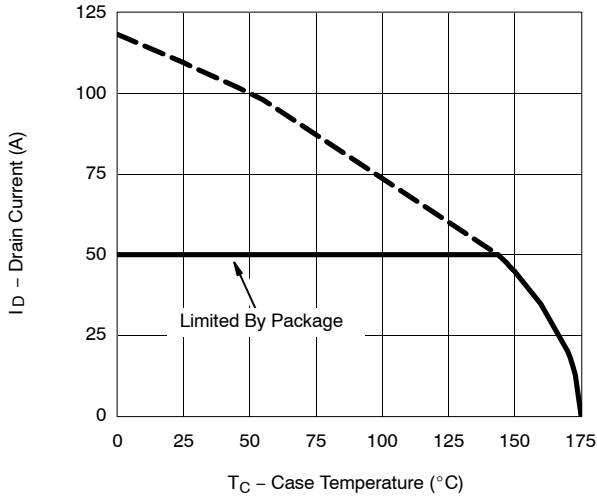
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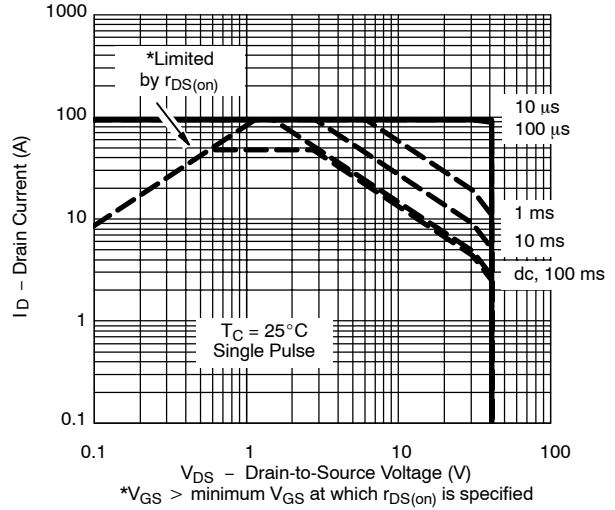


**THERMAL RATINGS**

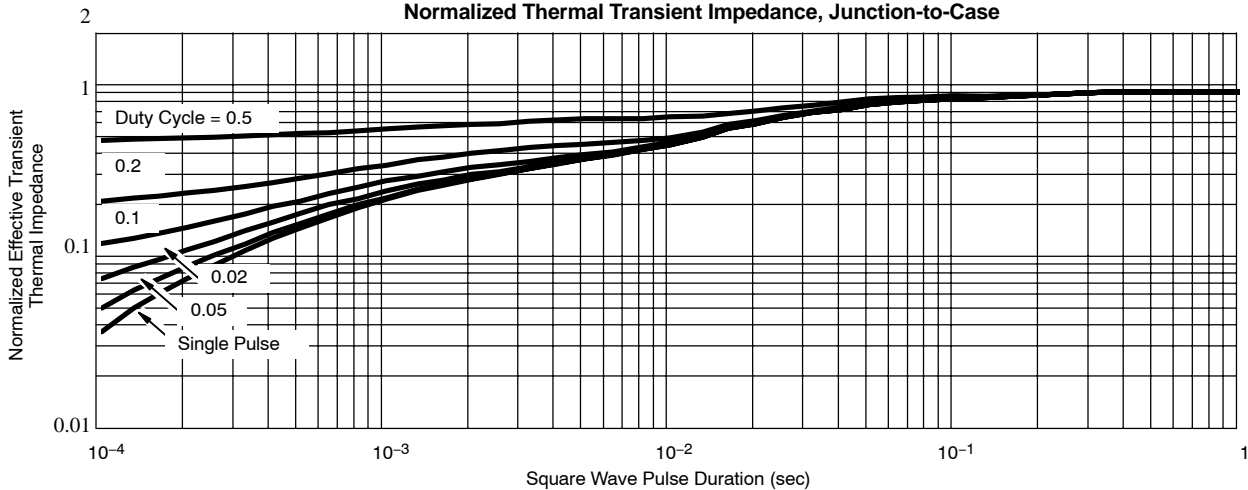
**Maximum Avalanche and Drain Current vs. Case Temperature**



**Safe Operating Area**



**Normalized Thermal Transient Impedance, Junction-to-Case**



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