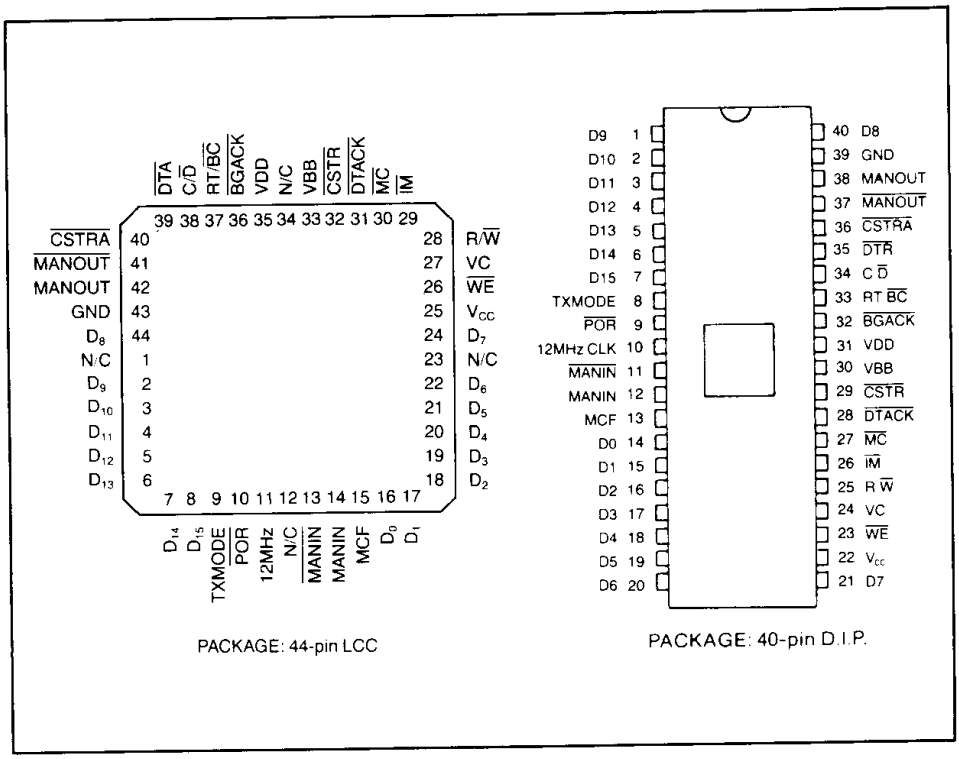
MIL-STD-1553B "SMART®"

FEATURES

- ☐ Support of MIL-STD-1553B
- ☐ Operates as both Remote Terminal and Bus Controller
- ☐ Manchester II Serial Biphase Input/Output
- ☐ 16 bit Microprocessor compatible
- ☐ Command/Data Sync Detection/Identification
- ☐ Automatic Command Response Generation
- ☐ On-Chip Address Recognition
- ☐ Error Detection For:
  - Sync Errors
  - Parity Errors
  - Word Count Errors
  - Bit Count Errors
  - Invalid Manchester Code
  - Incorrect Address
  - Incorrect Bus Response Time
- ☐ TTL Compatible
- ☐ Recognizes Mode Codes and Broadcast Commands
- ☐ Provides DMA handshaking signals
- ☐ COPLAMOS® n-Channel MOS Technology

PIN CONFIGURATION



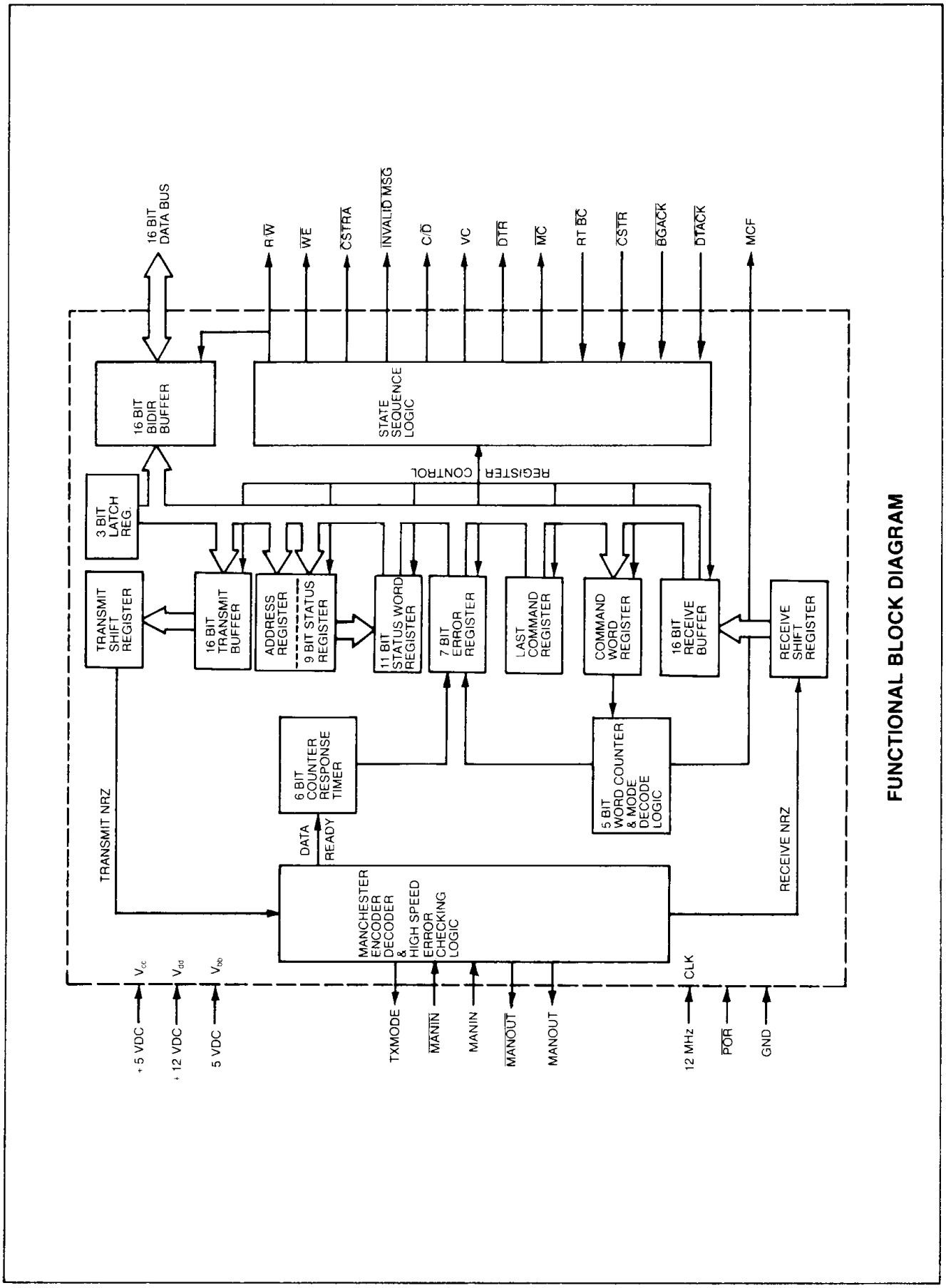
GENERAL DESCRIPTION

The COM1553B SMART® (Synchronous Mode Avionic Receiver-Transmitter) is a 40-pin COPLAMOS® n-Channel MOS/VLSI circuit designed to simplify the interface of a microprocessor or buffer to the serial MIL-STD-1553B data bus.

The COM1553B is a double buffered serial to parallel, parallel to serial converter. It receives serial Manchester II biphase encoded data from a 1553B bus receiver and converts it to 16 bit parallel data. When receiving Manchester II data, the COM1553B detects and identifies sync polarity, reconstructs the clock, detects zero crossing, checks for the proper number of bits and performs a parity check on the incoming data. In addition to parity check, the COM1553B also checks for sync errors, invalid Manchester code, improper word count, incorrect address and incorrect bus response time. The transmitter in turn, accepts 16 bits parallel data and serially transmits it as Manchester II data, appending the appropriate sync and parity.

The COM1553B recognizes protocol commands, and automatically generates the proper response, thereby offloading what otherwise would be microprocessor tasks. This feature eliminates critical software timing requirements.

The COM1553B is designed to work both as a Bus Controller and Remote Terminal, making it universal within the MIL-STD-1553B environment. The COM1553B automatically loads and recognizes its own address. It determines the type of transfer required in both the Bus Controller and Remote-Terminal modes and generates the proper control signals to complete the transfer. It automatically transmits the status word and detects message errors and mode commands. Furthermore, it generates the control signals for DMA operation, therefore eliminating processor intervention.



FUNCTIONAL BLOCK DIAGRAM

DESCRIPTION OF PIN FUNCTIONS

PIN NO.	NAME	SYMBOL	FUNCTION
1-7, 14-21, 40	16-bit Data Bus	D0-D15	Three-state bidirectional data lines used to transfer Command, Data, Error and Status Words between the COM1553B and external memory.
8	Transmit Mode	TXMODE	This output signal when high indicates that the COM1553B is transmitting information on the 1553B bus.
9	Power On Reset	$\overline{POR}$	Input signal used to initialize or reset the Error registers. The RT address must be reloaded after POR is issued.
10	12 MHz Clock	12 MHz CLK	12 MHz clock input.
11	Complementary Manchester In	$\overline{MANIN}$	This input is low when there is no data on the bus. A high level indicates that the data is in its negative state (Refer to receive waveform, figure 3).
12	Manchester In	MANIN	This input is low when there is no data on the bus. A high level indicates that the data is in its positive state (Refer to receive waveform, figure 3).
13	Mode Code Flag	MCF	Output signal that is active high when a mode command (all 1's or all 0's in subaddress) has been detected.
22	Power Supply	VCC	+ 5 volts DC supply.
23	Write Enable	$\overline{WE}$	Output signal. When low, $\overline{WE}$ indicates that the data on the 16 bit data bus is stable and can be written into the external memory.
24	Valid Command	VC	Output signal that is pulsed high to signify the reception of a valid command.
25	Read Write	R $\overline{W}$	Output signal that indicates whether a DMA transaction is a COM1553B read (when high) or a write (when low) operation.
26	Invalid Message	$\overline{IM}$	Output signal which is pulsed low at the same time as MC to indicate that a message error has occurred. IM is also pulsed low while MC remains high if there are errors in the Command word with matching address.
27	Message Complete	$\overline{MC}$	Output signal used as either an interrupt or flag to the processor whenever a COM1553B transaction has been completed.
28	Data Transfer Acknowledge	$\overline{DTACK}$	This input signal when low indicates that the Data Transfer Request ($\overline{DTR}$) and $\overline{BGACK}$ has been acknowledged and data is on the data bus.
29	Command Strobe	$\overline{CSTR}$	This input signal when low is used to inform the COM1553B that a Command Control Code is available in external memory. When the COM1553B is ready, it issues a Command Strobe Acknowledge and initiates a memory read cycle to load the Command Control Code bits CB2-CB0.
30	Power Supply	VBB	- 5 volts DC supply voltage.
31	Power Supply	VDD	+ 12 volts DC supply.
32	Bus Grant Acknowledge	$\overline{BGACK}$	This input signal, when low, indicates that the processor has acknowledged $\overline{DTR}$ and relinquished the data bus.
33	Remote Terminal Bus Controller	RT $\overline{BC}$	When this input is high the COM1553B operates as a Remote Terminal. When RT $\overline{BC}$ is low, the COM1553B operates as a Bus Controller.
34	Command Data	C $\overline{D}$	This output signal during memory write operations indicates either a Command or Data Word transfer. A low level indicates that the COM1553B is writing a Data Word, Status Word, the contents of the Error Register, or the contents of the Last Command Register into external memory. A high level indicates that the transferred word is a Command Word. During memory read operations this output is low. It goes high to indicate that data has been latched internally and the read operation is completed.
35	Data Transfer Request	$\overline{DTR}$	Output signal that initiates a DMA transfer with the processor.
36	Command Strobe Acknowledge	$\overline{CSTRA}$	This output pulse acknowledges the receipt of the command strobe and initiates the Command Control Code (CB2-CB0) transfer.
37	Complementary Manchester Output	$\overline{MANOUT}$	This output signal is high when the COM1553B is not transmitting. A low level indicates that output data is in a positive state (refer to driver waveform, figure 4).
38	Manchester	MANOUT	This output signal is high when the COM1553B is not transmitting. A low level indicates that output data is in a negative state (refer to driver waveform, figure 4).
39	Ground	GND	Ground

FUNCTIONAL DESCRIPTION

The COM1553B is organized into the following five sections:

Manchester Encoder/Decoder

This section performs the manchester encoder and decoder functions and code error check. The receiver continuously monitors the MANIN and the $\overline{\text{MANIN}}$ input lines for a valid sync. After the reception of the 3 bit sync, the receiver is in full synchronization. It then checks for transition errors and correct (odd) parity. If an error is detected in the Command Word the receiver resets itself, pulses IM and waits for another valid sync. If any errors are detected in Data and Status Words, the appropriate error bits in the Status and Error register are set.

The transmitter section encodes the NRZ data from the data bus into Manchester II and appends, depending on word type, the proper sync and parity.

State Sequencer Logic

The State Sequencer section generates the appropriate signals to various internal sections to control the overall device operation.

Inputs to the State Sequencer which establish its operational modes are as follows:

Remote Terminal/Bus Controller (RT/$\overline{\text{BC}}$)

Determines whether the data terminal is operating as a Remote Terminal or as a Bus Controller. As a result of Dynamic Bus Allocation, any terminal shall be capable of performing either function at different times.

Command Control Code bits D2-D0 (CB2-CB0)

These Command Control Code bits determine the type of memory operation the COM1553B will execute. Transfer of these commands to the COM1553B are initiated by asserting Strobe Command ($\overline{\text{CSTR}}$) low. This informs the COM1553B that a command is available in external memory. When the COM1553B acknowledges the $\overline{\text{CSTR}}$ signal, it sets the $\overline{\text{CSTRA}}$ output low. The $\overline{\text{CSTR}}$ must be reset within 1.5 μs after $\overline{\text{CSTRA}}$. The COM1553B then initiates a memory read cycle by setting R/$\overline{\text{W}}$ high, C/$\overline{\text{D}}$ low, and DATA TRANSFER REQUEST ($\overline{\text{DTR}}$) low. When the Command Control Code bits are valid on the bidirectional data bus (D2-D0), $\overline{\text{DTACK}}$ and $\overline{\text{BGACK}}$ are generated by the processor and these bits are loaded into the COM1553B 3-bit latch decode register. The command is then decoded in accordance with Table A. Timing associated with loading these control bits into the COM1553B is shown in Figure 1.

Transmit Last Command

Allows the State Sequencer to bypass a memory read cycle to external memory and transmit the Last Command from the TRLC register following the Status Word transmission.

Broadcast

When the address field of the Command Word is all ones (11111), the State Sequencer is informed that a Bus Controller or a Remote Terminal is transmitting a Broadcast Command.

Word Count Zero

Input from the 5-bit counter and count decode logic informing the State Sequencer that all Data Word memory cycles are complete.

Sync Input

Indicates the type of sync word just strobed into the receive register.

Address Compare

When programmed as a Remote Terminal, the COM1553B compares the contents of the address register with the address field of the received Command Word. If the addresses compare, the State Sequencer will respond to the received command.

Any Error

This input to the State Sequencer indicates that one of the seven possible errors have been set in the error register at the end of a message (Refer to Error register).

Contiguous Word

Set if there is a transition 2 μs. after the parity transition of the last word, this signifies that a contiguous word follows the word presently in the receive register (Refer to figure 5).

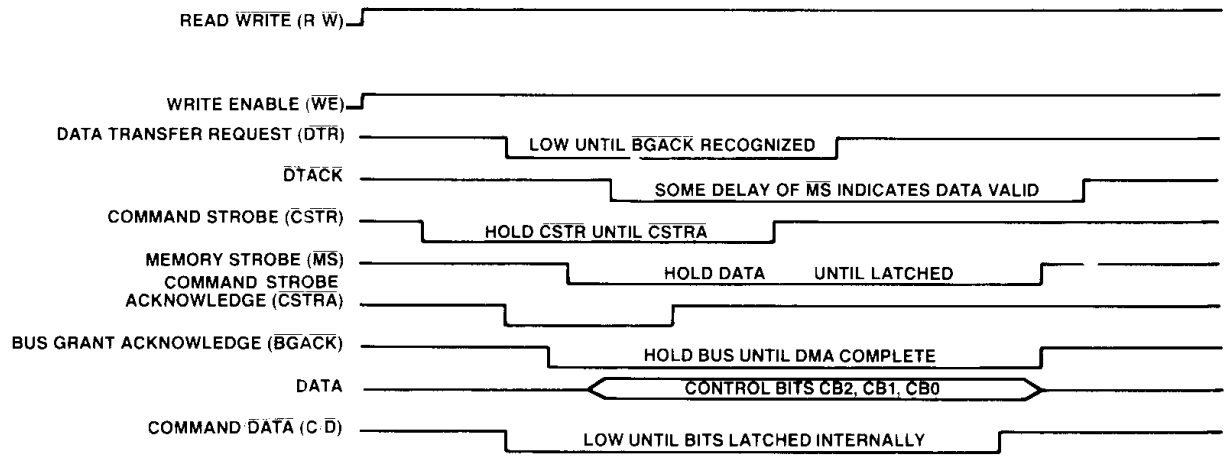


FIGURE 1:
BUS CONTROLLER TIMING SEQUENCE

Loading the Command Control Code Bits into the COM1553B prior to transmitting a Command or initiating a Diagnostic Sequence.

Error Detection Logic

The error detection logic of the COM1553B detects the following errors:

Improper Sync

One or more words have been received with incorrect sync polarity (For example a Status Word with Data Sync).

Invalid Manchester II Code

One or more words have been received with a missing transition during the 17 μs. data and parity bit time.

Information Field Greater Than 16 Bits

The decoder has detected a transition within one bit time (1 μs.) following the parity bit in one or more words.

Odd Parity Error

One or more words have been received with a parity error.

Improper Word Count

An improper word count error occurs when the number of Data Words received is not equal to the number of words indicated in the word count field of the Command Word. In the case of a Mode Code without data, no Data Words should follow the Mode command. Mode Codes with data should consist of only one Data Word. If the contents of the word counter are not zero, and there is no contiguous Data Word, then the receive message is considered incomplete (e.g., fewer words were received than indicated by the word count in the Command word). If the contents of the word counter are zero and there is a transition detected 2 μs. after the parity transition of the last Data Word, then this also will cause an improper word count. In either case, the Message Error bit of the Status Word is set and not transmitted and the invalid message ($\overline{IM}$) output pin pulsed at the same time as the message complete ($\overline{MC}$) signal output.

Response Time

The amount of time between the end of transmission of a Command or Data Word and the Status Word reply by a Remote Terminal should be less than 14 μs. If the response is greater than 14 μs. the response error bit is set in the error register.

Address Mismatch

An address mismatch occurs when a Bus Controller detects a mismatch between the address of the Status Word reply from a Remote Terminal and the Remote Terminal address of the Command.

Internal Register Description

Remote Terminal Address And Status Code Register

This register is loaded when the processor issues a load Remote Terminal Address (RTA) command. The word that is loaded in this register consists of 9 bits of status information (D0-D8) and the 5-bit address (D11-D15). The Remote Terminal Address may be checked any time by reading out the Error register. The RTA and Status Code register must be loaded before the COM1553B may respond as a Remote Terminal.

Table 1 defines the data bus bits which correspond to the Remote Terminal Address and Status Code register and Status Word that transmitted. Bits D0, D2, D3 and D8 are double buffered to allow the RT to retain this information after the Status Code register is updated. For all legal commands, other than Transmit Last Status and Transmit Last Command Mode command, the Status Word register is updated with these four bits, Any Error and the Broadcast flag. The Dynamic Bus Control and Terminal Flag bits are modified by the appropriate Mode Code commands whereas, the Broadcast Flag and Any Error bits are set by the COM1553B internal logic. The Reserved Bits and the RT address bits are transferred directly into the Status Word register during the RTA and Status Code command.

Bits D0, D2, D3, and D5-D9 are cleared after transmission for all commands except Transmit Last Status and Transmit Last Command Mode Code.

TABLE A:
COMMAND CONTROL CODE BIT DEFINITION

	DATA BITS													CONTROL BITS CB2-CB0			
RT/$\overline{BC}$	D_{15}	D_{14}	D_{13}	D_{12}	D_{11}	D_{10}	D_9	D_8	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	FUNCTION
X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	1	X	READ DATA REGISTER
X	X	X	X	X	X	X	X	X	X	X	X	X	X	1	0	X	LOAD RT ADDRESS REGISTER AND STATUS CODE REGISTER
X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	0	READ LAST CMD
X	X	X	X	X	X	X	X	X	X	X	X	X	X	0	0	1	READ ERROR AND REMOTE TERMINAL ADDRESS REGISTERS
0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	0	BUS CONTROLLER TRANSMISSION
0	X	X	X	X	X	X	X	X	X	X	X	X	X	0	1	1	BUS CONTROLLER RT TO RT TRANSFER

X—DON'T CARE

TABLE 1

Data Bus Bit	RTA and Status Code Reg. Bits	Internal Logic Signals	Status Word Transmitted
D15 (MSB)	RTA Bit 4 (MSB)	—	RTA Bit 4 (MSB)
D14	RTA Bit 3	—	RTA Bit 3
D13	RTA Bit 2	—	RTA Bit 2
D12	RTA Bit 1	—	RTA Bit 1
D11	RTA Bit 0 (LSB)	—	RTA Bit 0 (LSB)
D10	Not used	Any Error	Message Error
D9	Instrumentation Bit	—	Instrumentation
D8	Service Request Bit	—	Service Request
D7	Reserved	—	Reserved
D6	Reserved	—	Reserved
D5	Reserved	—	Reserved
D4	Not Used	Broadcast Flag	Broadcast Flag
D3	Busy	—	Busy
D2	Subsystem Flag Bit	—	Subsystem Flag
D1	Dynamic Bus Control Acceptance Enable Bit (See Note)	Dynamic Bus Mode Code command	Dynamic Bus Control Bit
D0 (LSB)	Terminal Flag Enable Bit (See Note)	Inhibit Terminal Flag (set) or Override Terminal Flag (reset) Mode Code command	Terminal Flag

Note: When the Dynamic Bus Control Acceptance Enable bit is set, the RT will accept a Dynamic Bus Mode code request. If this bit is reset the RT will reject a Dynamic Bus Mode Code command request. The Terminal Flag Bit (if enabled) is only set high if no Inhibit Terminal Mode Code command has been received, or if an Override Inhibit Terminal bit command is received.

Last Command Word Register

The last valid Command Word received by a Remote Terminal is stored in an internal 16 bit Last Command Register. This makes it readily available for transmission onto the data bus whenever the Remote Terminal receives a Mode Command to transmit the last Command Word. The Last Command Register contents are automatically written into external memory following a receive or a transmit message.

As a bus controller (BC), the Last Command Register is used to hold the command transmitted before the present command. In RT-RT transfers this register of the BC holds the receive command while the transmit command is being transmitted.

The processor has the option of reading the Last Command Register of either a bus controller or remote terminal, by issuing a Read Last Command Register command code.

Error Register And RTA Register (Error Register)

A 7-bit error register is provided in the COM1553B to hold any errors associated with the previous message. If one or more of the 7 error types exists, the COM1553B asserts the Invalid Message output pin ($\overline{IM}$) at the same time that Message Complete ($\overline{MC}$) is asserted, cueing either a Remote Terminal or a Bus Controller that an error occurred in the previous message. If desired, the processor may read out the 16-bit error word by issuing a read error register command code. When operating as a Remote Terminal, the COM1553B will write the Receive register, Error register and Last Command register automatically into external memory at the end of each command message because these registers may change before the processor has determined the necessity of reading them. The Error register may be read anytime during a message except during message transfers.

TABLE 2

The 16-bit error word is defined as follows:

DATA BUS LINE	ERROR BIT DEFINITION
D15	RT Address Bit 4
D14	RT Address Bit 3
D13	RT Address Bit 2
D12	RT Address Bit 1
D11	RT Address Bit 0
D10	Unused
D9	Improper Sync
D8	Address Mismatch Error
D7	Improper Word Count
D6	Response Time Error
D5	Information Field > 16 Bits
D4	Unused
D3	Invalid Manchester II
D2	Parity Error
D1	Unused
D0	Unused

*Unused bits are set high.

Mode Detection Logic

Both receive and transmit Command Words for a Remote Terminal and Bus Controller are decoded by the Mode Detection Logic. The Mode Detection Logic examines the following Command Word field to establish the correct operating mode for the COM1553B (Refer to TABLE B).

Subaddress/Mode Code Field (D5-D9) and Data Word Count/Mode Code (D0-D4)

This field Determines if the command is a normal command or a Mode command. A subaddress field of 00000 or 11111 implies a Mode command. All other codes are interpreted as a subaddress. Once a Mode Command is detected the most significant bit of the Data Word Count/Mode Code field is decoded. A most significant bit of "zero" implies no associated data with the Code Command. A "one" in this position implies that a Data Word will follow.

The COM1553B recognizes five Mode Code commands (Refer to TABLE B). Transmit Last Command or Transmit Last Status word Mode Code commands, when received by the COM1553B, will automatically transfer the contents of the Transmit Last Command or Transmit Last Status register onto the 1553B serial bus.

The Override/Inhibit Terminal Flag and Dynamic Bus Control Mode Code commands, when received by the COM1553B, may change the state of the Terminal Flag and Dynamic Bus Control bits of the Status Word register. The Inhibit Terminal Flag Bit Mode Code command resets the Terminal Flag bit.

The Override Inhibit Terminal Flag Mode Code command enables the Terminal Flag bit if it was previously disabled. Finally, Dynamic Bus Control Mode Code command sets the Dynamic Bus Control bit in the Status Word if the Dynamic Bus Control Enable bit is high. If the enable bit is low, the Dynamic Bus Control bit in the Status Word remains low when a Dynamic Bus Control Mode Code command is received.

Broadcast Mode Code

Broadcast Mode Code Commands are acknowledged if the T/$\overline{R}$ bit is low. If the T/$\overline{R}$ bit is high all Broadcast Mode Code commands without associated Data words are acknowledged except Dynamic Bus Control and Transmit Last Status Word.

Illegal Broadcast Commands are not acknowledged; the IM output pin is, however, pulsed low.

TABLE B
MODE CODE DEFINITION

FUNCTION	DETECT CONDITION	DETECTED BY	SPECIAL CONDITIONS	COMMENTS
Broadcast	All ones in RT address field of CMD WD	Broadcast Decode Logic	Status word is written into Memory but not transmitted	Address compare must recognize all ones as Broadcast
Mode Codes	All zeros or ones in sub-address field of CMD WD	Mode Code Decode Logic	MSB of Word Count 0 = No data Word 1 = With Data Word	Word Count is Decoded as mode code
(1) Dynamic Bus Control			Word Count Field = 00000	Dynamic Bus Accept Bit of Status word enabled for transmission
(2) Transmit Last Status Word			Word Count Field = 00010	Status Word remains unchanged
(3) Inhibit Terminal Flag Bit			Word Count Field = 00110	Terminal Flag Bit of Status word inhibited until overriden
(4) Override Inhibit Terminal Flag Bit			Word Count Field = 00111	Removes Inhibit from Terminal Flag Bit of Status Word
(5) Transmit Last Command			Word Count Field = 10010	Status Word Transmitted followed by Last Command Register. Status Word remains unchanged.

OPERATION

When operating as either a Bus Controller or Remote Terminal, the COM1553B decodes the Command Word and determines the type of message transfer. Having determined the type of message transfer, the COM1553B generates the proper control and timing signals to complete the transfer (refer to Figure 2). The types of messages are listed below:

1) Bus Controller to Remote Terminal
2) Remote Terminal to Bus Controller
3) Remote Terminal to Remote Terminal
4) Mode Code without Data Word
5) Mode Code with Data Word (transmit)
6) Mode Code with Data Word (receive)
7) Broadcast Bus Controller to Remote Terminal
8) Broadcast Remote Terminal to Remote Terminal
9) Broadcast Mode Code without data
10) Broadcast Mode Code with data

Bus Controller Transaction (RT/$\overline{BC}$ of the COM1553B set low)

The following section describes each 1553B information transfer format from the Bus Controller viewpoint. A table showing external memory operation is also provided for each message format.

Note that all MIL-STD-1553B serial bus activity is initiated by the Bus Controller.

Bus Controller-to-Remote Terminal Transfer (BC to RT)

This message format covers transactions where the Bus Controller transmits a receive Command and Data Words to a Remote Terminal. Initializing the COM1553B is accomplished by the processor loading an external memory address counter with the starting address of the COM1553B memory control block (address where the Command Control Code CB2-CB0 resides). The Bus Controller processor next issues a Command Strobe ($\overline{CSTR}$) and holds it low until the COM1553B issues a Command Strobe Acknowledge ($\overline{CSTRA}$). The COM1553B then responds with a Data Transfer Request ($\overline{DTR}$) which initiates a normal memory cycle.

Refer to figure 1 for timing associated with loading the Command Control Codes (CB2-CB0) into the COM1553B prior to transmitting the Command Word.

The first memory cycle loads the Command Control Code bits CB2-CB0 from external memory into the COM1553B functioning as Bus Controller (BC). The BC decodes this command to determine the type of memory transaction to perform (refer to TABLE A). The next read cycle loads the Command Word into the BC command register and then transmits it onto the 1553B bus. This Command Word, while in the command register, determines the BC mode of operation. The BC then completes this BC to RT transaction by issuing a predetermined number of read cycles (determined by the value in the word count field of the Command Word) and transmitting the data onto the 1553B bus. After transmission of the last Data word, the BC initializes its response timer, expecting a Status Word from the remote terminal within 14 μs.

After the reception of the Status Word, the BC initiates a memory write cycle which writes the Status Word into the external memory. If the BC doesn't receive the Status Word within the allowed response time the message error bit is set.

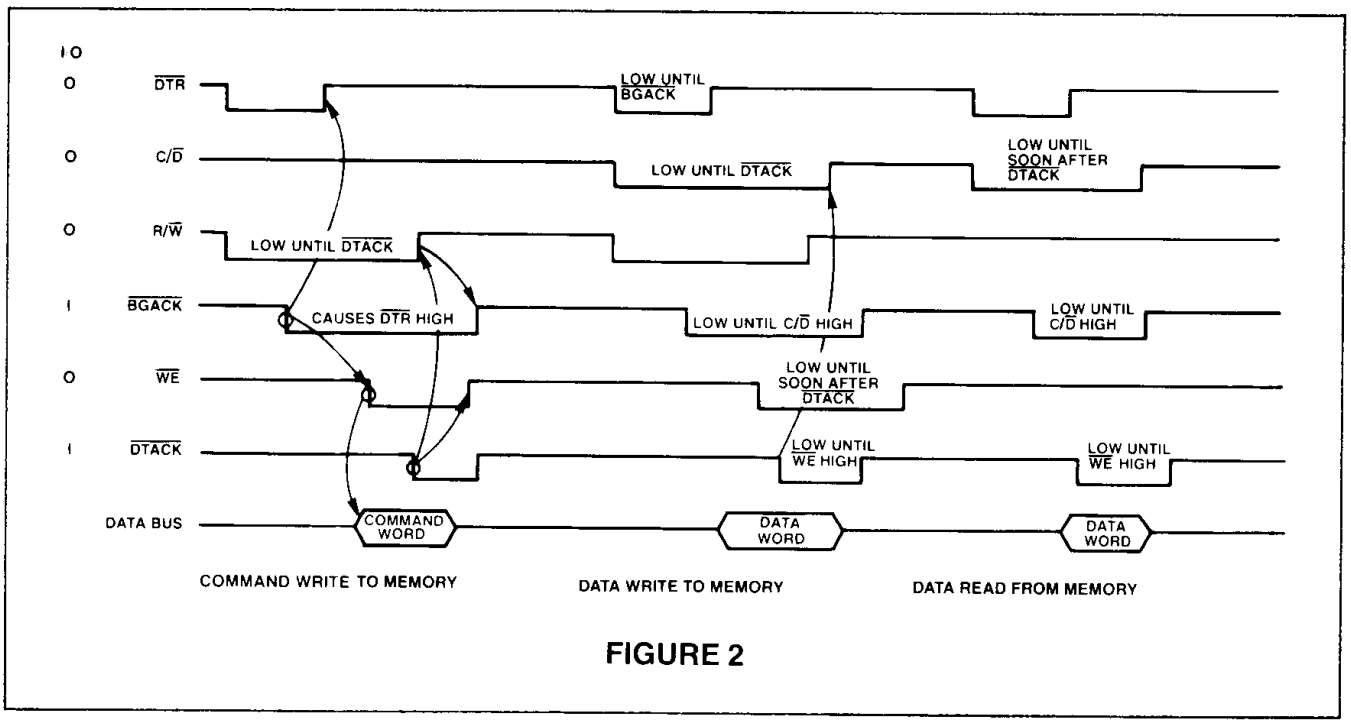


FIGURE 2

TABLE 3
BC to RT (The BC transmits a receive command to the RT)

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX2_H$	READ*
2	RECEIVE COMMAND	READ
3	DATA	READ
•	DATA	READ
•	DATA	READ
34	DATA	READ
	**	
35	STATUS	WRITE

*reads command control code bits CB2-CB0
** response time
X = don't care

Remote Terminal Transfer to Bus Controller

This message format covers transactions where the Bus Controller sends a transmit command to a Remote Terminal and requests data from it. Initialization of the BC for normal memory cycles is the same as the previous transfer. The difference between this transfer and the previous transfer is that after the Command Word is transmitted, the BC waits 14 μs for the Status Word and the requested number of Data Words. The Status and Data Words are written into external memory via write cycles as they are received by the BC.

TABLE 4
BC to RT (The BC transmits a Transmit Command to an RT)

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX2_H$	READ*
2	TRANSMIT COMMAND	READ
	**	
3	STATUS	WRITE
4	DATA	WRITE
•	DATA	WRITE
•	DATA	WRITE
35	DATA	WRITE

*reads command control code bits CB2-CB0
** response time
X = don't care

RT-to-RT Transfer

In this message format, the Bus Controller first issues a receive Command Word to the receiving Remote Terminal, followed by a transmit Command Word to the transmitting terminal. Next, the transmitting RT responds with a Status Word and the requested number of Data Words to both the receiving RT and BC. The receiving RT at the end of the message sends a Status Word to the BC. As Status and Data Words are received by the BC they are written into external memory.

TABLE 5
RT to RT

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX3_H$	READ*
2	RECEIVE COMMAND	READ
3	TRANSMIT COMMAND	READ
4	STATUS (transmitting RT)	WRITE
5	DATA	WRITE
•	DATA	WRITE
•	DATA	WRITE
36	DATA	WRITE
	**	
37	STATUS (receiving RT)	WRITE

*reads command control code bits CB2-CB0
** response time
X = don't care

Mode Code Command without Data

The Bus Controller transmits a specific Mode Command and expects a Status Word back from the addressed Remote Terminal.

TABLE 6

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX2_H$	READ*
2	COMMAND	READ
	**	
3	STATUS	WRITE

*reads command control code bits CB2-CB0
**response time
X = don't care

Mode Command with Data (BC receives a single word)

In this mode the Bus Controller issues a transmit Mode Command to an RT. The addressed Terminal responds to the Bus Controller with a Status Word and a single Data Word.

TABLE 7

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX2_H$	READ*
2	COMMAND	READ
	**	
3	STATUS	WRITE
4	DATA	WRITE

*reads command control code bits CB2-CB0
**response time
X = don't care

Mode Command with Data
(BC transmits a single word)

The Bus Controller issues a receive Mode Command and one Data Word to a Remote Terminal. A Status Word is returned by the Remote Terminal to the Bus Controller.

TABLE 8

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX2_H$	READ*
2	COMMAND	READ
3	DATA	READ
	**	
4	STATUS	WRITE

*reads command control code bits CB2-CB0
**response time
X = don't care

Bus Controller (Broadcast) to Remote Terminal Transfer

In this mode the Bus Controller issues a Broadcast Command followed by a number of Data Words. In all Broadcast Command transfers a BC will not expect to receive a Status Word back.

TABLE 9

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX2_H$	READ*
2	RECEIVE COMMAND	READ
3	DATA	READ
•	DATA	READ
•	DATA	READ
34	DATA	READ

*reads command control code bits CB2-CB0
** response time
X = don't care

RT to RT Transfer (Broadcast)

This transfer is similar to the normal RT to RT transfer with the exception that the Status Word is not returned by the receiving RT.

TABLE 10

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	$XXX3_H$	READ*
2	RECEIVE COMMAND	READ
3	TRANSMIT COMMAND	READ
	**	
4	STATUS	WRITE
5	DATA	WRITE
•	DATA	WRITE
•	DATA	WRITE
36	DATA	WRITE

*reads command control code bits CB2-CB0
**response time
X = don't care

THE FOLLOWING NOTE APPLIES TO THE CURRENT VERSION OF THE COM 1553B:

When operating as a Bus Controller in a RT (Remote Terminal) to RT transfer, the COM1553B may incorrectly set the Invalid Sync Bit in the Error Register if the status word response from the receiving RT occurs between 4 and 7 microseconds.

The Bus Controller (BC) may confirm that an error free message transmission occurred by requesting that the receiving RT transmit the last status word. If this status word matches the previous status word, then an error-free transmission occurred.

Remote Terminal Transaction (RT/$\overline{BC}$ input of the COM1553B set high)

The following section addresses each COM1553B information transfer format from the Remote Terminal viewpoint.

Bus Controller to Remote Terminal Transfer
(BC to RT, where RT receives data)

In this transfer the COM1553B designated as the RT receives a command to receive data. As the Command Word is completely shifted into the receive shift register, the RT compares the Command Word address field with the preloaded Remote Terminal address. This determines if the message is addressed to the receiving RT. If the Command Word is valid, the RT issues a Data Transfer Request ($\overline{DTR}$) to initiate a memory cycle. Once the processor relinquishes control of the data bus, during the Bus Acknowledge ($\overline{BGACK}$) time, the Command Word is placed on the data bus.

The Subaddress field is thereafter decoded by external logic and the Command word is written into external memory. The RT then receives a predetermined number of Data Words (specified by the word count field). As each Data Word is received it is written into external memory. After the reception of the last Data Word the RT transmits the Status Word, the Message Error, Broadcast Flag, Terminal Flag, Subsystem Flag, Busy, and Service Request bits are updated for all commands except for the Transmit Status Word and Transmit Last Command Code commands. While transmitting the Status, the RT writes it into memory. The RT also writes the Last Command Register, Error Register and Receive Register into memory and then asserts Message complete.

Note that the receive register of the RT will contain the transmitted Status Word.

TABLE 11
BC TO RT (RT receives data from BC)

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND	WRITE
2	DATA	WRITE
3	DATA	WRITE
•	•	WRITE
•	•	WRITE
34	DATA **	WRITE
35	STATUS	WRITE
36	LAST COMMAND	WRITE
37	ERROR REGISTER	WRITE
38	RECEIVE REGISTER	WRITE

Remote Terminal-to-Bus Controller Transfer (RT transmits data to BC)

The Remote Terminal receives a Transmit Command Word from the Bus Controller. The RT will then proceed to decode the Command Word, as in the previous case and within the response time transmits the Status Word.

While the Status Word is being transmitted the RT issues a write memory cycle to write the Status Word into external memory. Thereafter, the Data words are read from memory and transmitted. After the last word is transmitted the RT writes the contents of the Last Command Register, Error Register and the Receive Register into memory.

TABLE 12
Remote Terminal to Bus Controller (RT Transmits Data to BC)

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND **	WRITE
2	STATUS	WRITE
3	DATA	READ
•	DATA	READ
•	DATA	READ
34	DATA	READ
35	LAST COMMAND	WRITE
36	ERROR REGISTER	WRITE
37	RECEIVE REGISTER	WRITE

**response time

Remote Terminal-to-Remote Terminal Transfers

From the Remote Terminal viewpoint, RT-to-RT transfers are similar to the RT to BC receive or transmit data transfers. The only exception is that the receiving terminal waits for the first Data Word from the transmitting terminal. This satisfies the protocol requirement that the transmitting terminal first send its status to the controller before it transmits the data to the receiving terminal.

Mode Command with Data (RT receives a Mode Code Command to transmit)

In this transfer, after the Transmit Mode Command is received, the RT transmits the Status and one Data Word.

TABLE 13

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND **	WRITE
2	STATUS	WRITE
3	DATA	READ*
4	LAST COMMAND	WRITE
5	ERROR REGISTER	WRITE
6	RECEIVE REGISTER	WRITE

*For a Transmit Last command Mode Code, Data is not read from memory but transmitted from the internal Last Command register.

** response time

Mode Code Command with Data (RT receives a Mode Command to receive)

This transfer is similar to a Receive Command having only one Data Word.

TABLE 14

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND	WRITE
2	DATA **	WRITE
3	STATUS	WRITE
4	LAST COMMAND	WRITE
5	ERROR REGISTER	WRITE
6	RECEIVE REGISTER	WRITE

** response time

Bus Controller Broadcast Transfer to RT

The RT receives a Broadcast Command to receive data. If data received during a broadcast message is invalid, the COM1553B will set the message error bit.

TABLE 15
RT RECEIVE

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND	WRITE
2	DATA	WRITE
•	DATA	WRITE
•	DATA	WRITE
32	DATA	WRITE
33	STATUS	WRITE*
34	LAST COMMAND	WRITE
35	ERROR REGISTER	WRITE

*In all broadcast transfers, a memory cycle is shown for the Status Word but the RT does not transmit it on the 1553B bus.

Broadcast Mode Code Command with Data

This Broadcast Mode Code command is detected if the MSB of the word count field is a logical high.

Transmission of the Status Word is suppressed as in the previous case but is loaded into external memory.

TABLE 16
RT RECEIVE

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND	WRITE
2	DATA	WRITE
3	STATUS	WRITE*
4	LAST COMMAND	WRITE
5	ERROR REGISTER	WRITE

*In all broadcast transfers, a memory cycle is shown for the Status Word but the RT does not transmit it on the 1553B bus.

Broadcast Mode Code Command Without Data

This Mode Code command is detected if the MSB of the word count field is zero. This transaction is the same as the previous transfer except that there is no Data Word transfer.

TABLE 17

MEMORY ADDRESS	MEMORY CONTENTS	COM1553B MEMORY OPERATION
1	COMMAND	WRITE
2	STATUS	WRITE*
3	LAST COMMAND	WRITE
4	ERROR REGISTER	WRITE

*In all broadcast transfers, a memory cycle is shown for the Status Word but the RT does not transmit it on the 1553B bus.

Broadcast RT to RT Transfer

For this message transfer a Broadcast Command to receive is issued by the Bus Controller. This is followed by a normal Transmit Command to the transmitting Remote Terminal. The Remote Terminal responds with a normal transmit message format of Status Word and Data Word(s). The receiving terminals do not transmit a Status Word after receiving the data. However, they do go through a memory cycle to load the Status Word into their respective memories.

For the Remote Terminal receive transfer refer to Table 15. The only difference in this transfer is that there is a gap time between the Command and Data word.

For the Remote Terminal transmit transfer refer to Table 12. The only difference in this transfer is that the Receive Register is not written into memory.

MAXIMUM GUARANTEED RATINGS*

Operating Temperature Range ..... −55 to +125°C
Storage Temperature Range ..... −55 to +150°C
Lead Temperature (soldering, 10 seconds) ..... +325°C
Positive Voltage on any pin ..... +15V
Negative Voltage on any pin except VBB, with respect to ground ..... −.3V

*Stresses above those listed may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other condition above those indicated in the operational sections of this specification is not implied.

NOTE: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes or "glitches" on their outputs when the AC power is switched on and off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC ELECTRICAL CHARACTERISTICS $T_A = -55$ to 125°C, $V_{CC} = 5.0V \pm 5\%$, $V_{DD} = 12V \pm 5\%$, $V_{BB} = -5V \pm 5\%$

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
V_{IL}	Input Low Voltage	−0.3		0.8	V	
V_{IH}	Input High Voltage	3		V_{CC}	V	
V_{OL}	Output Low Voltage			0.4	V	$I_{OL} = -3.2$ mA
V_{OH}	Output High Voltage	2.4	4	5	V	$I_{OH} = .8$ mA
I_L	Input Leakage Current			10	µA	
C_{IN}	Input Capacitance		10	25	pf	
C_o	Output Capacitance		10	15	pf	
C_L	Load Capacitance		100	150	pf	
P_W	Power Dissipation		0.8		W	$T_A = 25$°C
I_{DD}				40	mA	
I_{CC}				100	mA	
I_{BB}				5	mA	

AC ELECTRICAL CHARACTERISTICS

	PARAMETER	MIN	TYP	MAX	UNITS	COMMENTS
clk	clock frequency		12		MHz	50% duty cycle
t_r	Clk, rise time		6		ns	
t_f	Clk, fall time		6		ns	
t_1	$\overline{DTR}$ and $\overline{WE}$	0.5	0.6	1	µs	
t_2	$\overline{BGACK}$ to $\overline{DTR}$	0.8	1.3	2	µs	
t_3	$\overline{WE}$ to DATA	50	100		ns	
t_4	$\overline{DTACK}$ to $\overline{WE}$		1.5	2	µs	
t_5	$\overline{DTACK}$ to R/$\overline{W}$		1	1.5	µs	
t_6	$\overline{DTACK}$ to C/$\overline{D}$		1.5	2.5	µs	
t_7	$\overline{CSTR}$ to $\overline{CSTRA}$			673	µs	
t_8	$\overline{CSTRA}$ to $\overline{CSTR}$			1.5	µs	
t_9	$\overline{CSTRA}$ width		500		ns	
t_{10}	C/$\overline{D}$ to DATA	0				
t_{11}	CMD to IM			3.25	µs	
t_{12}	IM width			500	ns	
t_{13}	VC width			1	µs	
t_{14}	VC to IM			1.75	µs	
t_{15}	C/$\overline{D}$ to MC			700	ns	
t_{16}	C/$\overline{D}$ to IM			2.25	µs	
t_{17}	C/$\overline{D}$ to MC			750	ns	
t_{18}	C/$\overline{D}$ to MC			1.25	µs	
t_{19}	CMD to MCF reset			3.75	µs	
t_{20}	CMD to MCF set			4.75	µs	
t_{21}	CMD to VC			2.75	µs	
t_{22}	C/$\overline{D}$ to MCF reset			1.5	µs	
t_{23}	C/$\overline{D}$ to MCF set			1	µs	
t_{24}	POR width	2.5			µs	
t_{25}	Receive CMD to $\overline{DTR}$			4.25	µs	
t_{26}	Transmit CMD to $\overline{DTR}$			5.75	µs	

FIGURE 3:
RECEIVER LOGIC WAVEFORMS

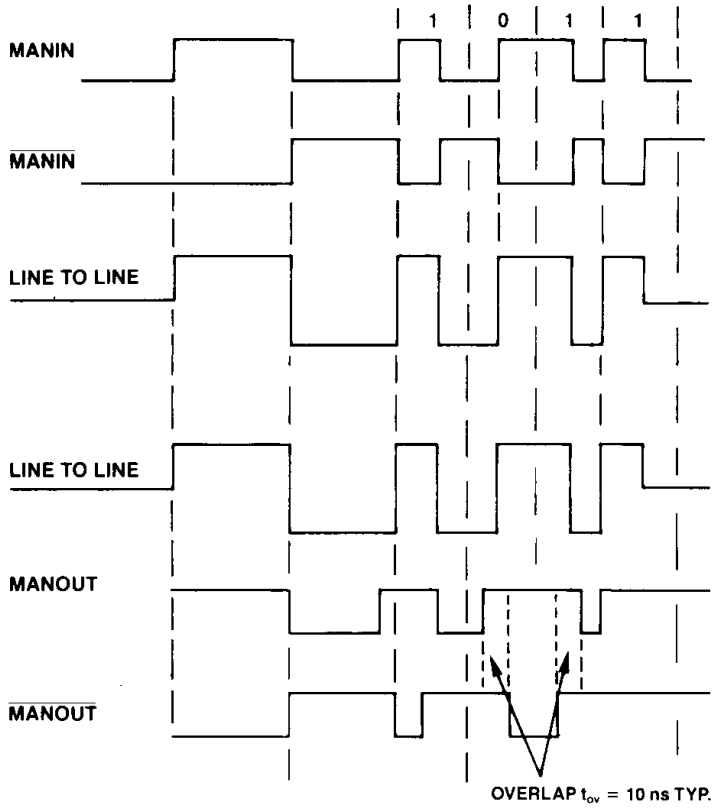
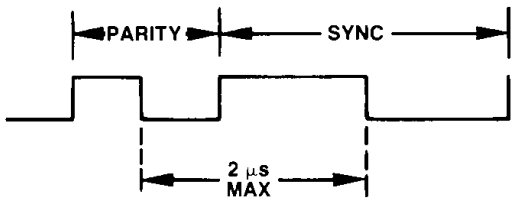
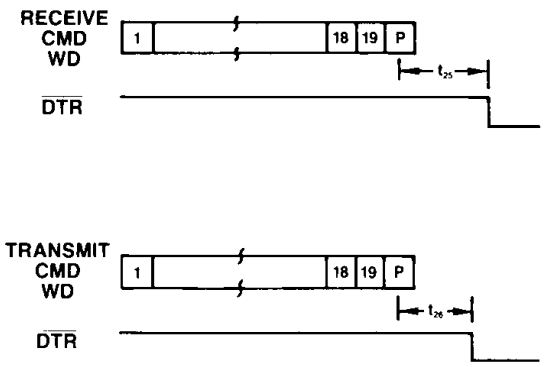


FIGURE 4:
DRIVER LOGIC WAVEFORMS

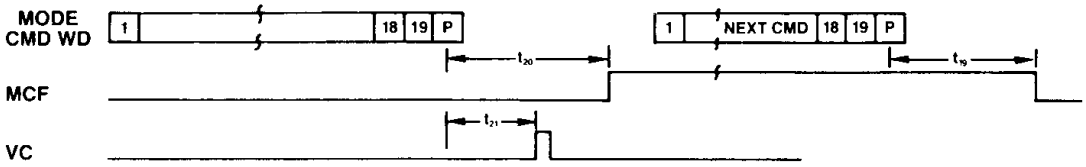
FIGURE 5:
CONTIGUOUS WORD



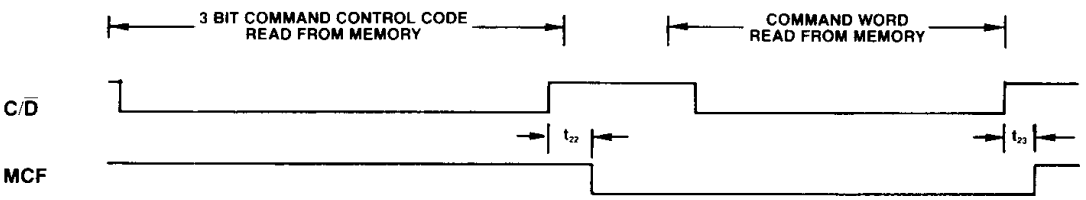
$\overline{DTR}$ VS COMMAND WORD



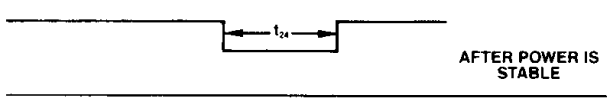
MODE CODE FLAG (MCF)
AS A RT



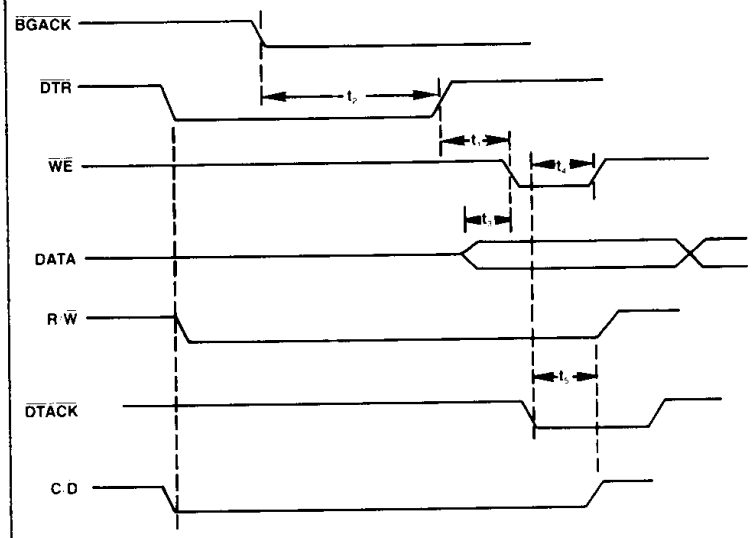
AS A BC



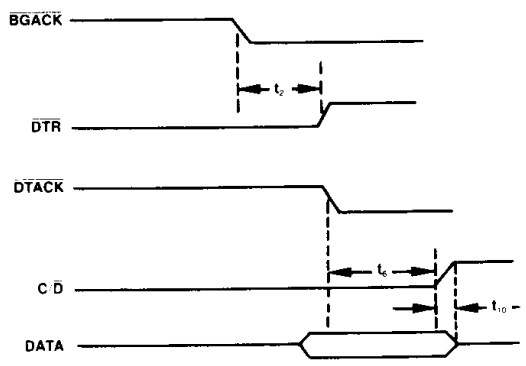
POR

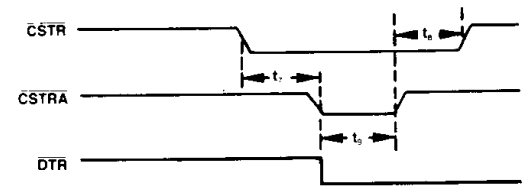


AC CHARACTERISTICS

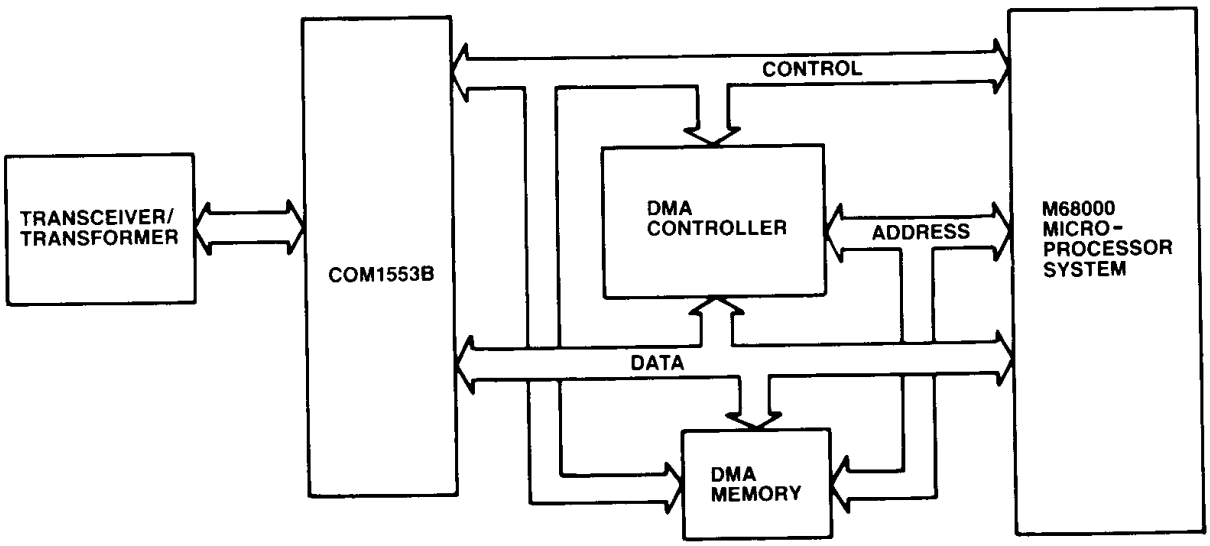


WRITE CYCLE





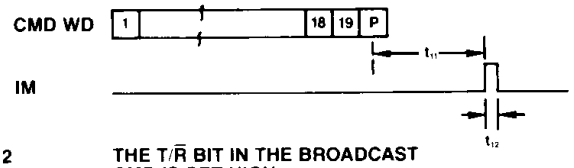
READ CYCLE



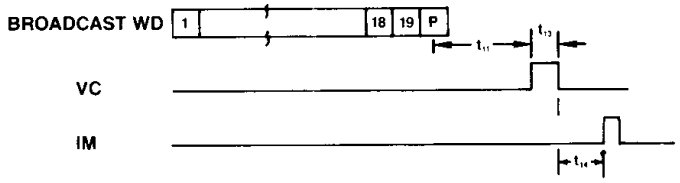
TYPICAL SYSTEM IMPLEMENTATION

INVALID MESSAGE (IM) AS A RT

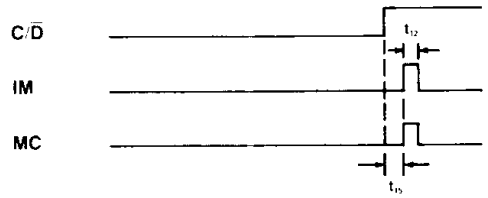
CASE 1



CASE 2 THE T/$\overline{R}$ BIT IN THE BROADCAST CMD IS SET HIGH.



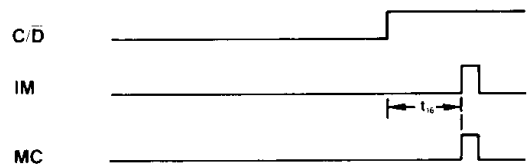
CASE 3 AN ERROR OCCURRED DURING A BROADCAST CMD



CASE 4 NON BROADCAST CMD

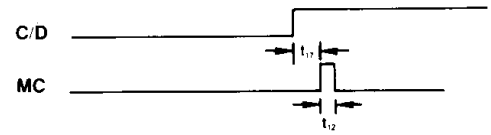
AS A BC

CASE 5 A TRANSMIT OR RECEIVE BC TRANSFER

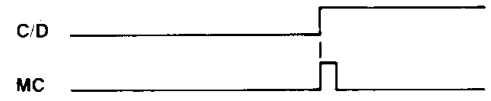


MESSAGE COMPLETE (MC) AS A RT

CASE 1 AT THE COMPLETION OF AN ERROR FREE BROADCAST COMMAND TRANSACTION AFTER THE ERROR REGISTER IS WRITTEN INTO MEMORY.

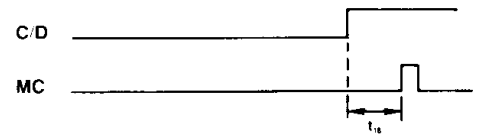


CASE 2 AT THE COMPLETION OF A TRANSMIT OR RECEIVE COMMAND TRANSACTION AFTER THE DATA REGISTER IS WRITTEN INTO MEMORY.



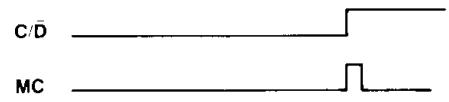
AS A BC

CASE 3 WHEN THE BC ISSUES A RECEIVE COMMAND, THE MC SIGNAL OCCURS AFTER THE STATUS WORD IS WRITTEN INTO MEMORY.
OR
WHEN THE BC ISSUES A TRANSMIT COMMAND, THE MC SIGNAL OCCURS AFTER THE LAST DATA WORD IS WRITTEN INTO MEMORY.

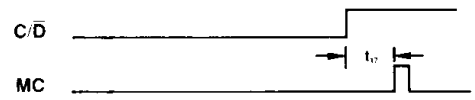


AS A BC OR RT

CASE 4 AT THE COMPLETION OF LOADING THE RT ADDRESS REGISTER OR READING THE DATA REGISTER.



CASE 5 AFTER READING THE ERROR REGISTER.



NOTE: Message complete and invalid message outputs of the COM 1553B are negative pulses i.e. $\overline{MC}$ and $\overline{IM}$.

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