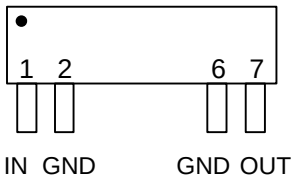
FIXED SIP DELAY LINE
$T_D/T_R = 5$
(SERIES 1514)

data delay devices, inc.

FEATURES

- Fast rise time for high frequency applications
- Very narrow device (SIP package)
- Stackable for PC board economy
- Low profile
- Epoxy encapsulated
- Meets or exceeds MIL-D-23859C

PACKAGES



1514-xxz
xx = Delay (T_D)
z = Impedance Code

FUNCTIONAL DESCRIPTION

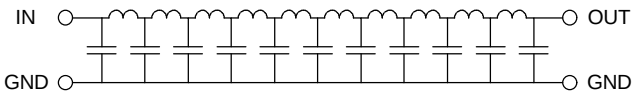
The 1514-series device is a fixed, single-input, single-output, passive delay line. The signal input (IN) is reproduced at the output (OUT), shifted by a time (T_D) given by the device dash number. The characteristic impedance of the line is given by the letter code that follows the dash number (See Table). The rise time (T_R) of the line is 20% of T_D, and the 3dB bandwidth is given by 1.75 / T_D.

PIN DESCRIPTIONS

IN	Signal Input
OUT	Signal Output
GND	Ground

SERIES SPECIFICATIONS

- **Dielectric breakdown:** 50 Vdc
- **Distortion @ output:** 10% max.
- **Operating temperature:** -55°C to +125°C
- **Storage temperature:** -55°C to +125°C
- **Temperature coefficient:** 100 PPM/°C



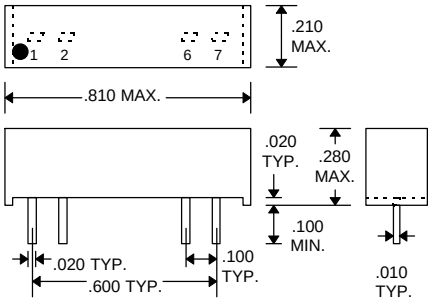
Functional Diagram

DASH NUMBER SPECIFICATIONS

Part Number	Delay (ns)	Rise Time (ns)	Impedance (Ω)
1514-2.5A	2.5 ± 1.0	1.0	50
1514-5A	5.0 ± 1.0	1.0	50
1514-10A	10.0 ± 1.0	2.0	50
1514-15A	15.0 ± 1.0	3.0	50
1514-20A	20.0 ± 1.0	4.0	50
1514-25A	25.0 ± 1.3	5.0	50
1514-30A	30.0 ± 1.5	6.0	50
1514-40A	40.0 ± 2.0	8.0	50
1514-50A	50.0 ± 2.5	10.0	50
1514-60A	60.0 ± 3.0	12.0	50
1514-80A	80.0 ± 4.0	16.0	50
1514-100A	100 ± 5.0	20.0	50
1514-3.5Y	3.5 ± 1.0	1.0	75
1514-7.5Y	7.5 ± 1.0	1.5	75
1514-15Y	15.0 ± 1.0	3.0	75
1514-22.5Y	22.5 ± 1.2	4.5	75
1514-30Y	30.0 ± 1.5	6.0	75
1514-37.5Y	37.5 ± 1.9	7.5	75
1514-45Y	45.0 ± 2.3	9.0	75
1514-60Y	60.0 ± 3.0	12.0	75
1514-75Y	75.0 ± 3.8	15.0	75
1514-90Y	90.0 ± 4.5	18.0	75
1514-105Y	105 ± 5.3	21.0	75
1514-120Y	120 ± 6.0	24.0	75
1514-135Y	135 ± 6.8	27.0	75
1514-150Y	150 ± 7.5	30.0	75

DASH NUMBER SPECIFICATIONS

Part Number	Delay (ns)	Rise Time (ns)	Impedance (Ω)
1514-5B	5.0 ± 1.0	1.0	100
1514-10B	10.0 ± 1.0	2.0	100
1514-20B	20.0 ± 1.0	4.0	100
1514-30B	30.0 ± 1.5	6.0	100
1514-40B	40.0 ± 2.0	8.0	100
1514-50B	50.0 ± 2.5	10.0	100
1514-60B	60.0 ± 3.0	12.0	100
1514-80B	80.0 ± 4.0	16.0	100
1514-100B	100 ± 5.0	20.0	100
1514-120B	120 ± 6.0	24.0	100
1514-140B	140 ± 7.0	28.0	100
1514-150B	150 ± 7.5	30.0	100
1514-50D	50.0 ± 2.5	10.0	250
1514-70D	70.0 ± 3.5	14.0	250
1514-120D	120 ± 6.0	24.0	250
1514-130D	130 ± 6.5	26.0	250
1514-150D	150 ± 7.5	30.0	250
1514-170D	170 ± 8.5	34.0	250
1514-270D	270 ± 13.5	54.0	250
1514-70E	70.0 ± 3.5	14.0	300
1514-140E	140 ± 7.0	28.0	300
1514-45G	45.0 ± 2.3	9.0	500
1514-50G	50.0 ± 2.5	10.0	500
1514-80G	80.0 ± 4.0	16.0	500
1514-100G	100 ± 5.0	20.0	500
1514-190G	190 ± 9.5	38.0	500



Package Dimensions

PASSIVE DELAY LINE TEST SPECIFICATIONS

TEST CONDITIONS

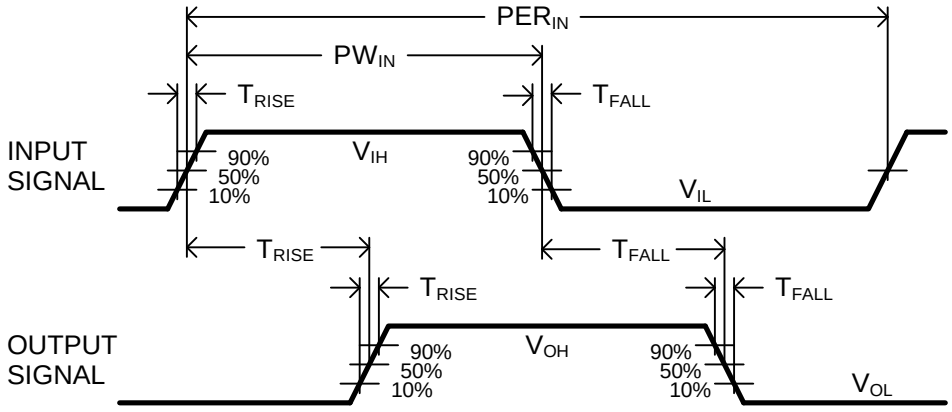
INPUT:

Ambient Temperature: 25°C ± 3°C
Input Pulse: High = 3.0V typical
Low = 0.0V typical
Source Impedance: 50Ω Max.
Rise/Fall Time: 3.0 ns Max. (measured at 10% and 90% levels)
Pulse Width (TD <= 75ns): PW_{IN} = 100ns
Period (TD <= 75ns): PER_{IN} = 1000ns
Pulse Width (TD > 75ns): PW_{IN} = 2 x T_D
Period (TD > 75ns): PER_{IN} = 10 x T_D

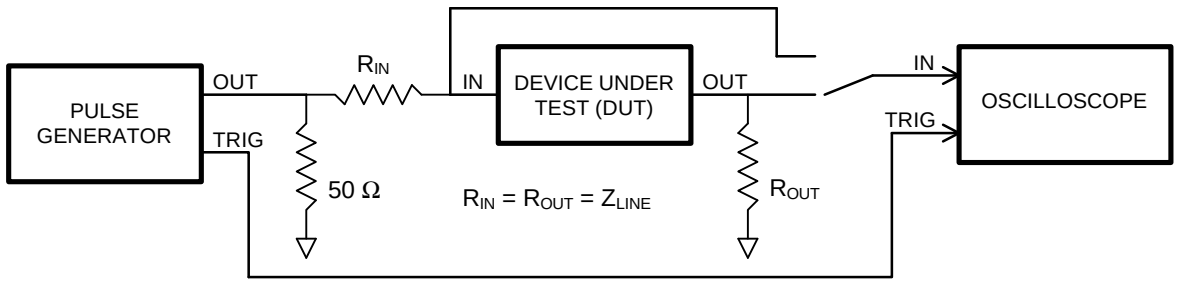
OUTPUT:

R_{load}: 10MΩ
C_{load}: 10pf
Threshold: 50% (Rising & Falling)

NOTE: The above conditions are for test only and do not in any way restrict the operation of the device.



Timing Diagram For Testing



Test Setup