

FEATURES

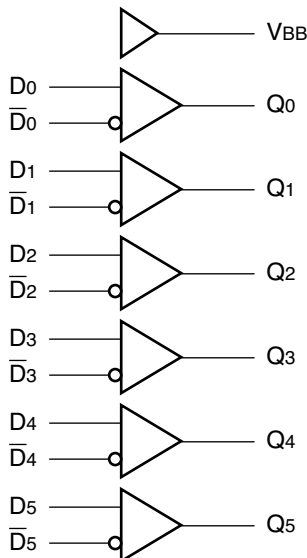
- Max. propagation delay of 3.7ns
- IEE min. of -37mA
- TTL outputs
- Extended supply voltage option:
VEE = -4.2V to -5.5V
- 25% faster than National's 325
- Differential inputs with built-in offset
- Voltage and temperature compensation for improved noise immunity
- VBB output for single-ended use
- Internal 75KΩ input pull-down resistors
- Function and pinout compatible with Fairchild F100K
- Available in 24-pin CERPACK and 28-pin PLCC packages

DESCRIPTION

The SY100S325 are hex translators for converting 100K ECL logic levels to TTL logic levels. Inputs can be used as inverting, non-inverting or differential receivers. An internal reference voltage generator provides VBB for single-ended operation or for use in Schmitt trigger applications. All inputs have 75KΩ pull-down resistors. The outputs will go LOW when the inputs are either open or have the same potential.

When used in single-ended operation, the apparent input threshold of the true inputs is 20mV to 40mV higher (positive) than the threshold of the complementary inputs. The VTTL and VEE power may be applied in either order.

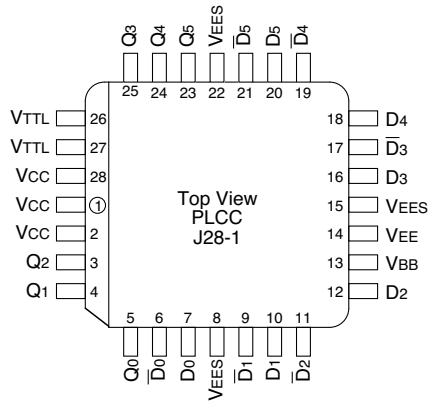
BLOCK DIAGRAM



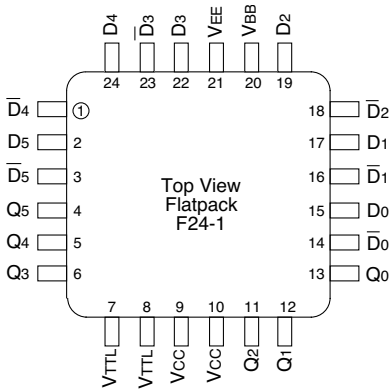
PIN NAMES

Pin	Function
D0-D5	Data Inputs
D̄0-D̄5	Inverting Data Inputs
Q0-Q5	Data Outputs
VEES	VEE Substrate
VTTL	TTL VCC Power Supply
VCCA	VCCO for ECL Outputs

PACKAGE/ORDERING INFORMATION



28-Pin PLCC (J28-1)



24-Pin Cerpack (F24-1)

Ordering Information

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S325FC	F24-1	Commercial	SY100S325FC	Sn-Pb
SY100S325FCTR ⁽¹⁾	F24-1	Commercial	SY100S325FC	Sn-Pb
SY100S325JC	J28-1	Commercial	SY100S325JC	Sn-Pb
SY100S325JCTR ⁽¹⁾	J28-1	Commercial	SY100S325JC	Sn-Pb
SY100S325JY ⁽²⁾	J28-1	Industrial	SY100S325JY with Pb-Free bar-line indicator	Matte-Tin
SY100S325JYTR ^(1, 2)	J28-1	Industrial	SY100S325JY with Pb-Free bar-line indicator	Matte-Tin

Notes:

1. Tape and Reel.
2. Pb-Free package is recommended for new designs.

DC ELECTRICAL CHARACTERISTICS

$V_{EE} = -4.2V$ to $-4.8V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition	
V_{OH}	Output HIGH Voltage	2.5	—	—	V	$I_{OH} = -2.0mA$	$V_{IN} = V_{IH} (Max.)$
V_{OL}	Output LOW Voltage	—	—	0.5	V	$I_{OL} = 24mA$	$V_{IN} = V_{IL} (Min.)$
V_{DIFF}	Input Voltage Differential	150	—	—	mV	Required for Full Output Swing	
V_{CM}	Common Mode Voltage	—	—	1.0	V	Permissible $\pm V_{CM}$ with Respect to V_{BB}	
I_{IH}	Input HIGH Current	—	—	350	μA	$V_{IN} = V_{IH} (Max.)$, $D_0-D_5 = V_{BB}$, $\underline{D_0-D_5} = V_{IL} (Min.)$	
I_{IL}	Input LOW Current	0.5	—	—	μA	$V_{IN} = V_{IH} (Min.)$, $D_0-D_5 = V_{BB}$	
I_{OS}	Output Short Circuit Current	-150	-80	-60	mA	$V_{OUT} = GND$	
I_{EE}	V_{EE} Power Supply Current	-37	-24	-17	mA	$D_0-D_5 = V_{BB}$	
I_{TTL}	V_{TTL} Power Supply Current	—	42	65	mA	$D_0-D_5 = V_{BB}$	
V_{BB}	Output Reference Voltage	-1380	-1320	-1260	mV	$I_{V_{BB}} = -2.1mA$	
V_{IH}	Single-Ended Input HIGH Voltage	-1165	—	-880	mV	Guaranteed HIGH Signal for All Inputs (with One Tied to V_{BB})	
V_{IL}	Single-Ended Input LOW Voltage	-1810	—	-1475	mV	Guaranteed LOW Signal for All Inputs (with One Tied to V_{BB})	

AC ELECTRICAL CHARACTERISTICS

PLCC/FLATPACK

$V_{EE} = -4.2V$ to $-5.5V$ unless otherwise specified, $V_{CC} = V_{CCA} = GND$, $V_{TTL} = +4.5V$ to $+5.5V$

Symbol	Parameter	Min.	Typ.	Max.	Unit	Condition
t_{PLH} t_{PHL}	Propagation Delay Data to Output	900	2100	2900	ps	$C_L = 15pF$, Figure 2
t_{PLH} t_{PHL}	Propagation Delay Data to Output	900	3100	3700	ps	$C_L = 50pF$, Figure 2

SWITCHING WAVEFORM

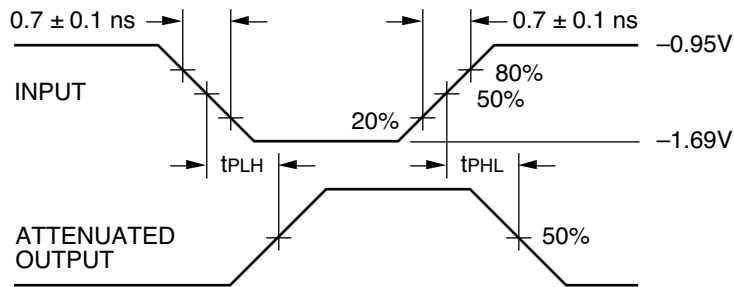


Figure 1. Propagation Delay

Note:

$V_{EE} = -4.2$ V to -5.5 V unless otherwise specified, $V_{CC} = V_{CCA} = GND$

TEST CIRCUITS

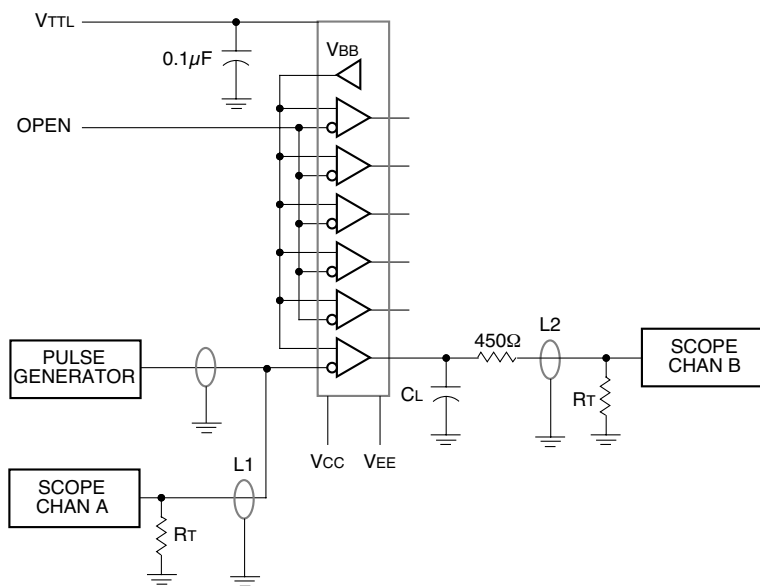


Figure 2. AC Test Circuit for 15pF Loading

Notes:

$V_{CC} = 0$ V, $V_{EE} = -4.5$ V, $V_{TTL} = +5$ V

L_1 and $L_2 =$ equal length 50Ω impedance lines

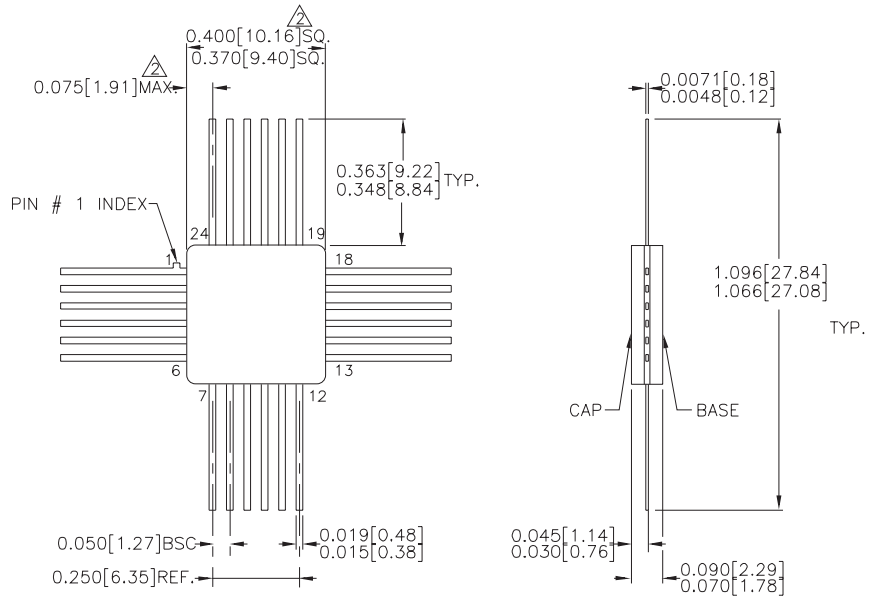
$R_T = 50 \Omega$ terminator internal to scope

Decoupling $0.1 \mu F$ from GND to V_{CC} , V_{EE} and V_{TTL}

All unused outputs are loaded with 500Ω to GND

$C_L =$ Fixture and stray capacitance = $3 pF$

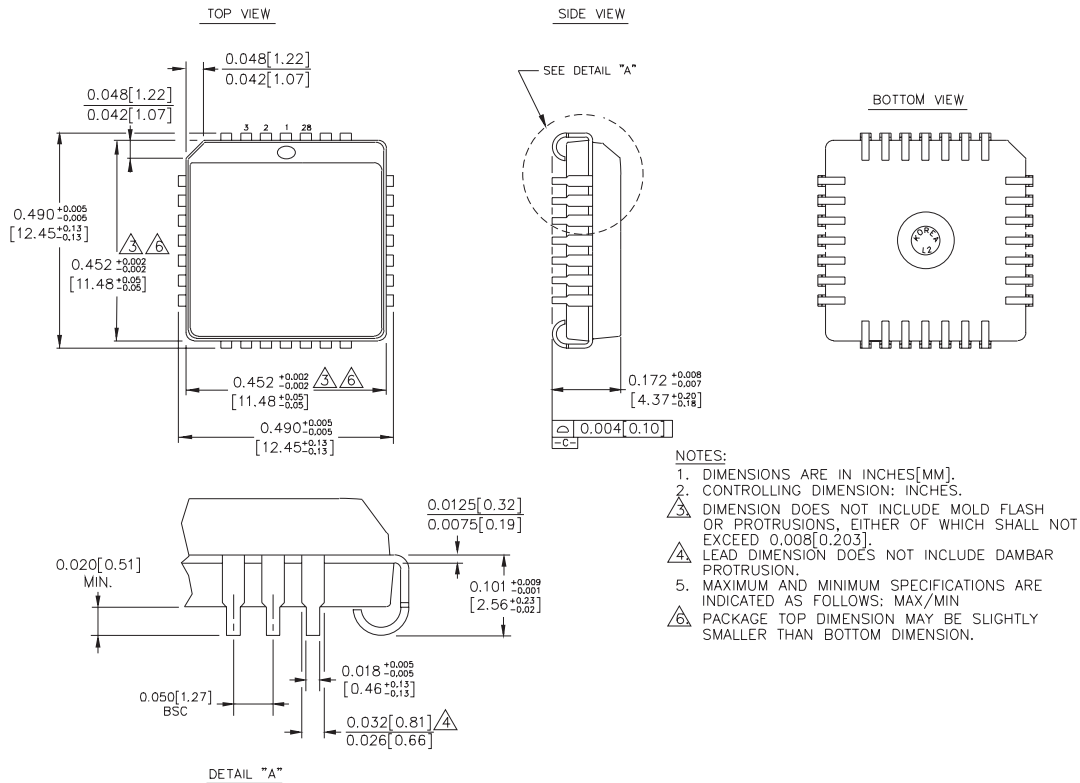
24-PIN CERPACK (F24-1)



- NOTES:**
1. DIMENSIONS ARE IN INCHES[MM].
 2. THIS DIMENSION INCLUDES GLASS PROTRUSION AND CAP TO BASE ALIGNMENT TOLERANCES.
 3. DIMENSIONS SHOWN ARE MAX/MIN, WHERE NOTED.

Rev. 03

28-PIN PLCC (J28-1)



Rev. 03

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