5GHz, 1:2 LVPECL FANOUT BUFFER/TRANSLATOR WITH INTERNAL INPUT TERMINATION

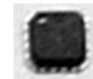
Precision Edge™
SY58012U

FEATURES

- **Precision 1:2, 800mV LVPECL fanout buffer**
- **Guaranteed AC performance over temperature/ voltage:**
  - **> 5GHz f_{MAX} (clock)**
  - **< 110ps t_r / t_f times**
  - **< 260ps t_{pd}**
  - **< 15ps max skew**
- **Low jitter performance**
  - **< 10ps$_{(pk-pk)}$ total jitter (clock)**
  - **< 1ps$_{(rms)}$ random jitter (data)**
  - **< 10ps$_{(pk-pk)}$ deterministic jitter (data)**
- **Accepts an input signal as low as 100mV**
- **Unique input termination and V_T pin accepts DC-coupled and AC-coupled differential inputs: LVPECL, LVDS, and CML**
- **Outputs are 100k LVPECL compatible, 800mV swing**
- **Power supply 2.5V ±5% and 3.3V ±10%**
- **–40°C to +85°C temperature range**
- **Available in 16-pin (3mm × 3mm) MLF™ package**

APPLICATIONS

- **All SONET and GigE clock distribution**
- **Fibre Channel clock and data distribution**
- **Backplane distribution**
- **High-end, low skew, multiprocessor synchronous clock distribution**



Precision Edge™

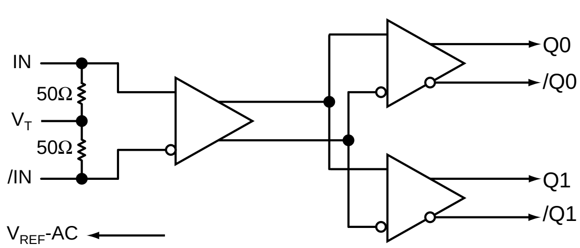
DESCRIPTION

The SY58012U is a 2.5V/3.3V precision, high-speed, fully differential 1:2 LVPECL fanout buffer. Optimized to provide two identical output copies with less than 15ps of skew and less than 10ps$_{(pk-pk)}$ total jitter, the SY58012U can process clock signals as fast as 5GHz or 5Gbps data.

The differential input includes Micrel's unique, 3-pin input termination architecture that interfaces to LVPECL, LVDS or CML differential signals, (AC-coupled or DC-coupled) as small as 100mV without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an on-board output reference voltage (V_{REF-AC}) is provided to bias the V_T pin. The outputs are 100k LVPECL compatible, with extremely fast rise/fall times guaranteed to be less than 110ps.

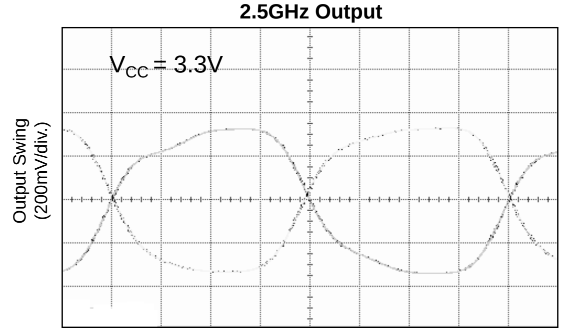
The SY58012U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require faster rise/fall times, or greater bandwidth, consider the SY58013U 1:2 fanout buffer with 400mV output swing, or the SY58011 1:2 CML (400mV) fanout buffer. The SY58012U is part of Micrel's high-speed, Precision Edge™ product line. Data sheets and support documentation can be found on Micrel's web site at www.micrel.com.

FUNCTIONAL BLOCK DIAGRAM



TYPICAL PERFORMANCE

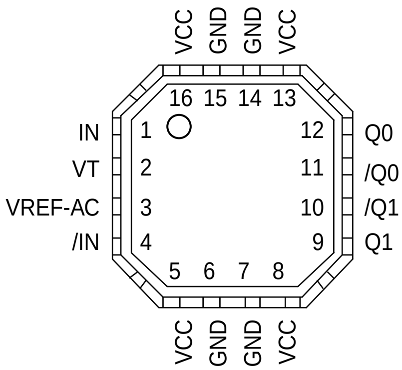
2.5GHz Output



2GHz with 100mV Input

Rev.: A Amendment: /0
Issue Date: July 2003

PACKAGE/ORDERING INFORMATION



16-Pin MLF™

Ordering Information(Note 1)

Part Number	Package Type	Operating Range	Package Marking
SY58012UMI	MLF-16	Industrial	012U
SY58012UMITR(Note 2)	MLF-16	Industrial	012U

Note 1. Contact factory for die availability. Die are guaranteed at T_A = 25°C, DC electricals only.

Note 2. Tape and Reel.

PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1, 4	IN, /IN	Differential Input: This input pair is the signal to be buffered. Each pin of this pair internally terminates with 50Ω to the V_T pin. Note that this input will default to an indeterminate state if left open. See *"Input Interface Applications"* section.
2	VT	Input Termination Center-Tap: Each input terminates to this pin. The V_T pin provides a center-tap for each input (IN, /IN) to a termination network for maximum interface flexibility. See *"Input Interface Applications"* section.
3	VREF-AC	Reference Output Voltage: This output biases to V_{CC} –1.4V. It is used when AC-coupling the inputs (IN, /IN). Connect V_{REF-AC} directly to the V_T pin. Bypass with 0.01µF low ESR capacitor to V_{CC}. Maximum current source or sink is 0.5mA. See *"Input Interface Applications"* section.
5, 8, 13, 16	VCC	Positive Power Supply: Bypass with 0.1µF//0.01µF low ESR capacitors as close to the V_{CC} pins as possible.
6, 7, 14, 15	GND, Exposed Pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
12, 11 9, 10	Q0, /Q0, Q1, /Q1	LVPECL Differential Output Pairs: Differential buffered output copy of the input signal. The output swing is typically 800mV. Unused output pairs may be left floating with no impact on jitter. See "*LVPECL Output Termination"* section.

Absolute Maximum Ratings(Note 1)

Power Supply Voltage (V_{CC}) .... –0.5V to +4.0V
Input Voltage (V_{IN}) .... –0.5V to V_{CC}
LVPECL Output Current (I_{OUT})
Continuous 50mA
Surge 100mA
Source or sink current on V_T pin
V_T Current .... ±100mA
Source or sink current on IN, /IN
Input Current .... ±50mA
Source or sink current on V_{REF-AC}, **Note 4**
V_{REF} Current .... ±1.5mA
Soldering, (10 seconds) .... 270°C
Storage Temperature Range (T_{STORE}) ... –65°C to +150°C

Operating Ratings(Note 2)

Power Supply Voltage (V_{CC}) .... 2.375V to 3.60V
Operating Temperature Range (T_A) .... –40°C to +85°C
Package Thermal Resistance, **Note 3**
MLF™ (θ_{JA})
Still-Air .... 60°C/W
500 lpfm .... 54°C/W
MLF™ (ψ_{JB}) .... 33°C/W

INPUT DC ELECTRICAL CHARACTERISTICS(Note 5)

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage		2.375		3.60	V
I_{CC}	Power Supply Current	Max. V_{CC}, no load		55	80	mA
V_{IH}	Input HIGH Voltage	IN, /IN, **Note 6**	V_{CC}–1.6		V_{CC}	V
V_{IL}	Input LOW Voltage	IN, /IN	0		V_{IH} –0.1	V
V_{IN}	Input Voltage Swing	IN, /IN; see Figure 1a	0.1		1.7	V
V_{DIFF_IN}	Differential Input Voltage Swing	IN,/IN; see Figure 1b	0.2		3.4	V
R_{IN}	In to V_T Resistance		40	50	60	Ω
IN to V_T					1.28	V
V_{REF-AC}	Output Reference Voltage		V_{CC}–1.525	V_{CC} –1.4	V_{CC}–1.325	V

LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS(Note 5)

V_{CC} = 3.3V ±10% or 2.5 ±5%; R_L= 50Ω to V_{CC}–2V; T_A= –40°C to 85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{OH}	Output HIGH Voltage	Q0, /Q0, Q1, /Q1	V_{CC}–1.145		V_{CC}–0.895	V
V_{OL}	Output LOW Voltage	Q0, /Q0, Q1, /Q1	V_{CC}–1.945		V_{CC}–1.695	V
V_{OUT}	Output Voltage Swing	Q0, /Q0, Q1, /Q1; see Figure 1a	550	800		mV
V_{DIFF_OUT}	Differiential Output Voltage Swing	Q0, /Q0, Q1, /Q1; see Figure 1b	1100	1600		mV

Note 1. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. This is a stress rating only and functional operation is not implied at conditions other than those detailed in the operational sections of this data sheet. Exposure to ABSOLUTE MAXIMUM RATINGS conditions for extended periods may affect device reliability.

Note 2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.

Note 3. Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential on the PCB.

Note 4. Due to the limited drive capability, use for input of the same package only.

Note 5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

Note 6. $V_{IH(min.)}$ not lower than 1.2V.

AC ELECTRICAL CHARACTERISTICS(Note 7)

V_{CC} = 2.5V ±5% or 3.3V ±10%; T_A = –40°C to +85°C; R_L = 50Ω to V_{CC}–2V, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f_{MAX}	Maximum Operating Frequency	NRZ Data		5		Gbps
		V_{OUT} ≥ 400mV Clock	5			GHz
t_{pd}	Propagation Delay	V_{IN} ≥ 100mV	110	170	260	ps
t_{CHAN}	Channel-to-Channel Skew	**Note 8**		3	15	ps
t_{SKEW}	Part-to-Part Skew	**Note 9**			100	ps
t_{JITTER}	Data Random Jitter (RJ) Deterministic Jitter (DJ)	**Note 10** **Note 11**			1 10	ps(rms) ps(pk-pk)
	Clock Cycle-to-Cycle Jitter Total Jitter (TJ)	**Note 12** **Note 13**			1 10	ps(rms) ps(pk-pk)
t_r, t_f	Output Rise/Fall Time	20% to 80% at full output swing	35	80	110	ps

Note 7. High frequency AC Electricals are guaranteed by design and characterization.

Note 8. Skew is measured between outputs of the same bank under identical transitions.

Note 9. Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.

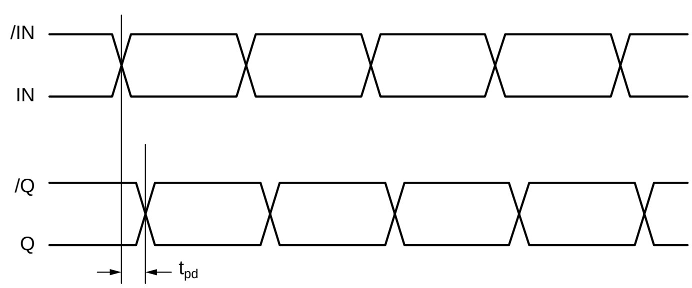
Note 10. RJ is measured with a K28.7 comma detect character pattern, measured at 10.7Gbps and 2.5Gbps/3.2Gbps.

Note 11. DJ is measured at 10.7Gbps and 2.5Gbps/3.2Gbps with both K28.5 and 2^{23}–1 PRBS pattern

Note 12. Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles, T_n–T_{n-1} where T is the time between rising edges of the output signal.

Note 13. Total jitter definition: With an ideal clock input of frequency ≤ f_{MAX}, no more than one output edge in 10^{12} output edges will deviate by more than the specified peak-to-peak jitter value.

TIMING DIAGRAM



SINGLE-ENDED AND DIFFERENTIAL SWINGS

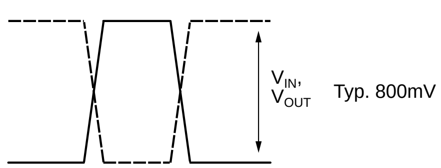


Figure 1a. Single-Ended Voltage Swing

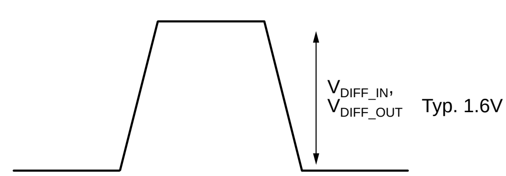
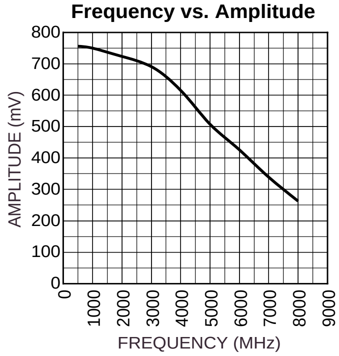


Figure 1b. Differential Voltage Swing

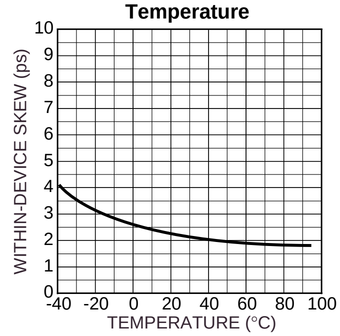
TYPICAL OPERATING CHARACTERISTICS

V_{CC} = 3.3V, GND = 0, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

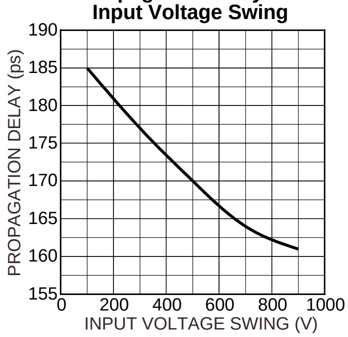
Frequency vs. Amplitude



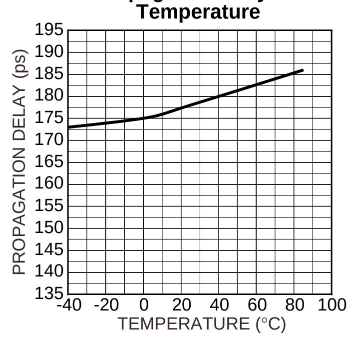
Within-Device Skew vs. Temperature



Propagation Delay vs. Input Voltage Swing



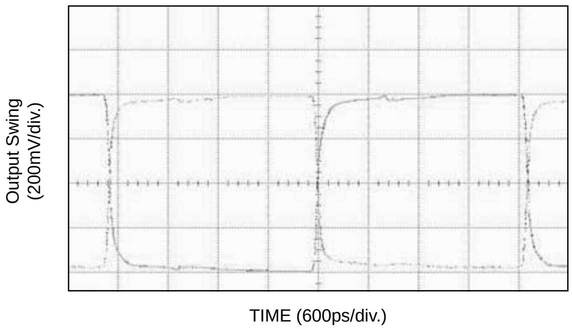
Propagaton Delay vs. Temperature



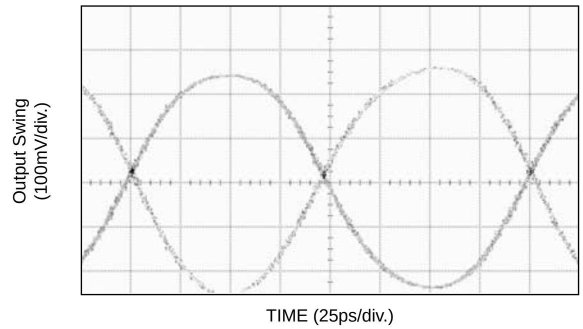
FUNCTIONAL CHARACTERISTICS

V_{CC} = 3.3V, GND = 0, V_{IN} = 100mV, T_A = 25°C, unless otherwise stated.

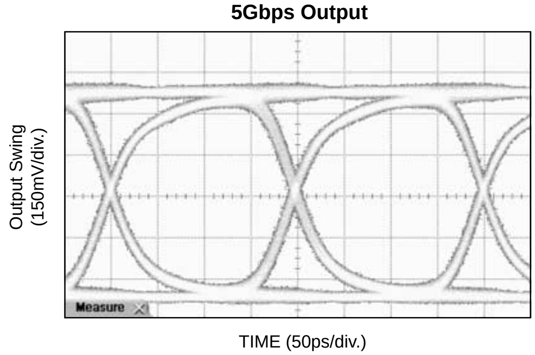
200MHz Output



5GHz Output



5Gbps Output



(2^{23}–1 PRBS Pattern)

INPUT STAGE

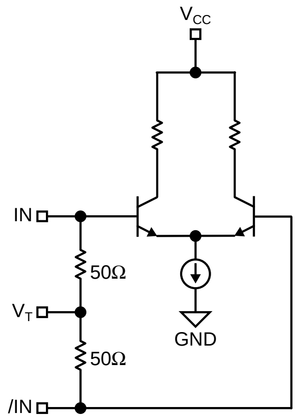
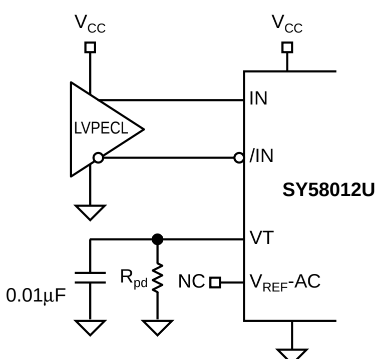


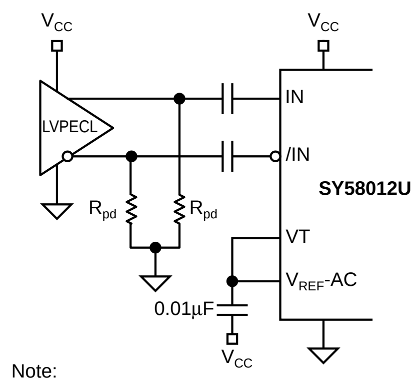
Figure 2. Simplified Differential Input Buffer

INPUT INTERFACE APPLICATIONS



Note:
For V_{CC} = 2.5V system, R_{pd} = 19Ω
For V_{CC} = 3.3V system, R_{pd} = 50Ω

Figure 3a. LVPECL Input Interface



Note:
For V_{CC} = 3.3V system, R_{pd} = 100Ω
For V_{CC} = 2.5V system, R_{pd} = 50Ω

Figure 3b. AC-Coupled LVPECL Input Interface

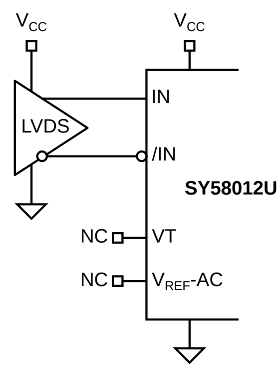


Figure 3c. LVDS Input Interface

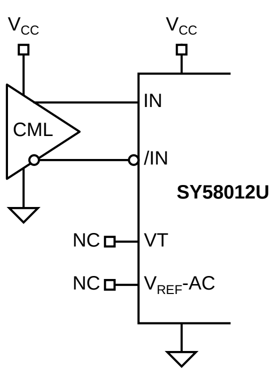


Figure 3d. DC-Coupled CML Input Interface
(option: may connect V_T to V_{CC})

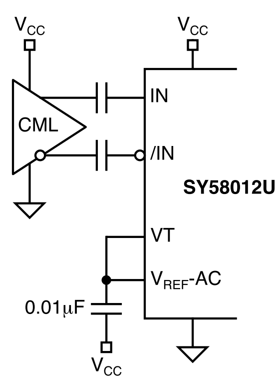


Figure 3e. AC-Coupled CML Input Interface

LVPECL OUTPUT

LVPECL output have very low output impedance (open emitter), and small signal swing which results in low EMI. LVPECL is ideal for driving 50Ω and 100Ω controlled impedance transmission lines. There are several techniques in terminating the LVPECL output, as shown in Figures 5 through 7.

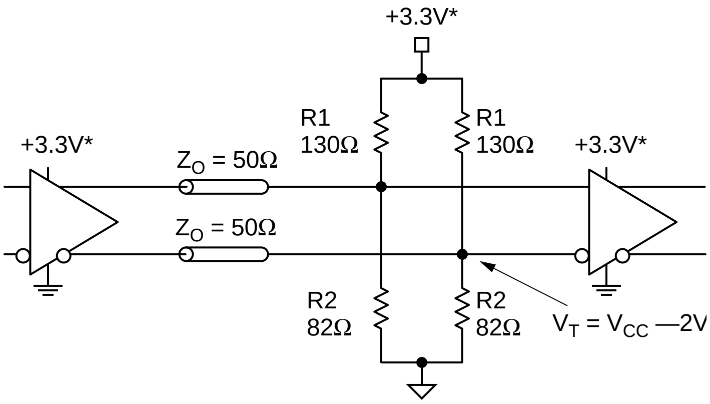


Figure 5. Parallel Termination-Thevenin Equivalent

Note 1. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω

Note 2. For +3.3V systems: R1 = 130Ω, R2 = 82Ω

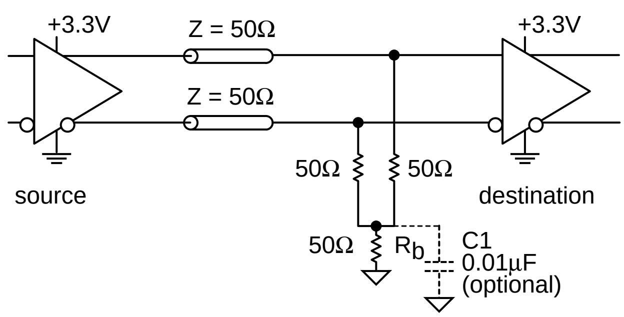


Figure 6. Three-Resistor "Y–Termination"

Note 1. Power-saving alternative to Thevenin termination.

Note 2. Place termination resistors as close to destination inputs as possible.

Note 3. R_b resistor sets the DC bias voltage, equal to V_T.
For +2.5V systems R_b = 19Ω.
For +3.3V systems R_b = 46Ω to 50Ω.

Note 4. C1 is an optional bypass capacitor intended to compensate for any t_r/t_f mismatches.

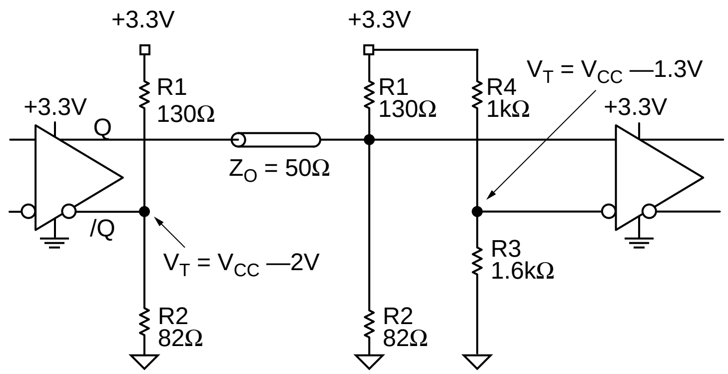


Figure 7. Terminating Unused I/O

Note 1. Unused output (/Q) must be terminated to balance the output.

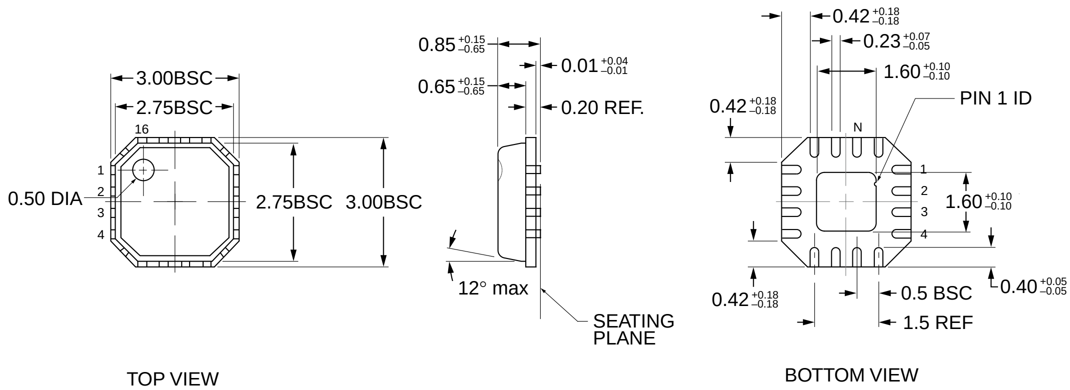
Note 2. For +2.5V systems: R1 = 250Ω, R2 = 62.5Ω, R3 = 1.25kΩ, R4 = 1.2kΩ.
For +3.3V systems: R1 = 130Ω, R2 = 82Ω, R3 = 1kΩ, R4 = 1.6kΩ.

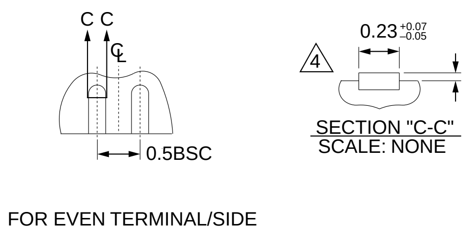
Note 3. Unused output pairs (Q and /Q) may be left floating.

RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY58011U	7GHz, 1:2 CML Fanout Buffer/Translator With Internal Input Termnations	http://www.micrel.com/product-info/products/sy58011u.shtml
SY58012U	5GHz, 1:2 LVPECL Fanout Buffer/Translator With Internal Input Termination	http://www.micrel.com/product-info/products/sy58012u.shtml
SY58013U	6GHz, 1:2 Fanout Buffer/Translator w/400mV LVPECL Outputs and Internal Terminations	http://www.micrel.com/product-info/products/sy58013u.shtml
	16-MLF™ Manufacturing Guidelines Exposed Pad Application Note	www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf
M-0317	HBW Solutions	http://www.micrel.com/product-info/as/solutions.shtml

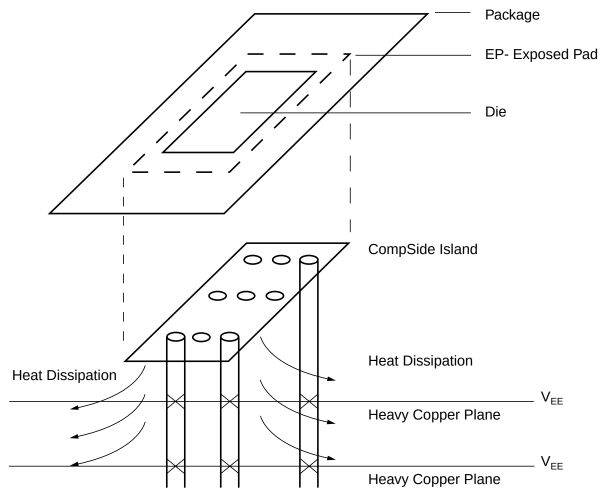
16 LEAD *Micro*LeadFrame™ (MLF-16)





1. DIMENSIONS ARE IN mm.
2. DIE THICKNESS ALLOWABLE IS 0.305mm MAX.
3. PACKAGE WARPAGE MAX 0.05mm.
4. THIS DIMENSION APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.20mm AND 0.25mm FROM TIP.
5. APPLIES ONLY FOR TERMINALS

Rev. 02



PCB Thermal Consideration for 16-Pin MLF™ Package
(Always solder, or equivalent, the exposed pad to the PCB)

Package Notes:

Note 1. Package meets Level 2 qualification.

Note 2. All parts are dry-packaged before shipment.

Note 3. Exposed pads must be soldered to a ground for proper thermal management.

MICREL, INC. 1849 FORTUNE DRIVE SAN JOSE, CA 95131 USA

TEL + 1 (408) 944-0800 FAX + 1 (408) 944-0970 WEB http://www.micrel.com