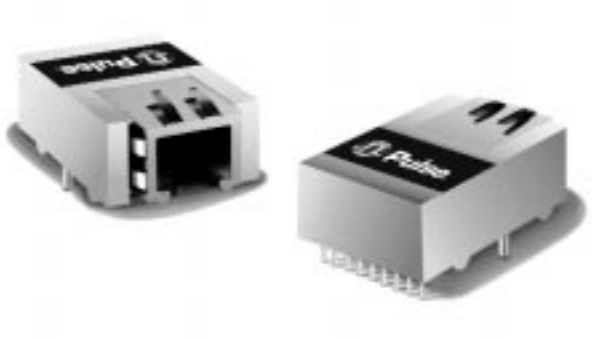
FASTPULSE HIGH SPEED LAN TRANSCEIVERS



- High performance transceivers for ATM 155 Mbps, 100Base-TX, and TP-FDDI
- Integrated drop-in frontend solution
- Footprint compatible with popular LCF 9-pin Fiber Optic Transceivers

Part Number Chart

Part Number	Application	Standard
PE-68531G	TP-FDDI	ANSI X3T12, TP-PMD
PE-68532G, PE-68538G	ATM 155 Mbps	ATM-UNI-PMD STS-3c
PE-68537G	100Base-TX	IEEE 802.3u PMD

Note: Also available without metallic case: use suffix “C”, eg. PE-68532**C**.

General Description

The ***FASTPULSE*** high speed LAN transceivers provide high performance, cost-effective solutions for ATM 155 Mbps, TP-FDDI and Fast Ethernet 100Base-TX frontends. The transceivers interface the standard “fiber” PECL interface to UTP-5 cable, integrating the transceiver IC, magnetics and connector in the process. The highly compact design implements the entire Physical Media Dependent (PMD) circuit in the standard 9-pin form factor, which reduces component count and board space. This modular transceiver approach, minimizes the design effort and risk of implementing 100 Mbps + frontends.

Employing ***FASTPULSE*** technology, these transceivers integrate the full transmit/receive interface functions of signal encoding/decoding, adaptive equalization, DC restoration, signal filtering, and isolation. This integrated approach, coupled to the novel circuit design, results in a high performance frontend which eliminates many of the conventional design compromises and parasitic elements which plague high speed designs. The long design cycle of selecting and optimizing the sensitive analog IC/magnetic frontend is essentially replaced with a single-shot, single-device approach. The compact 9-pin footprint matches the industry standard 9-pin LCF fiber optic transceivers (AMP, HP, etc.), allowing a common board design to accommodate both fiber and copper options. The transceiver also allows existing fiber designs to be upgraded for UTP support with minimal design effort.

The PE68531G is a TP-FDDI transceiver which adheres to the ANSI TP-PMD standard and employs MLT3 signaling to support 100 Mbps (125 Mbaud) over 100 m UTP-5 cable. The PE68532/38G are ATM transceivers which adhere to ATM-UNI-PMD standard and employ NRZ signaling to support 155 Mbps over 100 m UTP-5 cable. The PE-68532G is configured for the adapter node of a network and the PE-68538G for the switch or hub node. The PE-68537G is a 100Base-TX transceiver which adheres to IEEE802.3u standard and employs MLT3 signaling to support 100 Mbps (125 Mbaud) over 100 m of UTP-5 (2-pair) cable.

Features

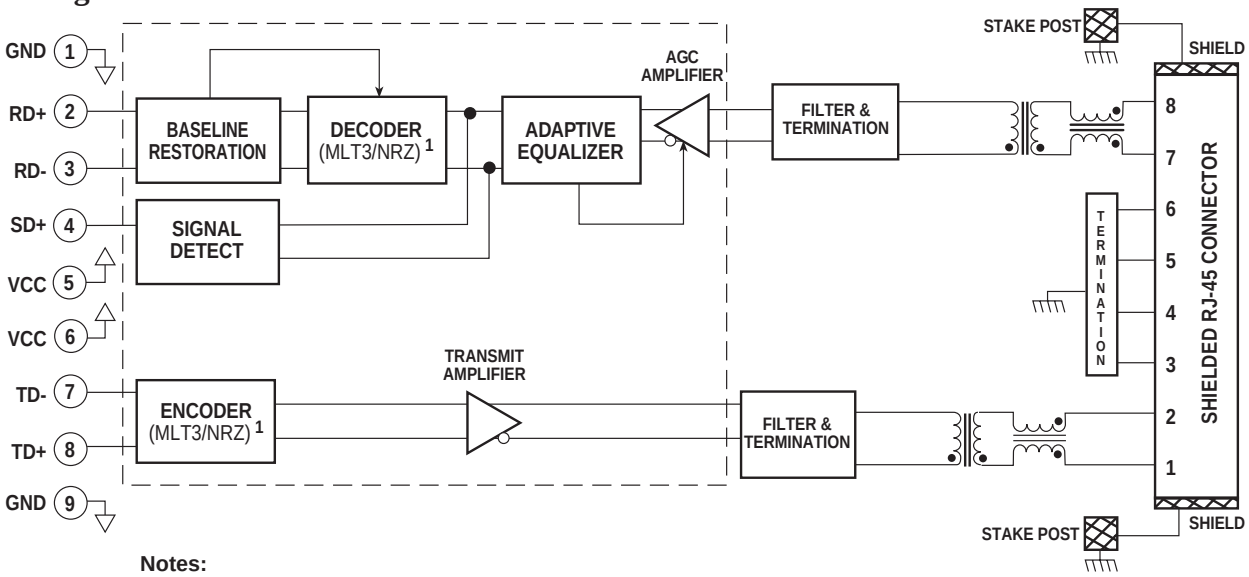
- UTP Transceivers for ATM 155 Mbps, TP-FDDI and 100Base-TX
- Drop in replacement for standard 9-pin fiber optic transceivers
- Full compliance with PMD standards: ATM, ANSI and IEEE
- Supports 100 m of Unshielded Twisted Pair, Category 5 cable
- Implements full adaptive equalization and baseline wander correction
- Excellent transmit and receive jitter performance
- EMC optimized design provides for low emissions and high immunity (ESD protection per IEC 801)
- Direct PECL logic interface to PHY layer chip sets
- Offers simple, low-cost upgrade from existing fiber designs
- Offers flexibility of single UTP/fiber board
- Compact footprint enables efficient single/multiport designs
- 1500 Vrms voltage isolation
- Wavesolder and aqueous wash compatible
- ISO 9001 quality
- Two package options: with metallic case “G” and without case “C”

Applications

The following products for ATM 155, TP-FDDI or 100Base-TX:

- Network adapter cards (ISA, PCI, VME etc.)
- Hubs or concentrators
- Motherboards (PC, workstation, industrial)
- Bridges, routers, switches
- Switch uplink modules
- LAN analyzers/test equipment
- Point to point links (Telecom)
- Peripherals: storage, print servers, etc.

Block Diagram



Notes:

1. PE-68531/37G implement MLT3. PE-68532/38G implement NRZ

2. Dotted line indicates the transceiver IC function.

3. RJ-45 pinout shown is for PE-68531/32G. See pinout specifications for PE-68537/36G.

Functional Description

The key functions of the transceivers are outlined in the block diagram above.

In the transmit channel, the PECL (100 K) signals from the PHY chip set (TD±) are encoded to appropriate line coding and driven out differentially by the edge-controlled transmit amplifier in the transceiver IC. The wideband transformer provides the required 1500 V isolation and the common mode choke eliminates high frequency common mode noise. The magnetics are tuned specifically to the characteristics of the transceiver IC to give a highly balanced system with optimum signal rise-time, minimum jitter and low emissions. The transformers exhibit a high minimum inductance in order to counter signal droop in the presence of DC bias. The outputs are fully terminated with cable impedance (100 Ω) to meet return loss specification. See electrical characteristics section for full transmitter specifications.

In the receive channel, the incoming differential signal from the cable passes through a wideband isolation transformer and the choke, before being filtered and terminated for high frequency noise rejection. The resulting differential signal is fed to transceiver IC for adaptive equalization, baseline restoration and line decoding. Adaptive equalization is necessary to compensate for the frequency dependent attenuation and phase distortion which the signal suffers in the cable. The optimum compensation required will vary with cable length and so a high performance adaptive equalizer is employed which constantly adjusts itself by means of a data quantized feedback loop. The equalizer characteristics reflect the EIA/TIA 568 cable standard and extensive modeling of UTP-5 cable characteristics under real life conditions. The operation of the equalizer can be seen in the performance section. The baseline restoration loop performs a DC restoration on the incoming signal (as defined in ANSI TP-PMD recommendation) which may occur due to data pattern dependent DC shifts and the inherent low frequency bandwidth limitations of the channel and AC coupling transformers. If not corrected, this DC drift (or baseline wander) can cause degradation in signal/noise ratio and can result in data errors. The baseline restoration loop in the transceiver constantly monitors the incoming signal and restores the DC level to a nominal level. The resulting amplified, equalized and DC restored signal is decoded in the line decoder as per appropriate scheme and driven out as differential 100 K PECL signals RD±. See electrical characteristics section for full receiver specifications.

The signal detect function monitors the equalized incoming signal to notify PHY controller that a valid signal is received. This is explicitly required by the TP-FDDI specification and is optional for ATM system designers. The SD signal is driven out as single-ended PECL signal.

The unused signal pairs in the RJ-45 are terminated at their common mode impedance to minimize EMI emissions.

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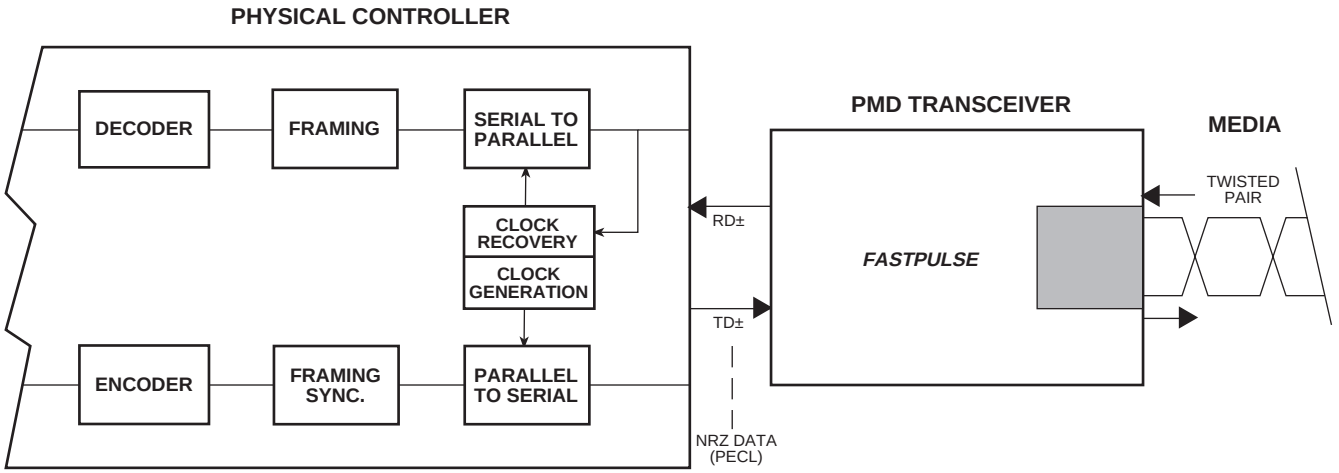
System Application

ATM155/100Base-TX



Notes:
ATM Controllers: Texas Instruments, PMC, Fujitsu, AMCC . . .
100BTX/FDDI Controllers: National Semiconductor, AMD, Motorola . . .

The transceiver provides all Physical Media Dependent (PMD) functions required to allow digital Physical layer controller to send/receive data integrally over the twisted pair media.

The TP-FDDI/100Base-TX PHY chip set will perform clock recovery/generation, scrambling, 4B/5B codec, serial-parallel conversion, etc. These functions are available from several vendors in different chip set partitioning. Please refer to vendor list in appendix for more information. The PECL interface is a standard interface used by fiber optic transceivers in FDDI and 100Base-FX applications. Since 100Base-TX employs the basic TP-FDDI PMD scheme, the PE-68531G and PE-68537G are electrically identical with different RJ-45 pinouts as per the standards (refer to pinout specification). The PE-68537G fits the following Fast Ethernet product architectures: 100Base-TX only with adapter and repeater, 10/100 adapter with separate 10/100 RJ-45 connectors.

The ATM PHY chip set will perform clock recovery/generation, serial-parallel conversion, framing, scrambling, cell extraction/insertion, etc. These functions are available from several vendors in different chip set partitioning. The PECL interface is a standard interface used by fiber optic transceivers in ATM applications. The PE-68532G and the PE-68538G are electronically identical but have “mirror” RJ-45 pinouts as required by standard for adapter (user) node and switch (hub) node of network respectively (refer to pinout specification).

Pin Descriptions

Signal	Pin #	Description	I/O	Type
GND	1	Analog Ground	—	Supply
RD+	2	Differential Receive Data +	O	PECL
RD-	3	Differential Receive Data -	O	PECL
SD+	4	Signal Detect Output	O	PECL
Vcc	5	Power Supply Voltage	—	Supply
Vcc	6	Power Supply Voltage	—	Supply
TD-	7	Differential Transmit Data -	I	PECL
TD+	8	Differential Transmit Data +	I	PECL
GND	9	Analog Ground	—	Supply

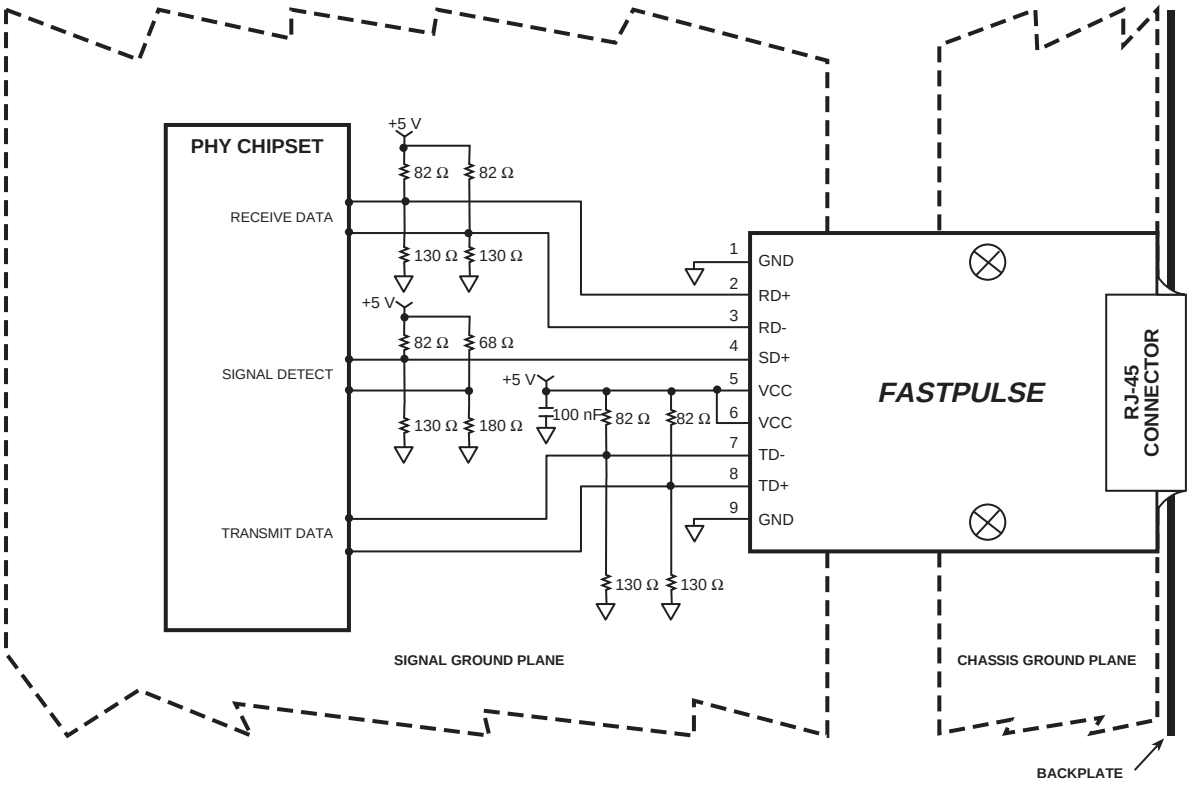
Note: Two Mechanical Stake Posts are connected to RJ-45 Shield and Body Shield.

RJ-45 Connector Pinout

Pin #	PE-68531/32G	PE-68537G	PE-68538G
1	Transmit (TX+)	Transmit (TX+)	Receive (RX+)
2	Transmit (TX-)	Transmit (TX-)	Receive (RX-)
3	Unused P1	Receive (RX+)	Unused P1
4	Unused P2	Unused P1	Unused P2
5	Unused P2	Unused P1	Unused P2
6	Unused P1	Receive (RX-)	Unused P1
7	Receive (RX+)	Unused P2	Transmit (TX+)
8	Receive (RX-)	Unused P2	Transmit (TX-)

Note: Unused pairs (P1, P2) are terminated onboard

Application Circuit



Application Notes

1. The PECL termination networks shown (Thevenin 50 Ω) are typical. Signal traces should be effective for 50 Ω transmission lines. Other suitable termination schemes may be used.
2. Place termination networks near input data pins of Transceiver (TD) and PHY device (SD, RD) for optimum termination.
3. Make all differential signal paths short and the same length to avoid unbalancing effects and unwanted loops.
4. For chip sets with differential SD inputs, the unused SD signal can be terminated as shown.
5. VCC signals may be connected together at transceiver as shown. Decouple very close to transceiver.
6. Use low inductance, ceramic SMD bypass capacitors and optional ferrite inductors for optimum high frequency decoupling.
7. Device ground pins should be directly connected to low impedance ground plane for signal return current.
8. Use multi-layer PCB type with dedicated GND and VCC layers for best high frequency and EMC performance. At least four layers are recommended with outside layers for signal routing and inner layers for supply planes.
9. Use of ground plane partitions, as indicated, is recommended for best EMC performance. The signal ground plane extends back to controller from edge of transceiver. The chassis ground plane extends to media side of board and is generally connected directly to the backplate.
10. RJ-45 flanges should make galvanic contact to backplate cutout. Stake posts should be soldered to chassis plane for best EMC performance. Refer to EMC section for further EMC considerations.

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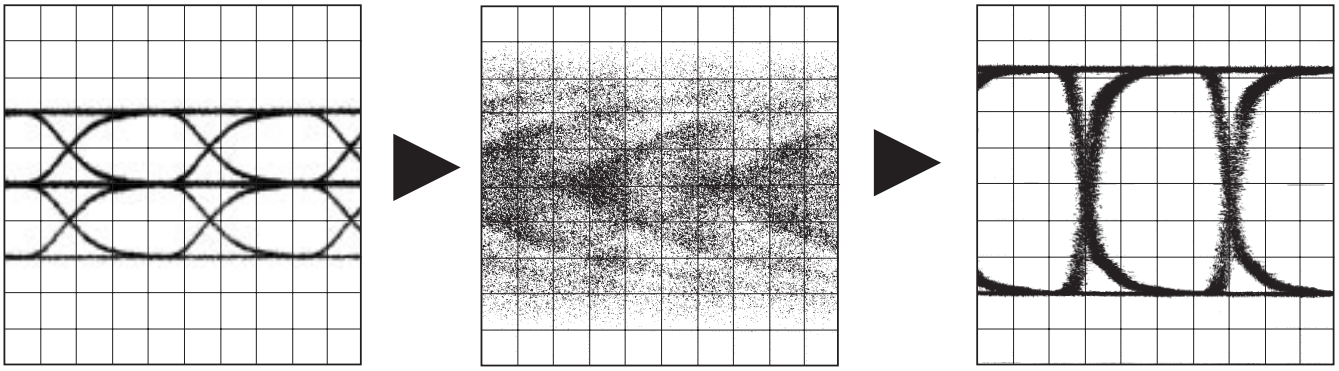
Performance

The following eye pattern measurements show the operation of the adaptive equalizer and indicate the jitter performance of the transceivers. All jitter measurements shown are peak values resulting from combination of Transmit, Receive and cable contributions. Figure A shows the MLT3 transmit output waveform for 0 m cable. Figure B shows the waveform at receiver input after massive attenuation and phase distortion effects of 100m UTP-5. Figure C shows the recovered NRZI data for the same signal. The same measurements are repeated in Figures D, E, and F for ATM 155 Mbps NRZ signal.

TP-FDDI/100Base-TX (PE-68531G/37G)

MLT3 Transmit Output (TX±) | **Receiver Input (RX±)** | **NRZI Receiver Output (RD±)**



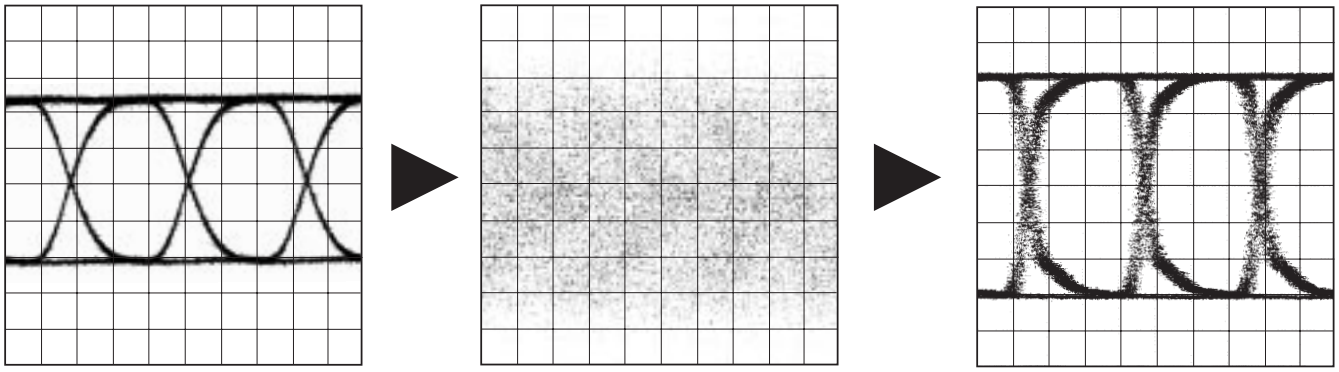
A 0 Meter UTP-5 Cable
500mV/DIV, 2ns/DIV

B 100 Meter UTP-5 Cable
200mV/DIV, 2ns/DIV

C 100 Meter UTP-5 Cable
200mV/DIV, 2ns/DIV

ATM-155 (PE-68532G/38G)

NRZ Transmit Output (TX±) | **Receiver Input (RX±)** | **NRZI Receiver Output (RD±)**



D 0 Meter UTP-5 Cable
200mV/DIV, 2ns/DIV

E 100 Meter UTP-5 Cable
100mV/DIV, 2ns/DIV

F 100 Meter UTP-5 Cable
200mV/DIV, 2ns/DIV

Notes:

The PE-68531G/68537G MLT-3 transmit eye pattern is optimized for minimum overshoot (< 3%) and a 3.5 ns rise time. It has < 1 ns transmit jitter and as a result of its fast rise time, the receive eye pattern has ≤ 2 ns of jitter at 100 meters. Similarly, the PE-68532G/38G NRZ transmit eye pattern has a 3 ns rise time, < 5% overshoot and less than 1 ns of transmit jitter. Due to its relatively fast rise time and low transmit jitter, the data dependent jitter from the channel is ≤ 1.6 ns at the receiver output as shown. There is a trade-off design choice: A faster rise time will minimize jitter and produce a low bit error rate (BER). In contrast, a fast rise time, while reducing jitter, can produce excessive overshoot and EMI emissions when the signal encounters impedance mismatches in the cable or punch down blocks. The transceivers have been optimized and tested to provide optimum balance between low BER and minimum emissions.

Electrical Characteristics

Absolute Maximum Ratings

Parameter	Symbol	MIN	Typical	MAX	Units
Supply Voltage	Vcc	0	—	6.0	V
Input Voltage	VI	GND - 0.3V	—	Vcc + 0.3	V
Lead Solder Temp/Time	—	—	—	240/10	°C/S

Recommended Operating Conditions

Supply Voltage	Vcc	4.75	5.0	5.25	V
Supply Current	Is	—	170	200	mA
Operating Temperature	TA	0	25	70	°C
Storage Temperature	Ts	-40	—	+125	°C

Transmitter Input Characteristics

PECL High Level Input	TD+/-VIH	Vcc—1170	—	Vcc—720	mV
PECL Low Level Input	TD+/-VIL	Vcc—1950	—	Vcc—1440	mV

Transmitter Output Interface — PE-68531G/37G

Transmit Signal Level [1]	Vo	1.90	2.00	2.1	Vpp
Rise Time (10%-90%)	TR	3.0	3.4	5.0	ns
Fall Time (10%-90%)	TF	3.0	3.4	5.0	ns
Total Peak-Peak Jitter [2]	—	—	0.5	1.0	ns

Transmitter Output Interface — PE-68532G/38G

Transmit Signal Level [1]	Vo	0.94	1.00	1.06	Vpp
Rise Time (10%-90%)	TR	1.5	2.8	3.5	ns
Fall Time (10%-90%)	TF	1.5	2.8	3.5	ns
Total Peak-Peak Jitter	—	—	0.5	1.0	ns

Receiver Output Interface — PE-68531G/37G & PE-68532G/38G

PECL High Level Output [3]	RD ±VOH	Vcc—1220	—	Vcc—720	mV
PECL Low Level Output [3]	RD ±VOL	Vcc—1950	—	Vcc—1600	mV
PECL Output Voltage Swing	VOH -VOL	600	—	—	mV
Rise Time (10%-90%)	TR	0.3	0.7	1.2	ns
Fall Time (10%-90%)	TF	0.3	0.7	1.2	ns
Total of Peak-Peak Duty Cycle Distortion	PE-68531G/37G	—	1.5	2.5	ns
and Data Dependent Jitter [2]	PE-68532G/38G	—	1.0	2.0	ns

Signal Detect Output — PE-68531G/37G & PE-68532G/38G

PECL High Level Output [3]	SD+/VOH	Vcc—1220	—	Vcc—720	mV
PECL Low Level Output [3]	SD+/VOL	Vcc—1950	—	Vcc—1600	mV

Part Number	Overshoot (MAX)	Return Loss (TX±, RX±)		Voltage Isolation	Bit Error (MAX)	Power Dissipation	Transformer Inductance	Signal Detect (µS MAX)	
		1-60 MHz	60-100 MHz			(mW MAX)	(0-8mA$_{DC}$ Bias)	Assert	De-assert
PE-68531G/7G	50mV	-16 dB	-12 dB	1500 VRMS	10^{-12}	1000	350 µH	1000	350
PE-68532G/38G	50mV	-16 dB	-12 dB	1500 VRMS	10^{-10}	1000	350 µH	1000	350

Notes:

1. Transmit signal level is differential and measured with a 100 Ω differential load between pins 1 and 2 of the RJ-45.
2. Including jitter from the transmitter cable and receiver.
3. Measured with standard PECL load, 50 Ω to VCC-2 V.

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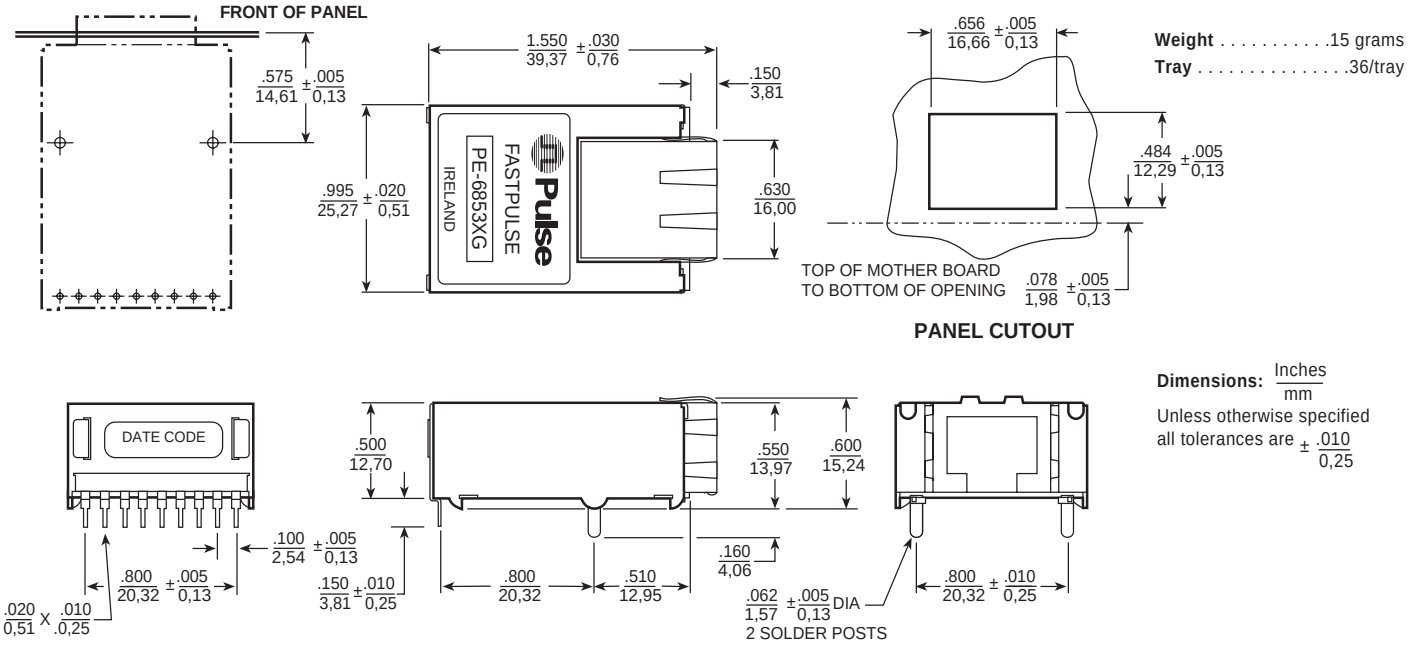
Mechanicals

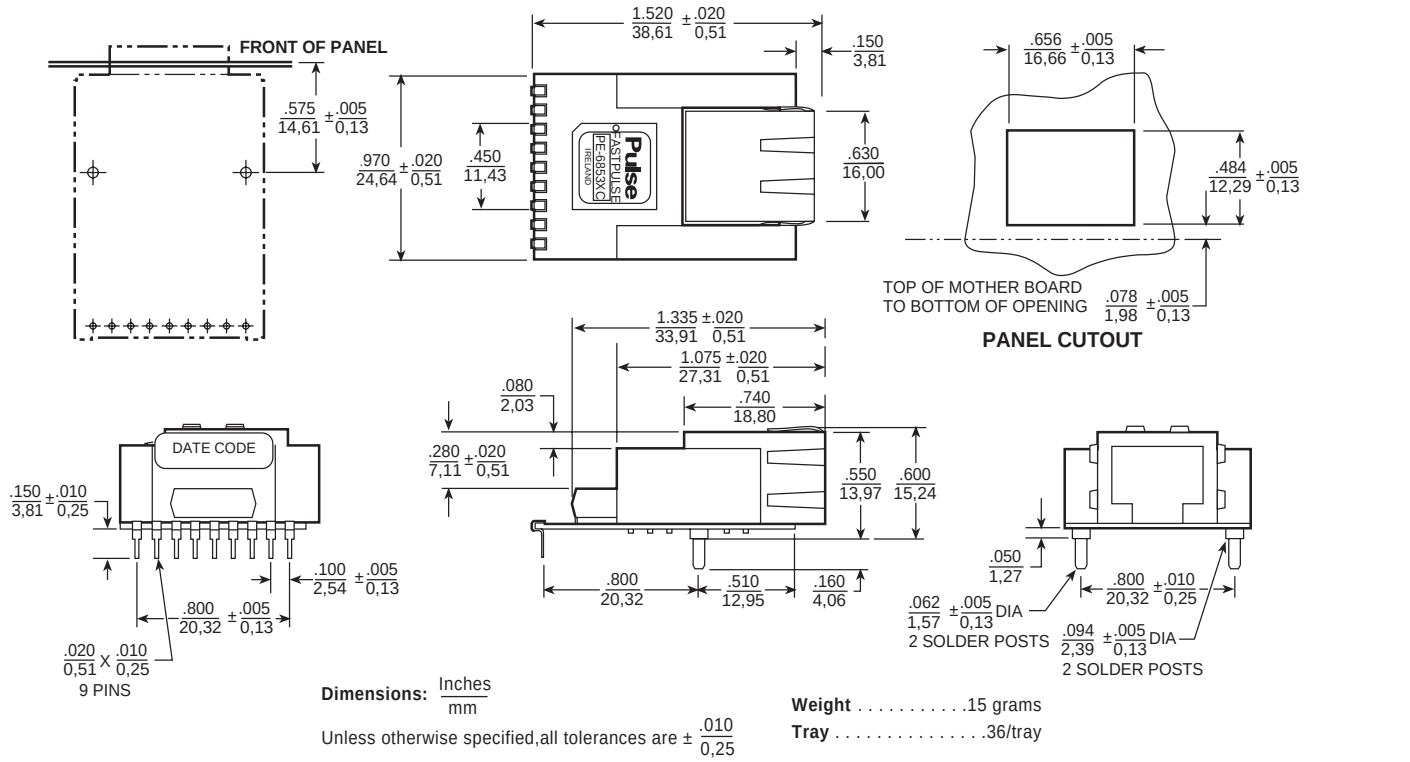
FASTPULSE-G



Weight . . . . . .15 grams
Tray 36/tray

Dimensions: Inches / mm
Unless otherwise specified all tolerances are ± .010 / 0,25

FASTPULSE-C



Dimensions: Inches / mm
Unless otherwise specified,all tolerances are ± .010 / 0,25

Weight . . . . . .15 grams
Tray 36/tray

Notes:

1. Pin composition is 60/40 tin/lead phosphor bronze.
2. This device contains active components and standard ESD precautions should be employed in handling the device.
3. Components on underside have maximum height of .030" (0,76 mm), less than standoff height of .050" (1,27 mm) as determined by pins/supports. This ensures the recommended .020" (0,51 mm) wash clearance height. For safety, there should be no exposed signal routing used under the device.

FASTPULSE HIGH SPEED LAN TRANSCEIVERS

EMC Considerations

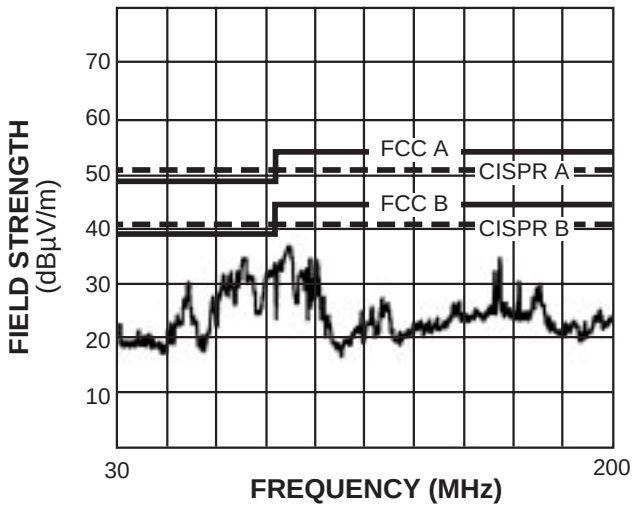
The ***FASTPULSE*** high speed LAN transceiver has been designed and tested to minimize EMI emissions and maximize its immunity. Some of the key measures employed on the transceivers are as follows:

- Multi-Layer board design, with optimized ground plane partitioning
- Edge-Rate control on transceiver IC outputs and signal filtering
- High-Performance magnetics tuned to transceiver silicon
- Galvanic shield formed from RJ-45 shield, body shield and connected to stake posts for direct chassis ground connection
- Onboard termination of unused cable pairs to chassis ground
- Extensive on-board decoupling of power signals
- Integrated design eliminates board parasitic effects

These built-in measures ease the difficult task normally facing the designer. Nevertheless, it is still crucial to employ good high speed PCB design rules in laying out the board, as outlined in the application section.

Physical shielding is an important factor in further minimizing emissions. The shielded RJ-45 connector has flared extensions which are intended to form a galvanic connection to cutout in the backplate. The backplate is typically connected to chassis ground. The body shield (G version) is further connected to the RJ-45 shield and the two mechanical stake posts. These should be soldered directly to the chassis ground. This chassis grounding scheme will minimize EMI emissions and also provide a direct discharge path to ground for ESD discharges to the exterior of the device, in line with IEC801 requirements. As an indication, the graph below shows typical EMI measurements obtained on a standard setup. It should be noted that EMC performance is a system measurement and very implementation specific.

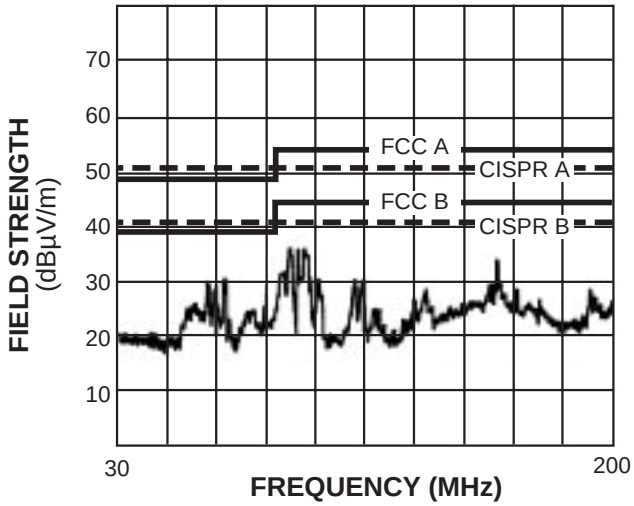
Typical EMI Field Strength (ATM-155)



Note:

PE-68532G in standard ATM 155 system @ 3 m, anechoic chamber. Contact Pulse for further setup details if required.

Typical EMI Field Strength (100Base-TX)



Note:

PE-68537G in standard 100-TX system @ 3 m, anechoic chamber. Contact Pulse for further setup details if required.

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