



3.3V CMOS BUFFER/CLOCK DRIVER

IDT49FCT3805/A

FEATURES:

- 0.5 MICRON CMOS Technology
- Guaranteed low skew < 500ps (max.)
- Very low duty cycle distortion < 1.0ns (max.)
- Very low CMOS power levels
- TTL compatible inputs and outputs
- Inputs can be driven from 3.3V or 5V components
- Two independent output banks with 3-state control
- 1:5 fanout per bank
- "Heartbeat" monitor output
- $V_{CC} = 3.3V \pm 0.3V$
- Available in SSOP, SOIC, and QSOP packages

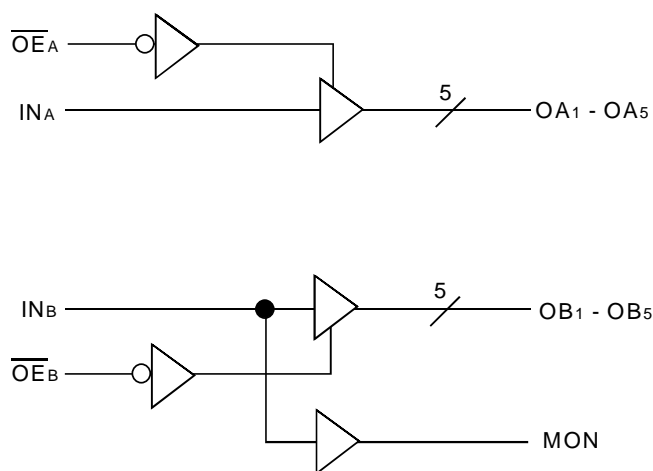
DESCRIPTION:

The FCT3805 is a 3.3 volt, non-inverting clock driver built using advanced dual metal CMOS technology. The device consists of two banks of drivers, each with a 1:5 fanout and its own output enable control. The device has a "heartbeat" monitor for diagnostics and PLL driving. The MON output is identical to all other outputs and complies with the output specifications in this document. The FCT3805 offers low capacitance inputs with hysteresis.

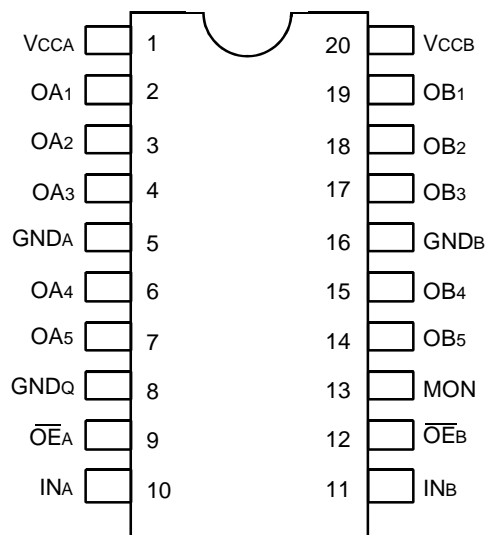
The FCT3805 is designed for high speed clock distribution where signal quality and skew are critical. The FCT3805 also allows single point-to-point transmission line driving in applications such as address distribution, where one signal must be distributed to multiple receivers with low skew and high signal quality.

For more information on using the FCT3805 with two different input frequencies on bank A and B, please see AN-236.

FUNCTIONAL BLOCK DIAGRAM



PIN CONFIGURATION



SOIC/ SSOP/ QSOP
TOP VIEW

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Description	Max	Unit
V _{TERM} (2)	Terminal Voltage with Respect to GND	-0.5 to +4.6	V
V _{TERM} (3)	Terminal Voltage with Respect to GND	-0.5 to +7	V
V _{TERM} (4)	Terminal Voltage with Respect to GND	-0.5 to V _{CC} +0.5	V
T _{STG}	Storage Temperature	-65 to +150	°C
I _{OUT}	DC Output Current	-60 to +60	mA

NOTES:

1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. V_{CC} terminals.
3. Input terminals.
4. Outputs and I/O terminals.

CAPACITANCE (T_A = +25°C, f = 1.0MHz)

Symbol	Parameter(1)	Conditions	Typ.	Max.	Unit
C _{IN}	Input Capacitance	V _{IN} = 0V	4.5	6	pF
C _{OUT}	Output Capacitance	V _{OUT} = 0V	5.5	8	pF

NOTE:

1. This parameter is measured at characterization but not tested.

PIN DESCRIPTION

Pin Names	Description
$\overline{OE}_A, \overline{OE}_B$	3-State Output Enable Inputs (Active LOW)
I _{NA} , I _{NB}	Clock Inputs
O _{AN} , O _{BN}	Clock Outputs
MON	Monitor Output

FUNCTION TABLE (1)

Inputs		Outputs	
$\overline{OE}_A, \overline{OE}_B$	I _{NA} , I _{NB}	O _{AN} , O _{BN}	MON
L	L	L	L
L	H	H	H
H	L	Z	L
H	H	Z	H

NOTE:

1. H = HIGH
L = LOW
Z = High-Impedance

DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified

Commercial: $T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, Industrial: $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$, $V_{CC} = 3.3\text{V} \pm 0.3\text{V}$

Symbol	Parameter	Test Conditions ⁽¹⁾	Min.	Typ.	Max.	Unit	
V _{IH}	Input HIGH Level (Input pins)	Guaranteed Logic HIGH Level	2	—	5.5	V	
	Input HIGH Level (I/O pins)		2	—	V _{CC} + 0.5		
V _{IL}	Input LOW Level (Input and I/O pins)	Guaranteed Logic LOW Level	-0.5	—	0.8	V	
I _{IH}	Input HIGH Current (Input pins)	V _{CC} = Max.	V _I = 5.5V	—	—	±1	μA
	Input HIGH Current (I/O pins)		V _I = V _{CC}	—	—	±1	
I _{IL}	Input LOW Current (Input pins)	V _{CC} = Max.	V _I = GND	—	—	±1	
	Input LOW Current (I/O pins)		V _I = GND	—	—	±1	
I _{OZH}	High Impedance Output Current (3-State Output Pins)	V _{CC} = Max.	V _O = V _{CC}	—	—	±1	μA
I _{OZL}			V _O = GND	—	—	±1	
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = -18mA	—	-0.7	-1.2	V	
I _{ODH}	Output HIGH Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾	-36	-60	-110	mA	
I _{ODL}	Output LOW Current	V _{CC} = 3.3V, V _{IN} = V _{IH} or V _{IL} , V _O = 1.5V ⁽³⁾	50	90	200	mA	
V _{OH}	Output HIGH Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OH} = -0.1mA	V _{CC} -0.2	—	—	V
			I _{OH} = -8mA	2.4 ⁽⁵⁾	3	—	
V _{OL}	Output LOW Voltage	V _{CC} = Min. V _{IN} = V _{IH} or V _{IL}	I _{OL} = 0.1mA	—	—	0.2	V
			I _{OL} = 16mA	—	0.2	0.4	
			I _{OL} = 24mA	—	0.3	0.5	
I _{OFF}	Input Power Off Leakage	V _{CC} = 0V, V _{IN} = 4.5V	—	—	±1	μA	
I _{OS}	Short Circuit Current ⁽⁴⁾	V _{CC} = Max., V _O = GND ⁽³⁾	-60	-135	-240	mA	
V _H	Input Hysteresis	—	—	150	—	mV	
I _{CC1}	Quiescent Power Supply Current	V _{CC} = Max. V _{IN} = GND or V _{CC}	—	0.1	10	μA	
I _{CC2}							
I _{CC3}							

NOTES:

1. For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 3.3V, +25°C ambient.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is guaranteed but not tested.
5. V_{OH} = V_{CC} - 0.6V at rated current.

POWER SUPPLY CHARACTERISTICS

Symbol	Parameter	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Unit
ΔI_{CC}	Quiescent Power Supply Current TTL Inputs HIGH	V _{CC} = Max. V _{IN} = V _{CC} - 0.6V ⁽³⁾		—	10	30	μA
I _{CCD}	Dynamic Power Supply Current ⁽⁴⁾	V _{CC} = Max. Outputs Open $\overline{OE}_A = \overline{OE}_B = GND$ Per Output Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND	—	0.035	0.06	mA/MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max. Outputs Open f _o = 25MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = V_{CC}$ Mon. Output Toggling	V _{IN} = V _{CC} V _{IN} = GND	—	0.9	1.6	mA
			V _{IN} = V _{CC} - 0.6V V _{IN} = GND	—	0.9	1.6	
		V _{CC} = Max. Outputs Open f _o = 50MHz 50% Duty Cycle $\overline{OE}_A = \overline{OE}_B = GND$ Eleven Outputs Toggling	V _{IN} = V _{CC} V _{IN} = GND	—	20	33 ⁽⁵⁾	
			V _{IN} = V _{CC} - 0.6V V _{IN} = GND	—	20	33 ⁽⁵⁾	

NOTES:

- For conditions shown as Max. or Min., use appropriate value specified under Electrical Characteristics for the applicable device type.
- Typical values are at V_{CC} = 3.3V, +25°C ambient.
- Per TTL driven input (V_{IN} = V_{CC} - 0.6V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply calculations.
- Values for these conditions are examples of the I_C formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}
 $I_C = I_{CC} + \Delta I_{CC} D_{HNT} + I_{CCD} (f_o N_o)$
 I_{CC} = Quiescent Current (I_{CC1}, I_{CC2} and I_{CC3})
 ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = V_{CC} - 0.6V)
 D_H = Duty Cycle for TTL Inputs High
 N_T = Number of TTL Inputs at D_H
 I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
 f_o = Output Frequency
 N_o = Number of Outputs at f_o
 All currents are in milliamps and all frequencies are in megahertz.

SWITCHING CHARACTERISTICS OVER OPERATING RANGE - COMMERCIAL^(3,4)

Symbol	Parameter	Conditions ⁽¹⁾	FCT3805		FCT3805A		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay INA to OAn, INb to OBn	CL = 50pF RL = 500Ω	1.5	5.8	1.5	5	ns
t _R	Output Rise Time		—	2	—	2	ns
t _F	Output Fall Time		—	2	—	2	ns
tsk(O)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.5	—	0.5	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output (t _{PHL} - t _{PLH})		—	1	—	1	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.5	—	1.2	ns
t _{PZL} t _{PZH}	Output Enable Time $\overline{OE}A$ to OAn, $\overline{OE}B$ to OBn		1.5	6.5	1.5	6	ns
t _{PLZ} t _{PHZ}	Output Disable Time $\overline{OE}A$ to OAn, $\overline{OE}B$ to OBn		1.5	5.5	1.5	5	ns

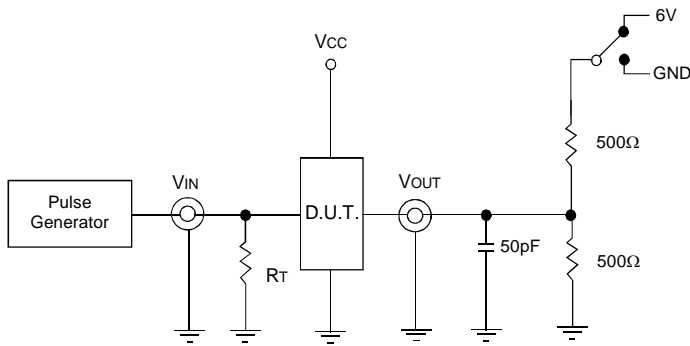
SWITCHING CHARACTERISTICS OVER OPERATING RANGE - INDUSTRIAL^(3,4)

Symbol	Parameter	Conditions ⁽¹⁾	FCT3805		FCT3805A		Unit
			Min. ⁽²⁾	Max.	Min. ⁽²⁾	Max.	
t _{PLH} t _{PHL}	Propagation Delay INA to OAn, INb to OBn	CL = 50pF RL = 500Ω	1.5	5.8	1.5	5.2	ns
t _R	Output Rise Time		—	2	—	2	ns
t _F	Output Fall Time		—	2	—	2	ns
tsk(O)	Output skew: skew between outputs of all banks of same package (inputs tied together)		—	0.6	—	0.6	ns
tsk(P)	Pulse skew: skew between opposite transitions of same output (t _{PHL} - t _{PLH})		—	1	—	1	ns
tsk(T)	Package skew: skew between outputs of different packages at same power supply voltage, temperature, package type and speed grade		—	1.5	—	1.2	ns
t _{PZL} t _{PZH}	Output Enable Time $\overline{OE}A$ to OAn, $\overline{OE}B$ to OBn		1.5	6.5	1.5	6	ns
t _{PLZ} t _{PHZ}	Output Disable Time $\overline{OE}A$ to OAn, $\overline{OE}B$ to OBn		1.5	5.5	1.5	5	ns

NOTES:

1. See test circuits and waveforms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. t_{PLH}, t_{PHL}, tsk(t) are production tested. All other parameters guaranteed but not production tested.
4. Propagation delay range indicated by Min. and Max. limit is due to V_{cc}, operating temperature and process parameters. These propagation delay limits do not imply skew.

TEST CIRCUITS AND WAVEFORMS



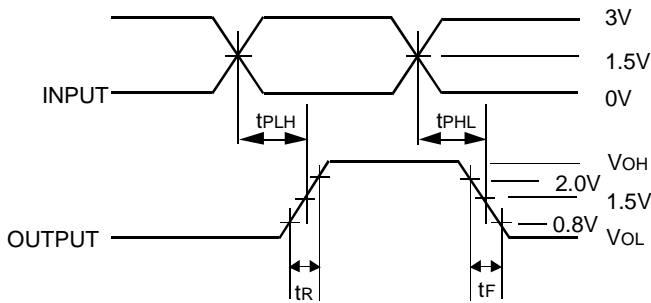
Test Circuits for All Outputs

SWITCH POSITION

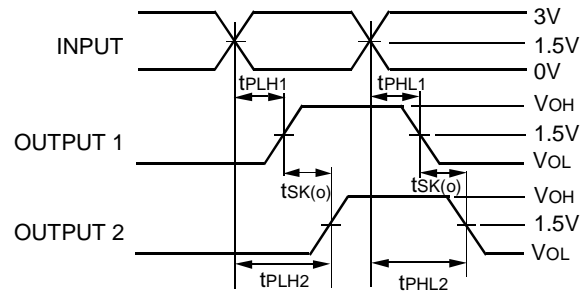
Test	Switch
Disable LOW Enable LOW	6V
Disable HIGH Enable HIGH	GND

DEFINITIONS:

CL = Load capacitance: includes jig and probe capacitance.
RT = Termination resistance: should be equal to Zout of the Pulse Generator.

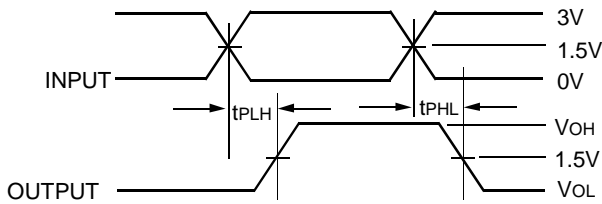


Package Delay

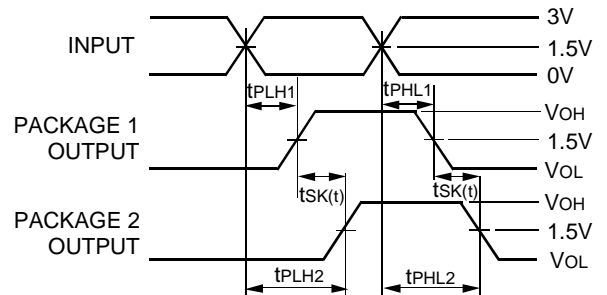


$$tsK(o) = |tPLH2 - tPLH1| \text{ or } |tPHL2 - tPHL1|$$

Output Skew - $tsK(o)$

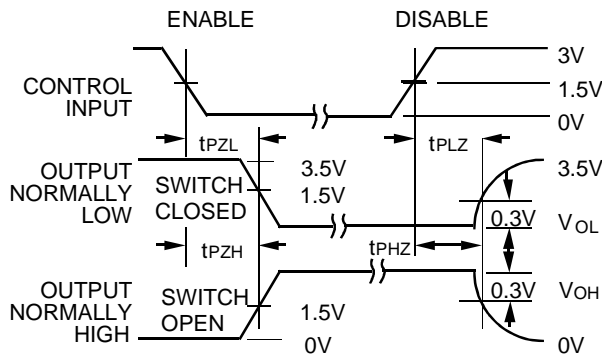


Pulse Skew - $tsK(p)$



$$tsK(t) = |tPLH2 - tPLH1| \text{ or } |tPHL2 - tPHL1|$$

Package Skew - $tsK(t)$

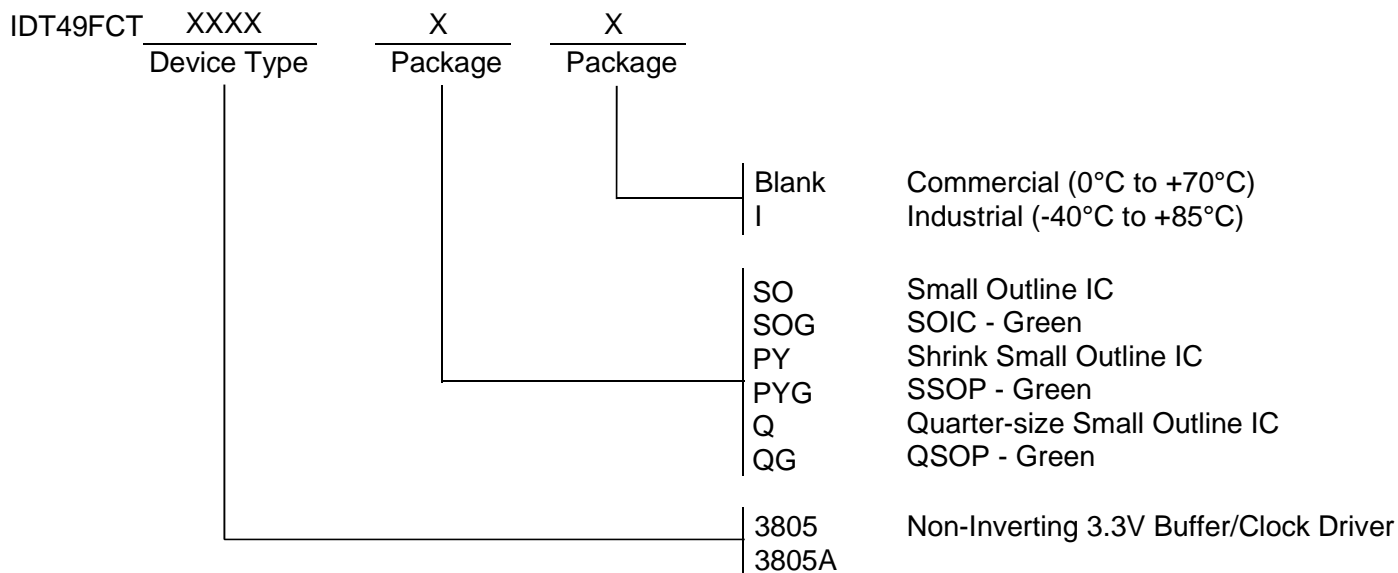


Output Skew - $tsK(x)$

NOTES:

1. Diagram shown for input Control Enable-LOW and input Control Disable-HIGH
2. Pulse Generator for All Pulses: $f \leq 1.0\text{MHz}$; $t_f \leq 2.5\text{ns}$; $t_r \leq 2.5\text{ns}$

ORDERING INFORMATION



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