650MHz, Gain of 5, Low Noise Amplifiers

The EL5134, EL5135, EL5234, and EL5235 are ultra-low voltage noise, high speed voltage feedback amplifiers that are ideal for applications requiring low voltage noise, including communications and imaging. These devices offer extremely low power consumption for exceptional noise performance. Stable at gains as low as 5, these devices offer 100mA of drive performance. Not only do these devices find perfect application in high gain applications, they maintain their performance down to lower gain settings.

These amplifiers are available in small package options (SOT-23) as well as the MSOP and the industry-standard SO packages. All parts are specified for operation over the -40°C to +85°C temperature range.

Features

- 650MHz -3dB bandwidth
- Ultra low noise 1.9nV/√Hz
- 450V/μs slew rate
- Low supply current = 7.3mA
- Single supplies from 5V to 12V
- Dual supplies from ±2.5V to ±5V
- Fast disable on the EL5134 and EL5234
- Duals EL5234 and EL5235
- Low cost
- Pb-free plus anneal available (RoHS compliant)

Applications

- Imaging
- Instrumentation
- Communications devices

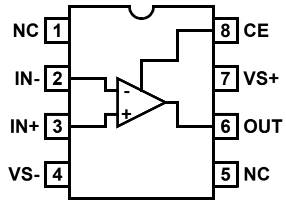
Ordering Information

PART NUMBER	PART MARKING	TAPE & REEL	PACKAGE	PKG. DWG. #
EL5134IS	5134IS	-	8 Ld SO	MDP0027
EL5134IS-T7	5134IS	7”	8 Ld SO	MDP0027
EL5134IS-T13	5134IS	13”	8 Ld SO	MDP0027
EL5134ISZ (See Note)	5134ISZ	-	8 Ld SO (Pb-Free)	MDP0027
EL5134ISZ-T7 (See Note)	5134ISZ	7”	8 Ld SO (Pb-Free)	MDP0027
EL5134ISZ-T13 (See Note)	5134ISZ	13”	8 Ld SO (Pb-Free)	MDP0027
EL5135IW-T7	BDAA	7” (3K pcs)	5 Ld SOT-23	MDP0038
EL5135IW-T7A	BDAA	7” (250 pcs)	5 Ld SOT-23	MDP0038
EL5135IWZ-T7 (See Note)	BTAA	7” (3K pcs)	5 Ld SOT-23 (Pb-Free)	MDP0038
EL5135IWZ-T7A (See Note)	BTAA	7” (250 pcs)	5 Ld SOT-23 (Pb-Free)	MDP0038
EL5234IY	BWAAA	-	10 Ld MSOP	MDP0043
EL5234IY-T7	BWAAA	7”	10 Ld MSOP	MDP0043
EL5234IY-T13	BWAAA	13”	10 Ld MSOP	MDP0043
EL5235IS	5235IS	-	8 Ld SO	MDP0027
EL5235IS-T7	5235IS	7”	8 Ld SO	MDP0027
EL5235IS-T13	5235IS	13”	8 Ld SO	MDP0027

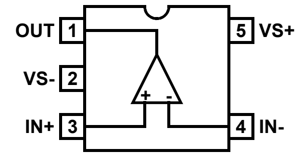
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Pinouts

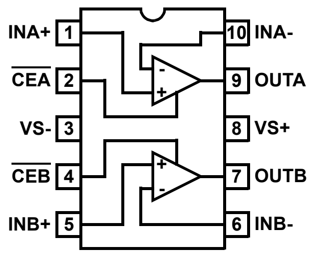
EL5134
(8 LD SO)
TOP VIEW



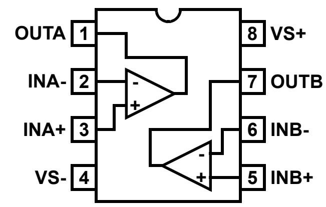
EL5135
(5 LD SOT-23)
TOP VIEW



EL5234
(10 LD MSOP)
TOP VIEW



EL5235
(8 LD SO)
TOP VIEW



Absolute Maximum Ratings (T_A = 25°C)

Supply Voltage from V_S+ to V_S- 13.2V
SR, Supply Rate of Supply Voltage Slew. . . . . Maximum 1V/µs
I_{IN}-, I_{IN}+, CE . . . . ±5mA
Continuous Output Current 100mA
Power Dissipation . . . . See Curves
Storage Temperature . . . .-65°C to +125°C
Operating Temperature . . . .-40°C to +85°C
Operating Junction Temperature . . . . +125°C

CAUTION: Stresses above those listed in “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

Electrical Specifications

V_S+ = +5V, V_S- = -5V, R_L = 500Ω, R_F = 100Ω, R_G = 25Ω, T_A = 25°C, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_{OS}	Offset Voltage		-1	0.2	1	mV
		EL5234		0.3	±1.5	mV
T_CV_{OS}	Offset Voltage Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		-0.8		µV/°C
IB	Input Bias Current	V_{IN} = 0V	2.5	3.7	5.5	µA
I_{OS}	Input Offset Current	V_{IN} = 0V	-0.7	0.3	0.7	nA
T_CI_{OS}	Input Bias Current Temperature Coefficient	Measured from T_{MIN} to T_{MAX}		-3		nA/°C
PSRR	Power Supply Rejection Ratio	V_S+ = 4.75V to 5.25V	75	85		dB
CMRR	Common Mode Rejection Ratio	V_{CM} = ±3V	80	108		dB
CMIR	Common Mode Input Range	Guaranteed by CMRR test	±3	±3.3		V
R_{IN}	Input Resistance	Common mode	5	16		MΩ
C_{IN}	Input Capacitance			1		pF
I_S	Supply Current		5.6	6.7	7.8	mA
AVOL	Open Loop Gain	R_L = 1kΩ to GND	4.0	8.0		kV/V
V_O	Voltage Swing	R_L = 1kΩ, R_F = 900Ω, R_G = 100Ω	±3.5	3.9		V
		R_L = 150Ω, R_F = 900Ω, R_G = 100Ω	±3.3	3.65		V
I_{SC}	Short Circuit Current	R_L = 10Ω	70	140		mA
BW	-3dB Bandwidth	A_V = 5, R_L = 1kΩ		600		MHz
BW	±0.1dB Bandwidth	A_V = 5, R_L = 1kΩ		40		MHz
GBWP	Gain Bandwidth Product			1500		MHz
PM	Phase Margin	R_L = 1kΩ, C_L = 6pF		55		°
SR	Slew Rate	V_S = +5V, R_L = 150Ω, V_{OUT} = 0V to 3V	350	475		V/µs
t_R	Rise Time	±0.1V_{STEP}		1.75		ns
t_F	Fall Time	±0.1V_{STEP}		1.75		ns
OS	Overshoot	±0.1V_{STEP}		25		%
t_S	0.01% Settling Time			14		ns
dG	Differential Gain	A_V = 5, R_F = 1kΩ		0.01		%
dP	Differential Phase	A_V = 5, R_F = 1kΩ		0.01		°
e_N	Input Noise Voltage	f = 10kHz		1.9		nV/√Hz
i_N	Input Noise Current	f = 10kHz		0.9		pA/√Hz

Electrical Specifications $V_S+ = +5V$, $V_S- = -5V$, $R_L = 500\Omega$, $R_F = 100\Omega$, $R_G = 25\Omega$, $T_A = 25°C$, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY (EL5134, EL5234)						
I_{SOFF+}	Supply Current - Disabled, per Amplifier		0		+25	µA
I_{SOFF-}	Supply Current - Disabled, per Amplifier	No load, V_{IN} = 0V	-25	-14	0	µA
ENABLE (EL5134, EL5234)						
I_{IHCE}	$\overline{CE}$ Pin Input High Current	$\overline{CE}$ = V_S+	1	10	+25	µA
I_{ILCE}	$\overline{CE}$ Pin Input Low Current	$\overline{CE}$ = (V_S+) -5V	-1	0	+1	µA
V_{IHCE}	$\overline{CE}$ Input High Voltage for Power-down		V_S+ - 1			V
V_{ILCE}	$\overline{CE}$ Input Low Voltage for Power-down				V_S+ - 3	V

Typical Performance Curves

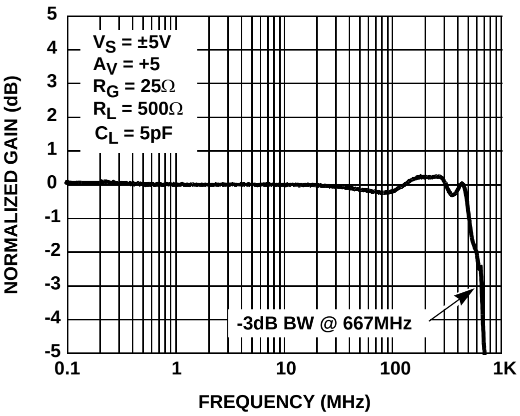


FIGURE 1. GAIN vs FREQUENCY (-3dB BANDWIDTH)

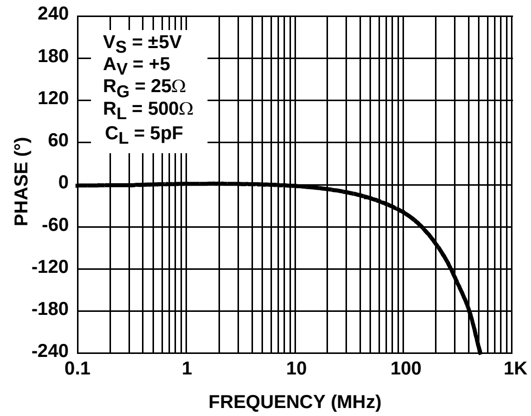


FIGURE 2. PHASE vs FREQUENCY

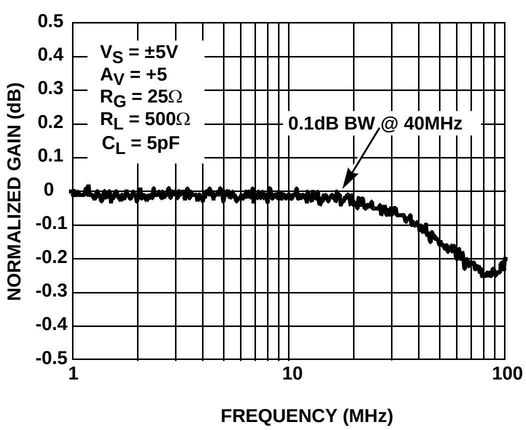


FIGURE 3. 0.1dB BANDWIDTH

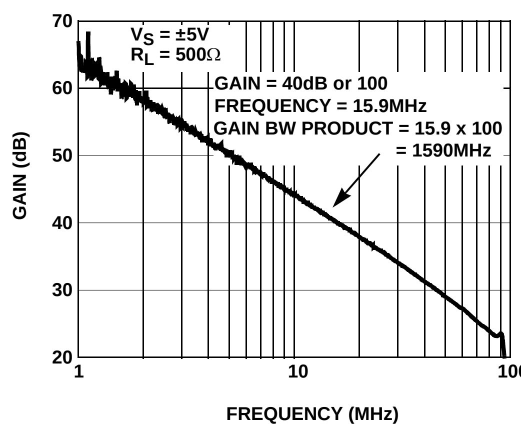


FIGURE 4. GAIN BANDWIDTH PRODUCT

Typical Performance Curves (Continued)

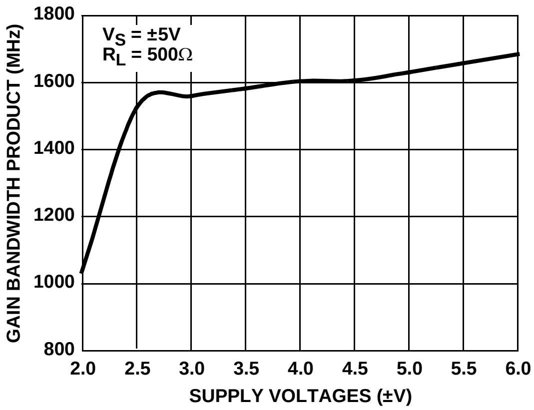


FIGURE 5. GAIN BANDWIDTH PRODUCT vs SUPPLY VOLTAGES

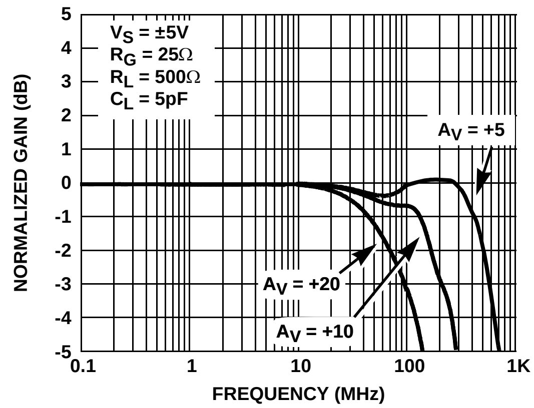


FIGURE 6. GAIN vs FREQUENCY FOR VARIOUS +A_V

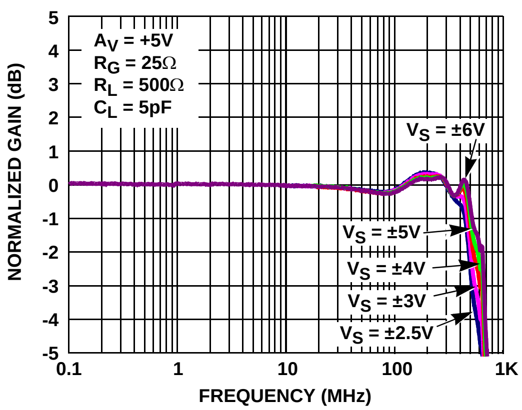


FIGURE 7. GAIN vs FREQUENCY FOR VARIOUS ±V_S

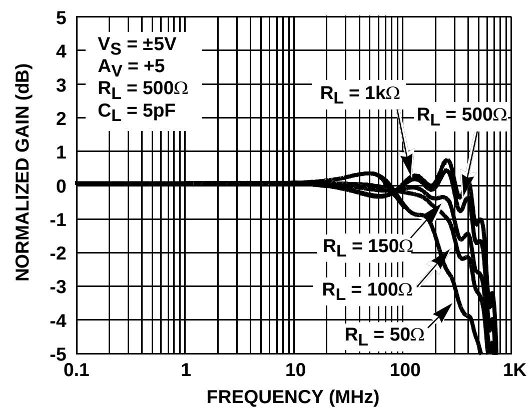


FIGURE 8. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD} (A_V = +5)

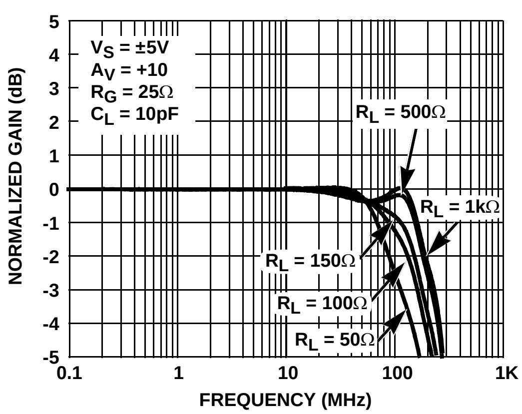


FIGURE 9. GAIN vs FREQUENCY FOR VARIOUS R_{LOAD} (A_V = +10)

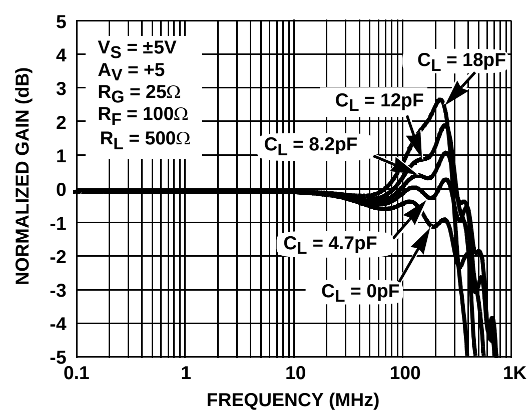


FIGURE 10. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD} (A_V = +5)

Typical Performance Curves (Continued)

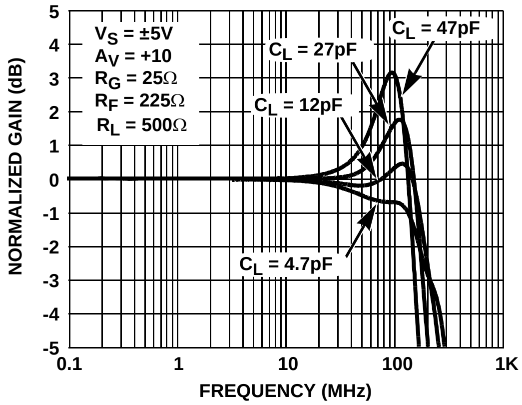


FIGURE 11. GAIN vs FREQUENCY FOR VARIOUS C_{LOAD} (A_V = +10)

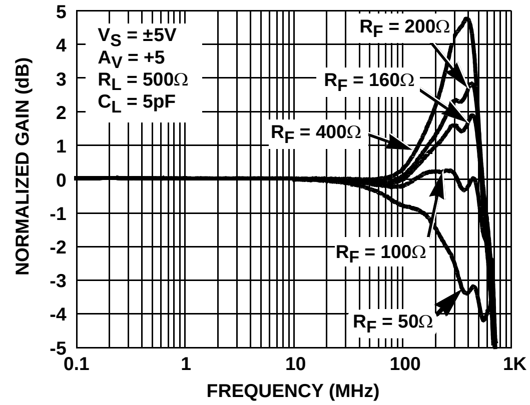


FIGURE 12. GAIN vs FREQUENCY FOR VARIOUS R_F (A_V = +5)

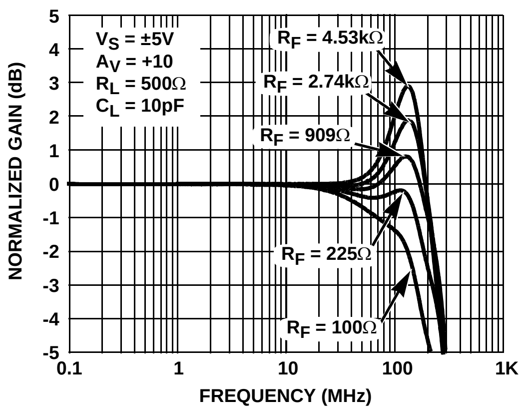


FIGURE 13. GAIN vs FREQUENCY FOR VARIOUS R_F (A_V = +10)

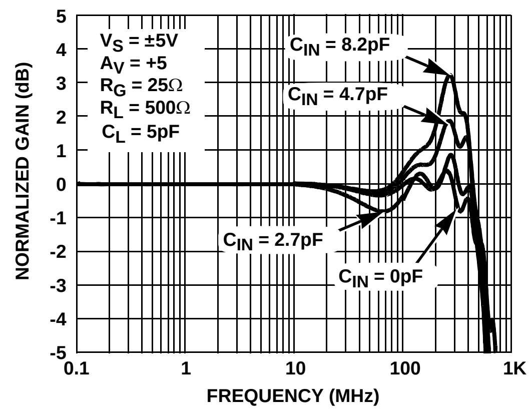


FIGURE 14. GAIN vs FREQUENCY FOR VARIOUS C_{IN}(-) (A_V = +5)

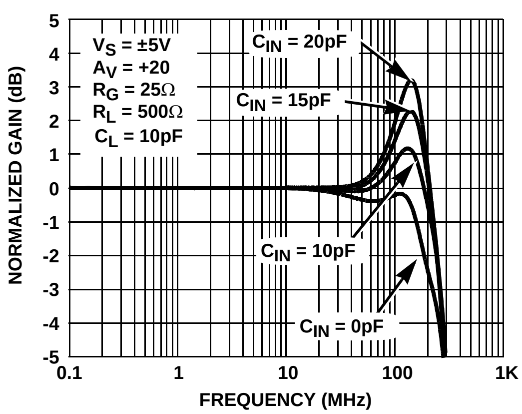


FIGURE 15. GAIN vs FREQUENCY FOR VARIOUS C_{IN}(-) (A_V = +10)

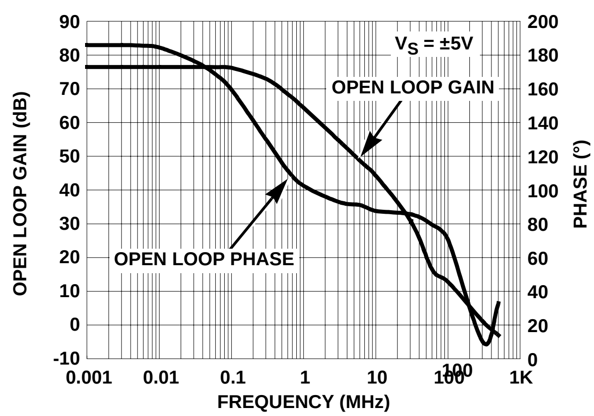


FIGURE 16. OPEN LOOP GAIN and PHASE vs FREQUENCY

Typical Performance Curves (Continued)

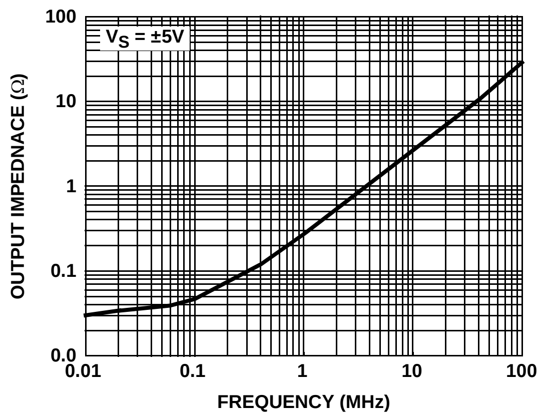


FIGURE 17. OUTPUT IMPEDANCE vs FREQUENCY

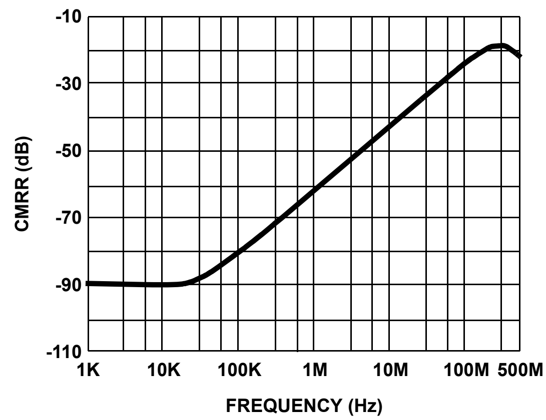


FIGURE 18. CMRR vs FREQUENCY

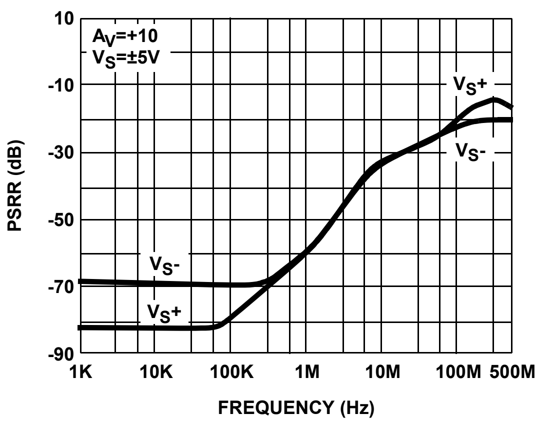


FIGURE 19. PSRR vs FREQUENCY

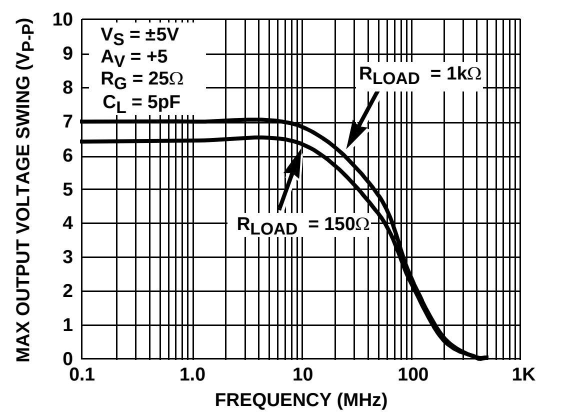


FIGURE 20. MAX OUTPUT VOLTAGE SWING vs FREQUENCY

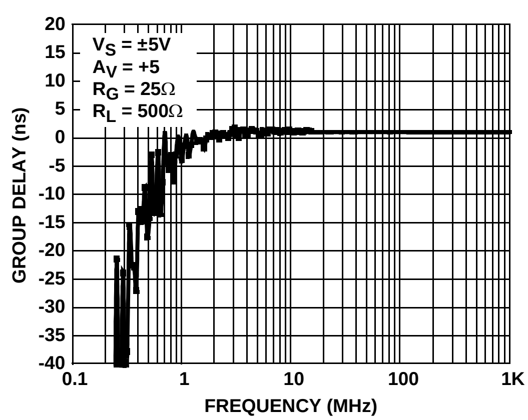


FIGURE 21. GROUP DELAY vs FREQUENCY

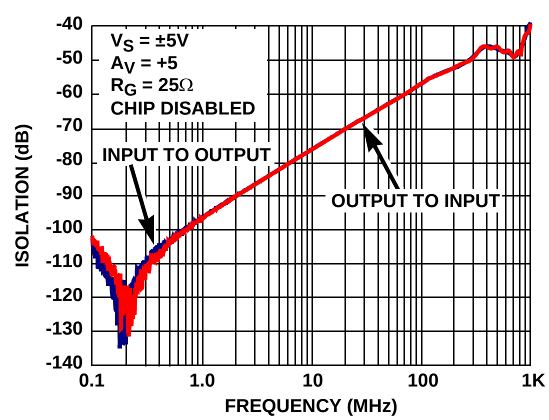


FIGURE 22. INPUT AND OUTPUT ISOLATION

Typical Performance Curves (Continued)

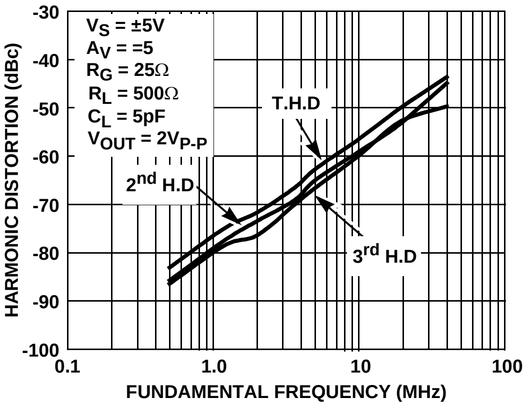


FIGURE 23. HARMONIC DISTORTION vs FREQUENCY

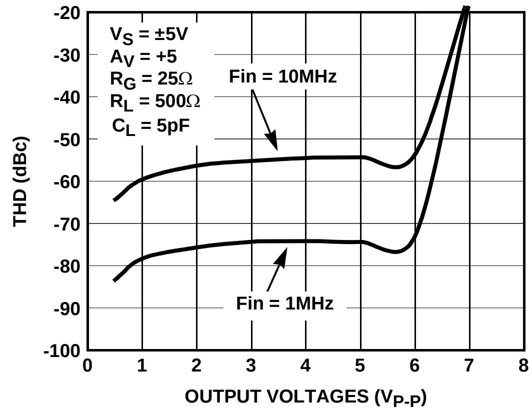


FIGURE 24. TOTAL HARMONIC DISTORTION vs OUTPUT VOLTAGES

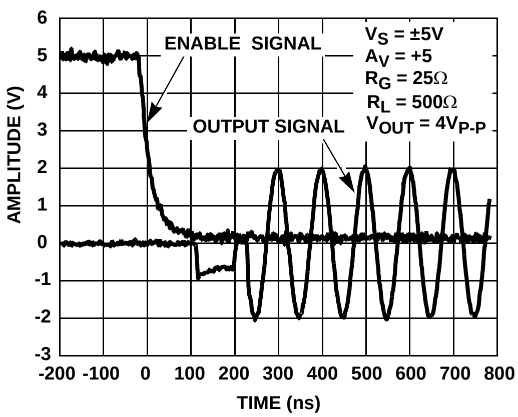


FIGURE 25. TURN-ON TIME

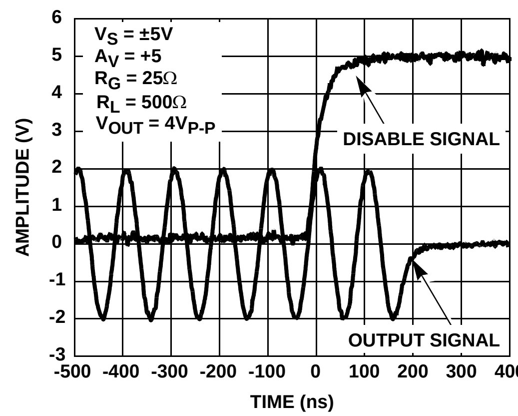


FIGURE 26. TURN-OFF TIME

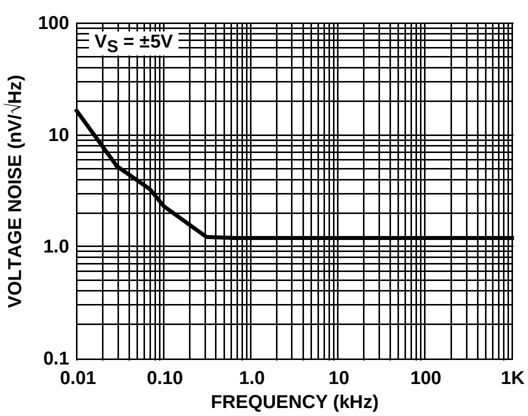


FIGURE 27. EQUIVALENT INPUT VOLTAGE NOISE vs FREQUENCY

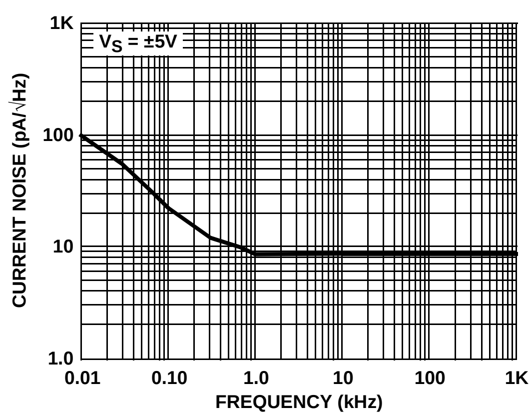


FIGURE 28. EQUIVALENT INPUT CURRENT NOISE vs FREQUENCY

Typical Performance Curves (Continued)

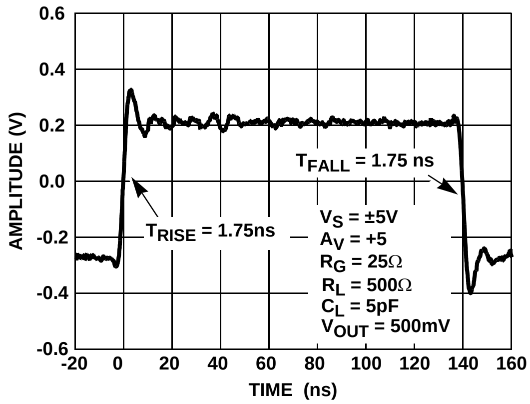


FIGURE 29. SMALL SIGNAL STEP RESPONSE_RISE AND FALL TIME

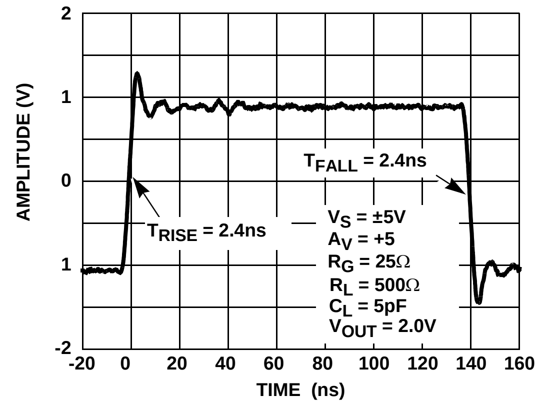


FIGURE 30. LARGE SIGNAL STEP RESPONSE_RISE AND FALL TIME

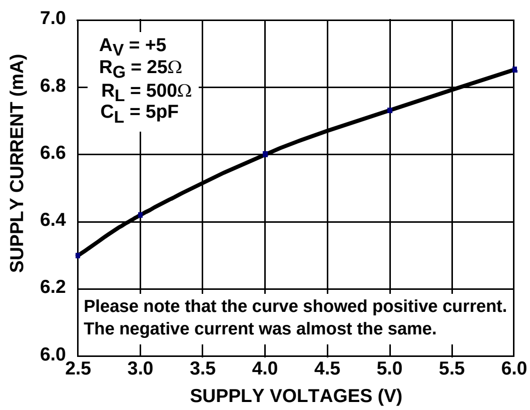


FIGURE 31. SUPPLY CURRENT vs SUPPLY VOLTAGE

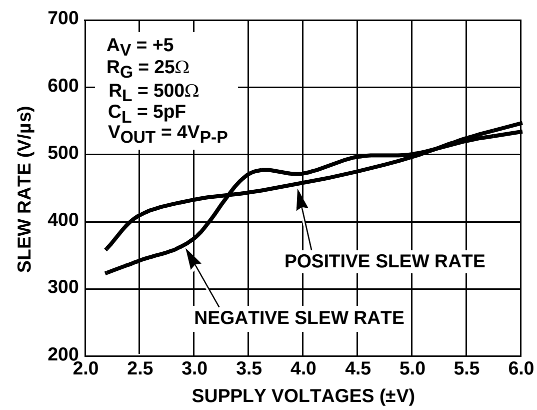


FIGURE 32. SLEW RATE vs SUPPLY VOLTAGES

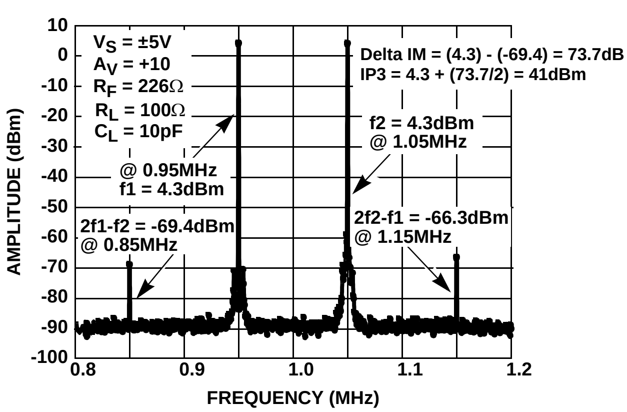


FIGURE 33. THIRD ORDER IMD INTERCEPT (IP3)

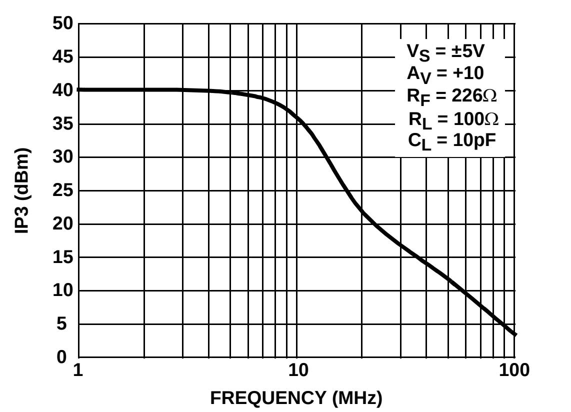


FIGURE 34. THIRD ORDER IMD INTERCEPT vs FREQUENCY

Typical Performance Curves (Continued)

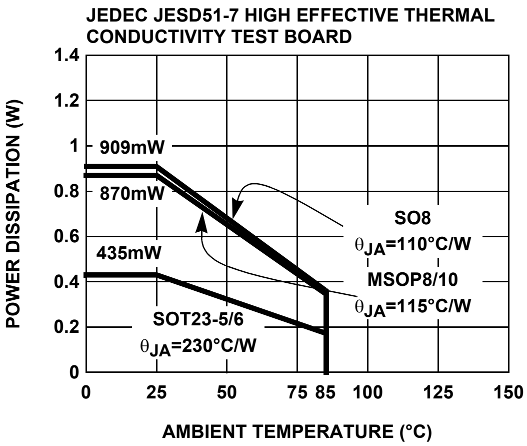


FIGURE 35. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

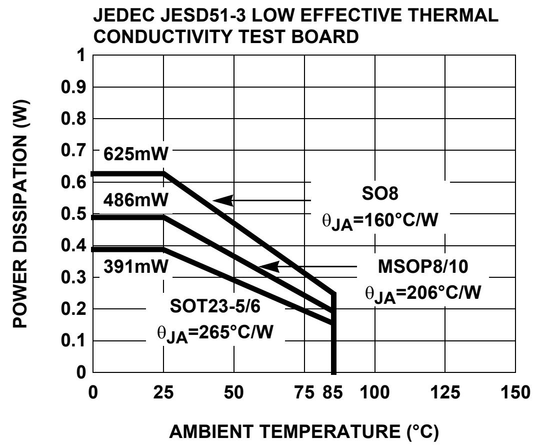


FIGURE 36. PACKAGE POWER DISSIPATION vs AMBIENT TEMPERATURE

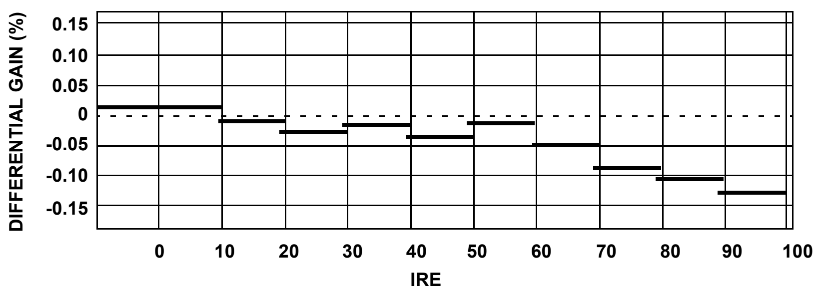


FIGURE 37. DIFFERENTIAL GAIN (%)

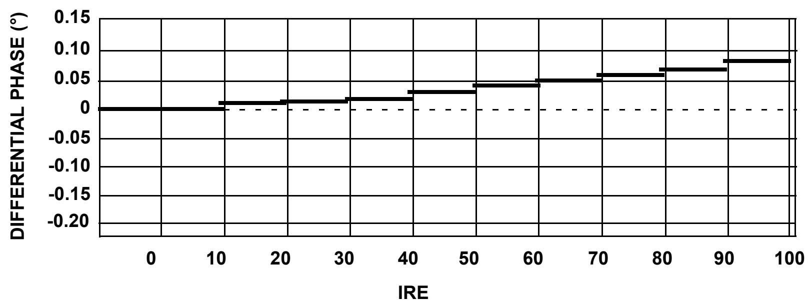


FIGURE 38. DIFFERENTIAL PHASE (°)