150mA, 4µA Quiescent Current Regulator

Features

- Ultra Low Quiescent Current: 4µA
- Ultra Low Dropout Voltage: 200mV@3.3V/150mA
- Fixed Output Voltages: 1.2V~3.5V, steps 100mV
- Guaranteed 150mA Output Current
- Stable with 1µF Output Capacitor
- Ceramic Capacitor can be used
- Current Limit Protection
- Controlled Short Circuit Current: 50mA
- Build in Thermal Protection
- SOT-23, SOT-23-5 and SOT-89 packages
- Lead Free Available (RoHS Compliant)

Applications

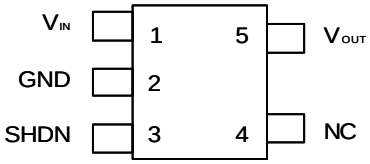
- Hand-held Equipment
- RTC or CMOS Backup Power
- Battery Powered Equipment

General Description

The APL5101/2 are micro-power, ultra low dropout linear regulator, which operate from 2V to 6V input voltage and deliver up to 150mA. Typical dropout voltage is only 200mV at 150mA loading. Designed for use in battery-powered system, the low 4µA quiescent current makes it an ideal choice. Design with an internal P-channel MOSFET pass transistor, the APL5101/2 maintain a low supply current, independent of the load current and dropout voltage. Other features include thermal-shutdown protection and current limit protection to ensure specified output current and controlled short-circuit current. The APL5101/2 regulator come in a miniature SOT-23, SOT-23-5 and SOT-89 packages.

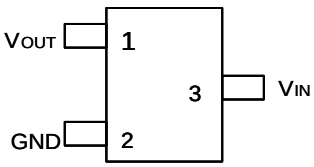
Pin Configuration

SOT-23-5



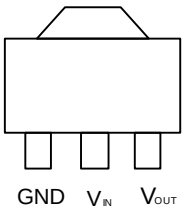
APL5101

SOT-23



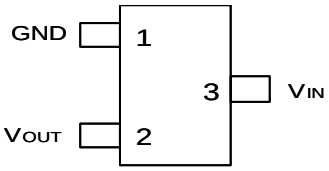
APL5101

SOT-89



APL5101

SOT-23



APL5102

Ordering and Marking Information

APL5101/2 - □□ □□ - □□□ Lead Free Code Handling Code Temp. Range Package Code Voltage Code	Package Code A : SOT-23 B : SOT-23-5 D : SOT-89 Operating Ambient Temp. Range I : -40 to 85°C Handling Code TR : Tape & Reel Voltage Code : 12 : 1.2V ~ 35 : 3.5V Lead Free Code L : Lead Free Device Blank : Original Device
APL5101 -12 A/B: 105X X - Date Code : 5 - 1.2V	APL5101 -12 D : APL5101 XXXXX12 XXXXX - Date Code : 12 - 1.2V
APL5102 -12 A/B: AB5X X - Date Code : 5 - 1.2V	APL5102 -12 D : APL5102 XXXXX12 XXXXX - Date Code : 12 - 1.2V

Note: ANPEC lead-free products contain molding compounds/die attach materials and 100% matte tin plate termination finish; which are fully compliant with RoHS and compatible with both SnPb and lead-free soldiering operations. ANPEC lead-free products meet or exceed the lead-free requirements of IPC/JEDEC J STD-020C for MSL classification at lead-free peak reflow temperature.

SOT-23 and SOT-23-5 packages

Product Name	Marking	Product Name	Marking
APL5101-12A/B	105X	APL5102-12A/B	AB5X
APL5101-13A/B	107X	APL5102-13A/B	AB7X
APL5101-14A/B	108X	APL5102-14A/B	AB8X
APL5101-15A/B	109X	APL5102-15A/B	AB9X
APL5101-16A/B	10AX	APL5102-16A/B	ABAX
APL5101-17A/B	10BX	APL5102-17A/B	ABBX
APL5101-18A/B	10CX	APL5102-18A/B	ABCX
APL5101-19A/B	10DX	APL5102-19A/B	ABDX
APL5101-20A/B	10EX	APL5102-20A/B	ABEX
APL5101-21A/B	10FX	APL5102-21A/B	ABFX
APL5101-22A/B	10GX	APL5102-22A/B	ABGX
APL5101-23A/B	10HX	APL5102-23A/B	ABHX
APL5101-24A/B	10IX	APL5102-24A/B	ABIX
APL5101-25A/B	10JX	APL5102-25A/B	ABJX
APL5101-26A/B	10KX	APL5102-26A/B	ABKX
APL5101-27A/B	10LX	APL5102-27A/B	ABLX
APL5101-28A/B	10MX	APL5102-28A/B	ABMX
APL5101-29A/B	10NX	APL5102-29A/B	ABNX
APL5101-30A/B	10OX	APL5102-30A/B	ABOX
APL5101-31A/B	10PX	APL5102-31A/B	ABPX
APL5101-32A/B	10QX	APL5102-32A/B	ABQX
APL5101-33A/B	10RX	APL5102-33A/B	ABRX
APL5101-34A/B	10SX	APL5102-34A/B	ABSX
APL5101-35A/B	10TX	APL5102-35A/B	ABTX

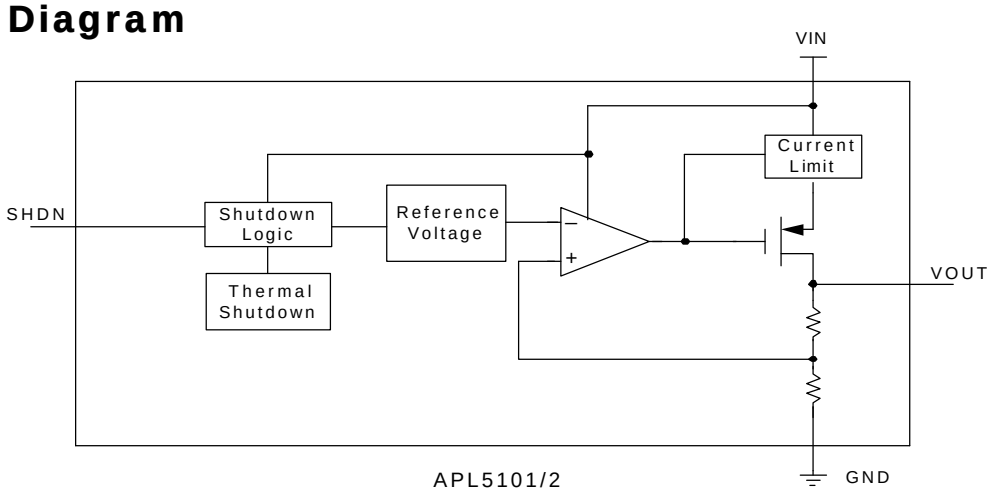
Pin Description

PIN		I/O	Description
No.	Name		
1	V_{IN}	I	Voltage supply input pin
2	GND		GND pin
3	SHDN	I	Shutdown control pin, high = off, low = normal
4	NC		Not connected
5	V_{OUT}	O	Regulator output pin

Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
V_{IN},V_{OUT}	Input Voltage or Out Voltage	6.5	V
SHDN	V_{OUT} Shutdown Control Pin	6.5	V
$R_{TH,JA}$	Thermal Resistance-Junction to Ambient SOT-23 SOT-23-5 SOT-89	 260 260 180	°C /W
$R_{TH,JC}$	Thermal Resistance-Junction to Ambient SOT-23 SOT-23-5 SOT-89	 130 130 90	°C /W
P_D	Power Dissipation	Internally Limited	W
T_J	Operating Junction Temperature Control Section Power Transistor	 0 to 125 0 to 140	°C
T_{STG}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (Soldering, 10 second)	260	°C

Block Diagram



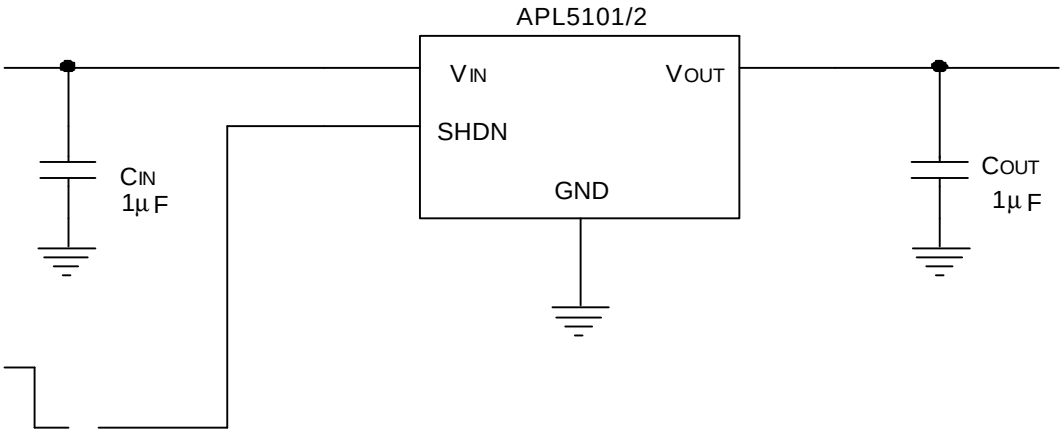
Electrical Characteristics

Unless otherwise noted these specificatons apply over full temperature, V_{IN} = 5V, C_{IN} = C_{OUT} = 1µF, T_A = -40 to 85°C. Typical values refer to T_A = 25°C.

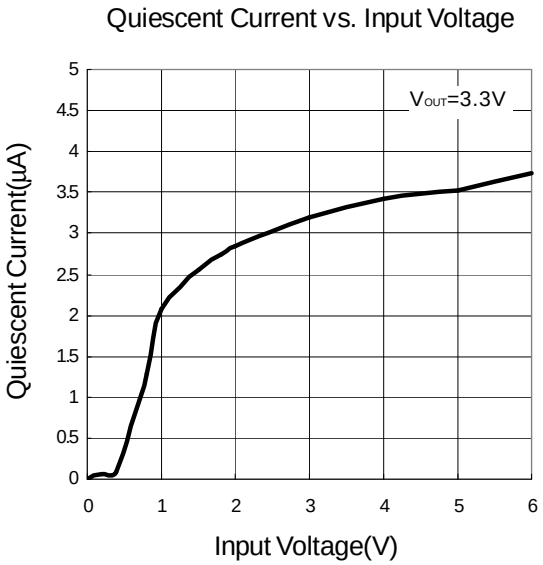
Symbol	Parameter	Test Condition	APL5101/2			Unit
			Min.	Typ.	Max.	
V_{IN}	Input Voltage		2		6	V
V_{OUT}	Output Voltage Accuracy	V_{IN} = 5V	-2		2	%
	Output Voltage Range		1.2		3.5	V
I_{LIMIT}	Current Limit	V_{IN} = 5V	250	300	370	mA
I_Q	Quiescent Current	I_{OUT} = 0mA		4	7	µA
		I_{OUT} = 150mA		4	10	
	Shutdown Supply Current	V_{SHDN} = High		0.1	1	
I_{OUT}	Load Current		150			mA
REG_{LINE}	Line Regulation	V_{OUT} + 0.5V<V_{IN}<6V, I_{OUT} = 10mA		2	10	mV
REG_{LOAD}	Load Regulation	V_{IN} = 5V, 0Ma<I_{OUT}<I_{MAX}		15	30	mV
V_{DROP}	Dropout Voltage (NOTE)	V_{OUT} = 1.4V, I_{OUT} = 150mA		1000	1300	mV
		V_{OUT} = 1.8V, I_{OUT} = 150mA		600	900	
		V_{OUT} = 3.3V, I_{OUT} = 150mA		200	300	
PSRR	Ripple Rejection	F = 1kHz, C_{OUT} = 1µF, I_{OUT} = 10mA	30	40		dB
I_{SHORT}	Short Circuit Current	V_{OUT} = 0V	40	50	60	mA
e_n	Noise	F = 22Hz to 80kHz, C_{OUT} = 1µF, I_{OUT} = 10mA		200	250	μV_{RMS}
I_{SHDN}	Shutdown Input Bias Current	V_{SHDN} = Low		0.1	1	µA
V_{SHDN}	High Threshold Voltage		1.6		V_{IN}+0.3	V
	Low Threshold Voltage		-0.3		0.4	V
T_{EXIT}	Shutdown Exit Delay	V_{OUT} = 90%, R_{LOAD} = 25Ω	1.5	2	2.5	mS
OTS	Over Temperature Shutdown		120	135		°C
	Over Temperature Shutdown Hysteresis		10	20	30	°C
TC	Output Voltage Temperature Coefficient	T_A = -40°C ~ 100°C		100	200	ppm/°C
C_{OUT}	Output Capacitor		1		10	µ F
	ESR		10		1000	mΩ

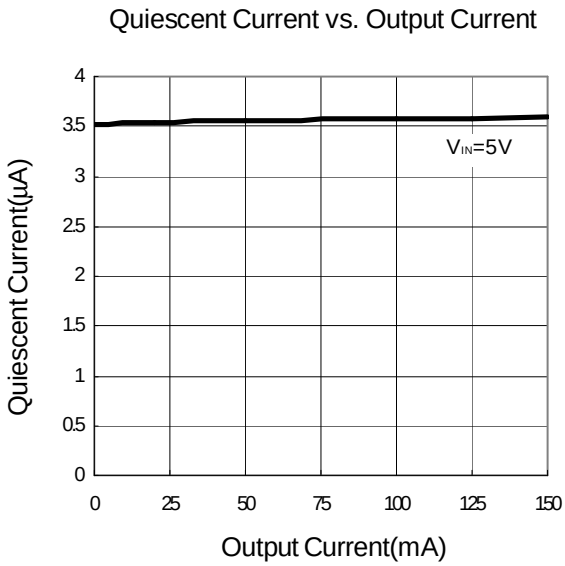
Note: Dropout voltage definition:V_{IN}-V_{OUT} when V_{OUT} is 2% below the value of V_{OUT} for V_{IN}= V_{OUT}+1V.

Application Circuit



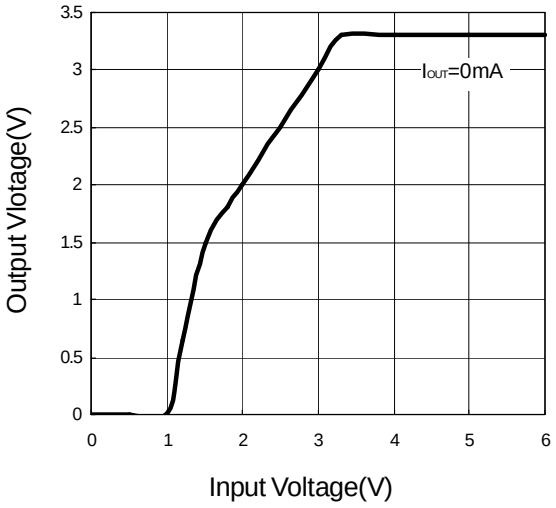
Application Characteristics



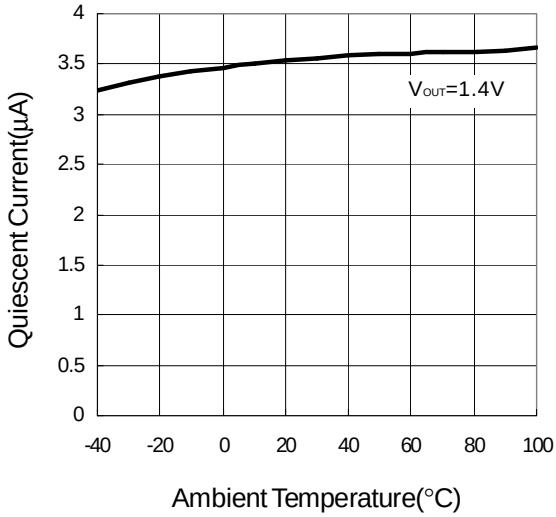


Application Characteristics (Cont.)

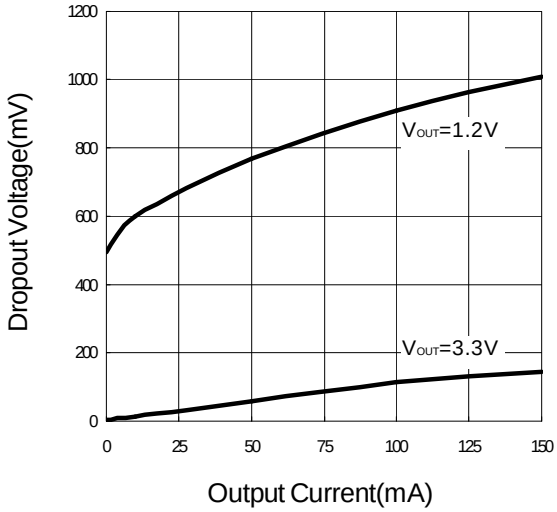
Output Voltage vs. Input Voltage



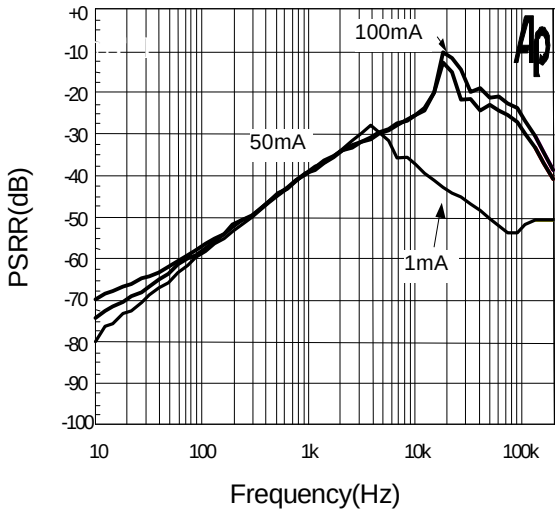
Quiescent Current vs. Ambient Temperature



Dropout Voltage vs. Output Current

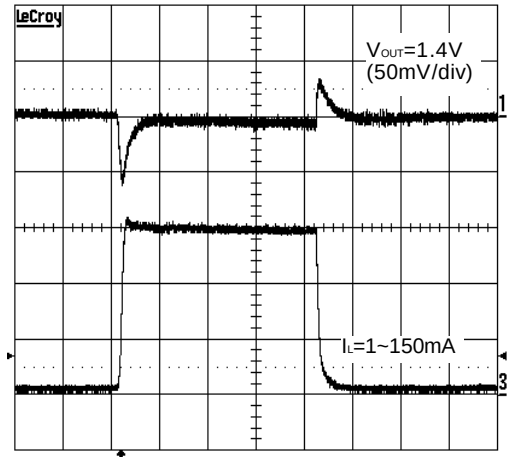


PSRR vs. Frequency



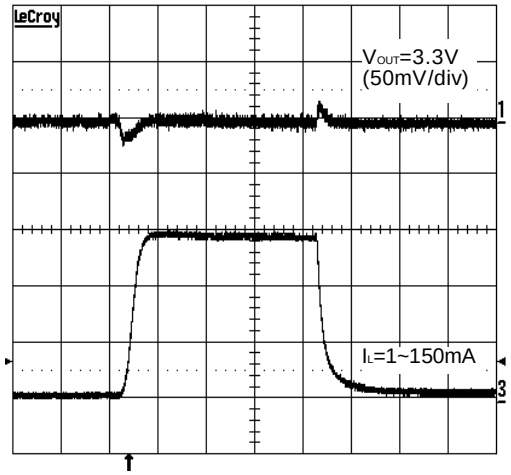
Application Characteristics (Cont.)

Load Transient Response



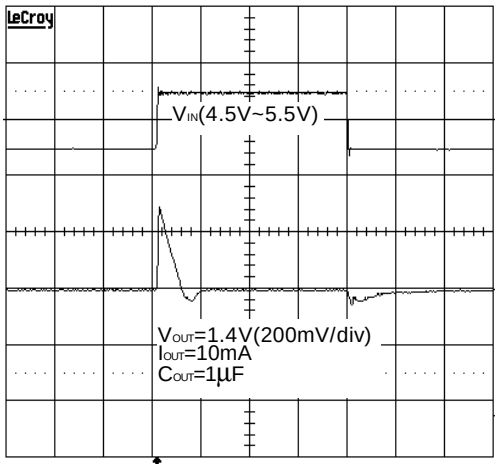
Time(0.5ms/div)

Load Transient Response



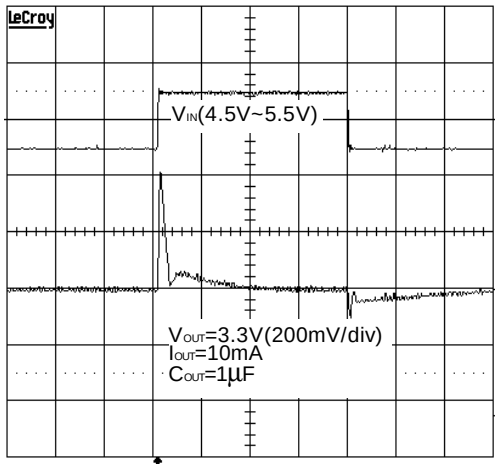
Time(0.5ms/div)

Line Transient Response



Time(0.1ms/div)

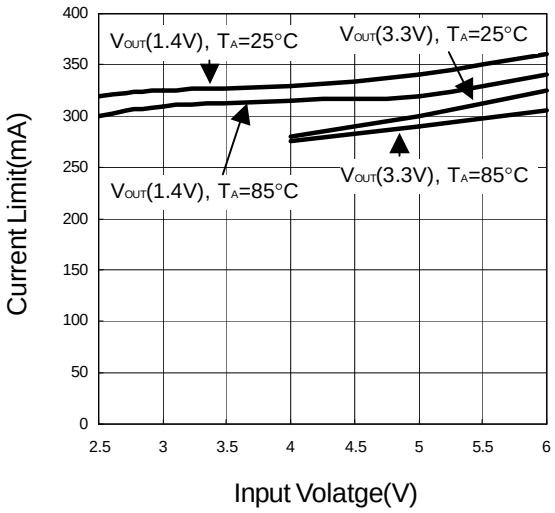
Line Transient Response



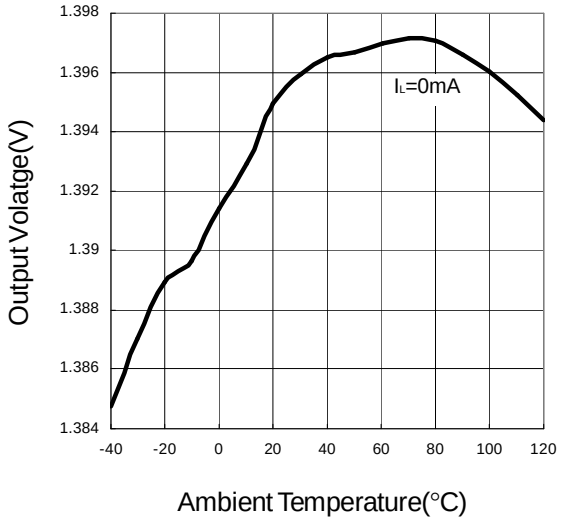
Time(0.1ms/div)

Application Characteristics (Cont.)

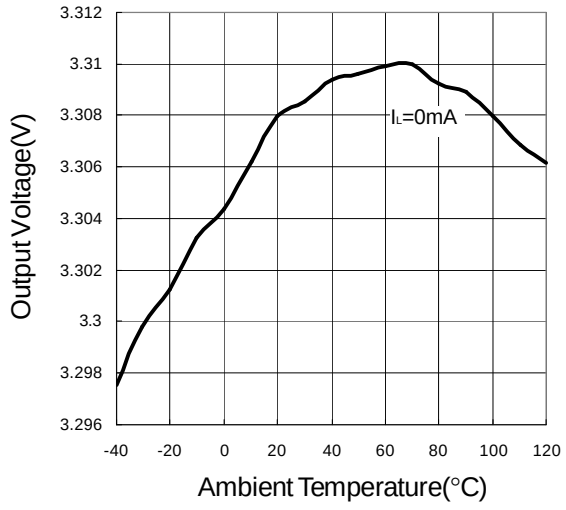
Current Limit vs. Input Voltage



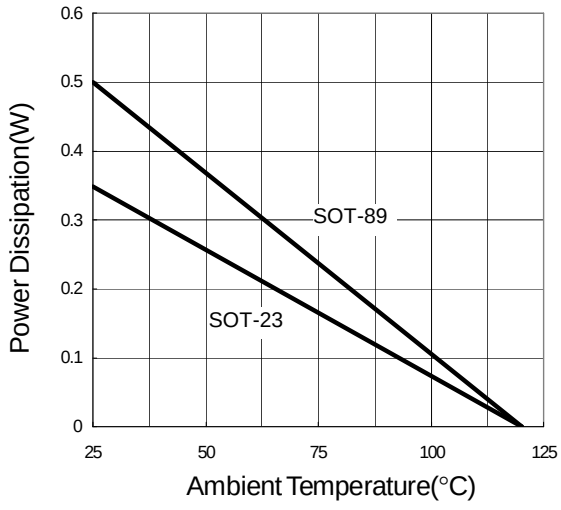
Output Voltage vs. Ambient Temperature



Output Voltage vs. Temperature



Power Dissipation vs. Ambient Temperature



Application Information

Capacitor Selection and Regulation Stability

The APL5101/2 use at least a 1μF capacitor on the input. This capacitor can use Aluminum, Tantalum or Ceramic capacitors. Input capacitor with large value and low ESR provides better PSRR and line transient response. The output capacitor also can use Aluminum, Tantalum or Ceramic capacitor, and its proper values is recommended 1μF, ESR must be above 10mΩ Large output capacitor values can reduce noise and improve load-transient response, stability, and PSRR. With X5R and Y5V dielectrics, 1μF is sufficient at all operating temperatures. The selection of output capacitor is important because it with COUT form a zero to provide the sufficient phase margin.

Input-Output (Dropout) Voltage

The minimum input-output voltage differential (dropout) determines the lowest usable supply voltage. The dropout voltage is a function of drain-to-source on resistance multiplied by the load current.

Current Limit and Short Circuit

APL5101/2 include a current-limit circuitry for this linear regulator. The current limit protection, which sense the current flows the P-channel MOSFET, and controls the output voltage. The point where limiting occurs is I_{OUT}=300mA. When output is shorted to ground, the APL5101/2 will keep short circuit current at 50mA .This design is a method for an indefinite amount of time without damaging to the part.

Thermal Protection

Thermal protection limits total power dissipation in the APL5101/2. When the junction temperature exceeds T_J = +135°C, the thermal sensor generate a logic signal to turn off the pass transistor and let IC to cool.When the IC's junction temperature cools by 20°C, the thermal sensor will turn the pass transistor on again, resulting in a pulsed output during continuous thermal protection. Thermal protection is designed to protect the IC in the event of fault conditions. For continual operation, do not exceed the absolute maximum junction temperature rating of T_J = +140°C.

Operating Region and Power Dissipation

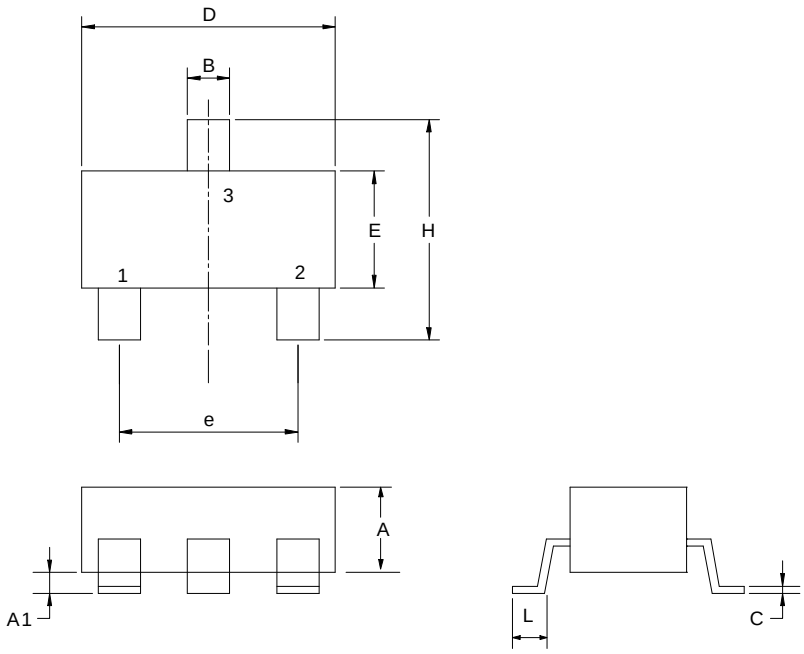
The thermal resistance of the case and circuit board, ambient and junction air temperature, and the rate of air flow all control the APL5101/2's maximum power dissipation. The power dissipation across the device is $P = I_{OUT}(V_{IN}-V_{OUT})$. The maximum power dissipation is:

$$P_{MAX} = (T_J-T_A) / (\theta_{JC} + \theta_{CA})$$

where T_J-T_A is the temperature difference between the junction and ambient air. θ_{JC} is the thermal resistance of the package, θ_{CA} is the thermal resistance through the printed circuit board, copper traces, and other materials to the surrounding air. The GND pin provides an electrical connection to ground and channeling heat away. The printed circuit board (PCB) forms a heat sink and dissipates most of the heat into ambient air.

Packaging Information

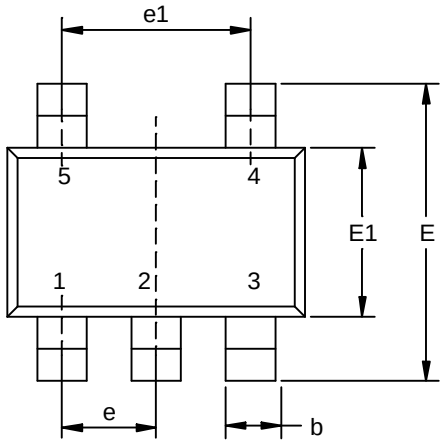
SOT-23

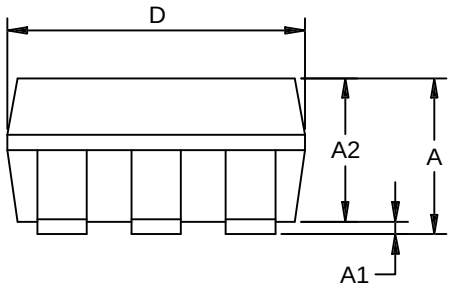


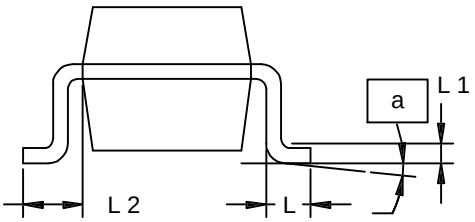
Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.00	1.30	0.039	0.051
A1	0.00	0.10	0.000	0.004
B	0.35	0.51	0.014	0.020
C	0.10	0.25	0.004	0.010
D	2.70	3.10	0.106	0.122
E	1.40	1.80	0.055	0.071
e	1.90/2.1 BSC.		0.075/0.083 BSC.	
H	2.40	3.00	0.094	0.118
L	0.37		0.015	

Packaging Information

SOT-23-5



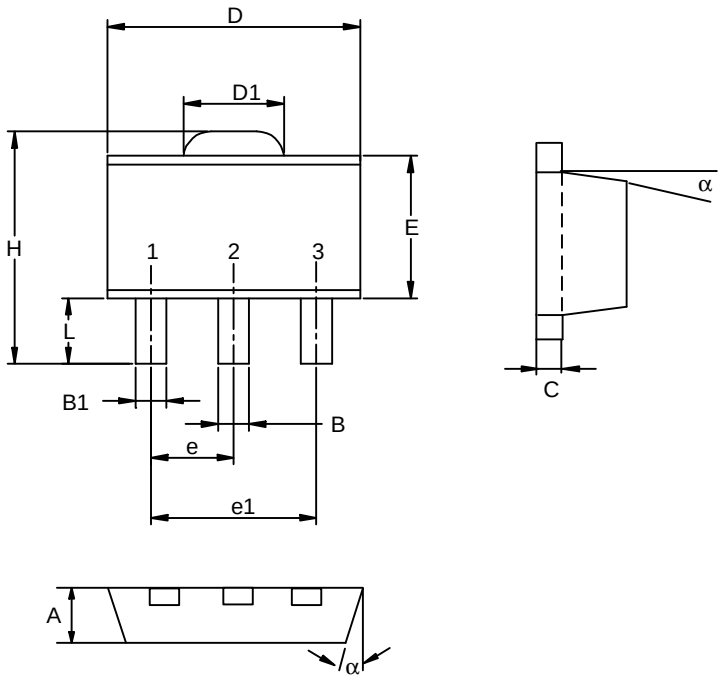




Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	0.95	1.45	0.037	0.057
A1	0.05	0.15	0.002	0.006
A2	0.90	1.30	0.035	0.051
b	0.35	0.55	0.0138	0.0217
D	2.8	3.00	0.110	0.118
E	2.6	3.00	0.102	0.118
E1	1.5	1.70	0.059	0.067
e	0.95		0.037	
e1	1.90		0.075	
L	0.35	0.55	0.014	0.022
L1	0.20 BSC		0.008 BSC	
L2	0.5	0.7	0.020	0.028
a	0°	10°	0°	10°

Packaging Information

SOT-89 (Reference EIAJ ED-7500A Reg stration SC-62)

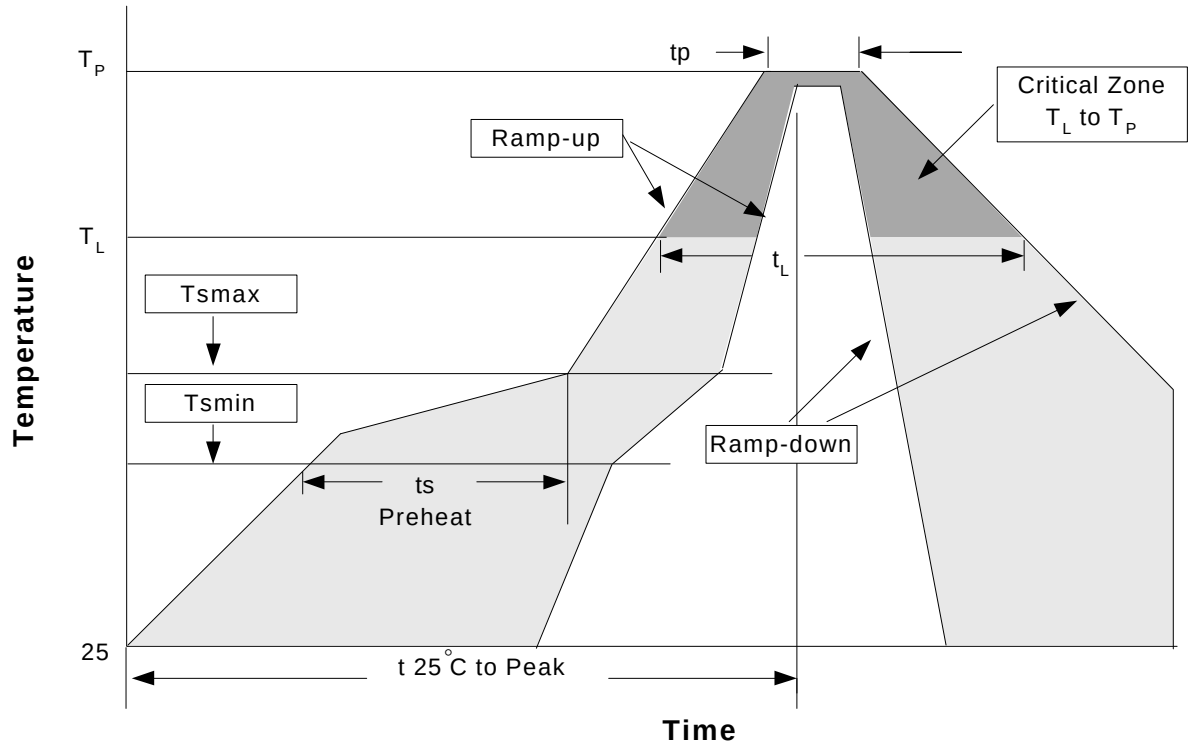


Dim	Millimeters		Inches	
	Min.	Max.	Min.	Max.
A	1.40	1.60	0.055	0.063
B	0.40	0.56	0.016	0.022
B1	0.35	0.48	0.014	0.019
C	0.35	0.44	0.014	0.017
D	4.40	4.60	0.173	0.181
D1	1.35	1.83	0.053	0.072
e	1.50 BSC		0.059 BSC	
e1	3.00 BSC		0.118 BSC	
E	2.29	2.60	0.090	0.102
H	3.75	4.25	0.148	0.167
L	0.80	1.20	0.031	0.047
α		10°		10°

Physical Specifications

Terminal Material	Solder-Plated Copper (Solder Material : 90/10 or 63/37 SnPb), 100%Sn
Lead Solderability	Meets EIA Specification RSI86-91, ANSI/J-STD-002 Category 3.

Reflow Condition (IR/Convection or VPR Reflow)



Classification Reflow Profiles

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average ramp-up rate (T_L to T_P)	3°C/second max.	3°C/second max.
Preheat - Temperature Min (Tsmin) - Temperature Max (Tsmax) - Time (min to max) (ts)	100°C 150°C 60-120 seconds	150°C 200°C 60-180 seconds
Time maintained above: - Temperature (T_L) - Time (t_L)	183°C 60-150 seconds	217°C 60-150 seconds
Peak/Classificatioon Temperature (Tp)	See table 1	See table 2
Time within 5°C of actual Peak Temperature (tp)	10-30 seconds	20-40 seconds
Ramp-down Rate	6°C/second max.	6°C/second max.
Time 25°C to Peak Temperature	6 minutes max.	8 minutes max.

Notes: All temperatures refer to topside of the package .Measured on the body surface.

Classification Reflow Profiles (Cont.)

Table 1. SnPb Entectic Process – Package Peak Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 ³350
<2.5 mm	240 +0/-5°C	225 +0/-5°C
≥2.5 mm	225 +0/-5°C	225 +0/-5°C

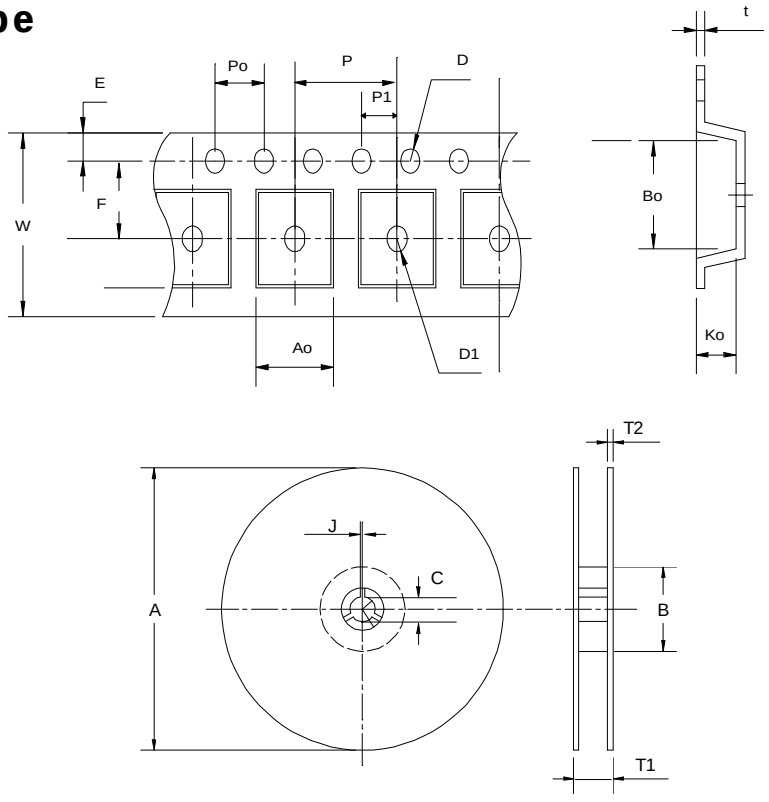
Table 2. Pb-free Process – Package Classification Reflow Temperatures

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 +0°C*	260 +0°C*	260 +0°C*
1.6 mm – 2.5 mm	260 +0°C*	250 +0°C*	245 +0°C*
≥2.5 mm	250 +0°C*	245 +0°C*	245 +0°C*
*Tolerance: The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature (this means Peak reflow temperature +0°C. For example 260°C+0°C) at the rated MSL level.			

Reliability test program

Test item	Method	Description
SOLDERABILITY	MIL-STD-883D-2003	245°C , 5 SEC
HOLT	MIL-STD-883D-1005.7	1000 Hrs Bias @ 125 °C
PCT	JESD-22-B, A102	168 Hrs, 100 % RH , 121°C
TST	MIL-STD-883D-1011.9	-65°C ~ 150°C, 200 Cycles
ESD	MIL-STD-883D-3015.7	VHBM > 2KV, VMM > 200V
Latch-Up	JESD 78	10ms , I_{tr} > 100mA

Carrier Tape



Cover Tape Dimensions

Application	A	B	C	J	T1	T2	W	P	E
SOT-23	178±1	60 ± 1.0	12.0	2.5 ± 0.15	9.0 ± 0.5	1.4	8.0+ 0.3 - 0.3	4.0	1.75
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	3.5 ± 0.05	1.5 +0.1	ϕ0.1MIN	4.0	2.0 ± 0.05	3.1	3.0	1.3	0.2±0.03
Application	A	B	C	J	T1	T2	W	P	E
SOT-23-5	178 ±1	72 ± 1.0	13.0 + 0.2	2.5 ± 0.15	8.4 ± 2	1.5 ± 0.3	8.0 ± 0.3	4 ± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	3.5 ± 0.05	1.5± 0.1	1.5± 0.1	4.0 ± 0.1	2.0 ± 0.1	3.15 ± 0.1	3.2± 0.1	1.4± 0.1	0.2±0.033
Application	A	B	C	J	T1	T2	W	P	E
SOT-89	178 ±1	70 ± 2	13.5 ± 0.15	3 ± 0.15	14 ± 2	1.3 ± 0.3	12 + 0.3 12 - 0.1	8 ± 0.1	1.75± 0.1
	F	D	D1	Po	P1	Ao	Bo	Ko	t
	5.5 ± 0.05	1.5± 0.1	1.5± 0.1	4.0 ± 0.1	2.0 ± 0.1	4.8 ± 0.1	4.5± 0.1	1.80± 0.1	0.3±0.013

(mm)

Cover Tape Dimensions

Application	Carrier Width	Cover Tape Width	Devices Per Reel
SOT- 23	8	5.3	3000
SOT- 23-5	8	5.3	3000
SOT- 89	12	9.3	1000

Customer Service

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