

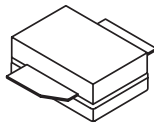


# AGR09045E

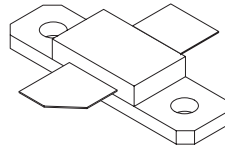
## 45 W, 865 MHz—895 MHz, N-Channel E-Mode, Lateral MOSFET

### Introduction

The AGR09045E is a high-voltage, gold-metalized, laterally diffused metal oxide semiconductor (LDMOS) RF power transistor suitable for cellular band, code-division multiple access (CDMA), global system for mobile communication (GSM), enhanced data for global evolution (EDGE), and time-division multiple access (TDMA) single and multicarrier class AB wireless base station amplifier applications. This device is manufactured on an advanced LDMOS technology, offering state-of-the-art performance, reliability, and thermal resistance. Packaged in an industry-standard CuW package capable of delivering a minimum output power of 45 W, it is ideally suited for today's RF power amplifier applications.



AGR09045EU (unflanged)



AGR09045EF (flanged)

Figure 1. Available Packages

### Features

- Typical performance ratings are for IS-95 CDMA, pilot, sync, paging, traffic codes 8—13:
  - Output power (POUT): 10 W.
  - Power gain: 20 dB.
  - Efficiency: 28%.
  - Adjacent channel power ratio (ACPR) for 30 kHz bandwidth (BW):
    - (750 kHz offset: -45 dBc)
    - (1.98 MHz offset: -60 dBc).
  - Input return loss: 10 dB.
- High-reliability, gold-metalization process.
- High gain, efficiency, and linearity.
- Integrated ESD protection.
- Si LDMOS.
- Industry-standard packages.
- 45 W minimum output power.

Table 1. Thermal Characteristics

Parameter	Sym	Value	Unit
Thermal Resistance, Junction to Case:			
AGR09045EU	R <sub>JC</sub>	1.2	°C/W
AGR09045EF	R <sub>JC</sub>	1.5	°C/W

Table 2. Absolute Maximum Ratings\*

Parameter	Sym	Value	Unit
Drain-source Voltage	V <sub>DSS</sub>	65	Vdc
Gate-source Voltage	V <sub>GS</sub>	-0.5, +15	Vdc
Drain Current—Continuous	I <sub>D</sub>	4.25	Adc
Total Dissipation at T <sub>c</sub> = 25 °C:			
AGR09045EU	P <sub>D</sub>	146	W
AGR09045EF	P <sub>D</sub>	117	W
Derate Above 25 °C:			
AGR09045EU	—	0.83	W/°C
AGR09045EF	—	0.67	W/°C
Operating Junction Temperature	T <sub>J</sub>	200	°C
Storage Temperature Range	T <sub>STG</sub>	-65, +150	°C

\* Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 3. ESD Rating\*

AGR09045E	Minimum (V)	Class
HBM	500	1B
MM	50	A
CDM	1500	4

\* Although electrostatic discharge (ESD) protection circuitry has been designed into this device, proper precautions must be taken to avoid exposure to ESD and electrical overstress (EOS) during all handling, assembly, and test operations. Agere employs a human-body model (HBM), a machine model (MM), and a charged-device model (CDM) qualification requirement in order to determine ESD-susceptibility limits and protection design evaluation. ESD voltage thresholds are dependent on the circuit parameters used in each of the models, as defined by JEDEC's JESD22-A114B (HBM), JESD22-A115A (MM), and JESD22-C101A (CDM) standards.

**Caution: MOS devices are susceptible to damage from electrostatic charge. Reasonable precautions in handling and packaging MOS devices should be observed.**

**AGR09045E**  
**45 W, 865 MHz—895 MHz, N-Channel E-Mode, Lateral MOSFET**

**Electrical Characteristics**

Recommended operating conditions apply unless otherwise specified: Tc = 30 °C.

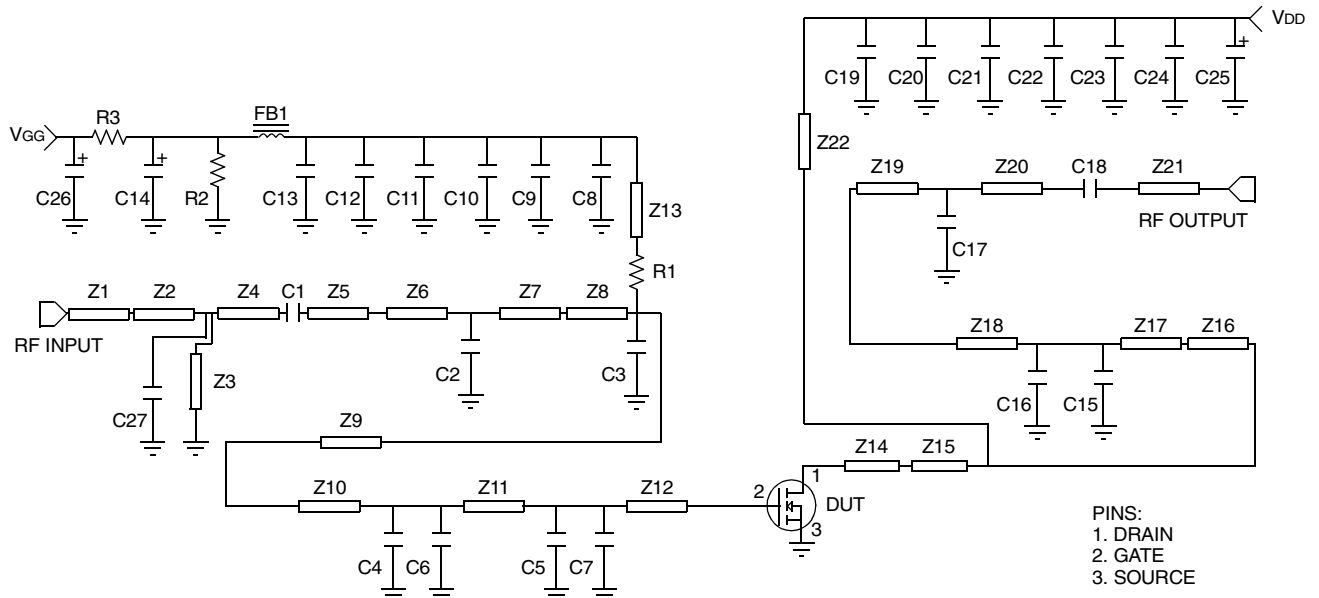
**Table 4. dc Characteristics**

Parameter	Symbol	Min	Typ	Max	Unit
<b>Off Characteristics</b>					
Drain-source Breakdown Voltage (VGS = 0, ID = 100 μA)	V(BR)DSS	65	—	—	Vdc
Gate-source Leakage Current (VGS = 5 V, VDS = 0 V)	IGSS	—	—	1.3	μAdc
Zero Gate Voltage Drain Leakage Current (VDS = 28 V, VGS = 0 V)	IDSS	—	—	4	μAdc
<b>On Characteristics</b>					
Forward Transconductance (VDS = 10 V, ID = 1.0 A)	GFS	—	3	—	S
Gate Threshold Voltage (VDS = 10 V, ID = 400 μA)	VGS(TH)	—	—	4.8	Vdc
Gate Quiescent Voltage (VDS = 28 V, IDQ = 450 mA)	VGS(Q)	—	3.5	—	Vdc
Drain-source On-voltage (VGS = 10 V, ID = 1.0 A)	VDS(ON)	—	0.25	—	Vdc

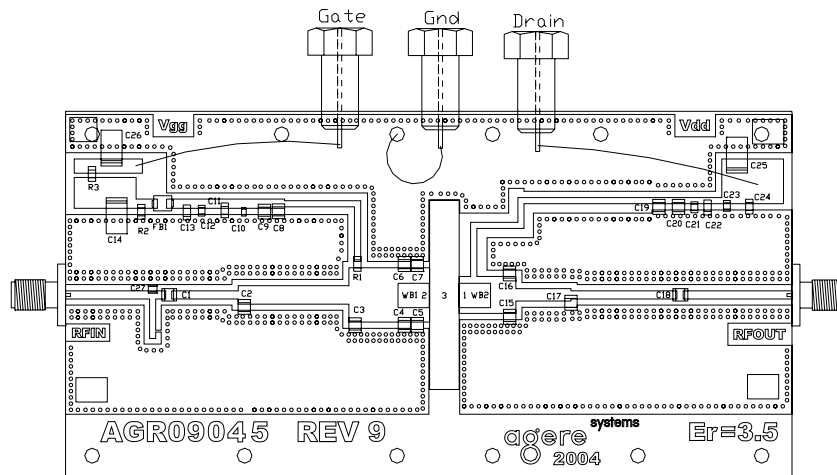
**Table 5. RF Characteristics**

Parameter	Symbol	Min	Typ	Max	Unit
<b>Dynamic Characteristics</b>					
Input Capacitance (VDS = 28 Vdc, VGS = 0, f = 1 MHz)	Ciss	—	73	—	pF
Output Capacitance (VDS = 28 Vdc, VGS = 0, f = 1 MHz)	Coss	—	23	—	pF
Reverse Transfer Capacitance (VDS = 28 Vdc, VGS = 0, f = 1 MHz)	CRSS	—	1.2	—	pF
<b>Functional Tests (in Agere Systems Supplied Test Fixture)</b> (Test frequencies (f) = 865 MHz, 880 MHz, 895 MHz)					
Linear Power Gain (VDS = 28 V, POUT = 6 W, IDQ = 450 mA)	GL	19	20	—	dB
Output Power (VDS = 28 V, 1 dB compression, IDQ = 450 mA)	P1dB	45	60	—	W
Drain Efficiency (VDS = 28 V, POUT = P1dB, IDQ = 450 mA)		—	59	—	%
Third-order Intermodulation Distortion (100 kHz spacing, VDS = 28 V, POUT = 45 WPEP, IDQ = 450 mA)	IMD	—	-31	—	dBc
Input Return Loss	IRL	—	10	—	dB
Ruggedness (VDS = 28 V, POUT = 45 W, IDQ = 450 mA, f = 880 MHz, VSWR = 10:1, all angles)	—	No degradation in output power.			

**Test Circuit Illustrations for AGR09045E**



**A. Schematic**



**Parts List:**

Microstrip line: Z1 0.670 in. x 0.066 in.; Z2 0.035 in. x 0.066 in.; Z3 0.297 in. x 0.050 in.; Z4 0.069 in. x 0.066 in.; Z5 0.538 in. x 0.066 in.; Z6 0.050 in. x 0.150 in.; Z7 0.797 in. x 0.150 in.; Z8 0.050 in. x 0.440 in.; Z9 0.299 in. x 0.440 in.; Z10 0.050 in. x 0.440 in.; Z11 0.050 in. x 0.440 in.; Z12 0.494 in. x 0.440 in.; Z13 1.024 in. x 0.050 in.; Z14 0.093 in. x 0.300 in.; Z15 0.050 in. x 0.300 in.; Z16 0.214 in. x 0.300 in.; Z17 0.050 in. x 0.300 in.; Z18 0.396 in. x 0.300 in.; Z19 0.050 x 0.300; Z20 0.808 in. x 0.066 in.; Z21 0.881 in. x 0.066 in.; Z22 2.048 in. x 0.050 in.

ATC<sup>®</sup> chip capacitor: C1, C8, C18, C19: 47 pF, 100B470JW; C2: 3.3 pF, 100B3R3BW; C3: 5.6 pF, 100B5R6BW;  
 C4, C5, C6, C7: 12 pF, 100B120JW; C9, C16, C20: 10 pF, 100B100JW; C15: 1.8 pF, 100B1R8BW; C17: 6.8 pF, 100B6R8BW;  
 C27: 8.2 pF, 100A8R2BW.

1206 size 0.25 W, fixed film, chip resistors: R1: 50  $\Omega$ , RM73B2B500J; R2: 43 k  $\Omega$ , RM73B2B433J; R3: 1 k  $\Omega$ , RM73B2B103J.

Murata<sup>®</sup> chip capacitor: C12, C23: 0.01  $\mu$ F, GRM40X7R103K100AL.

0603 chip capacitor: C10, C21: 220 pF.

Sprague<sup>®</sup> tantalum chip capacitor: C14, C25, C26: 22  $\mu$ F, 35 V.

Kreger<sup>®</sup> ferrite bead: FB1 2743D19447.

Kemet<sup>®</sup> chip capacitor: C13, C24: 0.10  $\mu$ F, C1206C104KRAC7800.

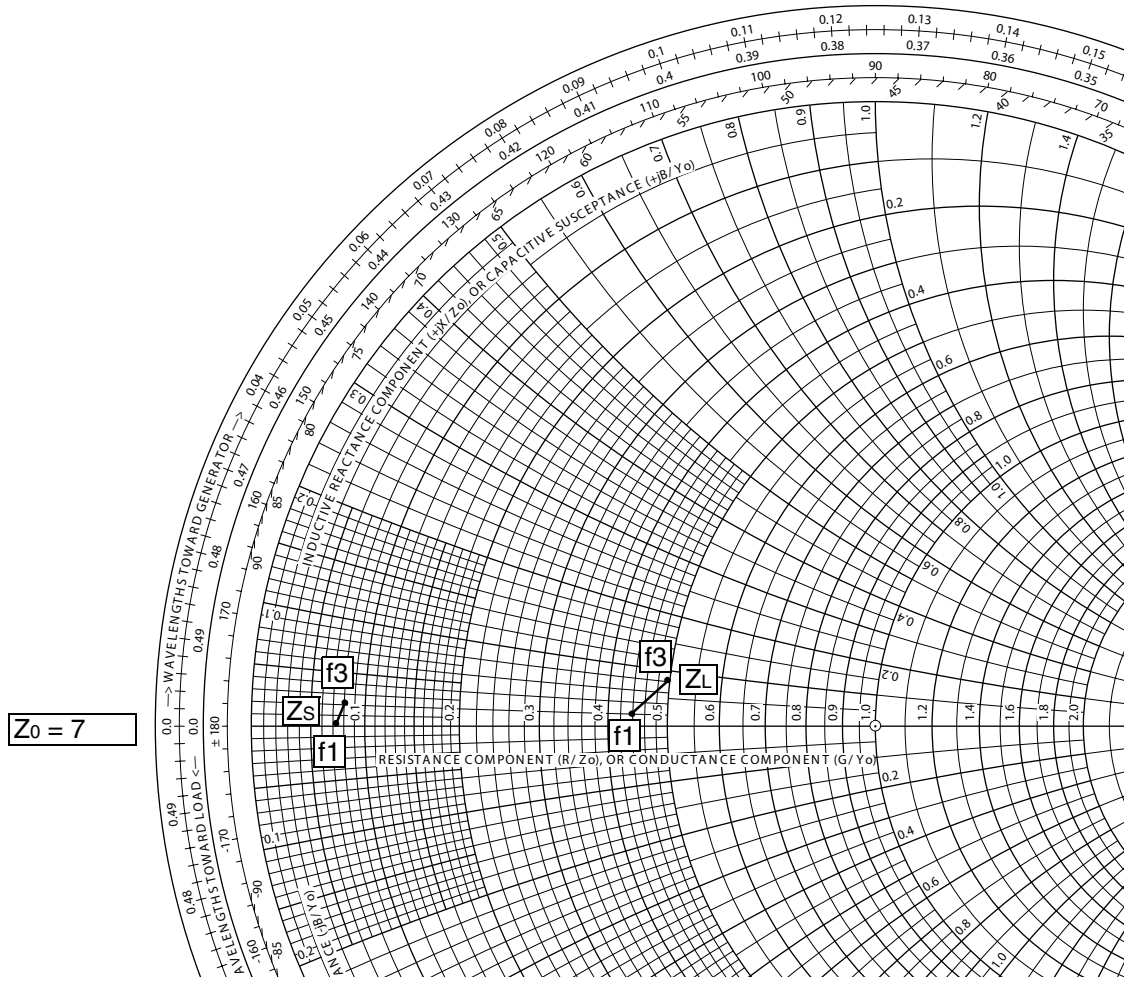
Vitramon<sup>®</sup> chip capacitor: C11, C22: 2200 pF, VJ1206Y222KXA.

Taconic<sup>®</sup> ORCER RF-35: board material, 1 oz. copper, 30 mil thickness,  $r = 3.5$ .

**B. Component Layout**

**Figure 2. AGR09045E Test Circuit**

Typical Performance Characteristics



MHz (f)	Zs (Complex Source Impedance)	ZL (Complex Optimum Load Impedance)
865 (f1)	0.479 + j0.043	3.12 + j0.070
880 (f2)	0.529 + j0.072	3.20 + j0.316
895 (f3)	0.553 + j0.101	3.32 + j0.590

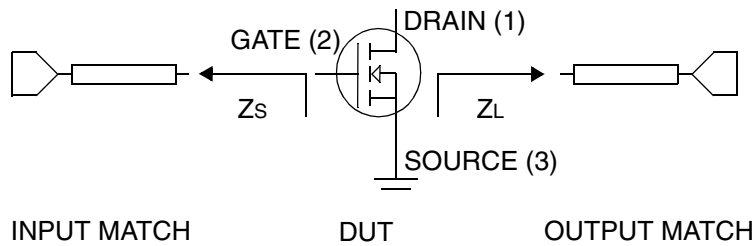


Figure 3. Series Equivalent Input and Output Impedances

Typical Performance Characteristics (continued)

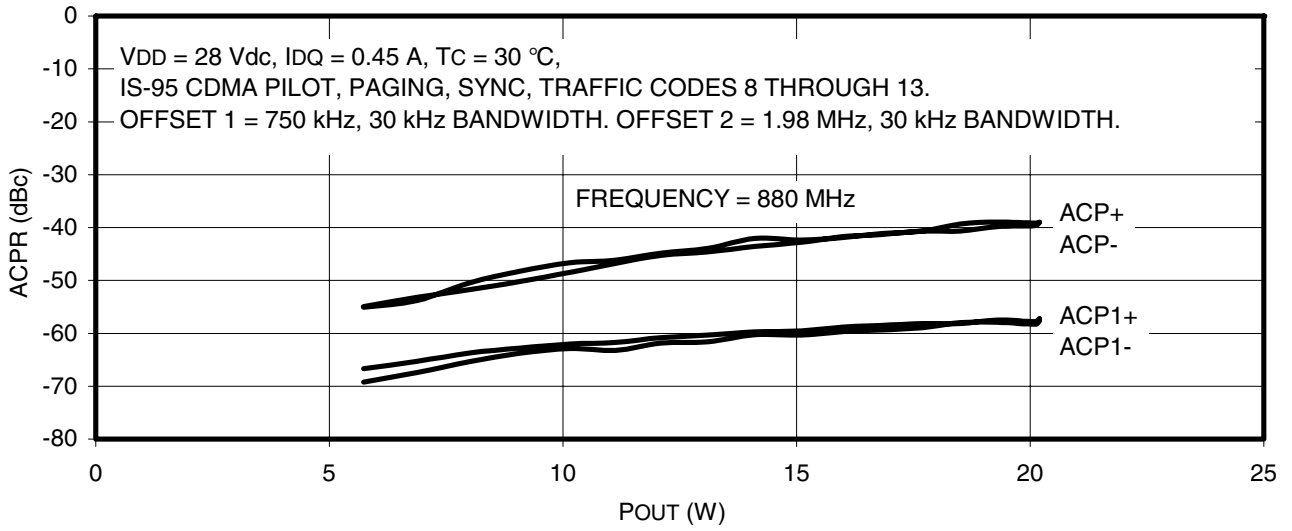


Figure 4. ACPR vs. Pout

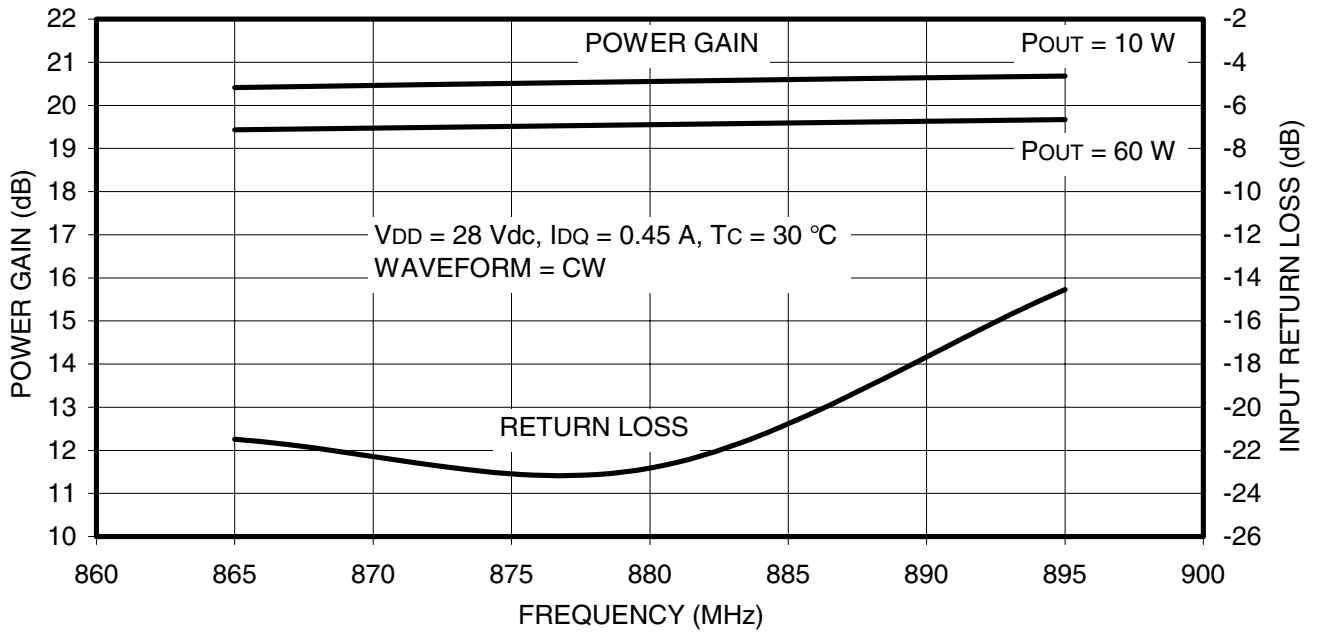


Figure 5. Power Gain and Return Loss vs. Frequency

Typical Performance Characteristics (continued)

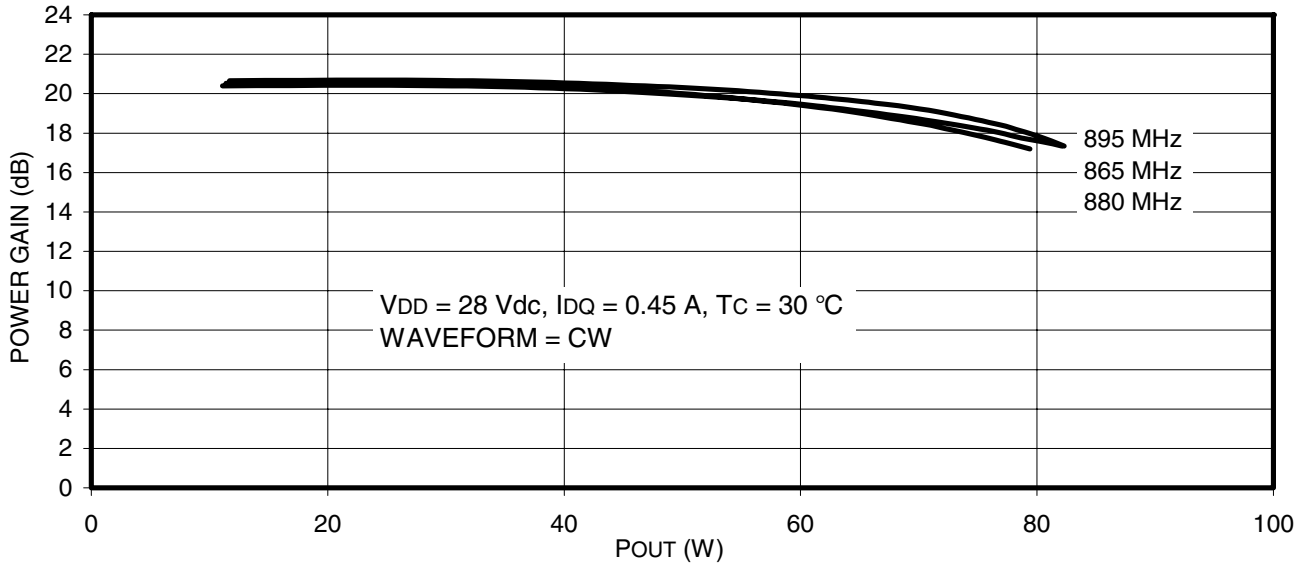


Figure 6. Power Gain vs. Power Out

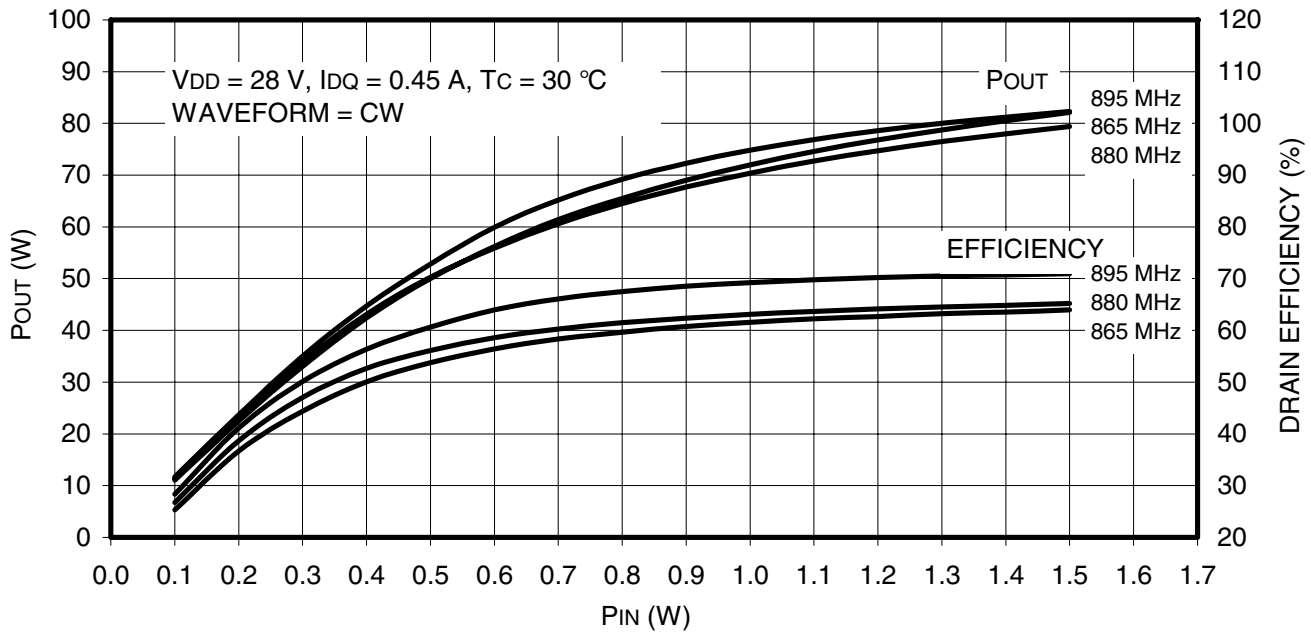
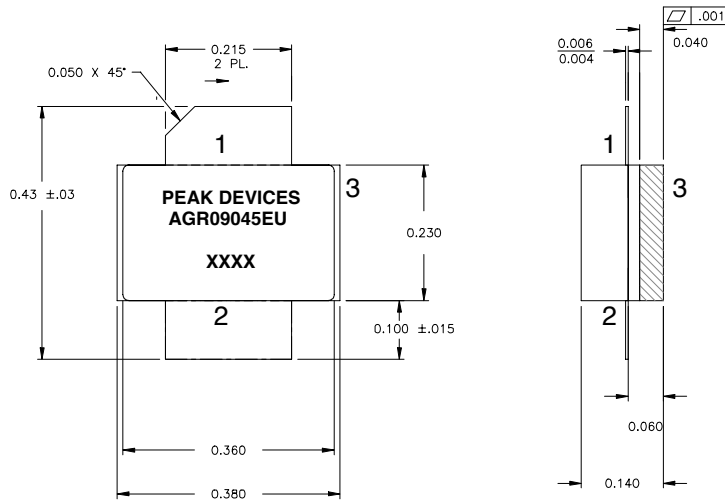


Figure 7. Power Out and Drain Efficiency vs. Input Power

## Package Dimensions

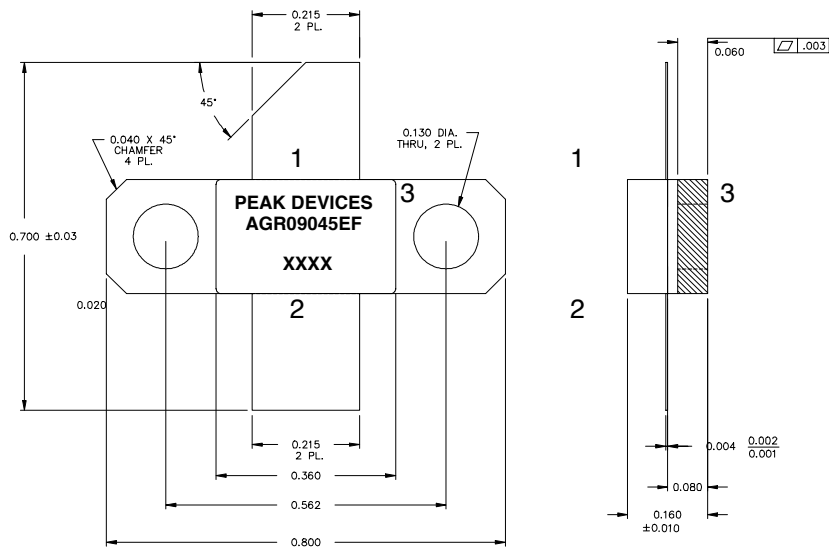
All dimensions are in inches. Tolerances are  $\pm 0.005$  in. unless specified.

### AGR09045EU



PINS:  
 1. DRAIN  
 2. GATE  
 3. SOURCE

### AGR09045EF



PINS:  
 1. DRAIN  
 2. GATE  
 3. SOURCE

XXXX - 4 Digit Trace Code

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**45 W, 865 MHz—895 MHz, N-Channel E-Mode, Lateral MOSFET**

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## **RF Power Product Information**

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