DATA SHEET

凌陽科技
SUNPLUS

SPRC201A/SPRC202A

10 Functions Remote Control Encoder/Decoder Pairs

Preliminary

AUG. 30, 2002

Version 0.1

10-FUNCTIONS REMOTE CONTROL ENCODER/DECODER PAIRS

1. GENERAL DESCRIPTION

These two devices are designed for encoder and decoder as pairs in remote control applications. The SPRC201A is a remote control encoder that encodes 10 lines of binary information into serial bit-stream data. When any of the 10 lines of information is activated, RF will be enabled or an infrared transmission medium will transmit encoded bit-stream data. After the 10 lines of information become inactive, the SPRC201A will transmit additional five data frames to improve transmitting reliability.

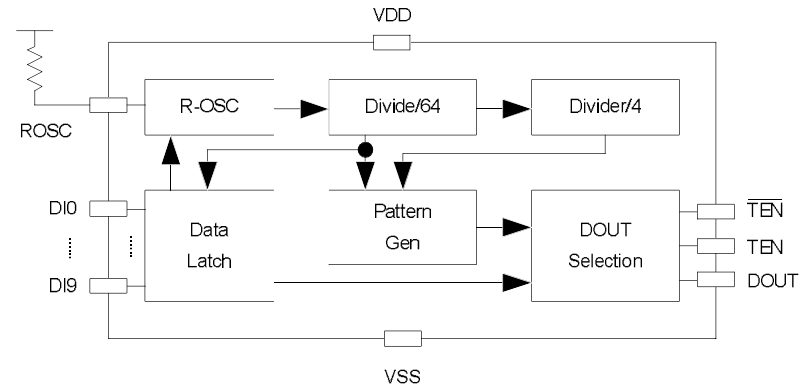
In contrast, the SPRC202A is a remote control decoder, which decodes the received serial bit-stream data from the SPRC201A and interprets 10 lines of information as 10 bits output data to control the corresponding external component. The SPRC202A provides nine types of momentary and one toggle types of outputs. The SPRC202A will be activated only when two consecutive and equal frames are received.

2. FEATURES

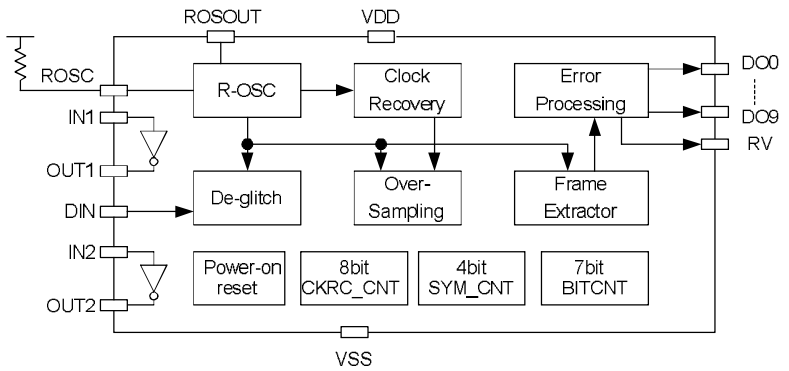
- Operating voltage range: 2.0V - 5.5V
- Built-in R-oscillator (5% accuracy resistor needed).
- Low standby and operating current
  - — $I_{STBY,SPRC201A}$ < 1.0μA, R-oscillator stops
  - — $I_{OPERATE,SPRC201A}$ < 100μA , R-oscillator free run
  - — $I_{OPERATE,SPRC202A}$ < 100μA , R-oscillator free run
- Built-in Power On Reset
- 10 function I/O pins
  - — 9 types of momentary outputs
  - — 1 types of toggle outputs
- Variable frame rate by controlling external resistor
- Valid transmission indicator
- 14/16-pin PDIP package available for SPRC201A
- 16/18/20-pin PDIP package available for SPRC202A

3. BLOCK DIAGRAM

SPRC201A



SPRC202A



4. SIGNAL DESCRIPTIONS

4.1. PIN Description

4.1.1. SPRC201A

Mnemonic	Type	PIN No.	Description
DI0	I	15	10-Function parallel data input
DI1		16	
DI2		2	
DI3		3	
DI4		4	
DI5		5	
DI6		10	
DI7		11	
DI8		13	
DI9		14	
DOUT	O	6	Serial bit stream data output
RESV		17	Reserving pin
TEN	O	8	Transmitting enable output for positive and negative polarity
$\overline{\text{TEN}}$		9	
ROSC	I	12	R-oscillator input, connected to VDD through a resistor.
VDD	P	7	Power supply voltage input
VSS	P	1	Power supply ground input

4.1.2. SPRC202A

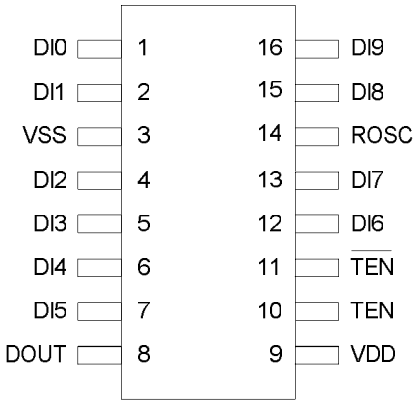
Mnemonic	Type	PIN No.	Description
DO0	I	4	10-Function parallel data output
DO1		5	
DO2		6	
DO3		8	
DO4		10	
DO5		11	
DO6		12	
DO7		13	
DO8		16	
DO9		17	
DIN	I	1	Serial bit-stream data input
RV	O	7	Receive valid indication output
ROSC	I	2	R-oscillator input, connect to VDD through a resistor.
ROSCOUT	O	3	R-oscillator clock output
IN1	I	14	Inverter input pins
IN2	I	18	
OUT1	O	15	Inverter output pins
OUT2	O	19	
VDD	P	9	Power supply voltage input
VSS	P	20	Power supply ground input

Legend: I = Input, O = Output, P = Power

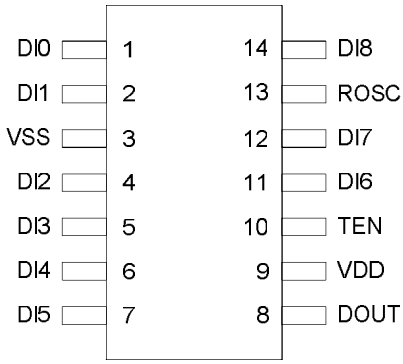
4.2. PIN Configuration

4.2.1. SPRC201A

1). SPRC201A - PDIP 16

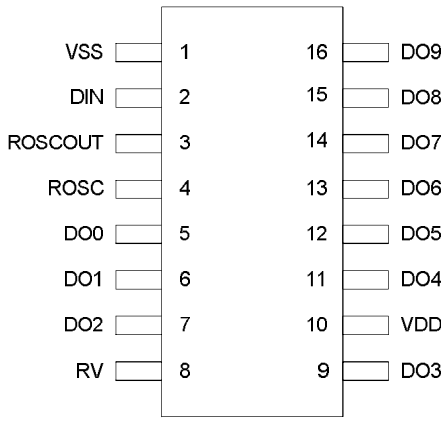


2). SPRC201A - PDIP 14



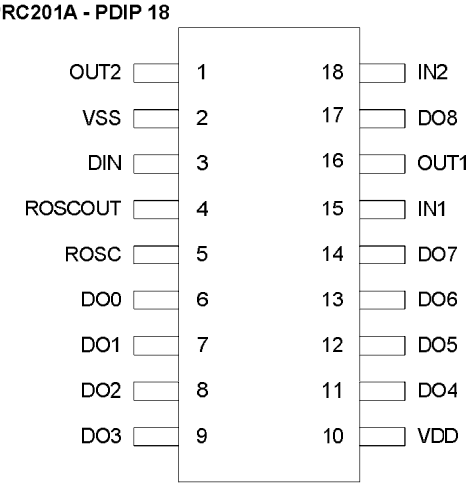
4.2.2. SPRC202A

1). SPRC202A - PDIP 16

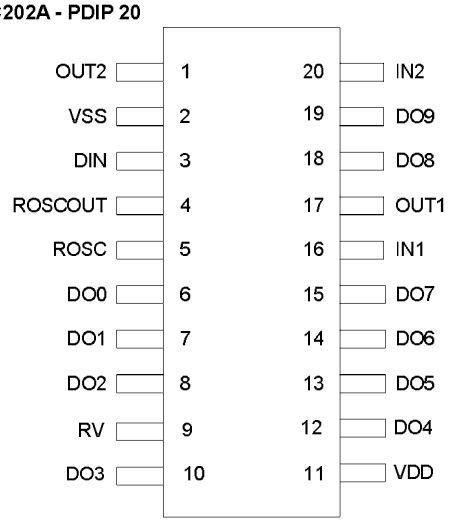


4.2.3. SPRC202A (with Super Regeneration Amplifier)

1). SPRC201A - PDIP 18



2). SPRC202A - PDIP 20



5. FUNCTIONAL DESCRIPTIONS

5.1. Frame Format

Preamble						PO	E	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9
P	P	P	P	P	P	A/I	A/I	A/I	A/I	A/I	A/I	A/I	A/I	A/I	A/I	A/I	A/I

Preamble field: 6 preamble fields

PO field: Even parity check field

E field: Frame polarity indication field, frame are transmitted in positive/negative order

Data field: 10 data fields

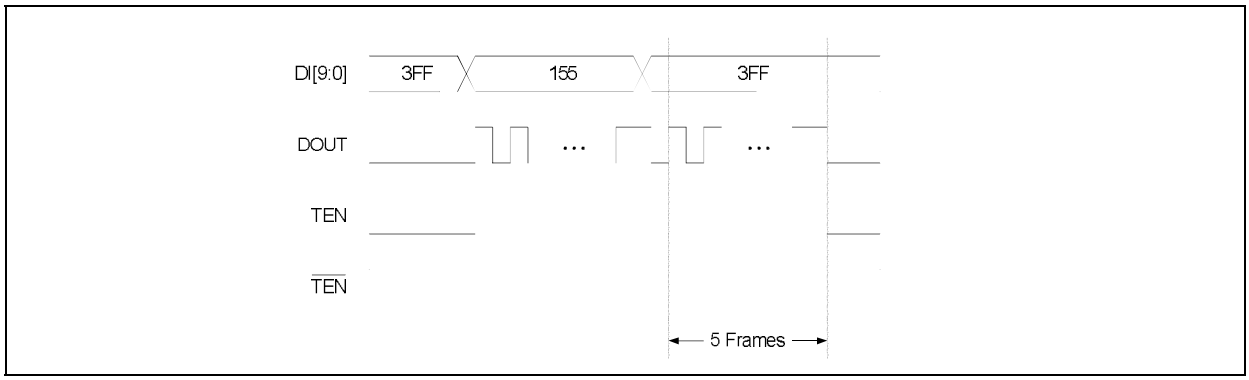
P pattern: encoded as 101

A pattern: encoded as 100

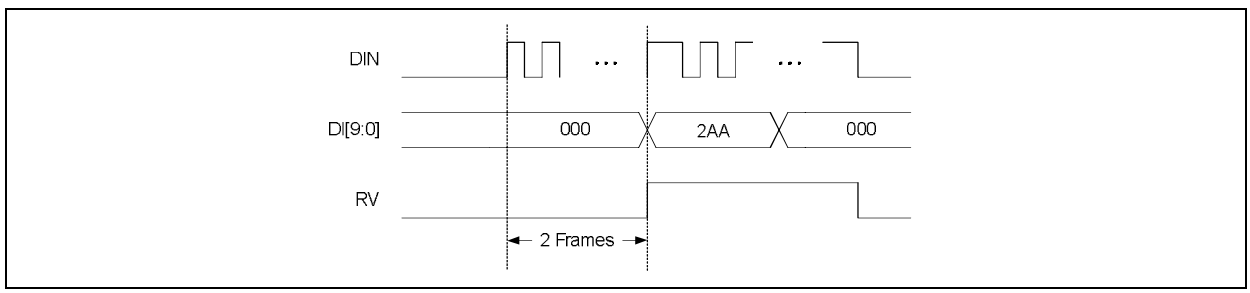
I pattern: encoded as 110

5.2. Operation

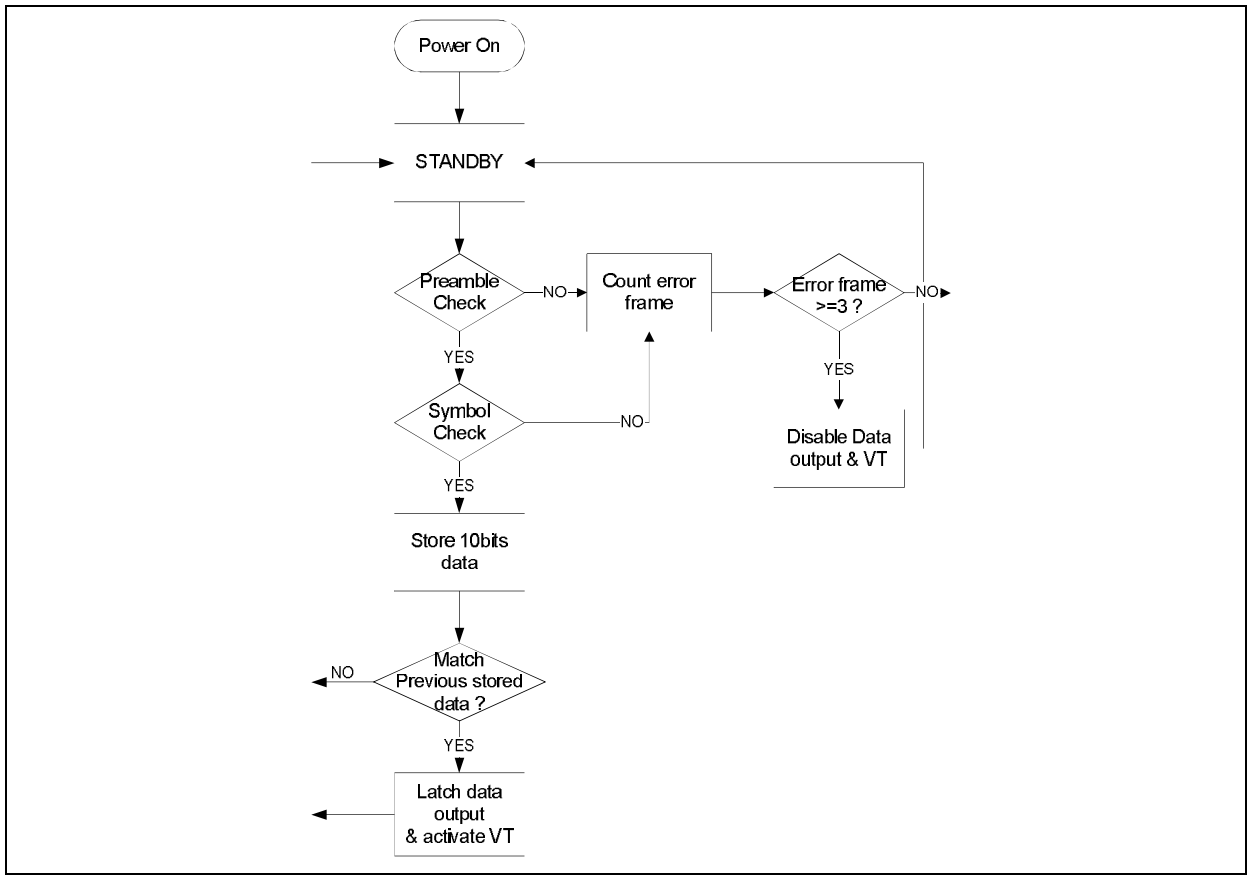
The SPRC201A encodes 10 function information into 2^{10} series of bit-stream data and asserts TEN or $\overline{\text{TEN}}$ to enable RF or Infrared transmission media when any of the 10 function I/Os is active. Same procedures will be repeated until all 10 I/Os become inactive. After these 10 I/Os become inactive, SPRC201A will transmit another five all-zero frames to inform SPRC202A turning back to disabled state. The transmitting timing is shown below:



The SPRC202A receives serial bit-stream data (transmitted from SPRC201A) and decodes the data fields to a 10-bit data output. Any signal on DIN pin will activate SPRC202A to decode the incoming data. When SPRC202A receives two consecutive, correct and equal frames, RV will be set to high to indicate a successful valid transmission, and DO [9:0] is activated to control the external component. The receiving timing is shown as follows:



5.3. Decoder Flow Chart



After Power on, the flow chart is reset at STANDBY state. When the signal on DIN is received, the SPRC202A will check the incoming data frame structure. If preamble or data field errors occur, the flow chart will go back to STANDBY state to check the next frames. If the receiving frame structures pass the preamble and symbol check, the 10-bits data is stored and compared to the previous stored 10-bits data. If the present data matches the previous one, DO[9:0] and RV are activated and the flow chart is back to STANDBY state to check the next frames.

5.4. R-oscillator

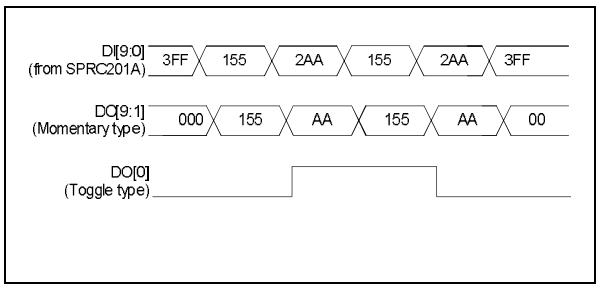
Both SPRC201A and SPRC202A have built-in R-oscillator. Users need only one resistor (or a capacitor if needed) to implement the clock input and to change the frame rate by replacing various resistors.

Frame rate = F_{OSC} / 64 / 54

In addition, the SPRC202A has a clock recovery block to automatically adjust the ratio of data rate to clock rate. To meet the rigorous specification, only 5% accuracy resistor is allowed to be used in SPRC201A and SPRC202A.

5.5. Output Type

The SPRC202A offers up to 10 data output pins. Nine out of ten data outputs are momentary type (DO[9:1]) and the other one are toggle types (DO[0]). The momentary and toggle output timing is given as follows:



5.6. Super Regeneration Amplifier

The SPRC202A also provides two inverter input and output as pins. The two inverters can be used for amplifier of the Super-Regeneration RF receiver data output. User can change the two inverters' gain by adjusting external resistor and capacitor.

6. ELECTRICAL SPECIFICATIONS

6.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to V_+ + 0.5V
Operating Temperature	T_A	-20℃ to +60℃
Storage Temperature	T_{STO}	-50℃ to +150℃

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

6.2. DC Characteristics of SPRC201A (VDD = 3.0V, T_A = 25℃)

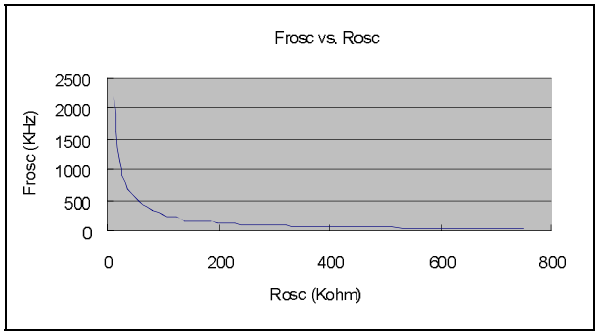
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.0	-	5.5	V	R-OSC resistor = 200KΩ
Operating Current	I_{OP}	-	-	100	μA	R-OSC resistor = 200KΩ
Standby Current	$I_{STBY,SPRC201A}$	-	-	1.0	μA	R-OSC disable
Input High level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High Current (TEN, $\overline{TEN}$, DOUT)	I_{OH}	-	-1.0	-	mA	VDD = 3.0V V_{OH} = 2.4V
Output Sink Current (TEN, $\overline{TEN}$, DOUT)	I_{OL}	-	1.0	-	mA	VDD = 3.0V V_{OL} = 0.4V
DI[9:0] pull high resistor	R_{DI}	-	200	-	KΩ	VDD = 3.0V
OSC Frequency	F_{OSC}	-	128	-	KHz	R_{OSC} = 200KΩ @ VDD from 2.0V - 5.5V

6.3. DC Characteristics of SPRC202A (VDD = 3.0V, T_A = 25℃)

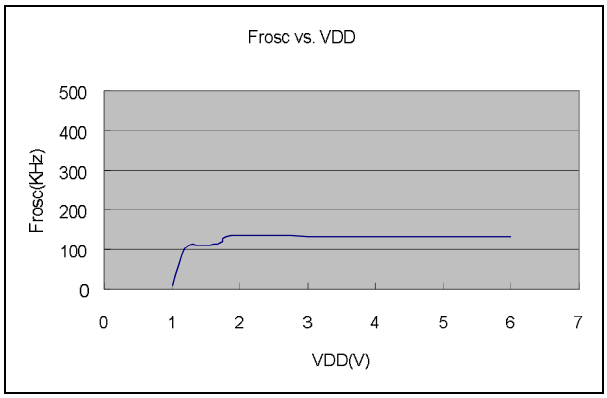
Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	2.0	-	5.5	V	R-OSC resistor = 200KΩ
Operating Current	I_{OP}	-	-	100	μA	R-OSC resistor = 200KΩ
Input High level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output High Current (DO)	I_{OH}	-	-6.0	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink Current (DO)	I_{OL}	-	6.0	-	mA	VDD = 3.0V, V_{OL} = 0.4V
Output High Current (RV)	I_{OH}	-	-1.0	-	mA	VDD = 3.0V, V_{OH} = 2.4V
Output Sink Current (RV)	I_{OL}	-	1.0	-	mA	VDD = 3.0V, V_{OL} = 0.4V
DIN pull low resistor	R_{DIN}	-	200	-	KΩ	VDD = 3.0V
OSC Frequency	F_{OSC}	-	128	-	KHz	R_{OSC} = 200KΩ @ VDD from 2.0V - 5.5V
Maximum tolerance data rate	$F_{TOR,MAX}$	2.4	-	-	KHz	F_{OSC} = 128KHz
Minimum tolerance data rate	$F_{TOR,MIN}$	-	-	1.6	KHz	F_{OSC} = 128KHz
Maximum rejection data rate	$F_{REJ,MAX}$	2.8	-	-	KHz	F_{OSC} = 128KHz
Minimum rejection data rate	$F_{REJ,MIN}$	-	-	1.3	KHz	F_{OSC} = 128KHz

6.4. The Relationships of the R_{OSC} and the F_{OSC}

6.4.1. VDD = 3.0V, T_A = 25℃

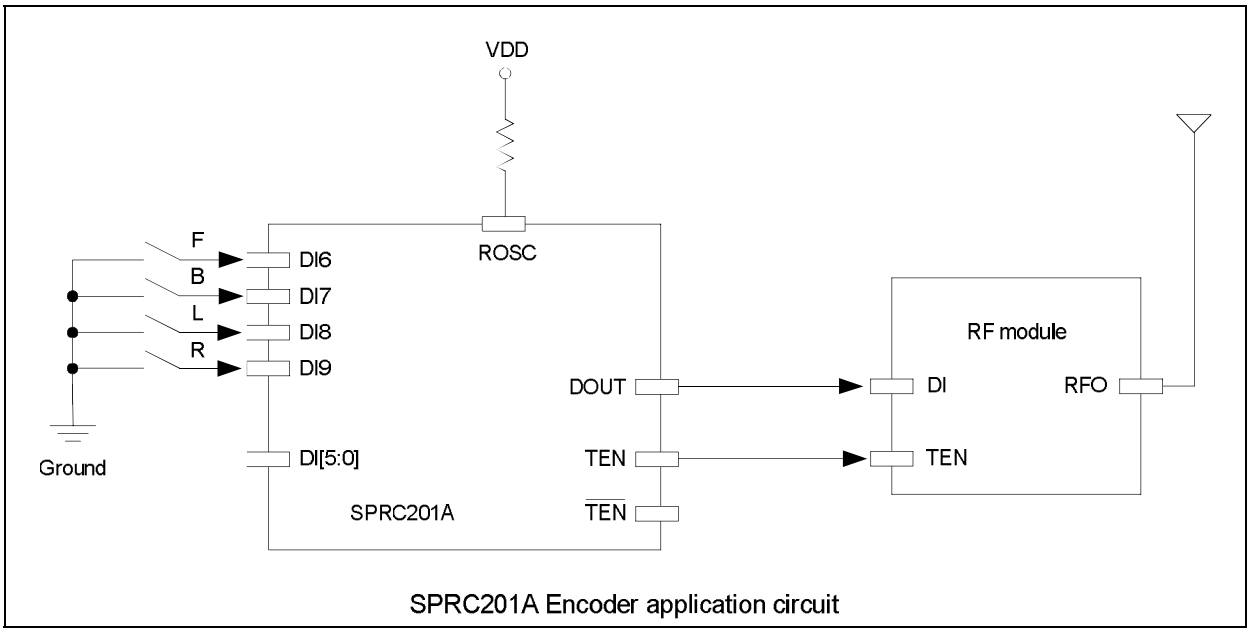


6.5. The Relationships of the VDD and the F_{OSC}



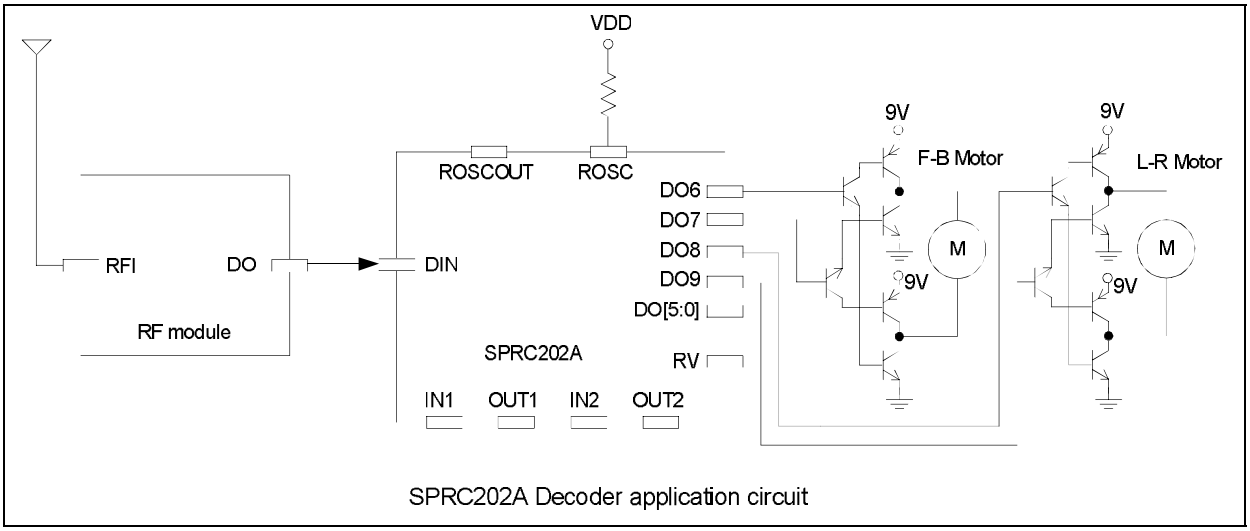
7. APPLICATION CIRCUITS

7.1. SPRC201A Application Circuit



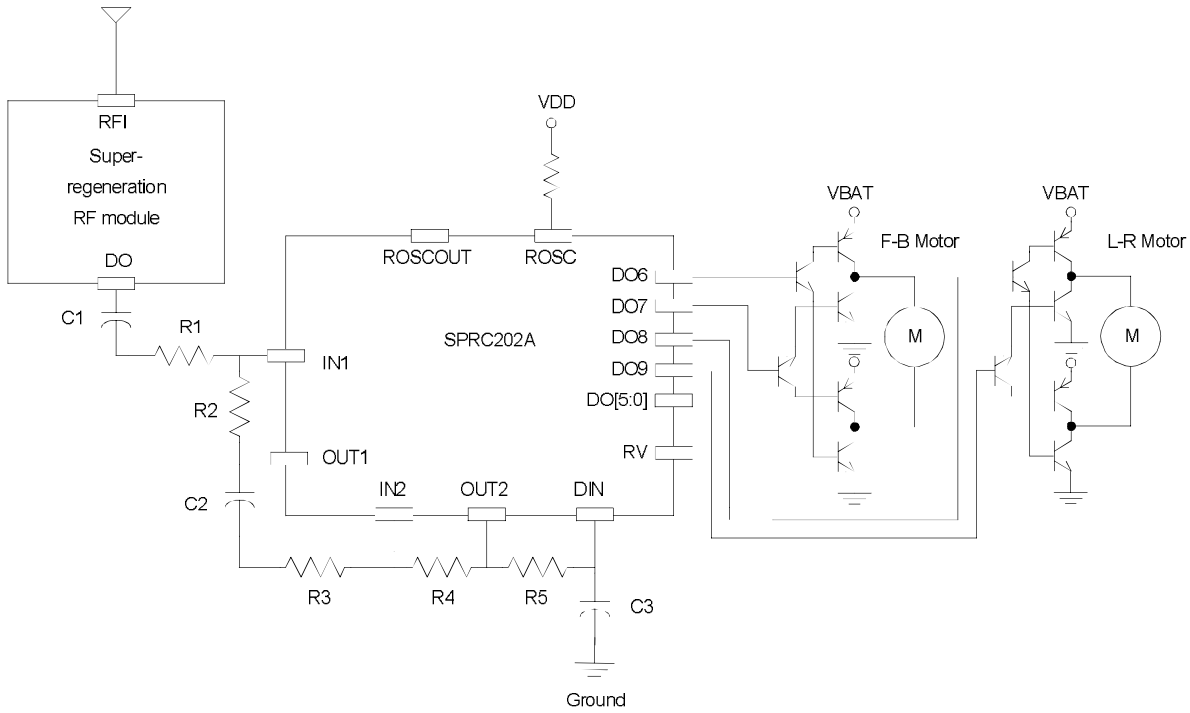
SPRC201A Encoder application circuit

7.2. SPRC202A Application Circuit



SPRC202A Decoder application circuit

7.3. SPRC202A Application Circuit (with Super Regeneration RF)

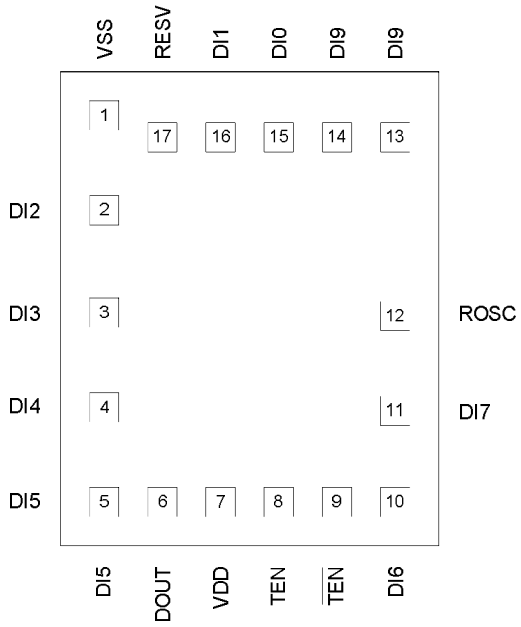


SPRC202A Decoder application circuit

8. PACKAGE/PAD LOCATIONS

8.1. PAD Assignment

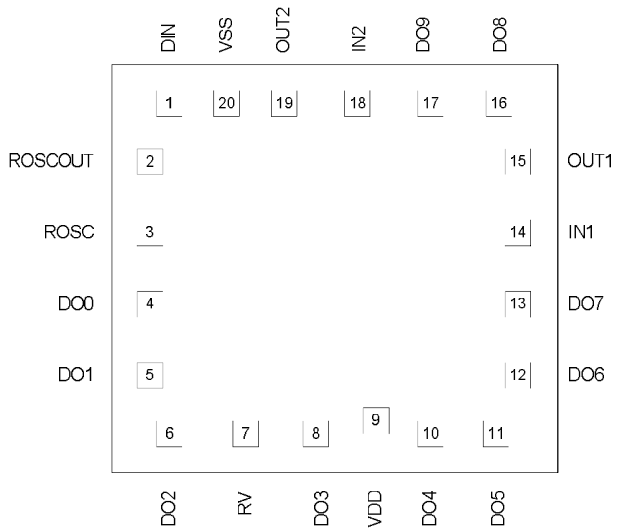
8.1.1. SPRC201A



Chip Size : 890μm × 1130μm

This IC substrate should be connected to VSS

8.1.2. SPRC202A



Chip Size : 1350μm × 1260μm

This IC substrate should be connected to VSS

Note1: Chip size included scribe line.
Note2: To ensure that the IC functions properly, please bond all of VDD and VSS pins.
Note3: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

8.2. Ordering Information

Product Number	Package Type
SPRC201A - C	Chip form
SPRC202A - C	Chip form
SPRC201A - PD02	Package form - PDIP14
SPRC201A - PD03	Package form - PDIP 16
SPRC202A - PD03	Package form - PDIP16
SPRC202A - PD04	Package form - PDIP18
SPRC202A - PD05	Package form - PDIP20

8.3. PAD Locations

8.3.1. SPRC201A

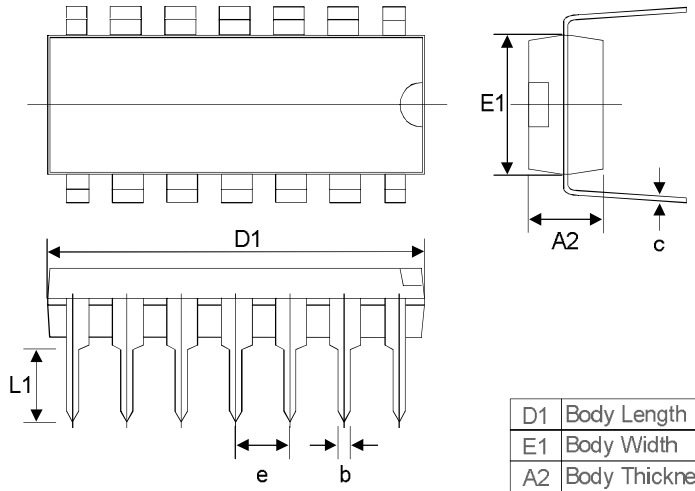
PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	VSS	-314	439	11	DI7	312	-169
2	DI2	-316	270	12	ROSC	312	34
3	DI3	-316	34	13	DI8	319	385
4	DI4	-316	-169	14	DI9	193	385
5	DI5	-316	-404	15	DI0	68	385
6	DOUT	-190	-404	16	DI1	-58	385
7	VDD	-64	-404	17	RESV	-183	385
8	TEN	62	-404				
9	$\overline{\text{TEN}}$	187	-404				
10	DI6	312	-404				

8.3.2. SPRC202A

PAD No.	PAD Name	X	Y	PAD No.	PAD Name	X	Y
1	DIN	-517	495	11	DO5	485	-515
2	ROSCOUT	-563	327	12	DO6	543	-331
3	ROSC	-563	91	13	DO7	543	-128
4	DO0	-563	-111	14	IN1	543	105
5	DO1	-563	-347	15	OUT1	543	308
6	DO2	-518	-515	16	DO8	485	495
7	RV	-282	-515	17	DO9	282	495
8	DO3	-79	-515	18	IN2	49	495
9	VDD	101	-484	19	OUT2	-153	495
10	DO4	282	-515	20	VSS	-335	495

8.4. Package Information

8.4.1. SPRC201A - PDIP 14



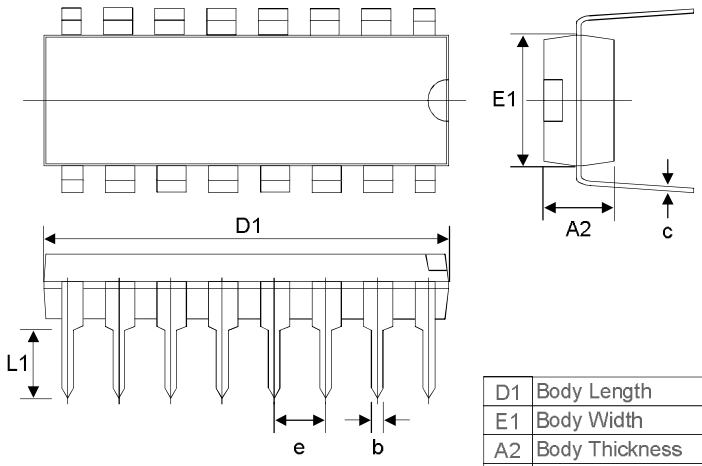
Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
750	250	130	115	18	10	100

All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-14-300

8.4.2. SPRC201A - PDIP 16



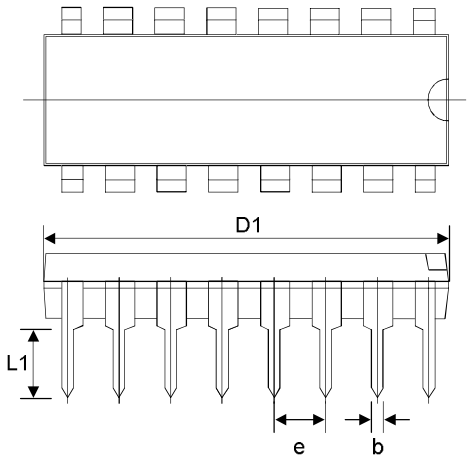
Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
750	250	130	115	18	10	100

All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-16-300

8.4.3. SPRC202A - PDIP 16



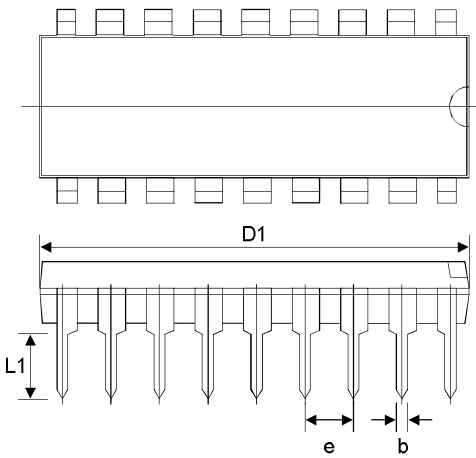
Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
750	250	130	115	18	10	100

All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-16-300

8.4.4. SPRC202A (with super regeneration amplifier) - PDIP 18



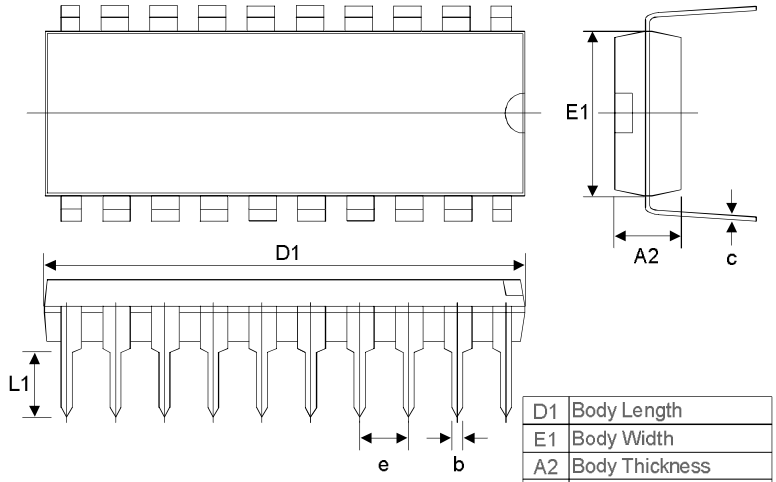
Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
900	250	130	115	18	10	100

All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-18-300

8.4.5. SPRC202A (with super regeneration amplifier) - PDIP 20



Body Size			Lead Size			
D1	E1	A2	L1	b	c	e
1020	250	130	115	18	10	100

All units are in mil. 1mil = 25.4μm

D1	Body Length
E1	Body Width
A2	Body Thickness
L1	Lead Length
b	Lead Width
c	Lead Thickness
e	Lead Pitch

PDIP-20-300

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10. REVISION HISTORY

Date	Revision #	Description	Page
AUG. 30, 2002	0.1	Original	19