S6A0071

32 COM / 60 SEG DRIVER & CONTROLLER FOR STN LCD

Jan. 2002.

Ver. 0.1

Precautions for Light

Light has characteristics to move electrons in the integrated circuitry of semiconductors, therefore may change the characteristics of semiconductor devices when irradiated with light. Consequently, the users of the packages which may expose chips to external light such as COB, COG, TCP and COF must consider effective methods to block out light from reaching the IC on all parts of the surface area, the top, bottom and the sides of the chip. Follow the precautions below when using the products.

1. Consider and verify the protection of penetrating light to the IC at substrate (board or glass) or product design stage.
2. Always test and inspect products under the environment with no penetration of light.

S6A0071 Specification Revision History		
Version	**Content**	**Date**
0.0	Original	Feb.1999
0.1	Modify a pad coordinates value(R/W).	Jan.2002

INTRODUCTION

The S6A0071 is a dot matrix LCD controller & driver LSI which is fabricated by low power CMOS technology. It can display 1 line × 24 characters or 2 line × 24 characters with 5 × 7 dots format.

FEATURES

— Character type dot matrix single chip LCD controller & driver
— Internal driver: 32 common and 60 segment signal output
— Easy interface with 4-bit or 8-bit MPU
— Display character pattern: 5 × 7 dots format (240 kinds)
— The Special character pattern is programmable by character generator RAM directly.
— A customer character pattern is programmable by mask option.
— Various instruction functions
— Built-in automatic power on reset
— Driving method is B-type (frame inversion)

FEATURES

Internal Memory

— Character Generator ROM (CGROM): 8,400 bits (240 characters × 5 × 7 dots)
— Character Generator RAM (CGRAM): 64 × 8 bits (8 characters × 5 × 8 dots)
— Display Data RAM (DDRAM): 80 × 8 bits (80 characters max.)

Low Power Operation

— Power supply voltage range (V_{DD}): 2.4 to 5.5V
— LCD drive voltage range (V_{DD} - V5): 3.0 to 12.0V

Voltage doubler generates about double from signals power supply

On chip generation of LCD supply voltage from voltage doubler (external supply also possible)

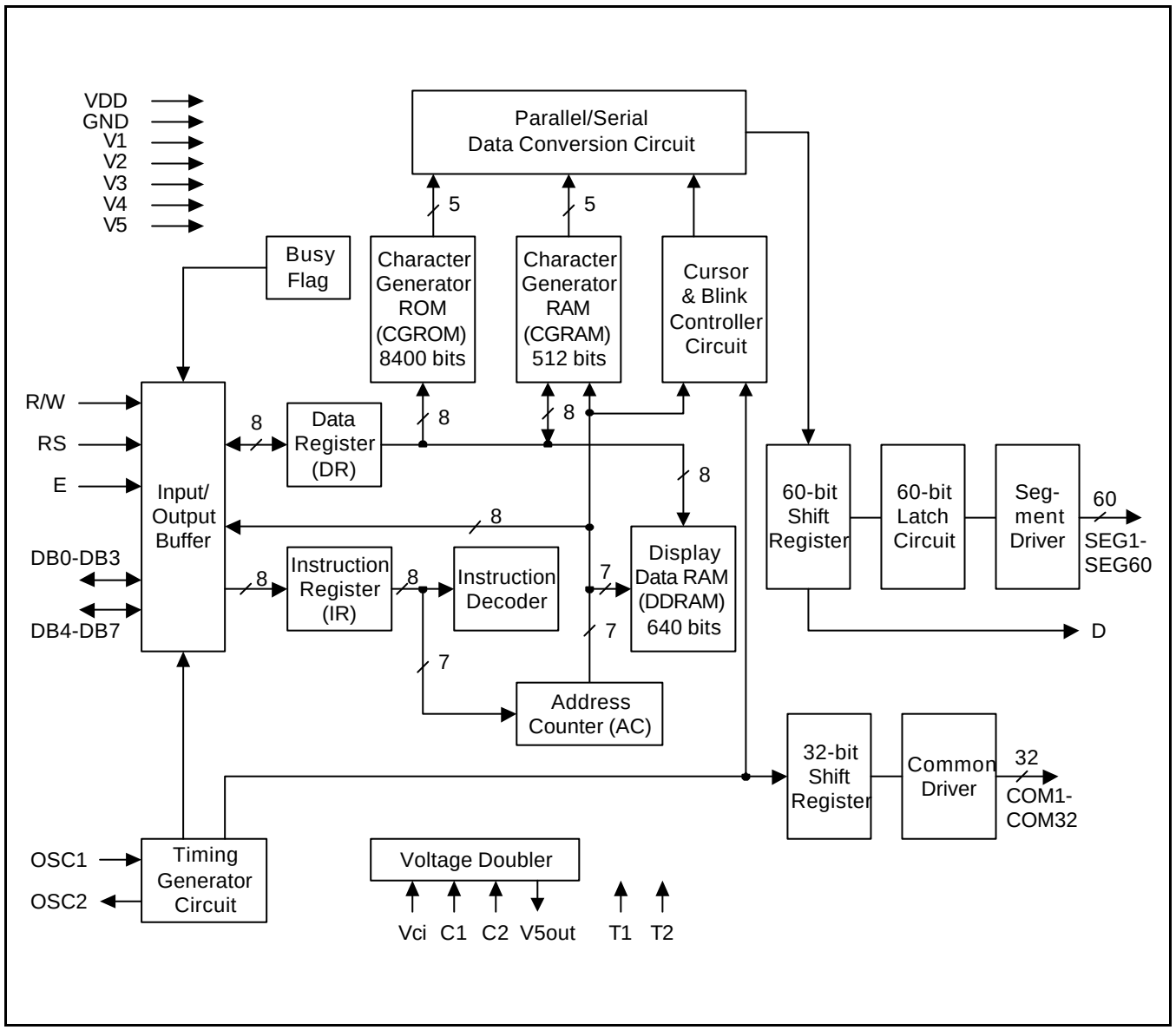
Programmable duty cycle

— 1/16 duty: 1 line × 5 × 7 dots + cursor × 24 characters
— 1/32 duty: 2 lines × 5 × 7 dots + cursor × 24 characters

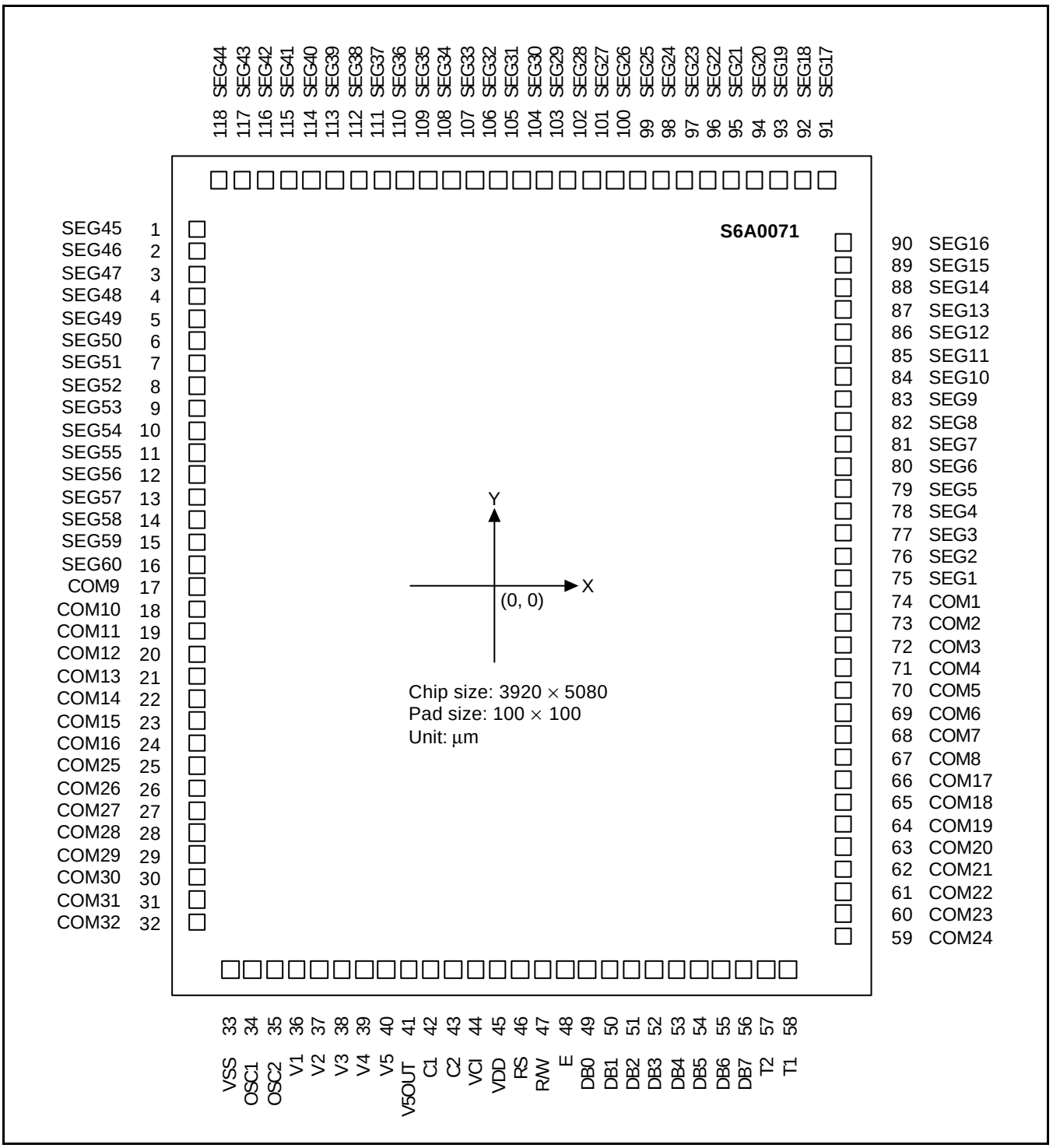
Internal oscillator with an external resistor

118 TCP or bare chip available

BLOCK DIAGRAM



PAD DIAGRAM



NOTE: "S6A0071" marking is to make the PAD No. 95 easy to find.

PAD CENTER COORDINATES

Pad Num.	Pad Name	Coordinate X	Coordinate Y	Pad Num.	Pad Name	Coordinate X	Coordinate Y	Pad Num.	Pad Name	Coordinate X	Coordinate Y
1	SEG45	-1794	2170	41	V5OUT	-562	-2374	81	SEG7	1794	910
2	SEG46	-1794	2030	42	C1	-438	-2374	82	SEG8	1794	1050
3	SEG47	-1794	1890	43	C2	-312	-2374	83	SEG9	1794	1190
4	SEG48	-1794	1750	44	VCI	-188	-2374	84	SEG10	1794	1330
5	SEG49	-1794	1610	45	VDD	-62	-2374	85	SEG11	1794	1470
6	SEG50	-1794	1470	46	RS	62	-2374	86	SEG12	1794	1610
7	SEG51	-1794	1330	47	R/W	188	-2374	87	SEG13	1794	1750
8	SEG52	-1794	1190	48	E	312	-2374	88	SEG14	1794	1890
9	SEG53	-1794	1050	49	DB0	438	-2374	89	SEG15	1794	2030
10	SEG54	-1794	910	50	DB1	562	-2374	90	SEG16	1794	2170
11	SEG55	-1794	770	51	DB2	688	-2374	91	SEG17	1686	2374
12	SEG56	-1794	630	52	DB3	812	-2374	92	SEG18	1561	2374
13	SEG57	-1794	490	53	DB4	938	-2374	93	SEG19	1436	2374
14	SEG58	-1794	350	54	DB5	1062	-2374	94	SEG20	1311	2374
15	SEG59	-1794	210	55	DB6	1188	-2374	95	SEG21	1186	2374
16	SEG60	-1794	70	56	DB7	1312	-2374	96	SEG22	1061	2374
17	COM9	-1794	-70	57	T2	1438	-2374	97	SEG23	936	2374
18	COM10	-1794	-210	58	T1	1562	-2374	98	SEG24	811	2374
19	COM11	-1794	-350	59	COM24	1794	-2170	99	SEG25	686	2374
20	COM12	-1794	-490	60	COM23	1794	-2030	100	SEG26	561	2374
21	COM13	-1794	-630	61	COM22	1794	-1890	101	SEG27	436	2374
22	COM14	-1794	-770	62	COM21	1794	-1750	102	SEG28	311	2374
23	COM15	-1794	-910	63	COM20	1794	-1610	103	SEG29	186	2374
24	COM16	-1794	-1050	64	COM19	1794	-1470	104	SEG30	61	2374
25	COM25	-1794	-1190	65	COM18	1794	-1330	105	SEG31	-64	2374
26	COM26	-1794	-1330	66	COM17	1794	-1190	106	SEG32	-189	2374
27	COM27	-1794	-1470	67	COM8	1794	-1050	107	SEG33	-314	2374
28	COM28	-1794	-1610	68	COM7	1794	-910	108	SEG34	-439	2374
29	COM29	-1794	-1750	69	COM6	1794	-770	109	SEG35	-564	2374
30	COM30	-1794	-1890	70	COM5	1794	-630	110	SEG36	-689	2374
31	COM31	-1794	-2030	71	COM4	1794	-490	111	SEG37	-814	2374
32	COM32	-1794	-2170	72	COM3	1794	-350	112	SEG38	-939	2374

PAD CENTER COORDINATES (Continued)

Pad	Pad	Coordinate		Pad	Pad	Coordinate		Pad	Pad	Coordinate	
Num.	Name	X	Y	Num.	Name	X	Y	Num.	Name	X	Y
33	VSS	-1562	-2374	73	COM2	1794	-210	113	SEG39	-1064	2374
34	OSC1	-1438	-2374	74	COM1	1794	-70	114	SEG40	-1189	2374
35	OSC2	-1312	-2374	75	SEG1	1794	70	115	SEG41	-1314	2374
36	V1	-1188	-2374	76	SEG2	1794	210	116	SEG42	-1439	2374
37	V2	-1062	-2374	77	SEG3	1794	350	117	SEG43	-1564	2374
38	V3	-938	-2374	78	SEG4	1794	490	118	SEG44	-1689	2374
39	V4	-812	-2374	79	SEG5	1794	630				
40	V5	-688	-2374	80	SEG6	1794	770				

PAD DESCRIPTION

Pad (No.)	Pad No.	I/O	Name	Description	Interface
V_{DD}	45		Supply voltage	For logical circuit (+3V, 5V)	Power supply
V_{SS}	33			Ground (0V)	
V1-V5	36-40			Bias voltage level for LCD driving	
S1-S60	75-118, 1-16	O	Segment output	Segment signal output for LCD drive	LCD
C1-C8 C9-C16 C17-C24 C25-C32	74-67, 17-24, 66-59, 25-32,	O	Common output	Common signal output for LCD drive	LCD
OSC1	34	I	Oscillator	When using internal oscillator, connect external Rf resistor.	External resistor OSC1/OSC2
OSC2	35	O	Oscillator	If external clock is used, connect it to OSC1.	External clock (OSC1)
RS	46	I	Register select	Used as register selection input. When RS = 1, Data register is selected. When RS = 0, Instruction register is selected.	MPU
R/W	47	I	Read/write	Used as read/write selection input. When RW = 1, read operation. When RW = 0, write operation.	MPU
E	48	I	Read/write Enable	Used as read/write enable signal.	MPU
DB0 - DB3	49 - 52	I/O	Data bus 0-7	In 8-bit bus mode, used as low order bi-directional data bus. In 4-bit bus mode, open these pins.	MPU
DB4 - DB7	53 - 56	I/O	Data bus 0-7	In 8-bit bus mode, used as high order bi-directional data bus. In 4-bit bus mode, used as both high and low order. DB7 used for busy flag output.	MPU
Vci	44	I	Voltage doubler output	Input terminal for voltage doubler. (normally Vci = V_{DD})	Power supply
C1,C2	42, 43	I	Capacitor	Capacitor for voltage doubler connecting terminal (+). Capacitor for voltage doubler connecting terminal (-).	Capacitor
V5OUT	41	O	Voltage doubler output	Voltage doubler output terminal connected to LCD supply voltage.	V5
T1, T2	58, 57	I	Test pin	Maker testing terminal (normally open)	

FUNCTION DESCRIPTION

System Interface

This chip has both kinds of interface type with MPU: 4-bit bus and 8-bit bus. 4-bit bus and 8-bit bus are selected by the DL bit in the instruction register.

During read or write operation, two 8-bit registers are used. One is the data register (DR), and the other is the instruction register (IR).

The data register (DR) is used as a temporary data storage place for being written into or read from DDRAW/CGRAM . Target RAM is selected by RAM address setting instruction. Each internal operation, reading from or writing into RAM, is done automatically. Thus, after MPU reads DR data, the data in the next DDRAM/CGRAM address is transferred into DR automatically. Also, after MPU writes data to DR, the data in DR is transferred into DDRAM/CGRAM automatically. The instruction register (IR) is used only to store instruction codes transferred from MPU. MPU cannot use it to read instruction data. To select a register, you can use the RS input pin in 4-bit/8-bit bus mode.

Table 1. Various Kinds of Operations to RS and R/W Bits

RS	R/W	Operation
0	0	Instruction Write operation (MPU writes instruction code into IR)
0	1	Read Busy flag (DB7) and address counter (DB0 - DB7)
1	0	Data Write operation (MPU writes data into DR)
1	1	Data Read operation (MPU reads data into DR)

Busy Flag (BF)

When BF = 1, it indicates that the internal operation is being processed. So during this time the next instruction cannot be accepted. BF can be read through DB7 port, when RS = 0, and R/W = 1. (Read Instruction Operation). Before executing the next instruction, be sure that BF is not 1.

Address Counter (AC)

The Address Counter (AC) stores DDRAM/CGRAM addresses, transferred from IR. After writing into (reading from) DDRAM/CGRAM. AC is automatically increased (decreased) by 1. When RS = 0 and R/W = 1, AC can be read through ports DB0 - DB6.

Display Data RAM (DDRAM)

The DDRAM stores display data of maximum 80 × 8 bits (80 characters). The DDRAM address is set in the address counter (AC) as a hexadecimal number. (Refer to fig-1).

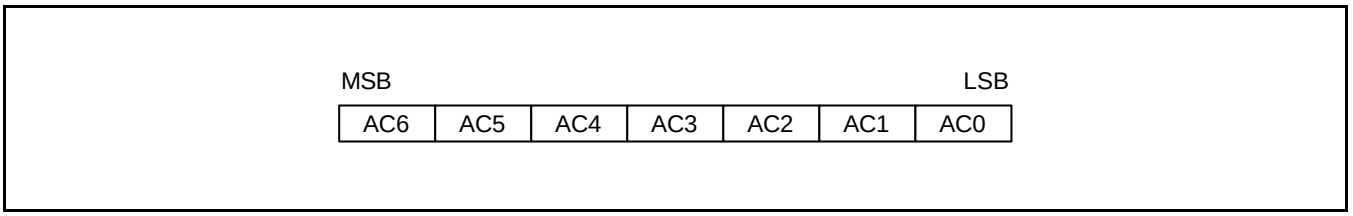


Figure 1. DDRAM Address

1) 1-line Display

In case of a 1-line display, the address range of DDRAM is 00H - 04H.

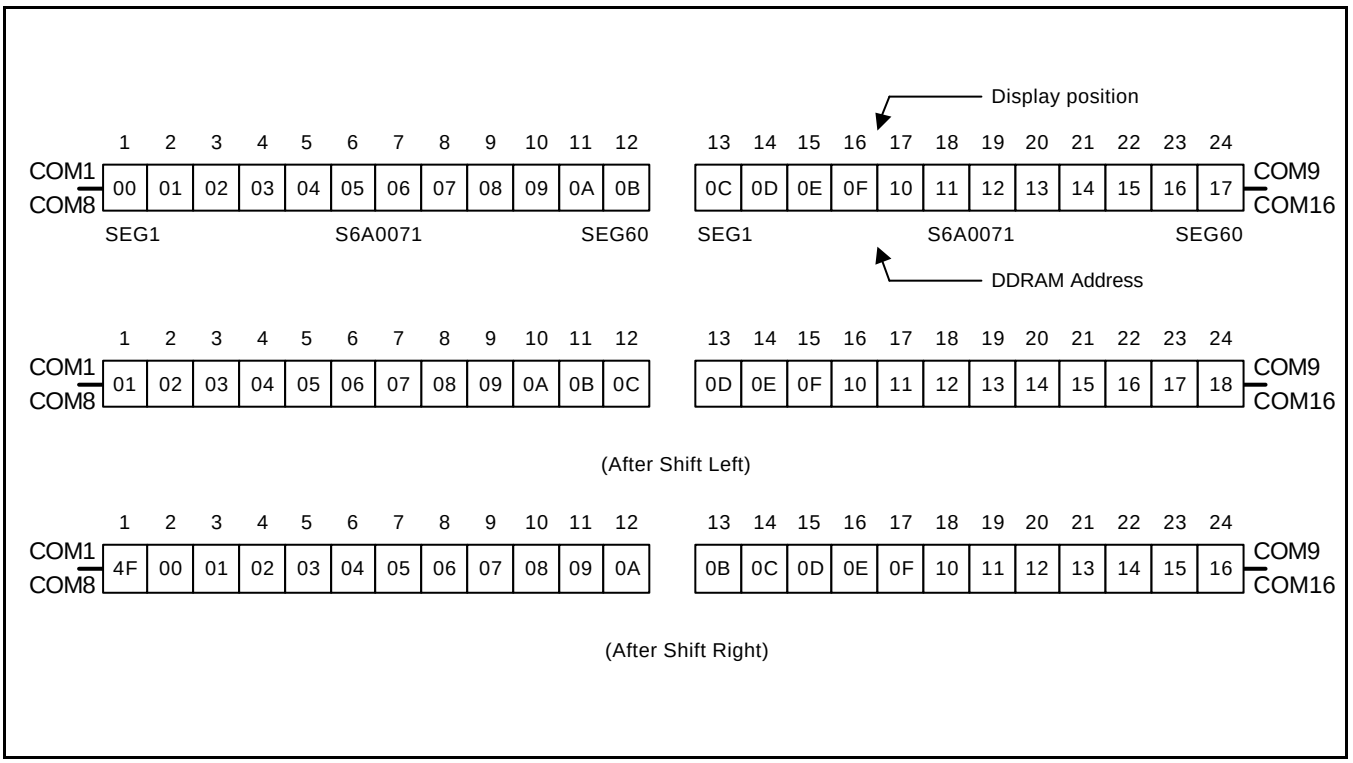


Figure 2. 1-line ´ 24 char. Display

2) 2-line Display

In case of a 2-line display, the address range of DDRAM is 00H - 27H and 40H - 67H.

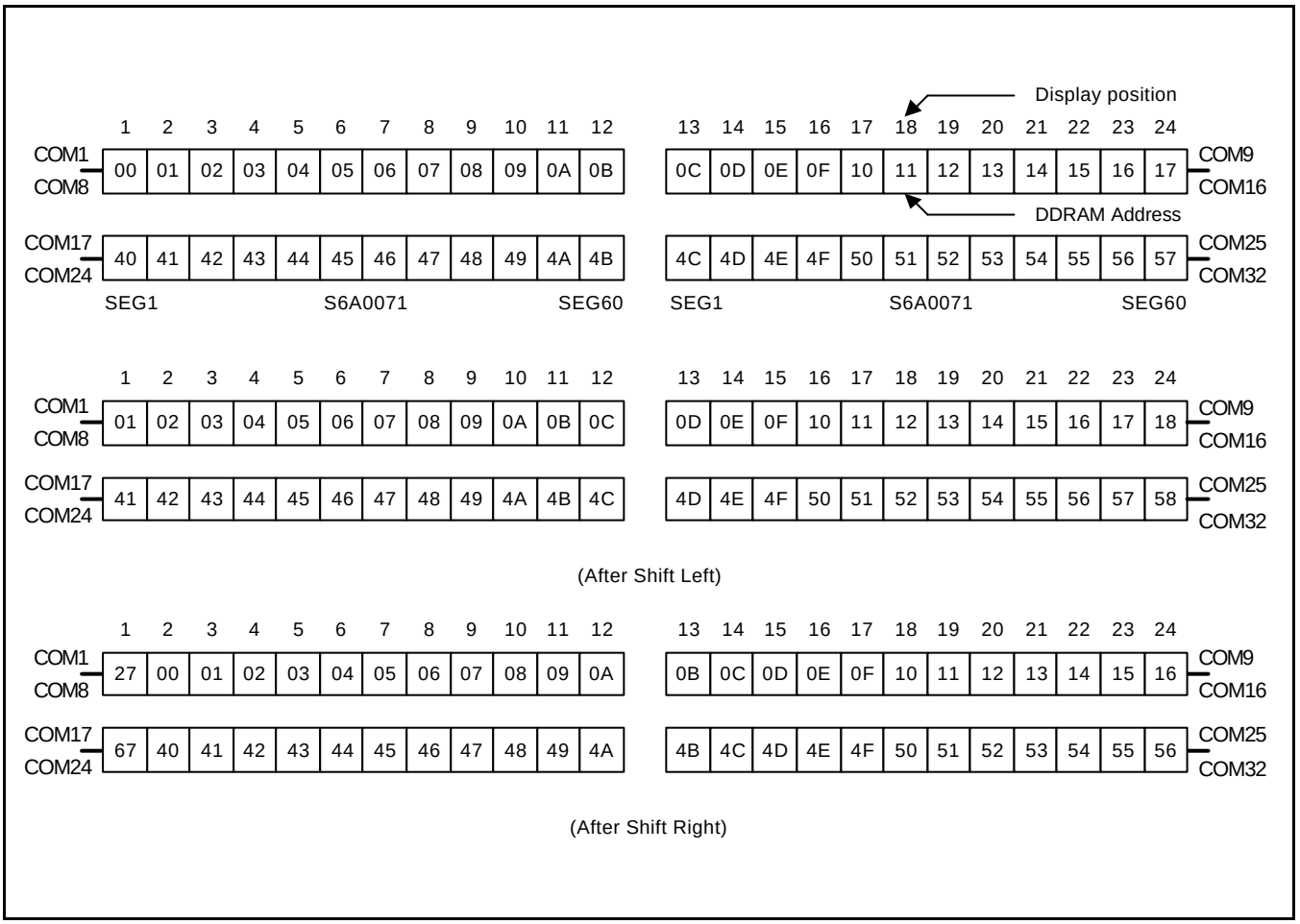


Figure 3. 2-line × 24 char. Display with 60 SEG. Extension Driver

CGROM (Characteristic Generator ROM)

CGROM has a 5 x 7 dots 240 character pattern.

CGRAM (Character Generator RAM)

CGRAM has up to 5 x 8 dots 8 characters. By writing font data to CGRAM, user defined characters can be used (Refer to Table 3).

Timing Generation Circuit

The timing generation circuit generates clock signals for the internal operations.

LCD Driver Circuit

LCD Driver circuit has 32 common and 60 segment signals for LCD driving. Data from CGRAM/CGROM is transferred to an 60-bit segment latch serially, and then stored to an 60-bit shift latch. When each com is selected by a 32-bit common register, segment data is also outputs through the segment driver from and 60-bit segment latch. In case of a 1-line display mode, COM1 - COM16 have 1/16 duty, and in 2-line display mode, COM1 - COM32 have 1/32 duty ratio.

Cursor/Blink Control Circuit

It controls cursor/blink ON/OFF at cursor position.

Table 3. Relationship Between Character Code (DDRAM) and Character Pattern (CGROM)

Character Code (DDRAM data)								CGRAM Address						CGRAM Data								Pattern number
D7	D6	D5	D4	D3	D2	D1	D0	A5	A4	A3	A2	A1	A0	P7	P6	P5	P4	P3	P2	P1	P0	
0	0	0	0	x	0	0	0	0	0	0	0	0	0	x	x	x	0	1	1	1	0	Pattern 1
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
				.							0	1	1				1	1	1	1	1	
				.							1	0	0				1	0	0	0	1	
				.							1	0	1				1	0	0	0	1	
				.							1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	
				.						.							.					.
				.						.							.					.
0	0	0	0	x	1	1	1	1	1	1	0	0	0	x	x	x	1	0	0	0	1	Pattern 8
											0	0	1				1	0	0	0	1	
											0	1	0				1	0	0	0	1	
				.							0	1	1				1	1	1	1	1	
				.							1	0	0				1	0	0	0	1	
				.							1	0	1				1	0	0	0	1	
											1	1	0				1	0	0	0	1	
											1	1	1				0	0	0	0	0	

"X": Don't care.

INSTRUCTION DESCRIPTION

OUTLINE

To overcome the speed difference between internal clock of S6A0071 and MPU clock, S6A0071 performs internal operation by storing control information to IR or DR. The internal operation is determined according to the signal from MPU, composed of read/write and data bus. (refer to Table 5) Instruction can be divided largely four kinds,

(1) S6A0071 function set instructions (set display methods, set data length, etc.)

(2) Address set instructions to internal RAM

(3) Data transfer instructions with internal RAM

(4) Others.

The address of internal RAM is automatically increased or decreased by 1.

NOTE

During internal operation, Busy Flag (DB7) is read "1". Busy Flag check must be precede by the next instruction. When you make an MPU program with checking the Busy Flag (DB7) is made, it must be necessary 1/2 fosc for executing the next instruction by falling E signal after the Busy Flag (DB7) goes to "0".

CONTENTS

Clear Display

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	0	1

Clear all the display data by writing "20H" (space code) to all DDRAM address, and set DDRAM address to "00H" into AC (address counter). Return cursor to the original status, namely, bring the cursor to the left edge on first line of the display. Make entry mode increment (I/D = "1").

Return Home

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	0	1	x

* "x": don't care

Return Home is cursor return home instruction. Set DDRAM address to "00H" into the address counter. Return cursor to its original site and return display to its original status, if shifted. Contents of DDRAM does not change.

Entry Mode Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	0	1	I/D	SH

Set the moving direction of cursor and display.

I/D: Increment/Decrement of DDRAM Address (Cursor or Blink)
When I/D = "1", cursor/blink moves to right and DDRAM address is increased by 1.
When I/D = "0", cursor/blink moves to left and DDRAM address is decreased by 1.
* CGRAM operates the same as DDRAM, when reading from or writing to CGRAM.

SH: Shift of Entire Display
When DDRAM is in the read (CGRAM read/write) operation or SH = "0", shift of entire display is not performed.
If SH = "1" and DDRAM is in the write operation, shift of entire display is performed according to I/D value (I/D = "1" : shift left, I/D = "0" : shift right).

Display ON/OFF Control

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	0	1	D	C	B

Control display/cursor/blink ON/OFF 1 bit register.

D: Display ON/OFF Control Bit
When D = "1", entire display is turned on.
When D = "0", display is turned off, but display data remained in DDRAM.

C: Cursor ON/OFF Control Bit
When C = "1", cursor is turned on.
When C = "0", cursor is disappeared in current display, but I/D register preserves its data.

B: Cursor Blink ON/OFF Control Bit
When B = "1", cursor blink is on, which performs alternate between all the "1" data and display character at the cursor position.
When B = "0", blink is off.

Cursor or Display Shift

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	0	1	S/C	R/L	x	x

Without waiting or reading the display data, shift right/left cursor position or display. This instruction is used to correct or search display data (Refer to table 6). During 2-line mode display, cursor moves to the 2nd line after the 40th digit of the 1st line. Note that display shift is performed simultaneously for the whole line. When displayed data is shifted repeatedly, each line is shifts individually. When display shift is performed, the contents of the address counter are not changed.

Table 6. Shift Patterns According to S/C and R/L Bits

S/C	R/L	Operation
0	0	Shift cursor to the left, AC is decreased by 1
0	1	Shift cursor to the right, AC is increased by 1
1	0	Shift all the display to the left, cursor moves according to the display
1	1	Shift all the display to the right, cursor moves according to the display

Function Set

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	DL	N	x	x	x

DL: Interface data length control bit
When DL = "1", it means 8-bit bus mode with MPU.
When DL = "0", it means 4-bit bus mode with MPU. Hence, DL is a signal to select 8-bit or 4-bit bus mode. When 4-bit bus mode, it needs to transfer 4-bit data by two times.

N: Display line number control bit
When N = "0", it means 1-line display mode.
When N = "1", 2-line display mode is set.

Set CGRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0

Set CGRAM address to AC. This instruction makes CGRAM data available from MPU.

Set DDRAM Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0

Set DDRAM address to AC. This instruction makes DDRAM data available from MPU. When 1-line display mode (N = 0), DDRAM address is from "00H" to "4FH". In 2-line display mode (N = 1), DDRAM address in the 1st line is from "00H" to "27H", and DDRAM address in the 2nd line is from "40H" to "67H".

Read Busy Flag & Address

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0

This instruction shows whether S6A0071 is in internal operation or not. If the resultant BF is "1", it means the internal operation is in progress and you have to wait until BF to be Low, and then the next instruction can be performed. In this instruction you can read also the value of address counter.

Write data to RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	D7	D6	D5	D4	D3	D2	D1	D0

Write binary 8-bit data to DDRAM/CGRAM. The selection of RAM from DDRAM, and CGRAM, is set by the previous address set instruction: (DDRAM address set, CGRAM address set). RAM set instruction can also determine the AC direction to RAM. After write operation, the address is automatically increased/decreased by 1, according to the entry mode.

Read data from RAM

RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	D7	D6	D5	D4	D3	D2	D1	D0

Read binary 8-bit data from DDRAM/CGRAM. The selection of RAM is set by the previous address set instruction. If the address set instruction of RAM is not performed before this instruction, the data that is read first is invalid, because the direction of AC is not determined. If you read RAM data several times without RAM address set instruction before read operation, you can get correct RAM data from the second, but the first data would be incorrect, because there is no time margin to transfer RAM data. In case of DDRAM read operation, cursor shift instruction plays the same role as DDRAM address set instruction; it also transfer RAM data to output data register. After read operation address counter is automatically increased/decreased by 1 according to the entry mode. After CGRAM read operation, display shift may not be executed correctly.

NOTE: In case of RAM write operation, AC is increased/decreased by 1 like read operation. In this time, AC indicates the next address position, but you can read only the previous data by read instruction.

Table 6. Instruction Table

Instruction	Instruction Code										Description	Execution
	RS	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0	Instruction Code	time (fsoc=270)
Clear Display	0	0	0	0	0	0	0	0	0	1	Write "20H" to DDRAM. and set DDRAM address to "00H" from AC.	1.53ms
Return Home	0	0	0	0	0	0	0	0	1	X	Set DDRAM address to "00H" from the AC and return cursor to its original position if shifted. The contents of DDRAM are not change.	1.53ms
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	SH	Assign cursor moving direction and make shift of entire display possible.	39µs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Set display(D), cursor(C), and blinking of cursor(B) on/off control bit.	39µs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	X	X	Set cursor moving and display shift control bit, and the direction, without changing of the AC.	39µs
Function Set	0	0	0	0	1	DL	N	X	X	X	Set interface data length (DL : 4-bit/8-bit), numbers of display line (N : 1-line/2-line).	39µs
Set CGRAM Address	0	0	0	1	AC5	AC4	AC3	AC2	AC1	AC0	Set CGRAM address in address counter.	39µs
Set DDRAM Address	0	0	1	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Set DDRAM address in address counter.	39µs
Read Busy Flag and Address	0	1	BF	AC6	AC5	AC4	AC3	AC2	AC1	AC0	Whether during internal operation or not can be known by reading BF. The contents of address counter can also be read.	0µs
Write Data to RAM	1	0	D7	D6	D5	D4	D3	D2	D1	D0	Write data into internal RAM (DDRAM/CGRAM).	43µs
Read Data from RAM	1	1	D7	D6	D5	D4	D3	D2	D1	D0	Read data from internal RAM (DDRAM/CGRAM).	43µs

*"x": don't care

NOTE: When you make an MPU program, checking the Busy Flag (DB7), a time margin of 1/2 f_{OSC} is necessary for executing the next instruction by the falling edge of the 'E' signal after the Busy Flag (DB7) goes to "0".

INTERFACE WITH MPU

Interface with 8-bit MPU

When the interfacing data length are 8-bit, transfer is performed all at once through 8 ports, from DB0 to DB7. An example of the timing sequence is shown below.

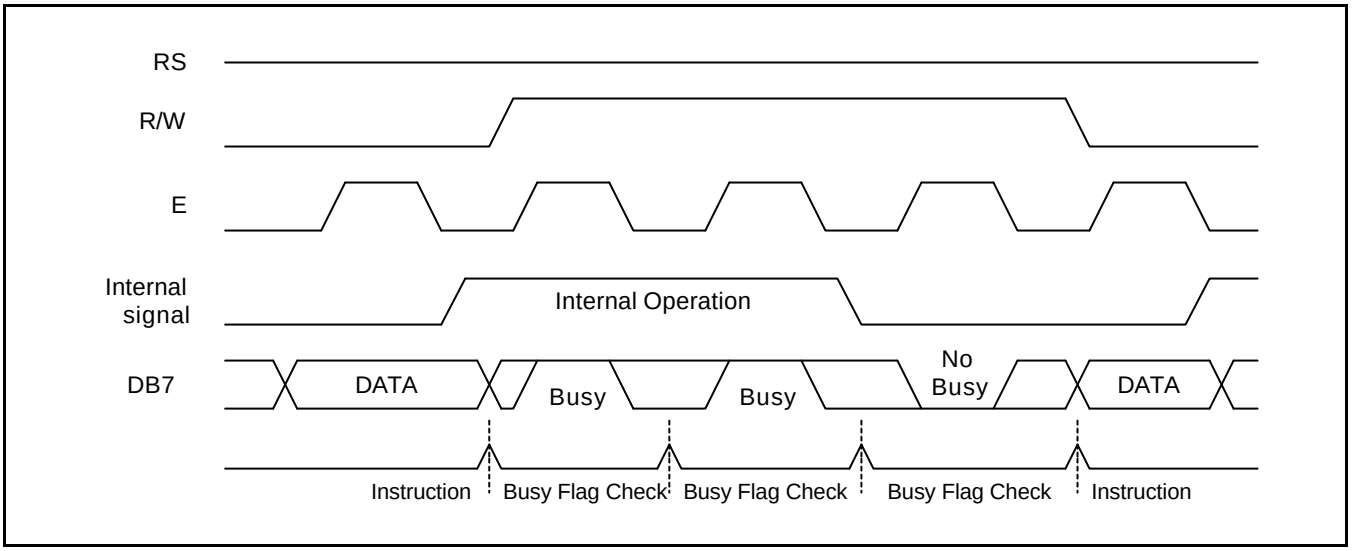


Figure 4. Example of 8-bit Bus Mode Timing Diagram

Interface with 4-bit MPU

When interfacing data length is 4-bit, only 4 ports, from DB4 to DB7, are used as data bus.
At first higher 4-bit (in the case of 8-bit bus mode, the contents of DB4 - DB7), and then lower 4-bit (in case of 8-bit bus mode, the contents of DB0 - DB3) are transferred. So transfer is performed twice Busy Flag outputs "high" after the second transfer are ended. An example of timing sequence is shown below.

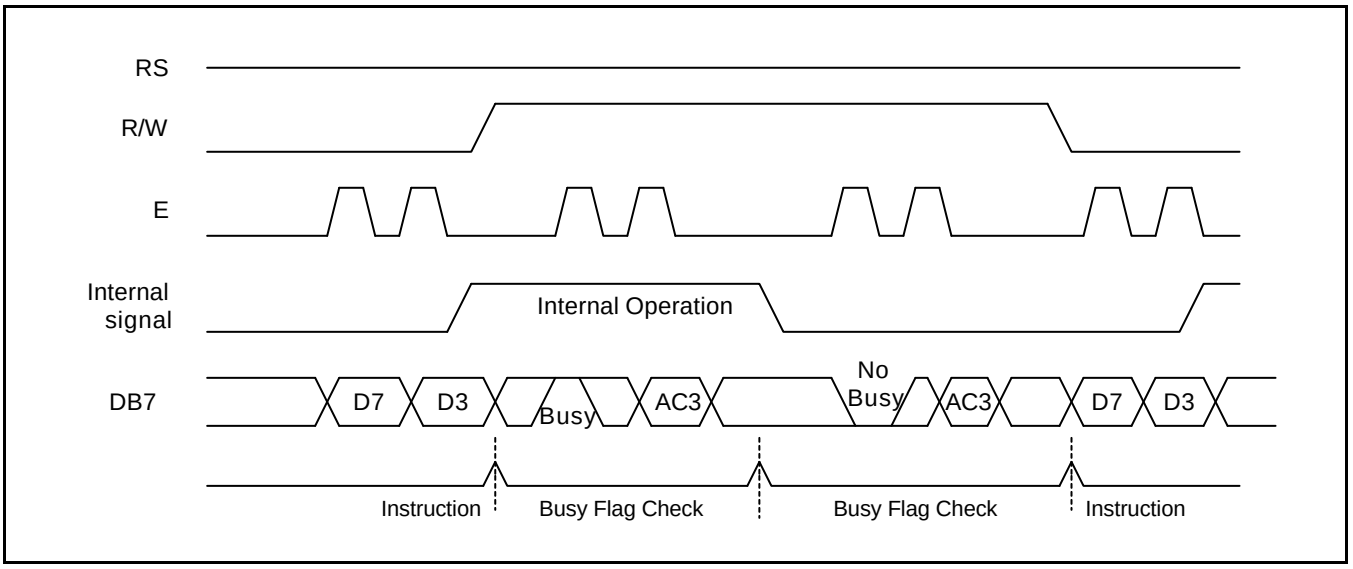
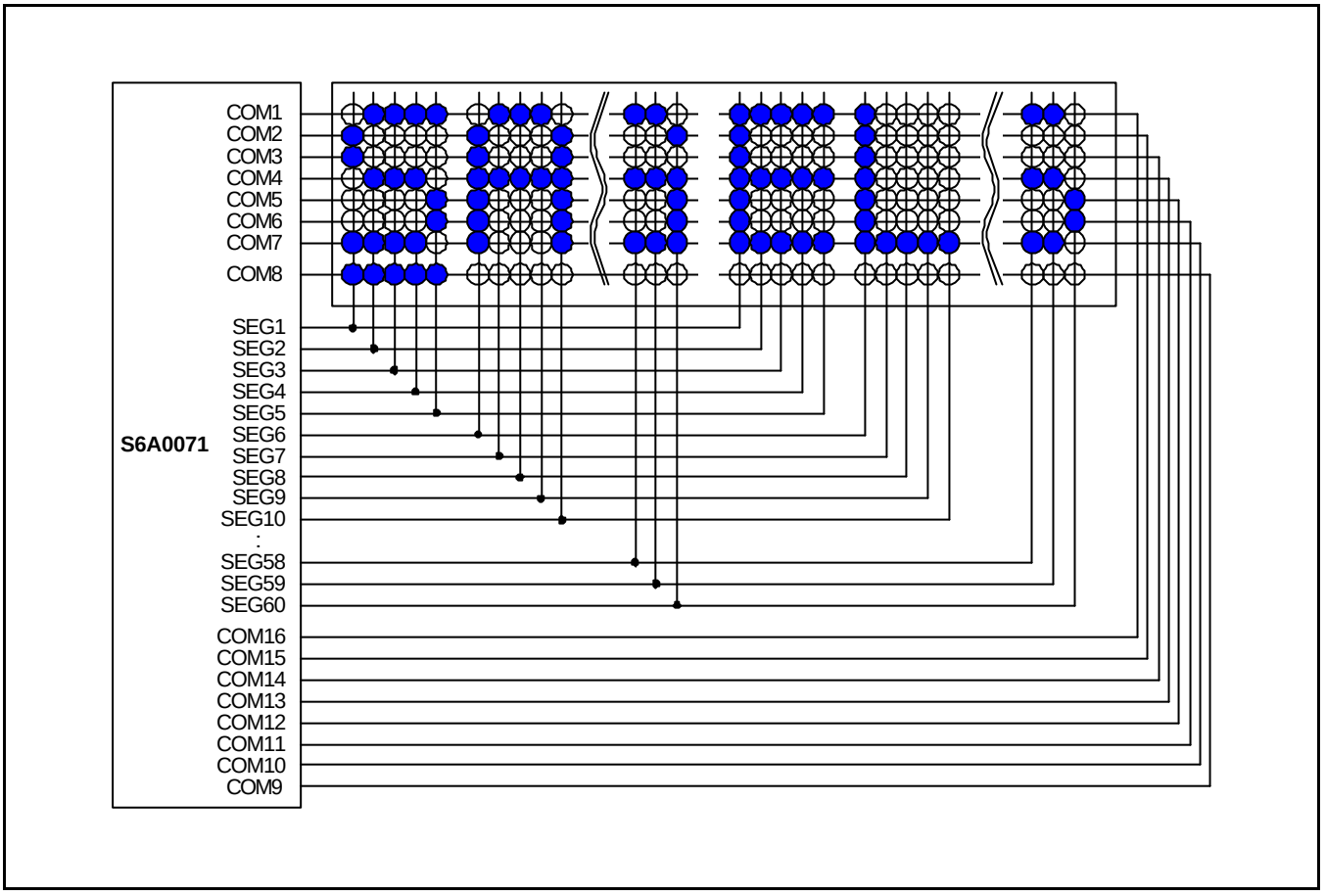


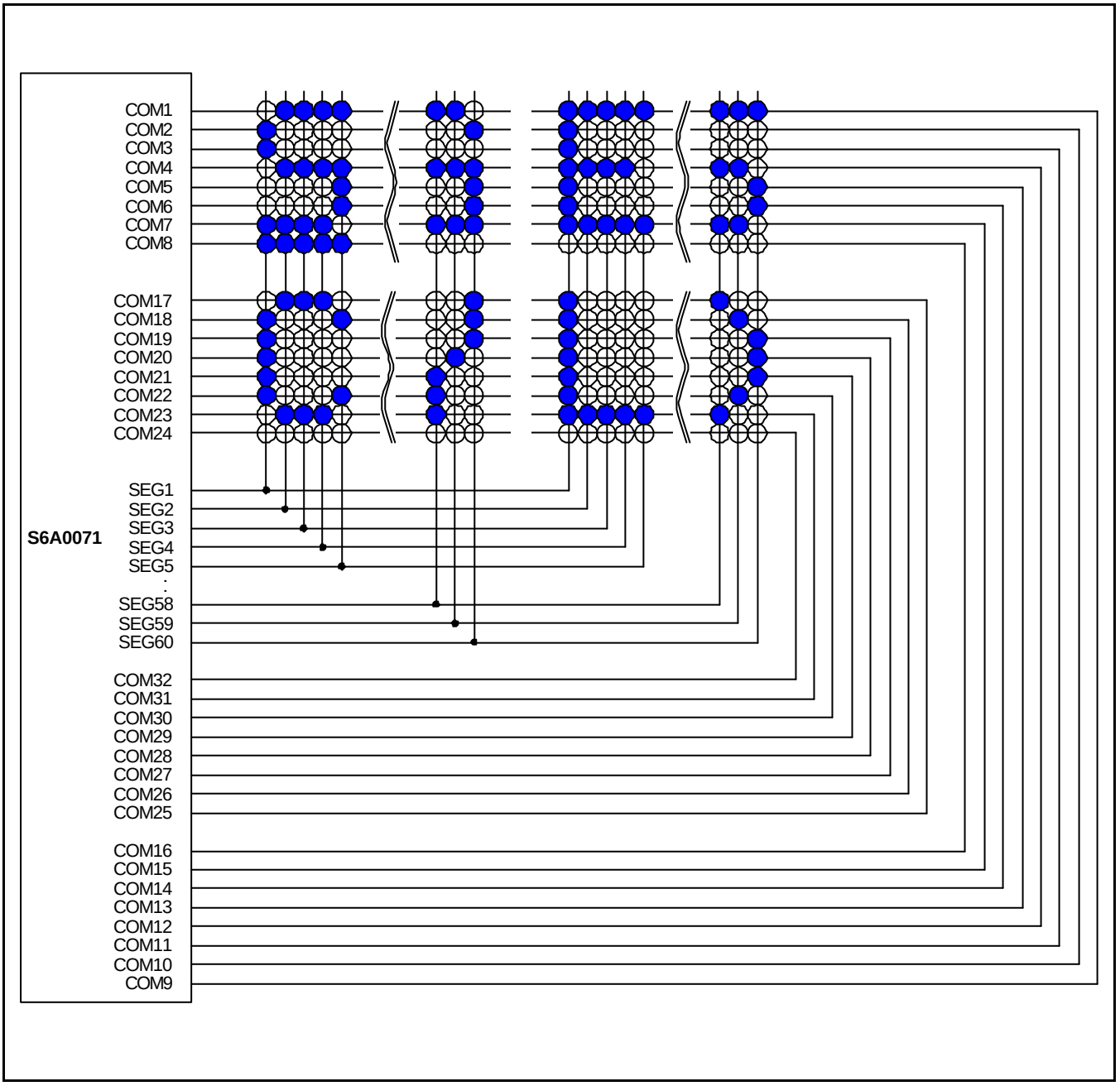
Figure 5. Example of 4-bit Bus Mode Timing Diagram

APPLICATION INFORMATION ACCORDING TO LCD PANEL

LCD Panel: 24 character ´ 1-line character format: 5 ´ 7 dots + 1 cursor line (1/5 bias, 1/16 duty)

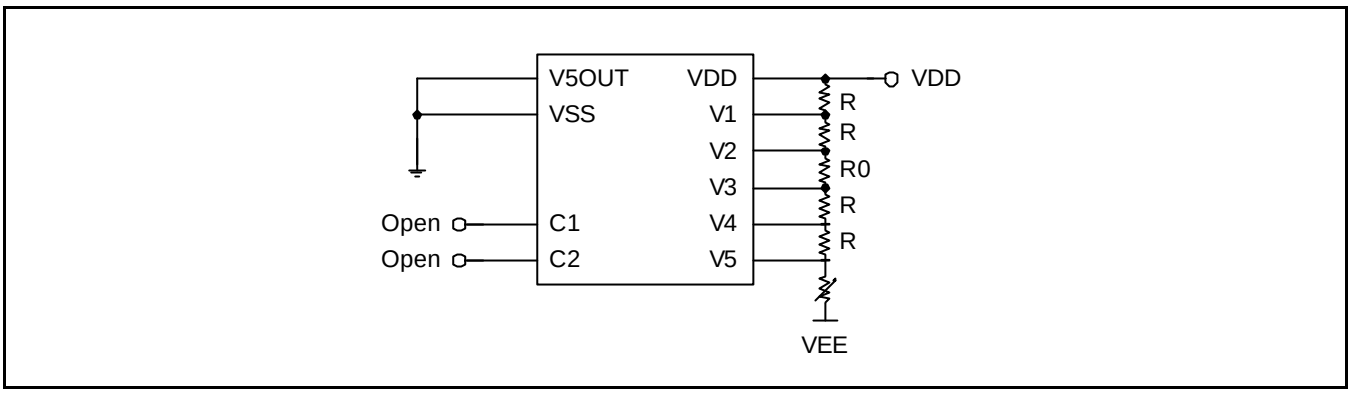


LCD Panel: 24 character ´ 2-line character format: 5 ´ 7 dots + 1 cursor line (1/6.7 bias, 1/32 duty)

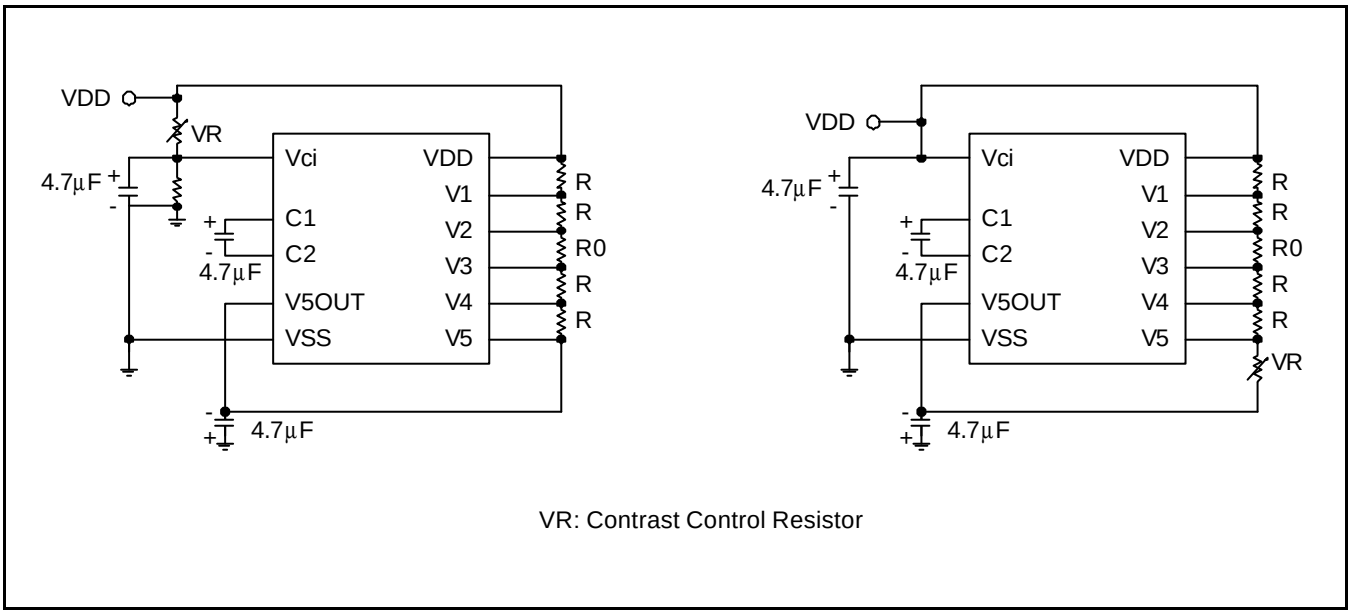


POWER SUPPLY FOR DRIVING LCD PANEL

When an external power supply is used



When an internal booster is used (Boosting twice)



NOTES:

1. Boosted output voltage should not exceed the maximum value (11V) of the LCD driving voltage.
2. A voltage of over 5.5V should not be input into the reference voltage (Vci) when boosting twice.
3. The value of resistance, according to the number of lines, duty ratio and the bias, is shown below. (Refer to table 8)

Table 8. Duty Ratio and Power Supply for LCD Driving

Item		Data	
Number		1	2
Duty Ratio		1/16	1/32
Bias		1/5	1/6.7
Divided Resistance	R	R	R
	R0	R	2.7R

INITIALIZING

When the power is turned on, S6A0071 is initialized automatically by power on reset circuit. During the initialization, the following instructions are executed, and BF(Busy Flag) is kept "High"(busy state) to the end of initialization.

(1) Display Clear instruction: Write "20H" to all DDRAM

(2) Set Functions instruction
DL = 1 : 8-bit bus mode
N = 1 : 2-line display mode

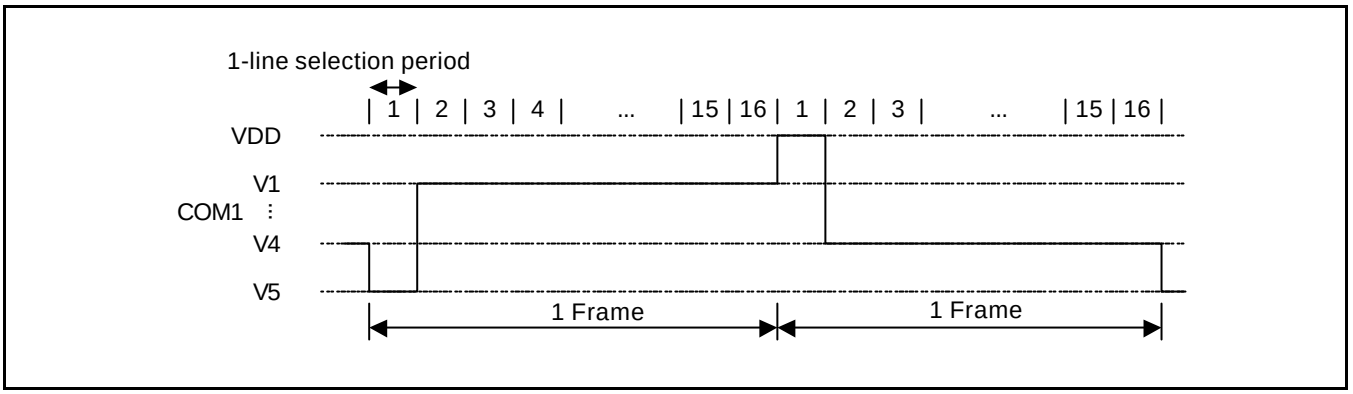
(3) Control Display ON/OFF instruction
D = 0 : Display OFF
C = 0 : Cursor OFF
B = 0 : Blink OFF

(4) Set Entry Mode instruction
I/D = 1 : Increment by 1
SH = 0 : No entire display shift

FRAME FREQUENCY

B-Type Waveform (Frame Inversion)

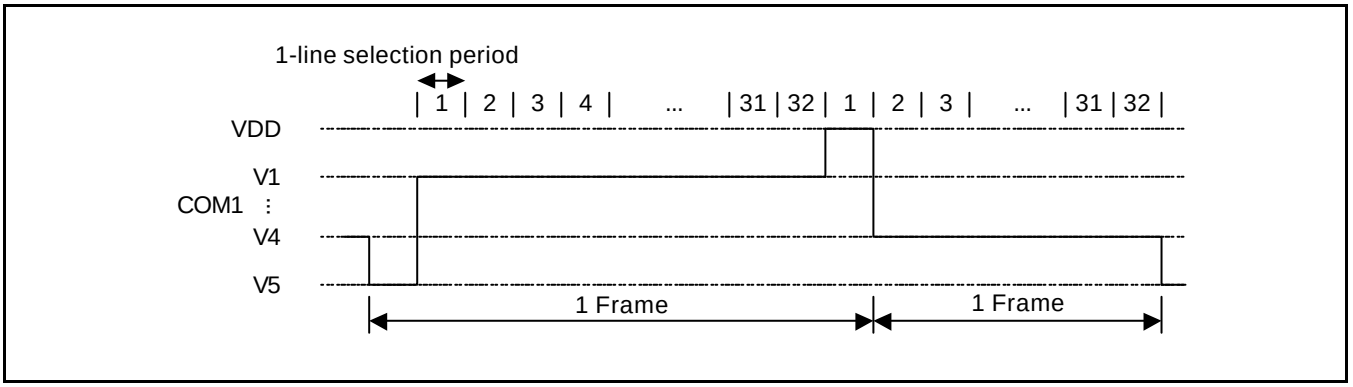
1) 1/16 Duty Cycle



Item	Clock/Frequency
1-line selection period	120 clocks
Frame frequency	140.7Hz

* f_{OSC} = 270kHz (1 clock = 3.7µs)

2) 1/32 duty cycle

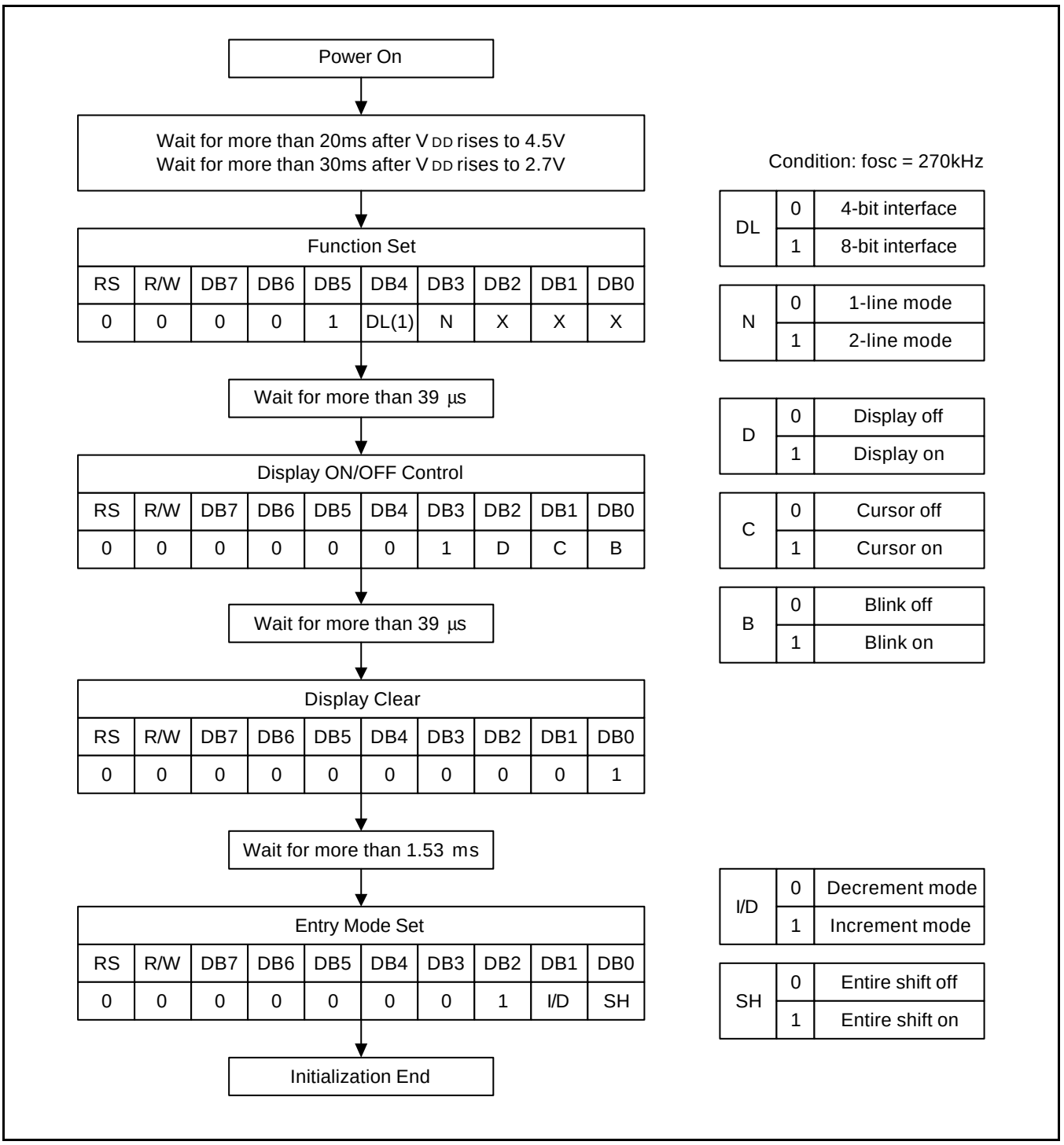


Item	Clock/Frequency
Line Selection Period	120 clocks
Frame Frequency	70.4Hz

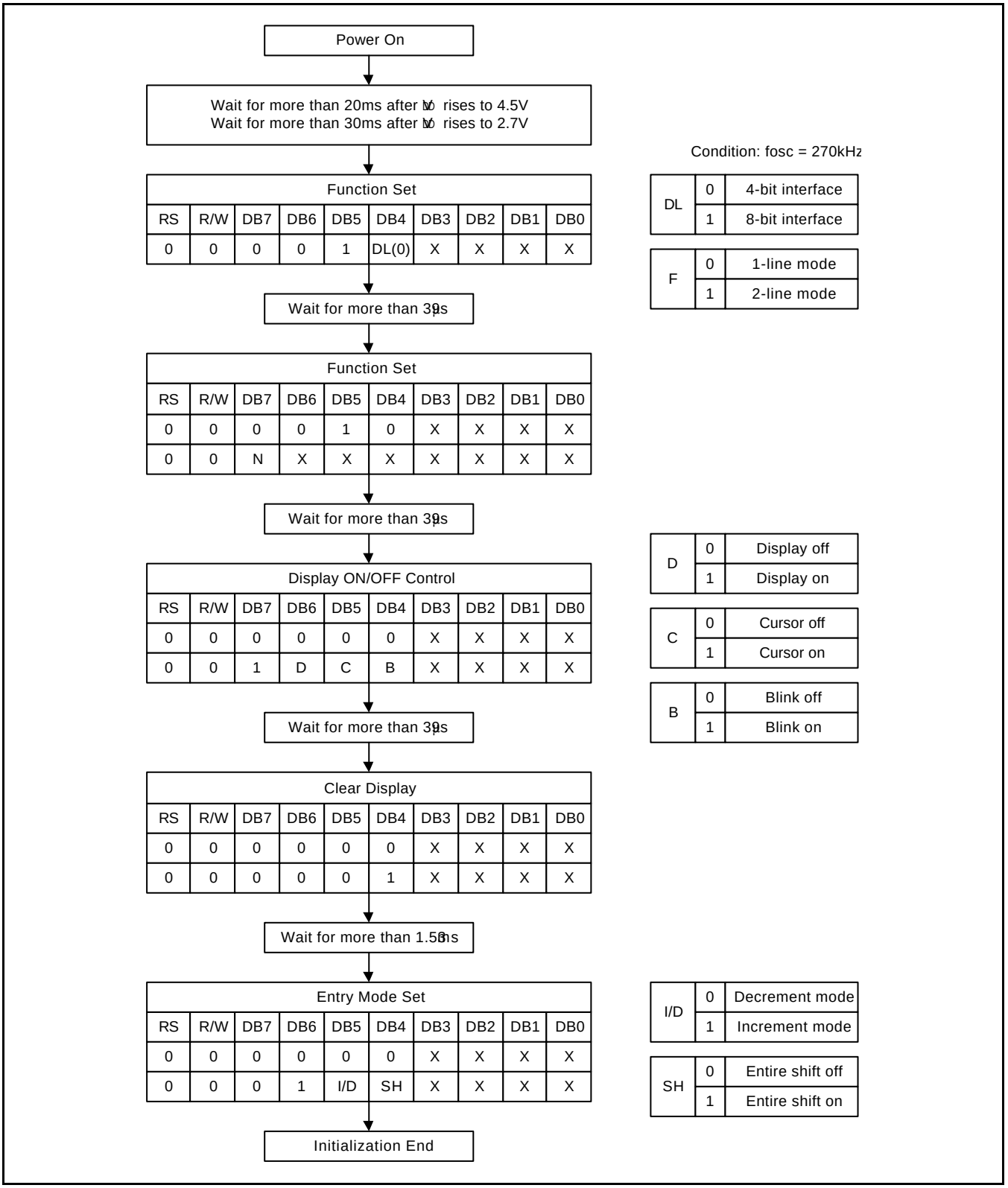
* f_{OSC} = 270kHz (1 clock = 3.7µs)

INITIALIZING BY INSTRUCTION

8-bit Interface mode



4-bit Interface mode



MAXIMUM ABSOLUTE LIMIT RATING

Maximum Absolute Power Ratings

Description	Symbol	Unit	Value
Power Supply Voltage (1)	V_{DD}	V	- 0.3 to +7.0
Power Supply Voltage (2)	V_{LCD}	V	V_{DD}-13.5 to V_{DD}+3.0
Input Voltage	V_{IN}	V	-0.3 to V_{DD}+0.3

NOTE: Voltage greater than above may damage the circuit. ($V_{DD} \geq V1 \geq 2 \geq V3 \geq V4 \geq V5$)

Temperature Characteristics

Description	Symbol	Unit	Value
Operating Temperature	T_{OPR}	°C	- 3.0 to +85
Storage Temperature	T_{STG}	°C	- 55 to +125

ELECTRICAL CHARACTERISTICS

DC Characteristics

(V_{DD} = +5V ± 10%, T_A = -30 to +85°C)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Operating voltage	V_{DD}	–	4.5	5.0	5.5	V
Supply current	I_{DD}	Internal oscillation or external clock operation. (V_{DD} = 5V, f_{OSC} = 270 kHz)	–	0.6	1.0	mA
Input voltage (1) (except OSC1)	V_{IH1}	–	2.3	–	V_{DD}	V
	V_{IL1}	–	–	–	0.8	
Input voltage (2) (OSC1)	V_{IH2}	–	V_{DD}-1.0	–	V_{DD}	V
	V_{IL2}	–	–	–	1.0	
Output voltage (1) (DB0 to DB7)	V_{OH1}	I_{OH} = -0.205mA	2.4	–	–	V
	V_{OL1}	I_{OL} = 1.6mA	–	–	0.4	
Output voltage (2) (OSC2)	V_{OH2}	I_O = -40µA	0.9V_{DD}	–	–	V
	V_{OL2}	I_O = 40µA	–	–	0.1V_{DD}	
Voltage drop	Vd_{COM}	I_O = ± 0.1mA	–	–	1	V
	Vd_{SEG}		–	–	1	
Input Leakage Current (1) E	I_{IL1}	V_{IN} = 0V to V_{DD}	-1	–	1	µA
Input leakage current(2) (R/W, RS, DB0 to DB7)	I_{IL2}	V_{IN} = V_{DD}	-5	–	5	
Low Input Current (R/W, RS, DB0 to DB7)	I_{IN}	V_{IN} = 0V, V_{DD} = 5V (pull up)	-50	-125	-250	
Internal Clock (external Rf)	f_{IC}	Rf = 91kΩ ± 2% (V_{DD} = 5V)	190	270	350	kHz
External Clock	f_{EC}	–	160	250	350	kHz
	duty		45	50	55	%
	t_R, t_F		–	–	0.2	µs
Voltage Doubler	V5out	Iout = 1mA, Ta = 25°C	-4.5	-4.7	–	V
	V_{EF}	R_L = ∞	95	99.9	–	%
	Vci	Input voltage	2.5	–	5.5	V
LCD Driving Voltage	V_{LCD}	V_{DD}-V_5 (1/5, 1/6.7 bias)	3.0	–	13.5	V

DC Characteristics

(V_{DD} = +3V ± 20%, T_A = -30 to +85°C)

Characteristic	Symbol	Condition	Min	Typ	Max	Unit
Operating voltage	V_{DD}	–	2.4	3.0	3.6	V
Supply current	I_{DD}	Internal oscillation or external clock. (V_{DD} = 3V, f_{OSC} = 270kHz)	–	0.2	0.3	mA
Input voltage (1) (except OSC1)	V_{IH1}	–	0.8V_{DD}	–	V_{DD}	V
	V_{IL1}	–	–	–	0.2V_{DD}	
Input voltage (2) (OSC1)	V_{IH2}	–	V_{DD}-1.0	–	V_{DD}	V
	V_{IL2}	–	–	–	1.0	
Output voltage (1) (DB0 to DB7)	V_{OH1}	I_{OH} = -0.205mA	2.0	–	–	V
	V_{OL1}	I_{OL} = 1.6mA	–	–	0.5	
Output voltage (2) (OSC2)	V_{OH2}	I_O = -40µA	0.9V_{DD}	–	–	V
	V_{OL2}	I_O = 40µA	–	–	0.1V_{DD}	
Voltage drop	Vd_{COM}	I_O = ± 0.1mA	–	–	1	V
	Vd_{SEG}		–	–	1	
Input Leakage Current (1) E	I_{IL1}	V_{IN} = 0V to V_{DD}	-1	–	1	µA
Input leakage current(2) (R/W, RS, DB0 to DB7)	I_{IL2}	V_{IN} = V_{DD}	-5	–	5	
Low Input Current (R/W, RS, DB0 to DB7)	I_{IN}	V_{IN} = 0V, V_{DD} = 3V (pull up)	-10	-25	-50	
Internal Clock (external Rf)	f_{IC}	Rf = 91kΩ ± 2% (V_{DD} = 3V)	160	240	320	kHz
Voltage Doubler	V5out	Iout = 1mA, Ta = 25°C	-2.5	-2.75	–	V
	V_{EF}	R_L = ∞	95	99.9	–	%
	Vci	Input voltage	1.8	–	V_{DD}	V
LCD Driving Voltage	V_{LCD}	V_{DD}-V_5 (1/5, 1/6.7 bias)	3.0	–	12.0	V

AC Characteristics

(V_{DD} = 4.5 to 5.5V, T_A = -30 to +85°C)

Mode	Characteristic	Symbol	Min	Typ	Max	Unit
Write Mode (Refer to figure 6)	E Cycle Time	t_C	500	–	–	ns
	E Rise Time/Fall Time	t_R, t_F	–	–	20	
	E Pulse Width (High, Low)	t_W	220	–	–	
	R/W and RS Setup Time	t_{SU1}	40	–	–	
	R/W and RS Hold Time	t_{h1}	10	–	–	
	Data Setup Time	t_{SU2}	60	–	–	
	Data Hold Time	t_{h2}	10	–	–	
Read Mode (Refer to figure 7)	E Cycle Time	t_C	500	–	–	ns
	E Rise Time/Fall Time	t_R, t_F	–	–	20	
	E Pulse Width (High, Low)	t_W	220	–	–	
	R/W and RS Setup Time	t_{SU}	40	–	–	
	R/W and RS Hold Time	t_h	10	–	–	
	Data Output Delay Time	t_D	–	–	120	
	Data Hold Time	t_{DH}	10	–	–	

AC Characteristics

(V_{DD} = 2.4 to 3.6V, T_A = -30 to +85°C)

Mode	Characteristic	Symbol	Min	Typ	Max	Unit
Write Mode (Refer to figure 6)	E Cycle Time	t_C	1400	–	–	ns
	E Rise Time/Fall Time	t_R, t_F	–	–	20	
	E Pulse Width (High, Low)	t_W	500	–	–	
	R/W and RS Setup Time	t_{SU1}	70	–	–	
	R/W and RS Hold Time	t_{h1}	10	–	–	
	Data Setup Time	t_{SU2}	195	–	–	
	Data Hold Time	t_{h2}	10	–	–	
Read Mode (Refer to figure 7)	E Cycle Time	t_C	1400	–	–	ns
	E Rise Time/Fall Time	t_R, t_F	–	–	20	
	E Pulse Width (High, Low)	t_W	500	–	–	
	R/W and RS Setup Time	t_{SU}	70	–	–	

	R/W and RS Hold Time	t_h	10	–	–
	Data Output Delay Time	t_D	–	–	600
	Data Hold Time	t_{DH}	20	–	–

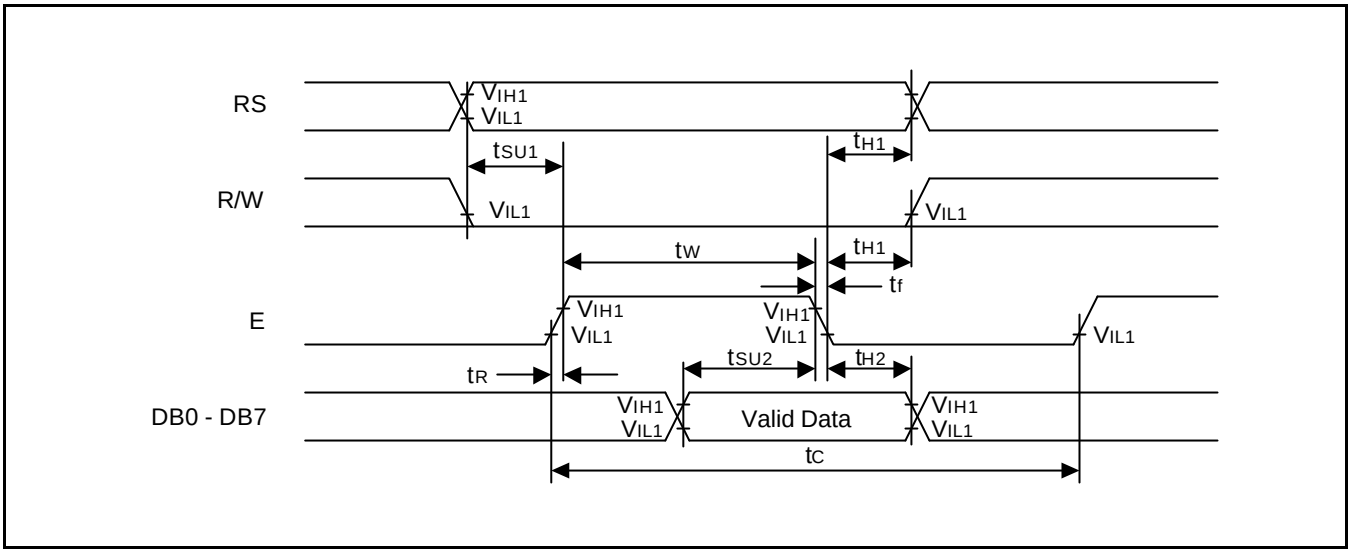


Figure 6. Write Mode Timing Diagram

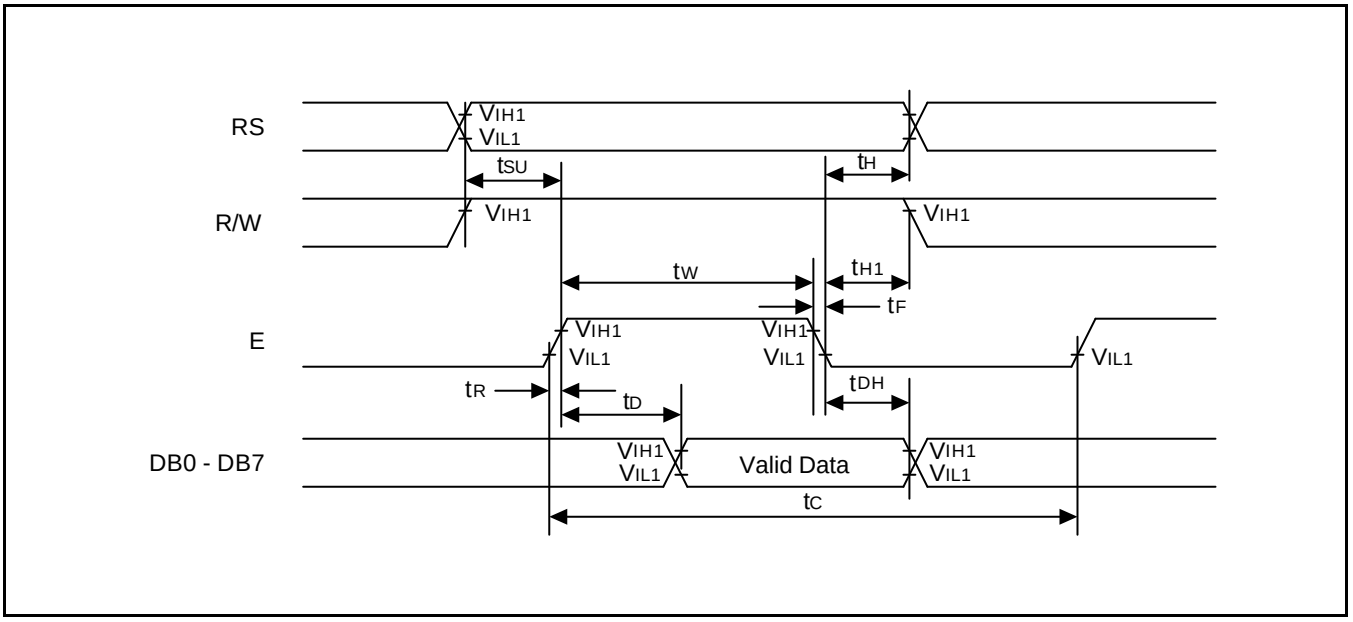


Figure 7. Read Mode Timing Diagram

NOTES