PEDL87V2104DIGEST-01
Issue Date: Jan. 20, 2003

OKI Semiconductor

ML87V2104 Preliminary

Video Signal Noise Reduction and Field Rate Conversion IC with a Built-in 4M Bit Field Memory

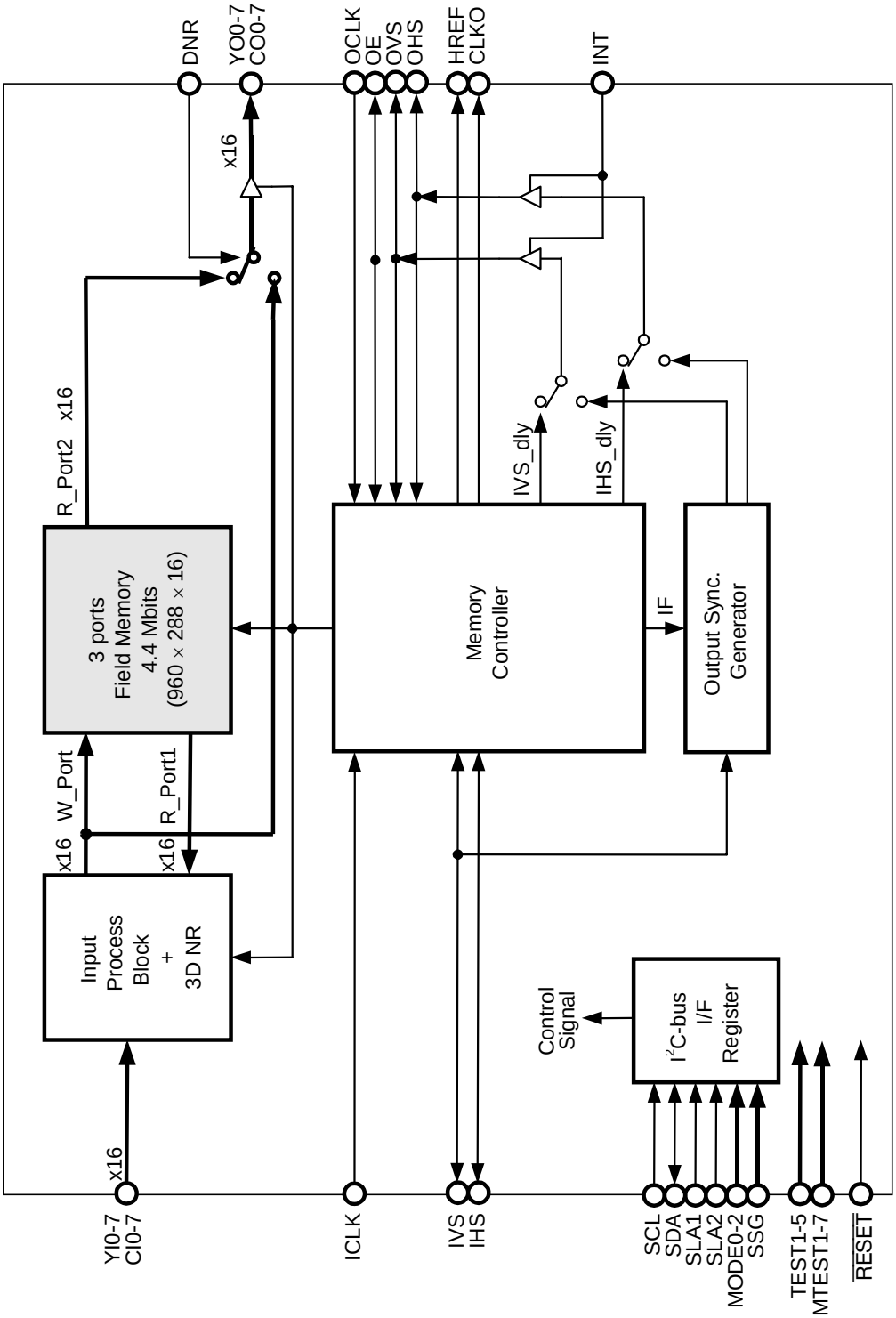
GENERAL DESCRIPTION

The ML87V2104 consists of a 3-port type (1 input port and 2 output ports) 4.4 Mbit (960 × 288 × 16bits) field memory and logic circuits for signal processing and memory control. The device can reduce field-recursive noise. Noise reduction auto mode can be set by detecting the noise in the vertical blanking period and by setting the noise reduction setting value according to the detected noise state. Moreover, an internal memory controller controls flicker-free conversion that doubles the vertical and horizontal direction frequencies.

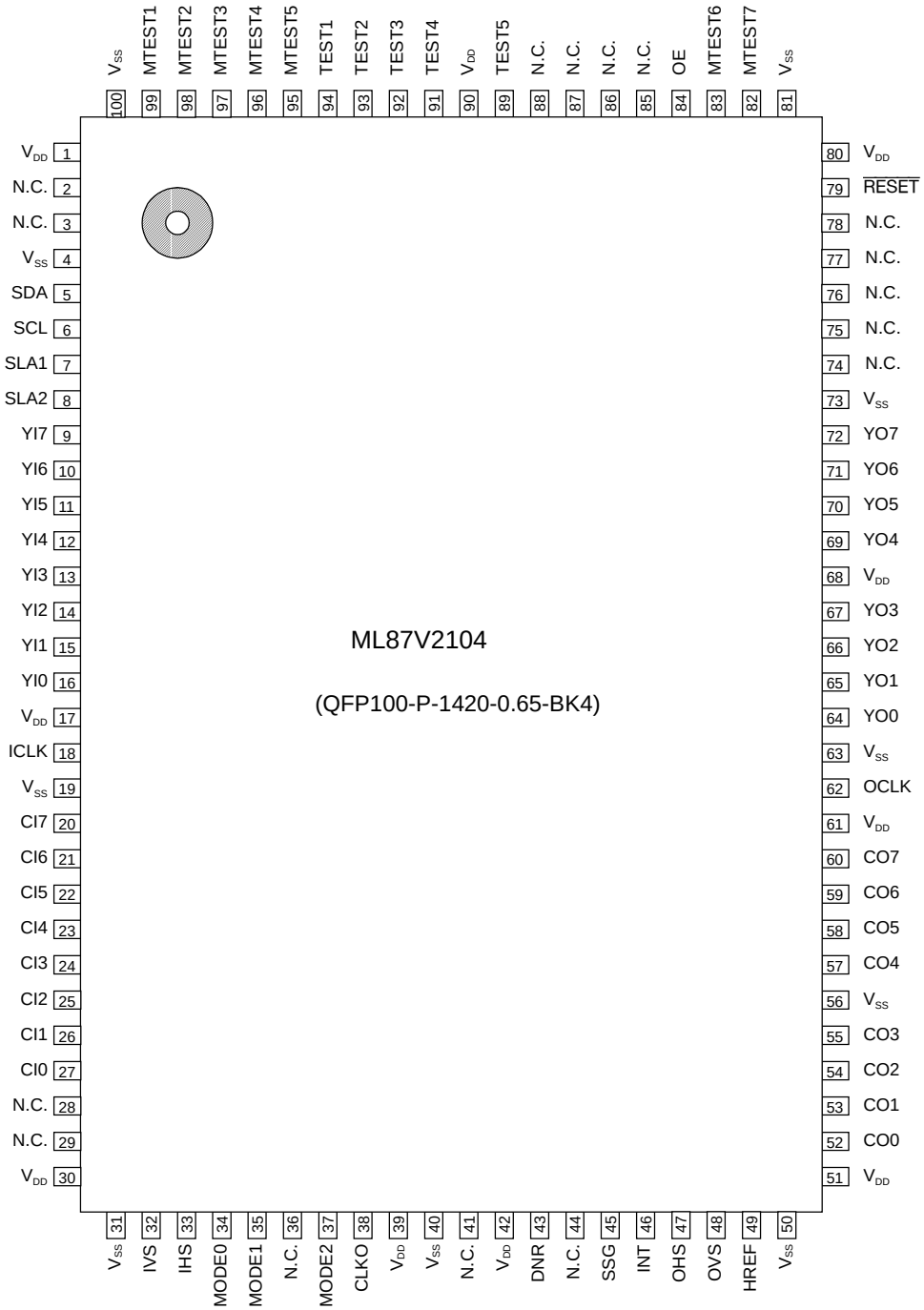
FEATURES

- Memory capacity :
  4.4 Mbit (960 × 288 × 16 bits) × 1 unit
- Maximum input operating frequencies (16 bits/8 bits, ITU-R BT.656):
  18/36 MHz (at 960 effective horizontal pixels)
- Maximum output operating frequencies (normal/flicker-free):
  18/36 MHz (at 960 effective horizontal pixels)
- Power supply voltage :
  3.3 V ± 0.3 V
- Input pin:
  TTL-5V tolerant (5 V withstand voltage)
- Input/output pins:
  Input TTL- output LVCMOS-5V tolerant (5 V withstand voltage)
- Output pin:
  LVCMOS (3.3 V)
- Input data format:
  YCbCr (8 bits (Y) + 8 bits (CbCr)) (4:2:2): Input 16-bit mode
  YCbCr (8 bits (YCbCr)) (4:2:2): Input 8-bit mode
  ITU-R656 (8 bits (YCbCr)): Input ITU-R BT.656 mode
- Output data format:
  YCbCr (8 bits (Y) + 8 bits (CbCr)) (4:2:2)
- Serial bus:
  I^2C-bus interface: (400 kHz, 100 kHz)
- Memory controller functions:
  Input: Compliant to 525/60 Hz 2:1, 625/50 Hz 2:1
  Output: 625/50 Hz 2:1, 525/60 Hz 2:1, 625/100 Hz 2:1, 525/120 Hz 2:1
- Sync generator functions:
  Can generate sync signals of 625/50 Hz 2:1, 525/60 Hz 2:1, 625/100 Hz 2:1, 525/120 Hz 2:1.
- Field-recursive type noise reduction function:
  Noise detection and noise subtraction type (with horizontal motion compensation)
  Auto mode noise reduction (noise is detected during vertical blanking period)
- Package:
  100 pin QFP (QFP100-P-1420-0.65-BK4)

BLOCK DIAGRAM



PIN CONFIGURATION (TOP VIEW)



PIN DESCRIPTIONS

No.	Symbol	I/O	Pad Remarks	Pin Description
1	V_{DD}	—		Power supply 3.3 V
2	N.C.	—		Unused pin
3	N.C.	—		Unused pin
4	V_{SS}	—		Ground
5	SDA	I/O	Schmitt(IN)/ OpenDrain(OUT)	I^2C-bus data pin
6	SCL	I	Schmitt	I^2C-bus clock pin
7	SLA1	I	pull-down 50k	Slave address setting pin
8	SLA2	I	pull-down 50k	Slave address setting pin
9	YI7	I		Luminance signal input pin bit 7 (MSB)
10	YI6	I		Luminance signal input pin bit 6
11	YI5	I		Luminance signal input pin bit 5
12	YI4	I		Luminance signal input pin bit 4
13	YI3	I		Luminance signal input pin bit 3
14	YI2	I		Luminance signal input pin bit 2
15	YI1	I		Luminance signal input pin bit 1
16	YI0	I		Luminance signal input pin bit 0 (LSB)
17	V_{DD}	—		Power supply 3.3 V
18	ICLK	I		Input system clock pin
19	V_{SS}	—		Ground
20	CI7	I		Chrominance signal input pin bit 7 (MSB)
21	CI6	I		Chrominance signal input pin bit 6
22	CI5	I		Chrominance signal input pin bit 5
23	CI4	I		Chrominance signal input pin bit 4
24	CI3	I		Chrominance signal input pin bit 3
25	CI2	I		Chrominance signal input pin bit 2
26	CI1	I		Chrominance signal input pin bit 1
27	CI0	I		Chrominance signal input pin bit 0 (LSB)
28	N.C.	—		Unused pin
29	N.C.	—		Unused pin
30	V_{DD}	—		Power supply 3.3 V
31	V_{SS}	—		Ground
32	IVS	I/O	Schmitt(IN) pull-down 50k	Input vertical sync signal input/output pin
33	IHS	I/O	Schmitt(IN) pull-down 50k	Input horizontal sync signal input/output pin
34	MODE0	I	pull-down 50k	Mode setting pin – bit 0
35	MODE1	I	pull-down 50k	Mode setting pin – bit 1
36	N.C.	—		Unused pin
37	MODE2	I	pull-down 50k	Mode setting pin – bit 2
38	CLKO	O		Clock output (I^2C-bus control possible)
39	V_{DD}	—		Power supply 3.3 V
40	V_{SS}	—		Ground
41	N.C.	—		Unused pin

No.	Symbol	I/O	Pad Remarks	Pin Description
42	V_{DD}	—		Power supply 3.3 V
43	DNR	I	pull-down 50k	Noise reduction output mode setting pin 0: Normal operation 1: Direct noise reduction mode
44	N.C.	—		Unused pin
45	SSG	I	pull-down 50k	Internally generated sync signal mode setting pin
46	INT	I	pull-down 50k	Output system sync signal input/output select setting pin 0: OVS, OHS input mode 1: OVS, OHS internally generated output mode
47	OHS	I/O	Schmitt(IN) pull-down 50k	Output system horizontal sync signal input/output pin
48	OVS	I/O	Schmitt(IN) pull-down 50k	Output system vertical sync signal input/output pin
49	HREF	O		Data output horizontal reference signal output pin
50	V_{SS}	—		Ground
51	V_{DD}	—		Power supply 3.3 V
52	CO0	O		Chrominance signal output pin – bit 0 (LSB)
53	CO1	O		Chrominance signal output pin – bit 1
54	CO2	O		Chrominance signal output pin – bit 2
55	CO3	O		Chrominance signal output pin – bit 3
56	V_{SS}	—		Ground
57	CO4	O		Chrominance signal output pin – bit 4
58	CO5	O		Chrominance signal output pin – bit 5
59	CO6	O		Chrominance signal output pin – bit 6
60	CO7	O		Chrominance signal output pin – bit 7(MSB)
61	V_{DD}	—		Ground
62	OCLK	I		Output system clock pin
63	V_{SS}	—		Ground
64	YO0	O		Luminance signal output pin – bit 0 (LSB)
65	YO1	O		Luminance signal output pin – bit 1
66	YO2	O		Luminance signal output pin – bit 2
67	YO3	O		Luminance signal output pin – bit 3
68	VDD	—		Power supply 3.3 V
69	YO4	O		Luminance signal output pin – bit 4
70	YO5	O		Luminance signal output pin – bit 5
71	YO6	O		Luminance signal output pin – bit 6
72	YO7	O		Luminance signal output pin – bit 7 (MSB)
73	V_{SS}	—		Ground
74	N.C.	—		Unused pin
75	N.C.	—		Unused pin
76	N.C.	—		Unused pin
77	N.C.	—		Unused pin
78	N.C.	—		Unused pin
79	$\overline{\text{RESET}}$	I		System reset input pin (0 active) 0: System reset 1: Normal operation Apply ICLK cycle one and more time during “0” level after VDD voltage has reached the specified level in System reset operation.

No.	Symbol	I/O	Pad Remarks	Pin Description
80	V_{DD}	—		Power supply 3.3 V
81	V_{SS}	—		Ground
82	MTEST7	I	pull-down 50k	Memory test input pin – bit 7 (1: test mode)
83	MTEST6	I	pull-down 50k	Memory test input pin – bit 6 (1: test mode)
84	OE	I	pull-down 50k	Output enable input pin (normally set to 1) 0: YO[7:0], CO[7:0] disable (Hi-z) 1: YO[7:0], CO[7:0] enable (drive) Equivalent operation to setting fixed to 1 in RESET=0 or DNR=1
85	N.C.	—		Unused pin
86	N.C.	—		Unused pin
87	N.C.	—		Unused pin
88	N.C.	—		Unused pin
89	TEST5	I	pull-down 50k	Test input pin – bit 5 (1: test mode)
90	V_{DD}	—		Power supply 3.3 V
91	TEST4	I	pull-down 50k	Test input pin – bit 4 (1: test mode)
92	TEST3	I	pull-down 50k	Test input pin – bit 3 (1: test mode)
93	TEST2	I	pull-down 50k	Test input pin – bit 2 (1: test mode)
94	TEST1	I	pull-down 50k	Test input pin – bit 1 (1: test mode)
95	MTEST5	I	pull-down 50k	Memory test input pin – bit 5 (1: test mode)
96	MTEST4	I	pull-down 50k	Memory test input pin – bit 4 (1: test mode)
97	MTEST3	I	pull-down 50k	Memory test input pin – bit 3 (1: test mode)
98	MTEST2	I	pull-down 50k	Memory test input pin – bit 2 (1: test mode)
99	MTEST1	I	pull-down 50k	Memory test input pin – bit 1 (1: test mode)
100	V_{SS}	—		Ground

Notes: In 8-bit YcbCr and ITU-R BT. 656 mode, CI0-7 pin should be connected to the Vss level.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD}	Ta = 25°C	–0.3 to 4.6	V
Input pin voltage	V_I	Ta = 25°C	–0.3 to 7.0	V
Output pin short-circuit current	I_{OS}	Ta = 25°C	50	mA
Power dissipation	P_D	Ta = 25°C	1	W
Operating temperature	T_{opr}	—	0 to 70	°C
Storage temperature	T_{stg}	—	–50 to 150	°C

Recommended Operating Conditions

Parameter	Symbol	Min.	Typ.	Max.	Unit
Power supply voltage	V_{DD}	3.0	3.3	3.6	V
Power supply voltage	V_{SS}	0	0	0	V
Operating temperature	Ta	0	—	70	°C

Pin Capacitance

(V_{CC} = 3.3 V ± 0.3 V, f = 1 MHz, Ta = 25°C)

Parameter	Symbol	Min.	Max.	Unit
Input capacitance	C_i	—	10	pF
Input/output capacitance (IVS, IHS, OVS, OHS)	C_{io1}	—	10	pF
Input/output capacitance (SDA)	C_{io2}	—	10	pF
Output capacitance	C_o	—	10	pF

DC Characteristics

(Ta = 0 to 70°C)

Parameter	Symbol	Condition	Min.	Max.	Unit
H level input voltage	V_{IH}	—	2.0	5.5	V
L level input voltage	V_{IL}	—	–0.3	0.8	V
Schmitt trigger threshold voltage (SDA, SCL, IVS, IHS, OVS, OHS)	V_{t+}	—	—	2.0	V
Schmitt trigger threshold voltage (SDA, SCL, IVS, IHS, OVS, OHS)	V_{t-}	—	0.8	—	V
Hysteresis voltage width	V_h	—	0.1	—	V
H level input current (pull-down)	I_{IH}	50 kΩ Pull Down	20	200	μA
Input leakage current	I_{IL}	TTL	–10	10	μA
H level output voltage (other than SDA)	V_{OH}	I_{OH} = –4 mA	2.2	V_{DD}	V
L level output voltage (other than SDA)	V_{OL}	I_{OL} = 4 mA	0	0.4	V
L level output voltage (N-Ch.OD) (SDA)	V_{OOL}	I_{OL} = 4 mA	0	0.4	V
Output leakage current	I_{OL}	$0 \le V_{out} \le V_{DD}$ Output is disabled	–10	10	μA
Supply current (during operation)	I_{DD1}	ICLK: 36 MHz OCLK: 36 MHz Output open	—	100	mA
Supply current (during standby)	I_{DD2}	Input pin = V_{IL}	—	10	mA

AC Characteristics

(Ta = 0 to 70°C)

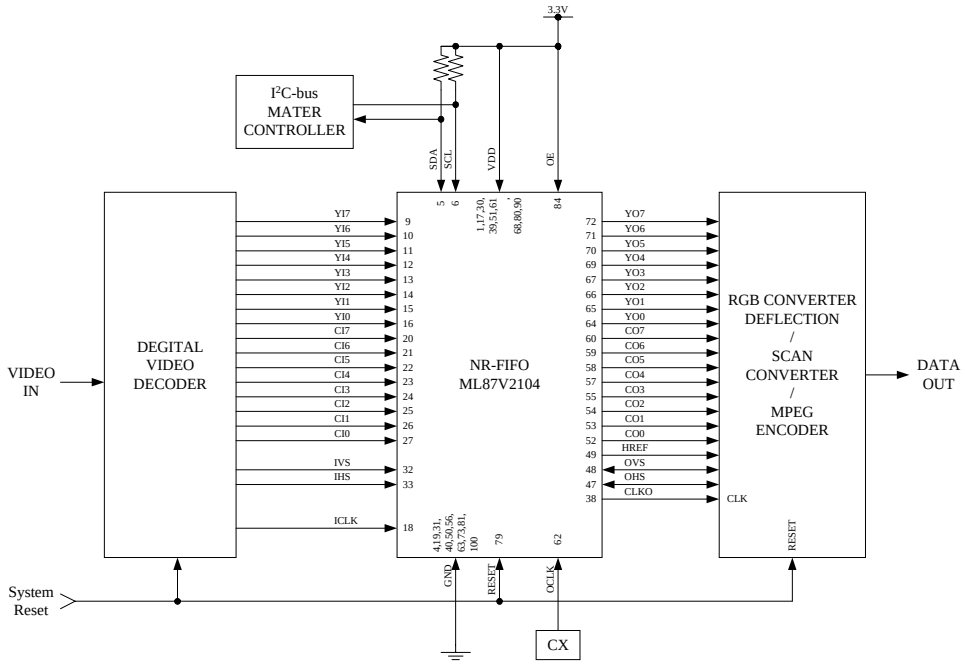
Parameter	Symbol	Condition	Min.	Max.	Unit
ICLK clock cycle time	t_{ICLK}	Input 16-bit mode	54	—	Ns
ICLK clock cycle time	t_{ICLK}	Input 8-bit mode	27	—	Ns
ICLK clock duty ratio	dt_{ICLK}	—	45	55	%
ICLK system input set-up time	t_{IISU}	—	5	—	ns
ICLK system input hold time	t_{IIH}	—	3	—	ns
ICLK system output delay time	t_{IOD}	C_L = 20 pF	5	22	ns
OCLK clock cycle time	t_{OCLK}	—	27	—	ns
OCLK clock duty ratio	dt_{OCLK}	—	45	55	%
OCLK system input set-up time	t_{OISU}	—	5	—	ns
OCLK system input hold time	t_{OIH}	—	3	—	ns
OCLK system output delay time	t_{OOD}	C_L = 20 pF	5	22	ns
CLKO delay time	t_{CKD}	C_L = 20 pF (OCLK output)	5	22	ns
		C_L = 20 pF (IICLK output)	6	25	
		C_L = 20 pF (ICLK output)	6	22	
Data through time	t_{DIDO}	C_L = 20 pF	3	20	ns

Notes: 1. Input signal reference levels for the parameter measurement are V_{IH} = 3.0 V and V_{IL} = 0 V.
Output reference levels are V_{OH} = 1.5 V and V_{OL} = 1.5 V.

Notes: 2. On power-up, the device is designed to begin proper operation after at least 100 μs after V_{CC} has stabilized to a value within the range of recommended operating conditions. After this 100 μs stabilization interval, a minimum of 1-field dummy write operations and read operations must be performed.

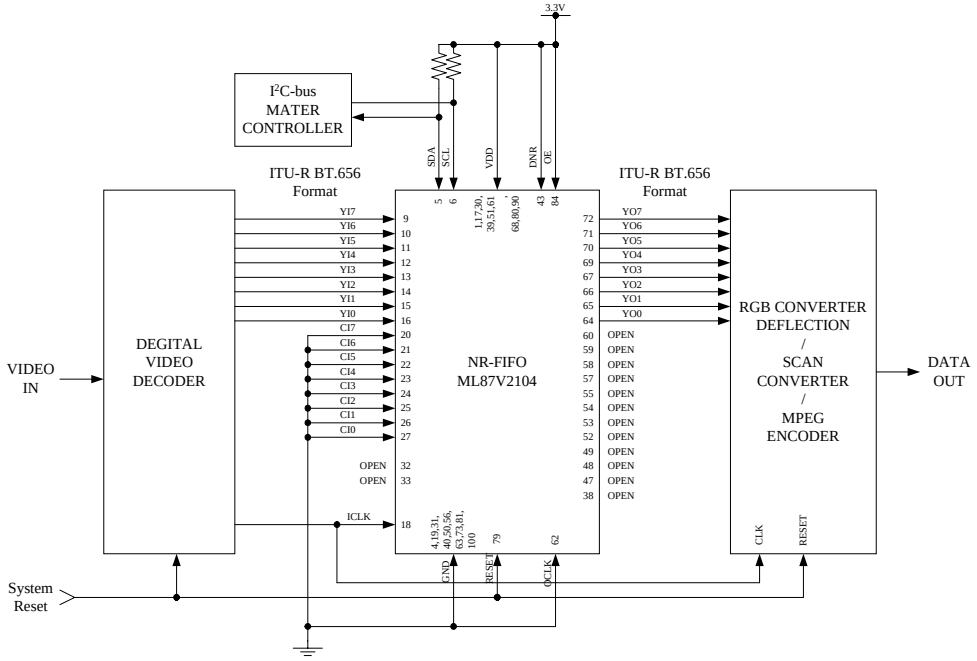
Application Example1

Mode setting: ALL Pin Open
Slave address: 1011100
Input format: 16bit YcbCr (Register setting: DISEL=0,R656=0)



Application Example2

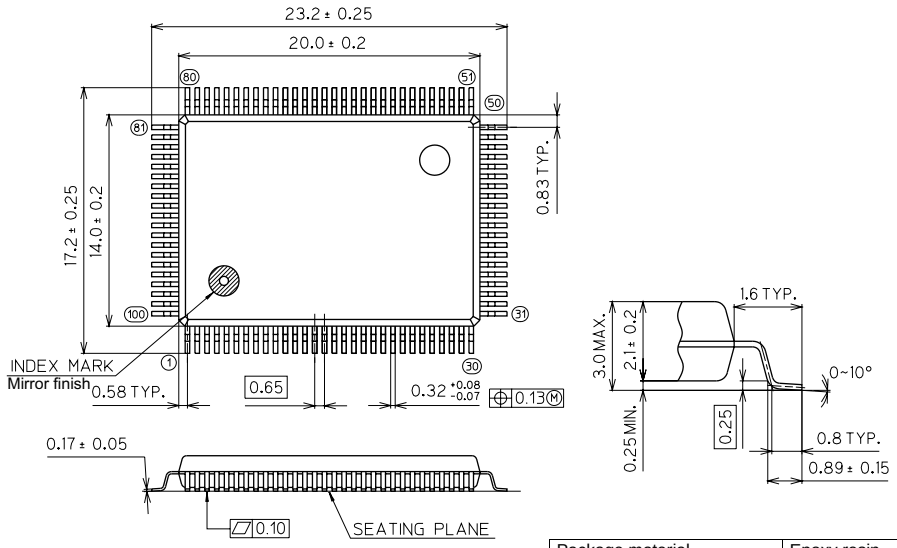
Mode setting: DNR=1(Direct Noise Reduction Mode), Others Pin:OPEN
Slave address: 1011100
Input format: ITU-R BT.656(Register setting: DISEL=0,R656=1)
Output format: ITU-R BT.656(Register setting: DOSEL=1)



PACKAGE DIMENSIONS

(Unit: mm)

QFP100-P-1420-0.65-BK4



Package material	Epoxy resin
Lead frame material	42 alloy
Pin treatment	Solder plating (≥5µm)
Package weight (g)	1.54 TYP.
Rev. No./Last Revised	4/Nov. 28, 1996

Oki Electric Industry Co., Ltd.

Notes for Mounting the Surface Mount Type Package

The QFP is a surface mount type package, which is very susceptible to heat in reflow mounting and humidity absorbed in storage. Therefore, before you perform reflow mounting, contact Oki's responsible sales person on the product name, package name, pin number, package code and desired mounting conditions (reflow method, temperature and times).

REVISION HISTORY

Document No.	Date	Page		Description
		Previous Edition	Current Edition	
PEDL87V2104DIGEST-01	Jan.20. 2003			Preliminary edition 1

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