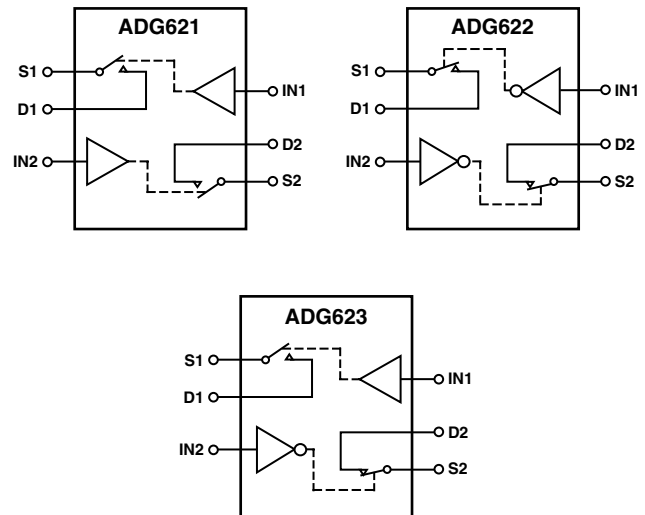


**ADG621/ADG622/ADG623**
**FEATURES**

**5.5  $\Omega$  (Max) On Resistance**  
**0.9  $\Omega$  (Max) On-Resistance Flatness**  
**2.7 V to 5.5 V Single Supply**  
 **$\pm 2.7$  V to  $\pm 5.5$  V Dual Supply**  
**Rail-to-Rail Operation**  
**10-Lead  $\mu$ SOIC Package**  
**Typical Power Consumption (<0.01  $\mu$ W)**  
**TTL/CMOS Compatible Inputs**

**APPLICATIONS**

**Automatic Test Equipment**  
**Power Routing**  
**Communication Systems**  
**Data Acquisition Systems**  
**Sample and Hold Systems**  
**Avionics**  
**Relay Replacement**  
**Battery-Powered Systems**

**FUNCTIONAL BLOCK DIAGRAM**

**SWITCHES SHOWN FOR A LOGIC "0" INPUT**
**GENERAL DESCRIPTION**

The ADG621, ADG622, and the ADG623 are monolithic, CMOS SPST (single-pole, single-throw) switches. Each switch of the ADG621, ADG622, and ADG623 conducts equally well in both directions when on.

The ADG621/ADG622/ADG623 contain two independent switches. The ADG621 and ADG622 differ only in that both switches are normally open and normally closed respectively. In the ADG623, Switch 1 is normally open and Switch 2 is normally closed. The ADG623 exhibits break-before-make switching action.

The ADG621/ADG622/ADG623 offers low on-resistance of 4  $\Omega$ , which is matched to within 0.25  $\Omega$  between channels. These switches also provide low power dissipation yet gives high switching speeds. The ADG621, ADG622, and ADG623 are available in a 10-lead  $\mu$ SOIC package.

**PRODUCT HIGHLIGHTS**

1. Low On Resistance ( $R_{ON}$ ) (4  $\Omega$  typ)
2. Dual  $\pm 2.7$  V to  $\pm 5.5$  V or Single 2.7 V to 5.5 V
3. Low Power Dissipation. CMOS construction ensures low power dissipation.
4. Tiny 10-Lead  $\mu$ SOIC Package

**REV. 0**

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# ADG621/ADG622/ADG623—SPECIFICATIONS

## DUAL SUPPLY<sup>1</sup> ( $V_{DD} = +5\text{ V} \pm 10\%$ , $V_{SS} = -5\text{ V} \pm 10\%$ , $GND = 0\text{ V}$ . All specifications $-40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>				
Analog Signal Range		$V_{SS}$ to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	4 5.5	7	$\Omega$ typ $\Omega$ max	$V_{DD} = +4.5\text{ V}$ , $V_{SS} = -4.5\text{ V}$ $V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$ , Test Circuit 1
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.25 0.35	0.4	$\Omega$ typ $\Omega$ max	$V_S = \pm 4.5\text{ V}$ , $I_S = -10\text{ mA}$
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	0.9	0.9 1.5	$\Omega$ typ $\Omega$ max	$V_S = \pm 3.3\text{ V}$ , $I_S = -10\text{ mA}$
<b>LEAKAGE CURRENTS</b>				
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$ $\pm 0.25$	$\pm 1$	nA typ nA max	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$ $V_S = \pm 4.5\text{ V}$ , $V_D = \mp 4.5\text{ V}$ , Test Circuit 2
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.01$ $\pm 0.25$	$\pm 1$	nA typ nA max	$V_S = \pm 4.5\text{ V}$ , $V_D = \mp 4.5\text{ V}$ , Test Circuit 2
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$ $\pm 0.25$	$\pm 1$	nA typ nA max	$V_S = V_D = \pm 4.5\text{ V}$ , Test Circuit 3
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005	$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
$C_{IN}$ , Digital Input Capacitance	2		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
$t_{ON}$	75 120	155	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3.3\text{ V}$ , Test Circuit 4
$t_{OFF}$	45 70	85	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3.3\text{ V}$ , Test Circuit 4
Break-Before-Make Time Delay, $t_{BBM}$ (ADG623 Only)	30	10	ns typ ns min	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_{S1} = V_{S2} = 3.3\text{ V}$ , Test Circuit 5
Charge Injection	110		pC typ	$V_S = 0\text{ V}$ , $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , Test Circuit 7
Off Isolation	-65		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , Test Circuit 8
Channel-to-Channel Crosstalk	-90		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , Test Circuit 10
Bandwidth -3 dB	230		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , Test Circuit 9
$C_S$ (OFF)	20		pF typ	$f = 1\text{ MHz}$
$C_D$ (OFF)	20		pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	70		pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.001	1.0	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = +5.5\text{ V}$ , $V_{SS} = -5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V
$I_{SS}$	0.001	1.0	$\mu\text{A}$ typ $\mu\text{A}$ max	Digital Inputs = 0 V or 5.5 V

### NOTES

<sup>1</sup>Temperature ranges are as follows: B Version,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

**SINGLE SUPPLY<sup>1</sup>** ( $V_{DD} = +5\text{ V} \pm 10\%$ ,  $V_{SS} = 0\text{ V}$ ,  $GND = 0\text{ V}$ . All specifications  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$  unless otherwise noted.)

Parameter	B Version		Unit	Test Conditions/Comments
	+25°C	-40°C to +85°C		
<b>ANALOG SWITCH</b>				
Analog Signal Range		0 V to $V_{DD}$	V	
On Resistance ( $R_{ON}$ )	7 10	12.5	$\Omega$ typ $\Omega$ max	$V_{DD} = 4.5\text{ V}$ , $V_{SS} = 0\text{ V}$ $V_S = 0\text{ V}$ to $4.5\text{ V}$ , $I_S = -10\text{ mA}$ , Test Circuit 1
On Resistance Match Between Channels ( $\Delta R_{ON}$ )	0.5 0.75	1	$\Omega$ typ $\Omega$ max	$V_S = 0\text{ V}$ to $4.5\text{ V}$ , $I_S = -10\text{ mA}$
On-Resistance Flatness ( $R_{FLAT(ON)}$ )	0.5	0.5 1	$\Omega$ typ $\Omega$ max	$V_S = 1.5\text{ V}$ to $3.3\text{ V}$ , $I_S = -10\text{ mA}$
<b>LEAKAGE CURRENTS</b>				
Source OFF Leakage $I_S$ (OFF)	$\pm 0.01$ $\pm 0.25$	$\pm 1$	nA typ nA max	$V_{DD} = 5.5\text{ V}$ $V_S = 1\text{ V}/4.5\text{ V}$ , $V_D = 4.5\text{ V}/1\text{ V}$ , Test Circuit 2
Drain OFF Leakage $I_D$ (OFF)	$\pm 0.01$ $\pm 0.25$	$\pm 1$	nA typ nA max	$V_S = 1\text{ V}/4.5\text{ V}$ , $V_D = 4.5\text{ V}/1\text{ V}$ , Test Circuit 2
Channel ON Leakage $I_D$ , $I_S$ (ON)	$\pm 0.01$ $\pm 0.25$	$\pm 1$	nA typ nA max	$V_S = V_D = 1\text{ V}/4.5\text{ V}$ , Test Circuit 3
<b>DIGITAL INPUTS</b>				
Input High Voltage, $V_{INH}$		2.4	V min	
Input Low Voltage, $V_{INL}$		0.8	V max	
Input Current $I_{INL}$ or $I_{INH}$	0.005	$\pm 0.1$	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{IN} = V_{INL}$ or $V_{INH}$
$C_{IN}$ , Digital Input Capacitance	2		pF typ	
<b>DYNAMIC CHARACTERISTICS<sup>2</sup></b>				
$t_{ON}$	120 210	260	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3.3\text{ V}$ , Test Circuit 4
$t_{OFF}$	50 75	100	ns typ ns max	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ $V_S = 3.3\text{ V}$ , Test Circuit 4
Break-Before-Make Time Delay, $t_{BBM}$ (ADG623 Only)	70	10	ns typ ns min	$R_L = 300\ \Omega$ , $C_L = 35\text{ pF}$ , $V_{S1} = V_{S2} = 3.3\text{ V}$ , Test Circuit 5
Charge Injection	6		pC typ	$V_S = 0\text{ V}$ ; $R_S = 0\ \Omega$ , $C_L = 1\text{ nF}$ , Test Circuit 6
Off Isolation	-65		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , Test Circuit 7
Channel-to-Channel Crosstalk	-90		dB typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , $f = 1\text{ MHz}$ , Test Circuit 9
Bandwidth -3 dB	230		MHz typ	$R_L = 50\ \Omega$ , $C_L = 5\text{ pF}$ , Test Circuit 8
$C_S$ (OFF)	20		pF typ	$f = 1\text{ MHz}$
$C_D$ (OFF)	20		pF typ	$f = 1\text{ MHz}$
$C_D$ , $C_S$ (ON)	70		pF typ	$f = 1\text{ MHz}$
<b>POWER REQUIREMENTS</b>				
$I_{DD}$	0.001	1.0	$\mu\text{A}$ typ $\mu\text{A}$ max	$V_{DD} = 5.5\text{ V}$ Digital Inputs = 0 V or 5.5 V

NOTES

<sup>1</sup>Temperature ranges are as follows: B Version,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

<sup>2</sup>Guaranteed by design, not subject to production test.

Specifications subject to change without notice.

# ADG621/ADG622/ADG623

## ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

(T<sub>A</sub> = +25°C unless otherwise noted)

V <sub>DD</sub> to V <sub>SS</sub> .....	13 V
V <sub>DD</sub> to GND .....	-0.3 V to +6.5 V
V <sub>SS</sub> to GND .....	+0.3 V to -6.5 V
Analog Inputs <sup>2</sup> .....	V <sub>SS</sub> - 0.3 V to V <sub>DD</sub> + 0.3 V
Digital Inputs <sup>2</sup> .....	-0.3 V to V <sub>DD</sub> + 0.3 V or 30 mA, Whichever Occurs First
Peak Current, S or D .....	100 mA (Pulsed at 1 ms, 10% Duty Cycle max)
Continuous Current, S or D .....	50 mA
Operating Temperature Range	
Industrial (B Version) .....	-40°C to +85°C
Storage Temperature Range .....	-65°C to +150°C
Junction Temperature .....	150°C
μSOIC Package	
θ <sub>JA</sub> Thermal Impedance .....	206°C/W
θ <sub>JC</sub> Thermal Impedance .....	44°C/W
Lead Temperature, Soldering (10 seconds) .....	300°C
IR Reflow, Peak Temperature .....	220°C

### NOTES

<sup>1</sup>Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

<sup>2</sup>Overvoltages at IN, S, or D will be clamped by internal diodes. Current should be limited to the maximum ratings given.

Table I. Truth Table for the ADG621/ADG622

ADG621 IN <sub>x</sub>	ADG622 IN <sub>x</sub>	Switch x Condition
0	1	OFF
1	0	ON

Table II. Truth Table for the ADG623

IN1	IN2	Switch S1	Switch S2
0	0	OFF	ON
0	1	OFF	OFF
1	0	ON	ON
1	1	ON	OFF

## ORDERING GUIDE

Model Option	Temperature Range	Description	Package	Branding Information*
ADG621BRM	-40°C to +85°C	μSOIC (microSmall Outline IC)	RM-10	SXB
ADG622BRM	-40°C to +85°C	μSOIC (microSmall Outline IC)	RM-10	SYB
ADG623BRM	-40°C to +85°C	μSOIC (microSmall Outline IC)	RM-10	SZB

\*Branding on μSOIC packages is limited to three characters due to space constraints.

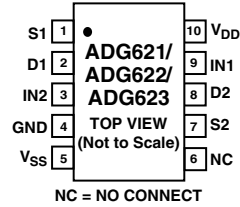
## CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADG621/ADG622/ADG623 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



## PIN CONFIGURATION

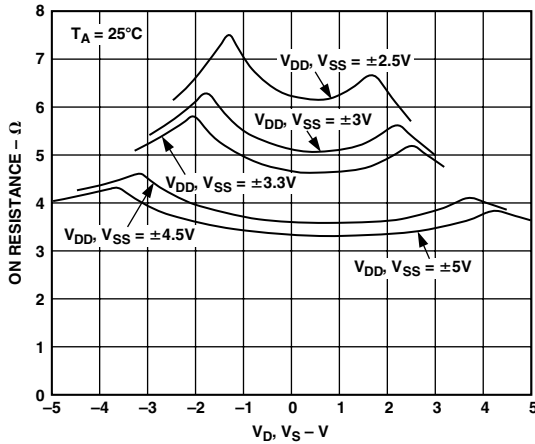
### 10-Lead $\mu$ SOIC (RM-10)



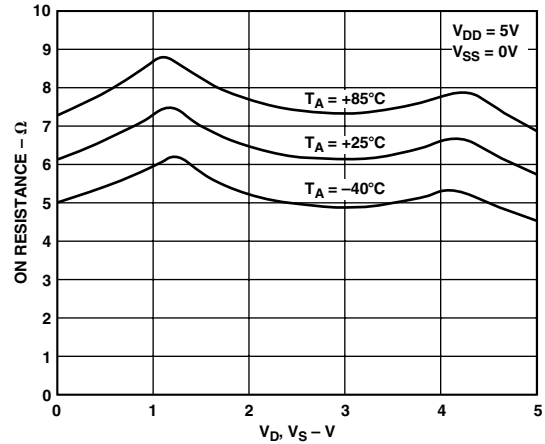
## TERMINOLOGY

$V_{DD}$	Most Positive Power Supply Potential.
$V_{SS}$	Most Negative Power Supply in a Dual Supply Application. In single supply applications, this should be tied to ground at the device.
GND	Ground (0 V) Reference
$I_{DD}$	Positive Supply Current
$I_{SS}$	Negative Supply Current
S	Source Terminal. May be an input or output.
D	Drain Terminal. May be an input or output.
IN	Logic Control Input
$R_{ON}$	Ohmic resistance between D and S.
$\Delta R_{ON}$	On resistance match between any two Channels i.e., $R_{ON\ max} - R_{ON\ min}$ .
$R_{FLAT(ON)}$	Flatness is defined as the difference between the maximum and minimum value of on resistance as measured over the specified analog signal range.
$I_S$ (OFF)	Source Leakage Current with the switch "OFF."
$I_D$ (OFF)	Drain Leakage Current with the switch "OFF."
$I_D, I_S$ (ON)	Channel Leakage Current with the switch "ON."
$V_D$ ( $V_S$ )	Analog Voltage on Terminals D, S.
$V_{INL}$	Maximum Input Voltage for Logic "0."
$V_{INH}$	Minimum Input Voltage for Logic "1."
$I_{INL}(I_{INH})$	Input Current of the Digital Input
$C_S$ (OFF)	"OFF" Switch Source Capacitance
$C_D$ (OFF)	"OFF" Switch Drain Capacitance
$C_D, C_S$ (ON)	"ON" Switch Capacitance
$t_{ON}$	Delay between applying the digital control input and the output switching on.
$t_{OFF}$	Delay between applying the digital control input and the output switching off.
$t_{BBM}$	"OFF" time or "ON" time measured between the 90% points of both switches, when switching from one address state to another.
Charge Injection	A measure of the Glitch Impulse transferred from the Digital input to the Analog output during switching.
Crosstalk	A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.
Off Isolation	A measure of unwanted signal coupling through an "OFF" switch.
Bandwidth	The frequency response of the "ON" switch.
Insertion Loss	The loss due to the ON resistance of the Switch.

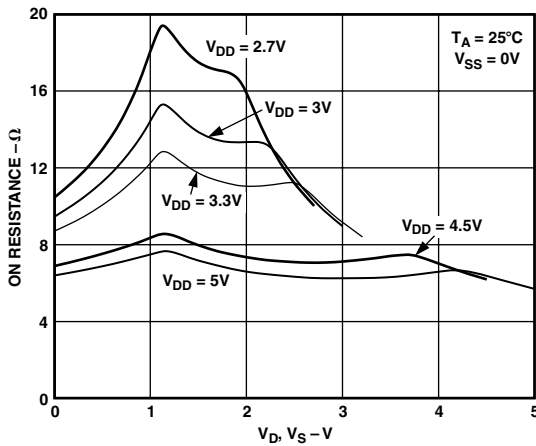
# ADG621/ADG622/ADG623—Typical Performance Characteristics



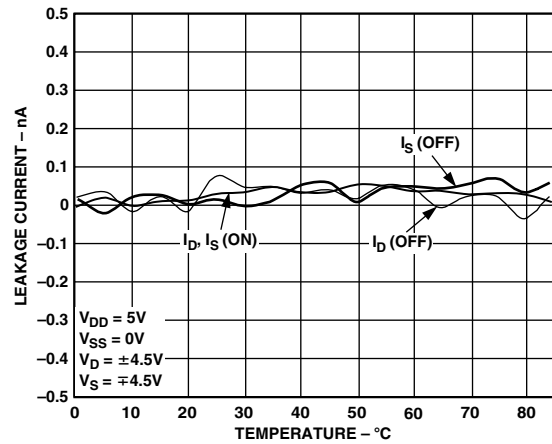
TPC 1. On Resistance vs.  $V_D$  ( $V_S$ ). (Dual Supply)



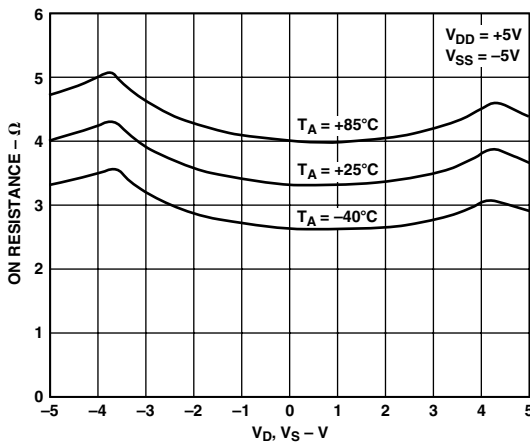
TPC 4. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperature. (Single Supply)



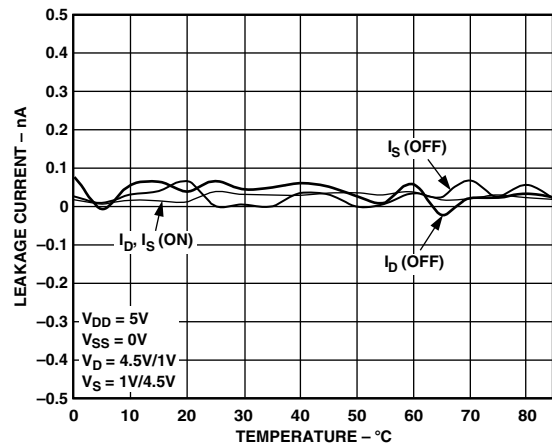
TPC 2. On Resistance vs.  $V_D$  ( $V_S$ ). (Single Supply)



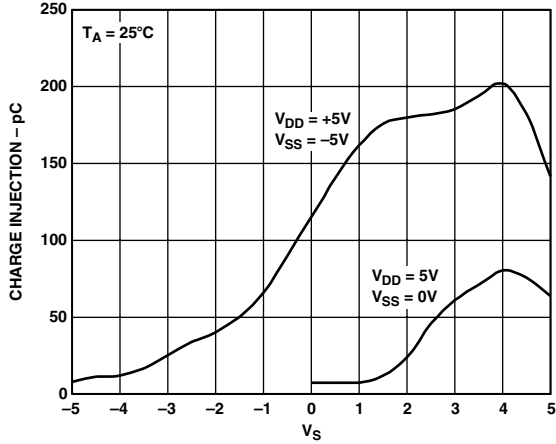
TPC 5. Leakage Currents vs. Temperature. (Dual Supply)



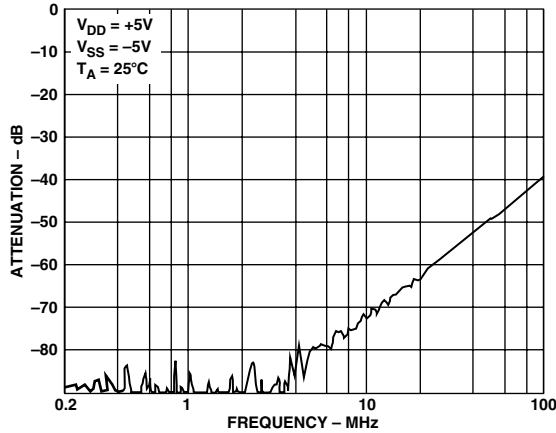
TPC 3. On Resistance vs.  $V_D$  ( $V_S$ ) for Different Temperatures. (Dual Supply)



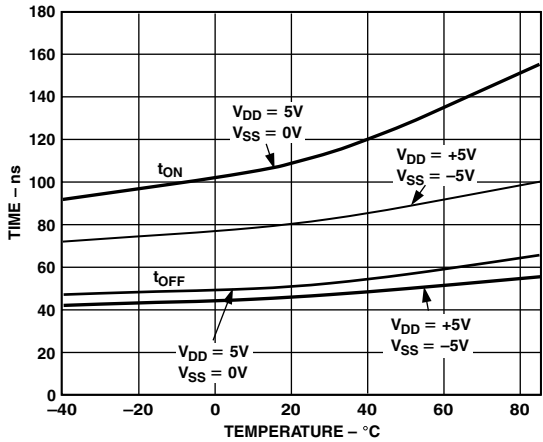
TPC 6. Leakage Currents vs. Temperature. (Single Supply)



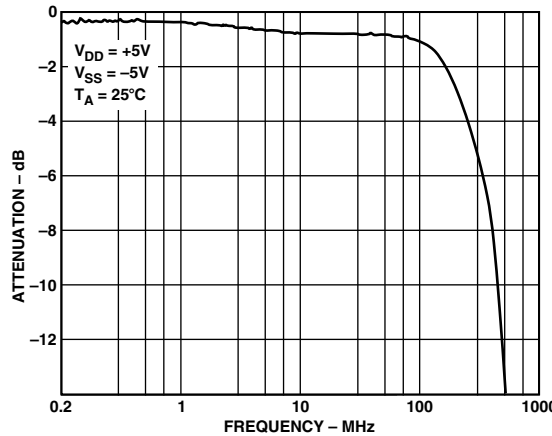
TPC 7. Charge Injection vs. Source Voltage



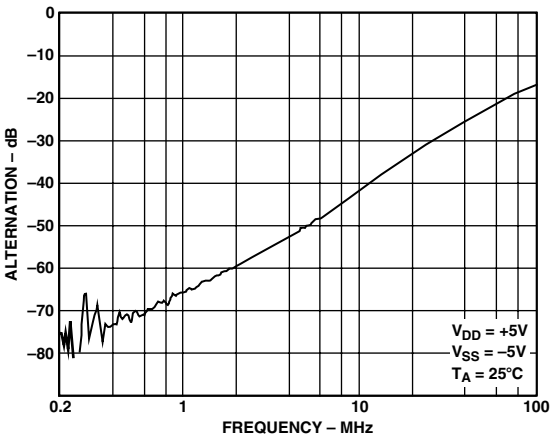
TPC 10. Crosstalk vs. Frequency



TPC 8.  $t_{ON}/t_{OFF}$  Times vs. Temperature



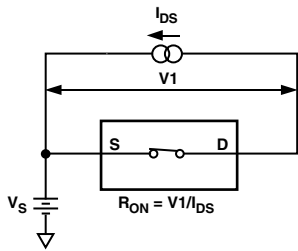
TPC 11. On Response vs. Frequency



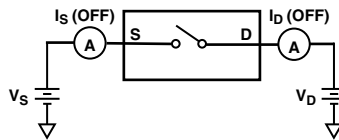
TPC 9. OFF Isolation vs. Frequency

# ADG621/ADG622/ADG623

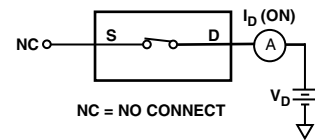
## Test Circuits



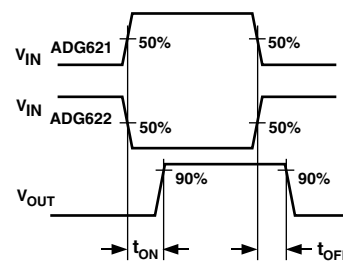
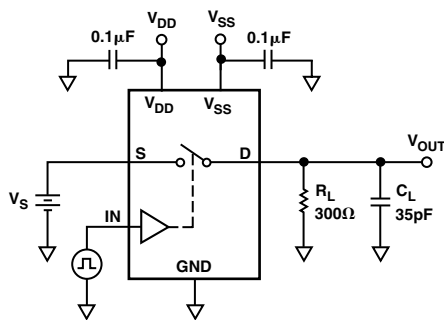
Test Circuit 1. On Resistance



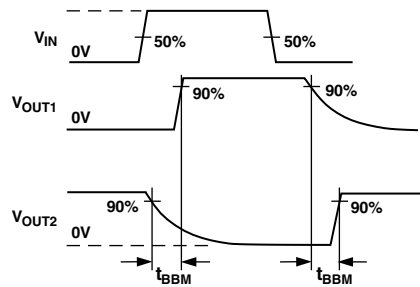
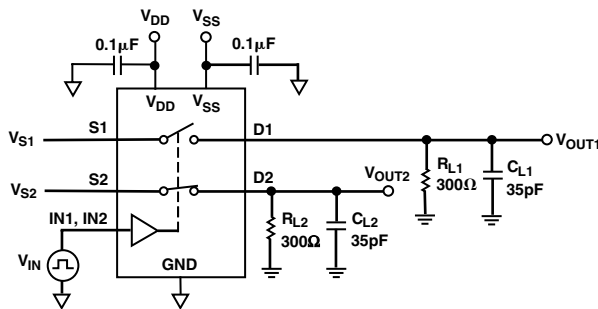
Test Circuit 2. Off Leakage



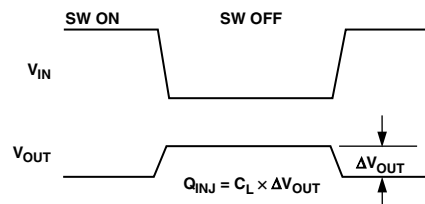
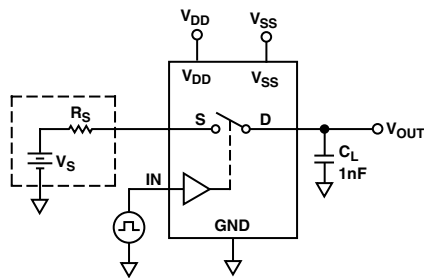
Test Circuit 3. On Leakage



Test Circuit 4. Switching Times

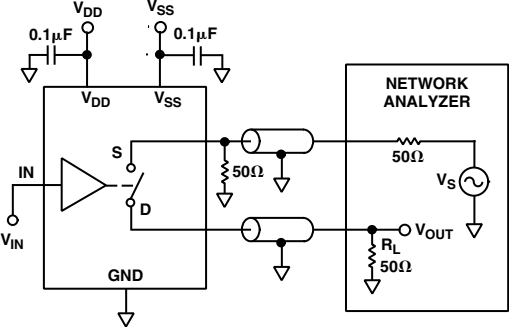


Test Circuit 5. Break-Before-Make Time Delay,  $t_{BBM}$  (ADG623 Only)



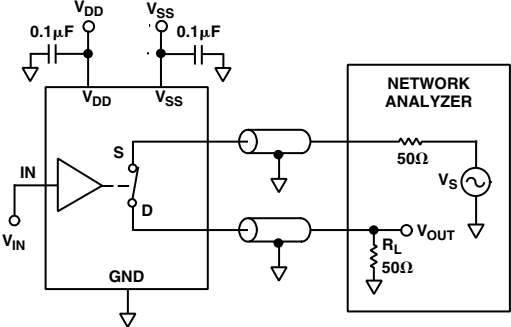
Test Circuit 6. Charge Injection





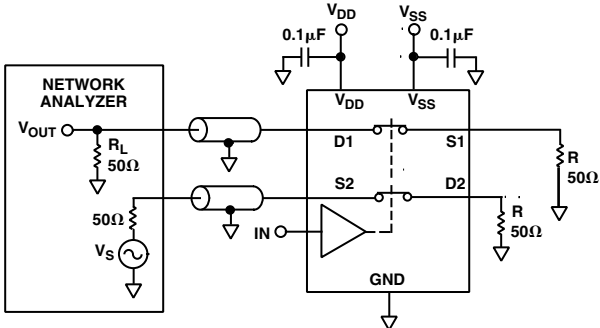
$$\text{OFF ISOLATION} = 20 \text{ LOG } \frac{V_{\text{OUT}}}{V_s}$$

Test Circuit 7. Off Isolation



$$\text{INSERTION LOSS} = 20 \text{ LOG } \frac{V_{\text{OUT WITH SWITCH}}}{V_{\text{OUT WITHOUT SWITCH}}}$$

Test Circuit 9. Bandwidth



$$\text{CHANNEL-TO-CHANNEL CROSSTALK} = 20 \text{ LOG } \frac{V_{\text{OUT}}}{V_s}$$

Test Circuit 8. Channel-to-Channel Crosstalk

# ADG621/ADG622/ADG623

## OUTLINE DIMENSIONS

Dimensions shown in inches and (mm).

### 10-Lead $\mu$ SOIC Package (RM-10)

