

H5N5006LD, H5N5006LS, H5N5006LM

Silicon N Channel MOS FET
High Speed Power Switching

HITACHI

ADE-208-1549 (Z)

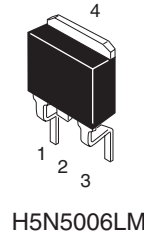
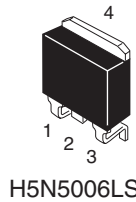
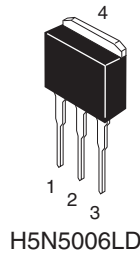
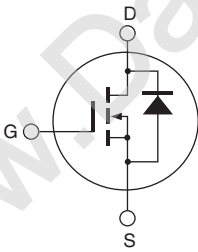
Rev.0
Aug.2002

Features

- Low on-resistance
- Low leakage current
- High speed switching
- Low gate charge
- Avalanche ratings

Outline

LDPAK



1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(T_a = 25°C)

Item	Symbol	Value	Unit
Drain to source voltage	V _{DSS}	500	V
Gate to source voltage	V _{GSS}	±30	V
Drain current	I _D	3.5	A
Drain peak current	I _D (pulse) ^{Note 1}	14	A
Body-drain diode reverse drain current	I _{DR}	3.5	A
Avalanche current	I _{AP} ^{Note 3}	3.5	A
Channel dissipation	P _{ch} ^{Note 2}	50	W
Channel to case thermal impedance	θ _{ch-c}	2.5	°C/W
Channel temperature	T _{ch}	150	°C
Storage temperature	T _{stg}	-55 to +150	°C

- Notes: 1. PW ≤ 10 μs, duty cycle ≤ 1%
2. Value at T_c = 25°C
3. T_{ch} ≤ 150°C

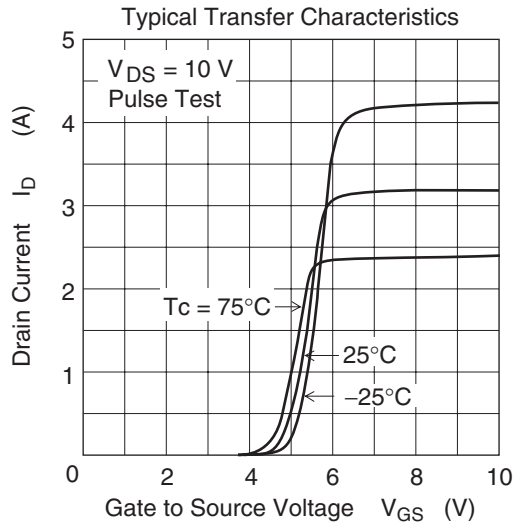
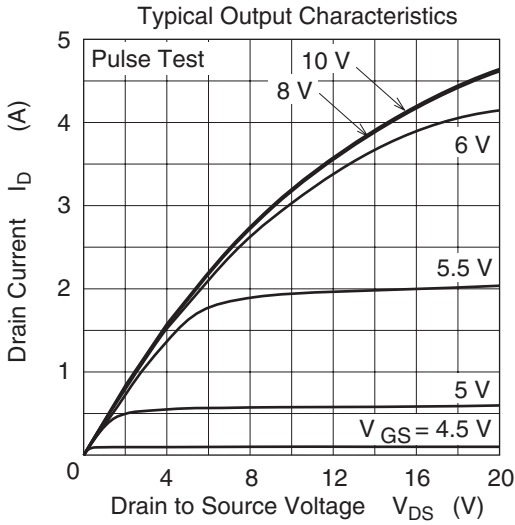
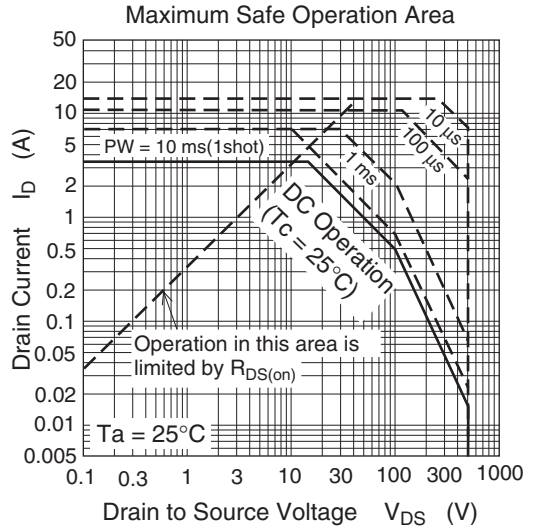
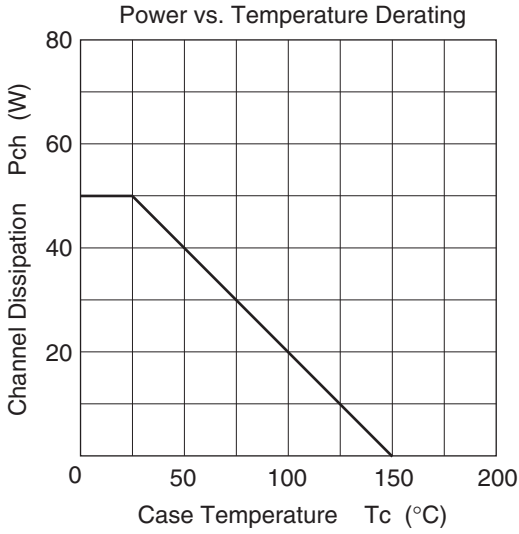
Electrical Characteristics

(Ta = 25°C)

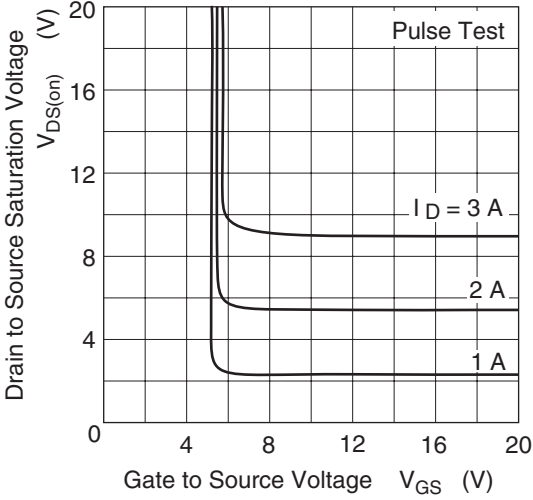
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	500	—	—	V	$I_D = 10 \text{ mA}, V_{GS} = 0$
Gate to source leak current	I_{DSS}	—	—	1	μA	$V_{DS} = 500 \text{ V}, V_{GS} = 0$
Zero gate voltage drain current	I_{GSS}	—	—	± 0.1	μA	$V_{GS} = \pm 30 \text{ V}, V_{DS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	3.0	—	4.5	V	$V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA}$
Forward transfer admittance	$ y_{fs} $	1.8	3.0	—	S	$I_D = 1.75 \text{ A}, V_{DS} = 10 \text{ V}$ ^{Note 4}
Static drain to source on state resistance	$R_{DS(on)}$	—	2.5	3.0	Ω	$I_D = 1.75 \text{ A}, V_{GS} = 10 \text{ V}$ ^{Note 4}
Input capacitance	Ciss	—	365	—	pF	$V_{DS} = 25 \text{ V}$
Output capacitance	Coss	—	35	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	8	—	pF	$f = 1 \text{ MHz}$
Turn-on delay time	td(on)	—	20	—	ns	$V_{DD} \cong 250 \text{ V}, I_D = 1.75 \text{ A}$
Rise time	tr	—	13	—	ns	$V_{GS} = 10 \text{ V}$
Turn-off delay time	td(off)	—	48	—	ns	$R_L = 143 \Omega$
Fall time	tf	—	14	—	ns	$R_g = 10 \Omega$
Total gate charge	Qg	—	14	—	nC	$V_{DD} = 400 \text{ V}$
Gate to source charge	Qgs	—	2	—	nC	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Qgd	—	8	—	nC	$I_D = 3.5 \text{ A}$
Body-drain diode forward voltage	V_{DF}	—	0.85	1.3	V	$I_F = 3.5 \text{ A}, V_{GS} = 0$
Body-drain diode reverse recovery time	trr	—	280	—	ns	$I_F = 3.5 \text{ A}, V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$
Body-drain diode reverse recovery charge	Qrr	—	0.8	—	μC	

Notes: 4. Pulse test

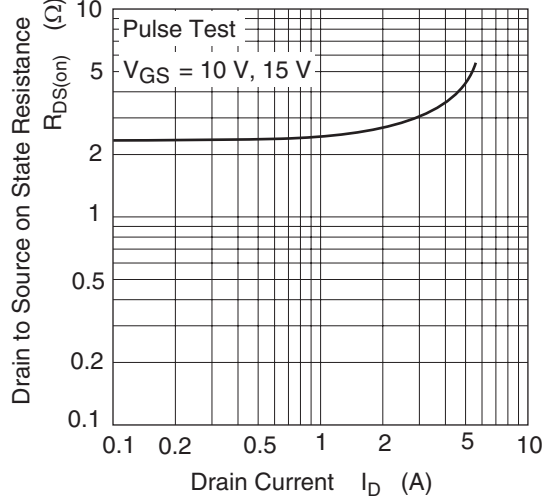
Main Characteristics



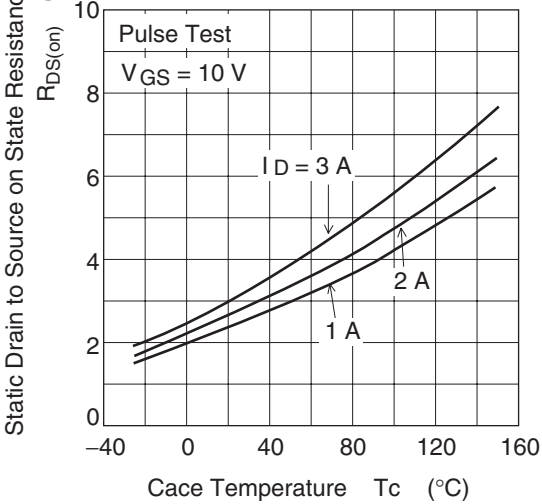
Drain to Source Saturation Voltage vs. Gate to Source Voltage



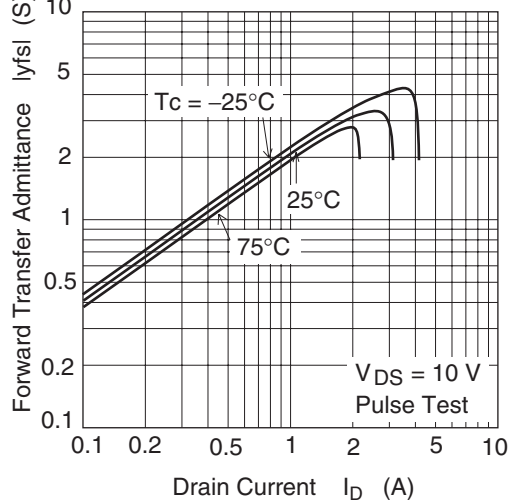
Static Drain to Source on State Resistance vs. Drain Current



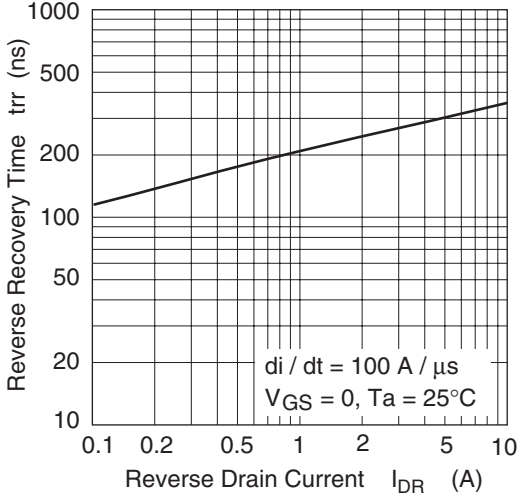
Static Drain to Source on State Resistance VS. Temperature



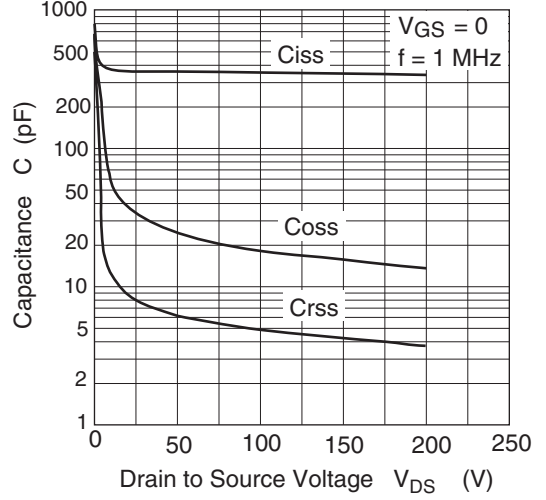
Forward Transfer Admittance vs. Drain Current



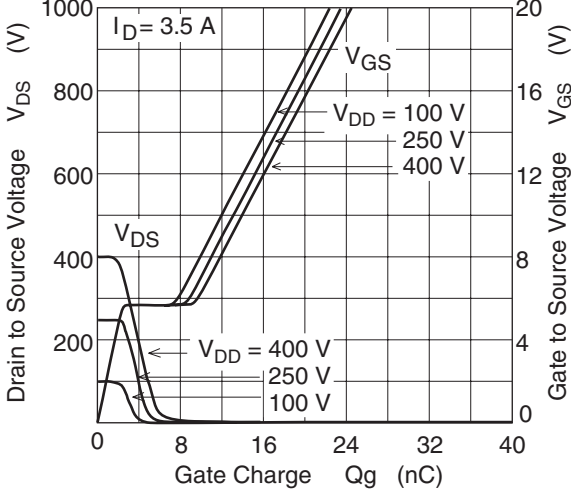
Body-Drain Diode Reverse Recovery Time



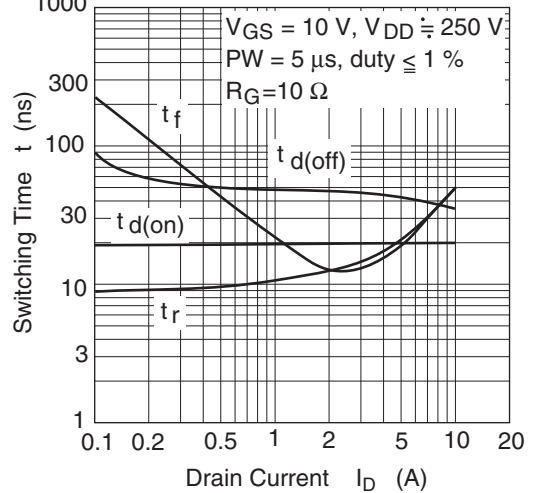
Typical Capacitance vs. Drain to Source Voltage



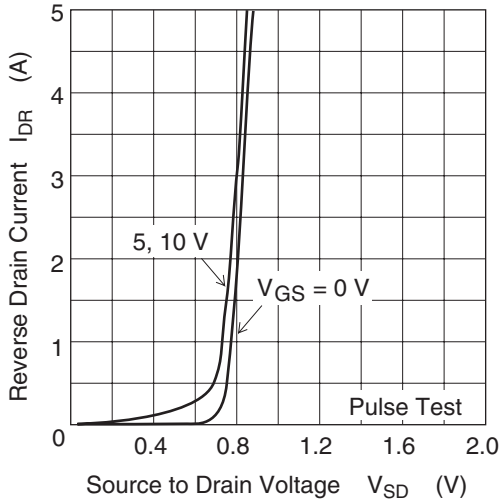
Dynamic Input Characteristics



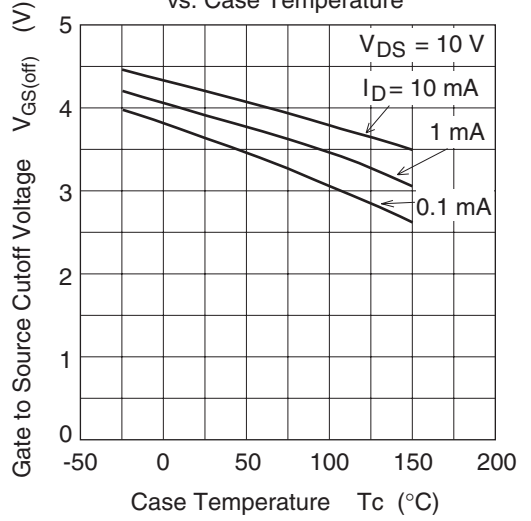
Switching Characteristics



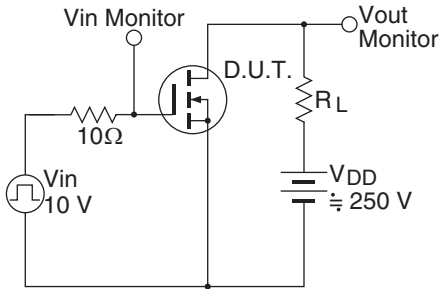
Reverse Drain Current vs. Source to Drain Voltage



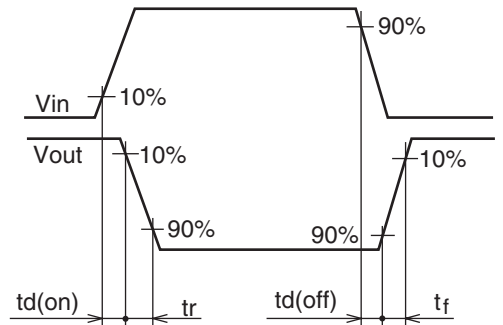
Gate to Source Cutoff Voltage vs. Case Temperature



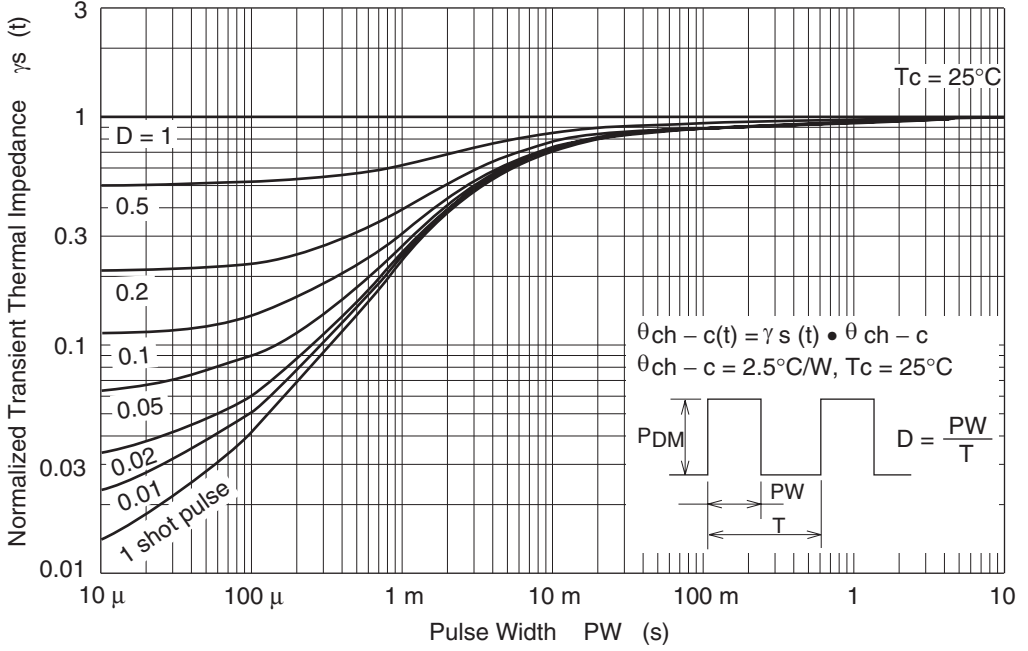
Switching Time Test Circuit



Waveform



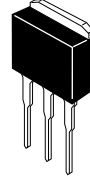
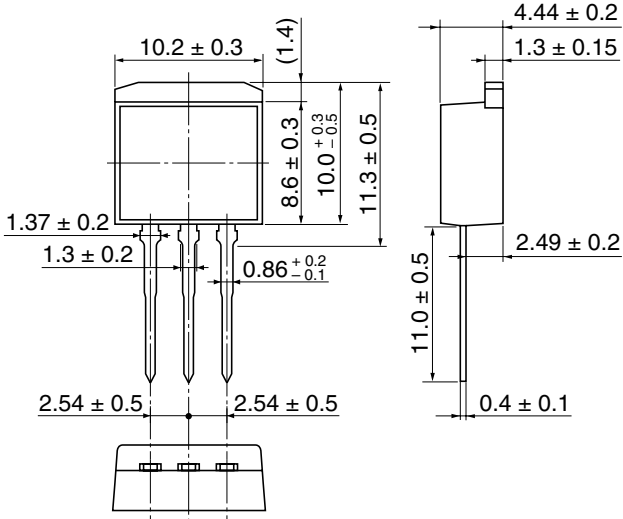
Normalized Transient Thermal Impedance vs. Pulse Width



Package Dimensions

• H5N5006LD

Unit: mm

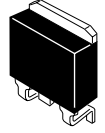
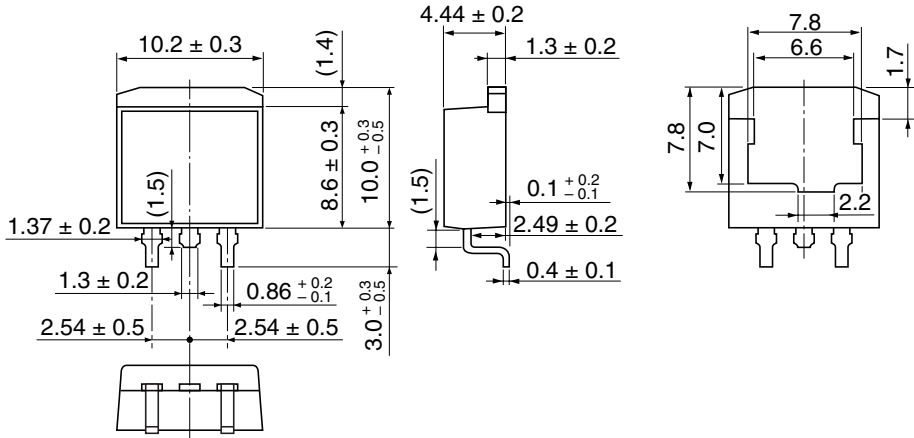


Hitachi Code	LDBAK (L)
JEDEC	—
JEITA	—
Mass (reference value)	1.4 g

H5N5006LD, H5N5006LS, H5N5006LM

• H5N5006LS

Unit: mm

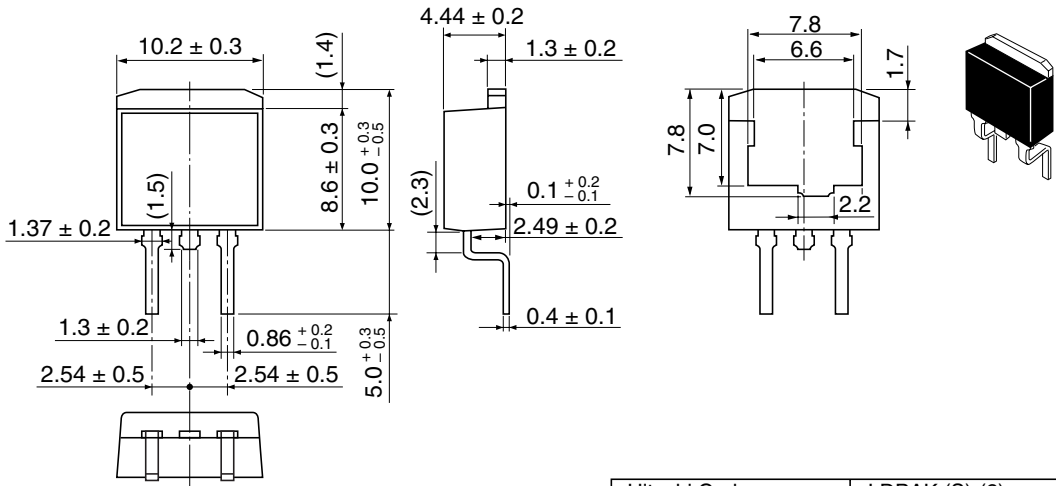


Hitachi Code	LDBPAK (S)-(1)
JEDEC	—
JEITA	—
Mass (reference value)	1.3 g

H5N5006LD, H5N5006LS, H5N5006LM

• H5N5006LM

Unit: mm



Hitachi Code	LDBPAK (S)-(2)
JEDEC	—
JEITA	—
Mass (reference value)	1.35 g

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