

# FAN7528

## Dual Output Critical Conduction Mode PFC Controller

### Features

- Low Total Harmonic Distortion (THD)
- Dual Output Voltage Control
- Precise Adjustable Output Over Voltage Protection
- Open-feedback Protection and Disable Function
- Zero Current Detector
- 160us Internal Start-up Timer
- MOSFET Over Current Protection
- Under Voltage Lock Out with 3.5V Hysteresis
- Low Start-up (40uA) and Operating Current (1.5mA)
- Totem Pole Output with High State Clamp
- ±400mA Peak Gate Drive Current
- 8-pin DIP or 8-pin SOP

### Applications

- Adapter

### Related Application Notes

- **AN6012** - Design of Power Factor Correction Circuit Using FAN7528

### Description

The FAN7528 is an active power factor correction (PFC) controller for boost PFC applications which operates in the critical conduction mode (CRM). It uses the voltage mode PWM that compares an internal ramp signal with the error amplifier output to generate MOSFET turn-off signal. Because the voltage mode CRM PFC controller does not need the rectified AC line voltage information, it can save the power loss of the input voltage sensing network that is necessary for the current mode CRM PFC controller.

The FAN7528 provides the dual output voltage control function without the AC line voltage sensing for adapter applications. It changes the PFC output voltage according to the AC line voltage.

It provides many protection functions such as over voltage protection, open-feedback protection, over current protection and under voltage lock out protection. The FAN7528 can be disabled if the INV pin voltage is lower than 0.45V and then the operating current decreases to 65uA. Using a new variable on-time control method, THD is lower than the conventional CRM boost PFC ICs.

### Ordering Information

Part Number	Operating Temp. Range	Pb-Free	Package	Packing Method	Marking Code
FAN7528N	-40°C to +125°C	Yes	8-DIP	Rail	FAN7528
FAN7528M	-40°C to +125°C	Yes	8-SOP	Rail	FAN7528
FAN7528MX	-40°C to +125°C	Yes	8-SOP	Tape & Reel	FAN7528



## Pin Assignments

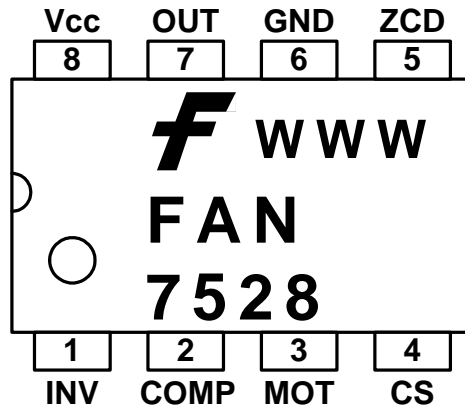


Figure 3. Pin Configuration (Top View)

## Pin Definitions

Pin Number	Pin Name	Pin Function Description
1	INV	This pin is the inverting input of the error amplifier. The output voltage of the boost PFC converter should be resistively divided to 2.5V at the high line condition and connected to this pin. If this pin voltage is controlled to be lower than 0.45V, the device is disabled.
2	COMP	This pin is the output of the transconductance error amplifier. Some components for the output voltage compensation should be connected between this pin and GND.
3	MOT	This pin is used to set the slope of the internal ramp. The voltage of this pin is maintained to be 1V. If a resistor is connected between this pin and GND, current flows out of the pin and the slope of the internal ramp is proportional to this current.
4	CS	This pin is the input of the over current protection comparator. The MOSFET current is sensed using a sensing resistor and the resulting voltage is applied to this pin. An internal RC filter is included to filter switching noise. This pin is sensitive to the negative voltage below -0.3V. For proper operation, the stray inductance in the sensing path and the inductance of the sensing resistor must be minimized.
5	ZCD	This pin is the input of the zero current detection block. If the voltage of this pin goes higher than 1.5V and then goes lower than 1.4V, the MOSFET is turned on.
6	GND	This pin is used for the ground potential of all the pins. For proper operation, the signal ground and the power ground should be separated.
7	OUT	This pin is the gate drive output. The peak sourcing and sinking current level is 400mA. For proper operation, the stray inductance in the gate driving path must be minimized.
8	Vcc	This pin is the IC supply pin. IC current and MOSFET drive current are supplied using this pin.

## Absolute Maximum Ratings

(Ta=25°C, unless otherwise specified)

Parameter	Symbol	Value	Unit
Supply Voltage	Vcc	23	V
Peak Drive Output Current	I <sub>OH</sub> , I <sub>OL</sub>	±400	mA
Driver Output Clamping Diodes Vo>Vcc or Vo<-0.3V	Iclamp	±10	mA
Detector Clamping Diodes	I <sub>det</sub>	±10	mA
Error Amp, MOT, CS Input Voltages	Vin	-0.3 to 6	V
Operating Junction Temperature	Tj	150	°C
Operating Temperature Range	T <sub>opr</sub>	-40 to 125	°C
Storage Temperature Range	T <sub>stg</sub>	-65 to 150	°C
ESD Capability, HBM Model (All pins except Vcc)	-	2.0	kV
ESD Capability, Machine Model	-	300	V

## Thermal Impedance

Parameter		Symbol	Value	Unit
Thermal Resistance, Junction to Ambient	8-DIP	R <sub>θja</sub>	110	°C/W
	8-SOP		150	°C/W

### Note:

- Regarding the test environment and PCB type, please refer to JESD51-2 and JESD51-10.

**Electrical Characteristics**(V<sub>CC</sub> = 14V, T<sub>a</sub> = -40°C~125°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>UNDER VOLTAGE LOCK OUT SECTION</b>						
Start Threshold Voltage	V <sub>th(start)</sub>	V <sub>CC</sub> increasing	11	12	13	V
Stop Threshold Voltage	V <sub>th(stop)</sub>	V <sub>CC</sub> decreasing	8	8.5	9	V
UVLO Hysteresis	HY(uvlo)	-	3	3.5	4	V
<b>SUPPLY CURRENT SECTION</b>						
Start-up Supply Current	I <sub>st</sub>	V <sub>CC</sub> = V <sub>th(start)</sub> - 0.2V	-	40	70	μA
Operating Supply Current	I <sub>CC</sub>	Output no switching	-	1.5	3	mA
Dynamic Operating Supply Current	I <sub>dCC</sub>	50kHz, C <sub>I</sub> =1nF	-	2.5	4	mA
Operating Current at Disable	I <sub>CC(dis)</sub>	V <sub>inv</sub> = 0V	40	65	90	μA
<b>ERROR AMPLIFIER SECTION</b>						
Voltage Feedback Input Threshold1	V <sub>ref1</sub>	T <sub>a</sub> = 25°C	2.465	2.5	2.535	V
		-	2.435	2.5	2.565	V
Voltage Feedback Input Threshold2	V <sub>ref2</sub>	-	1.45	1.5	1.55	V
Line Regulation	ΔV <sub>ref1</sub>	V <sub>CC</sub> = 14V ~ 23V	-	0.1	10	mV
Temperature Stability of V <sub>ref1</sub> <sup>(1)</sup>	ΔV <sub>ref3</sub>	-	-	20	-	mV
Input Bias Current	I <sub>b(ea)</sub>	V <sub>inv</sub> = 1V ~ 4V	-0.5	-	0.5	μA
Output Source Current	I <sub>source</sub>	V <sub>inv</sub> = 2.4V	-	-12	-	μA
Output Sink Current	I <sub>sink</sub>	V <sub>inv</sub> = 2.6V	-	12	-	μA
Output Upper Clamp Voltage	V <sub>ea0(H)</sub>	-	4.5	5.5	6.5	V
Zero Duty Cycle Output Voltage	V <sub>ea0(Z)</sub>	-	0.7	1	1.3	V
Transconductance <sup>(1)</sup>	g <sub>m</sub>	-	90	115	140	μmho
Output Voltage Selection Threshold	V <sub>th(in)</sub>	T <sub>a</sub> = 25°C	1.24	1.3	1.36	V
Output Voltage Reset Threshold <sup>(1)</sup>	V <sub>th(reset)</sub>	-	3	4.5	6	V
<b>MAXIMUM ON-TIME SECTION</b>						
Maximum On-time Voltage	V <sub>mot</sub>	R <sub>mot</sub> = 13.7k	0.95	1	1.05	V
Maximum On-time Programming	T <sub>on-max</sub>	R <sub>mot</sub> = 13.7k, T <sub>a</sub> = 25°C	18	22.5	27	μA
<b>CURRENT SENSE SECTION</b>						
Current Sense Input Threshold Voltage Limit	V <sub>cs(limit)</sub>	-	0.7	0.8	0.9	V
Input Bias Current	I <sub>b(cs)</sub>	V <sub>cs</sub> = 0V ~ 1V	-1	-0.1	1	μA
Current Sense Delay to Output <sup>(1)</sup>	T <sub>d(cs)</sub>	-	-	350	500	ns

**Electrical Characteristics (Continued)**(V<sub>CC</sub> = 14V, T<sub>a</sub> = -40°C~125°C, unless otherwise specified)

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
<b>ZERO CURRENT DETECT SECTION</b>						
Input Voltage Threshold <sup>(1)</sup>	V <sub>th(zcd)</sub>	-	1.35	1.5	1.65	V
Detect Hysteresis <sup>(1)</sup>	HY <sub>(zcd)</sub>	-	0.05	0.1	0.15	V
Input High Clamp Voltage	V <sub>clamp(h)</sub>	I <sub>det</sub> = 3mA	6	6.7	7.4	V
Input Low Clamp Voltage	V <sub>clamp(l)</sub>	I <sub>det</sub> = -3mA	0	0.6	1	V
Input Bias Current	I <sub>b(zcd)</sub>	V <sub>ZCD</sub> = 1V ~ 5V	-1	-0.1	1	μA
Source Current Capability <sup>(1)</sup>	I <sub>source(zcd)</sub>	-	-	-	-10	mA
Sink Current Capability <sup>(1)</sup>	I <sub>sink(zcd)</sub>	-	-	-	10	mA
Maximum Delay from ZCD to Output Turn-on <sup>(1)</sup>	T <sub>dead</sub>	-	100	-	200	ns
<b>OUTPUT SECTION</b>						
Output Voltage High	V <sub>oh</sub>	I <sub>o</sub> = -100mA	9.2	11	12.8	V
Output Voltage Low	V <sub>ol</sub>	I <sub>o</sub> = 100mA	-	1	2.5	V
Rising Time <sup>(1)</sup>	T <sub>r</sub>	C <sub>l</sub> = 1nF	-	50	100	ns
Falling Time <sup>(1)</sup>	T <sub>f</sub>	C <sub>l</sub> = 1nF	-	50	100	ns
Maximum Output Voltage	V <sub>o(max)</sub>	V <sub>CC</sub> = 20V, I <sub>o</sub> = 100μA	11.5	13	14.5	V
Output Voltage with UVLO Activated	V <sub>o(uvlo)</sub>	V <sub>CC</sub> = 5V, I <sub>o</sub> = 100μA	-	-	1	V
<b>RESTART TIMER SECTION</b>						
Restart Timer Delay	t <sub>d(rst)</sub>	-	40	160	360	μs
<b>OVER VOLTAGE PROTECTION SECTION</b>						
OVP Threshold Voltage	V <sub>ovp</sub>	T <sub>a</sub> = 25°C	2.6	2.66	2.72	V
OVP Hysteresis	HY <sub>(ovp)</sub>	-	0.06	0.11	0.16	V
<b>ENABLE SECTION</b>						
Enable Threshold Voltage	V <sub>th(en)</sub>	-	0.4	0.45	0.5	V
Enable Hysteresis	HY <sub>(en)</sub>	-	0.05	0.1	0.15	V

**Note:**

1. These parameters, although guaranteed by design, are not tested in mass production.

## Typical Performance Characteristics

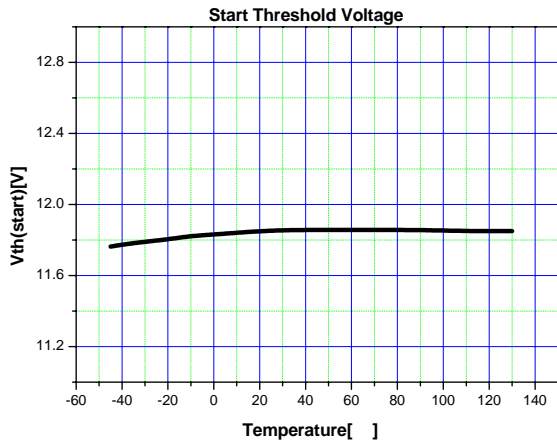


Figure 4. Start Threshold Voltage vs. Temp.

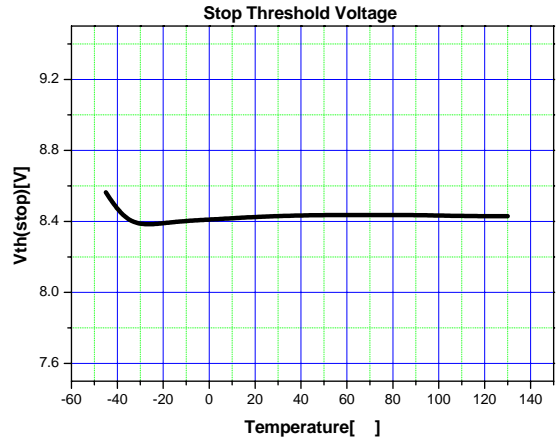


Figure 5. Stop Threshold Voltage vs. Temp.

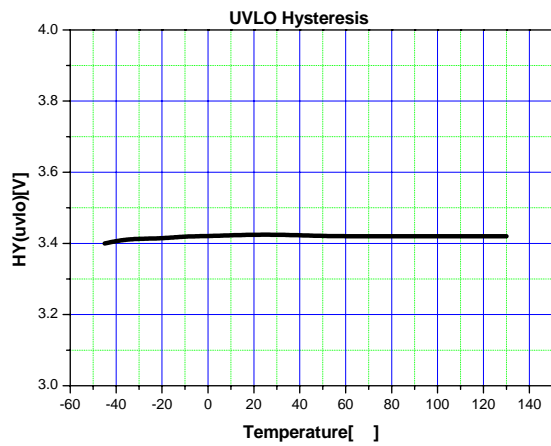


Figure 6. UVLO Hysteresis vs. Temp.

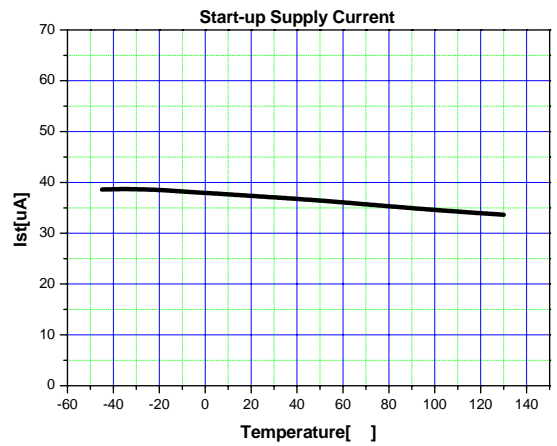


Figure 7. Start-up Supply Current vs. Temp.

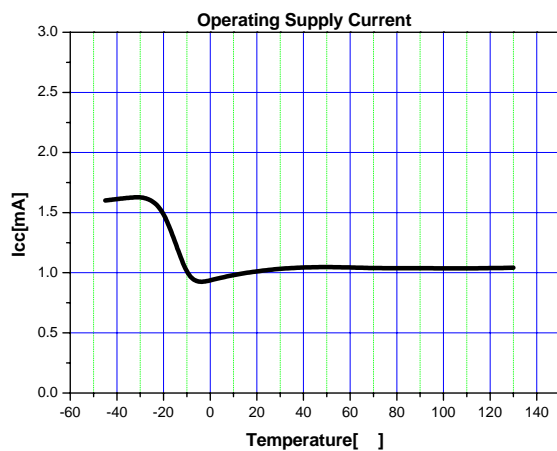


Figure 8. Operating Supply Current vs. Temp.

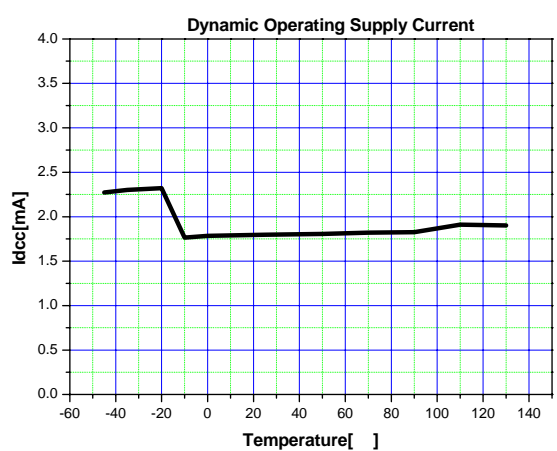


Figure 9. Dynamic Operating Current vs. Temp.

## Typical Performance Characteristics (Continued)

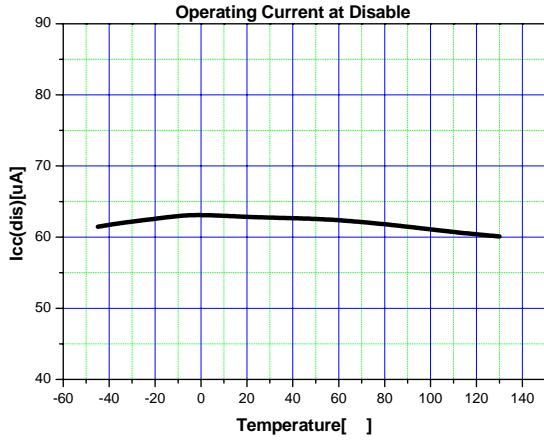


Figure 10. I<sub>cc</sub> at Disable vs. Temp.

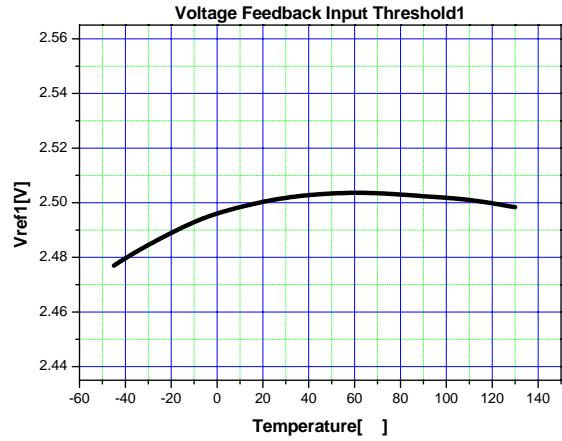


Figure 11. V<sub>ref1</sub> vs. Temp.

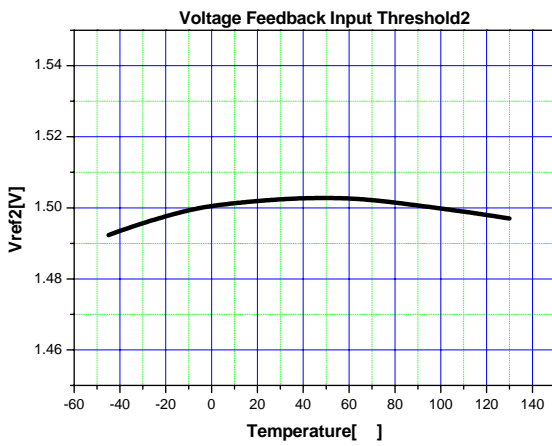


Figure 12. V<sub>ref2</sub> vs. Temp.

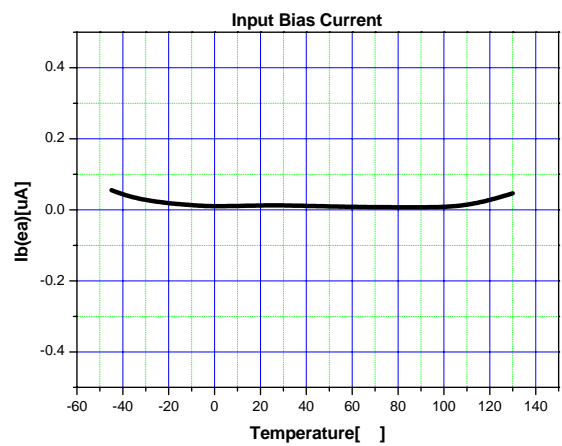


Figure 13. Input Bias Current vs. Temp.

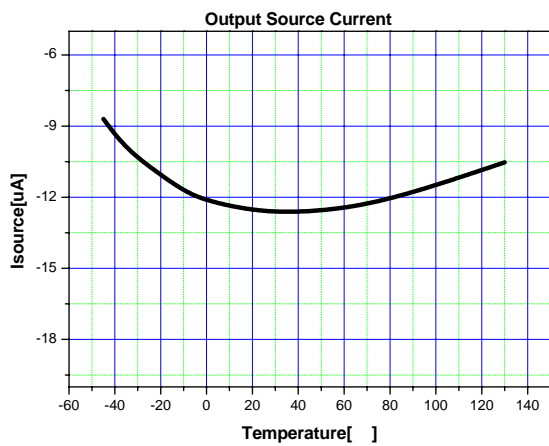


Figure 14. Error Amp. Source Current vs. Temp.

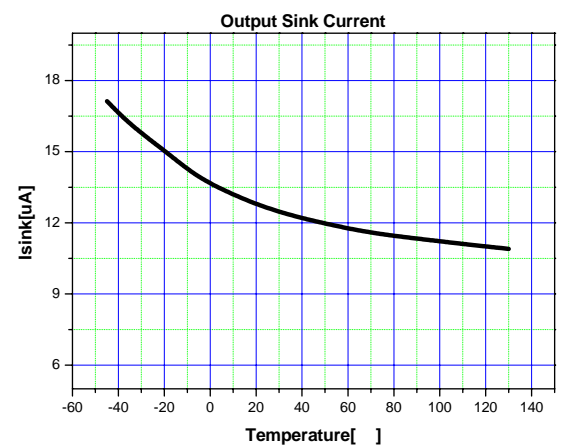


Figure 15. Error Amp. Sink Current vs. Temp.



## Typical Performance Characteristics (Continued)

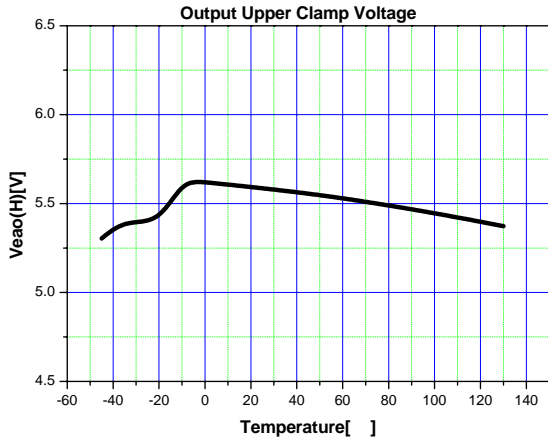


Figure 16. Error Amp. Clamp Voltage vs. Temp.

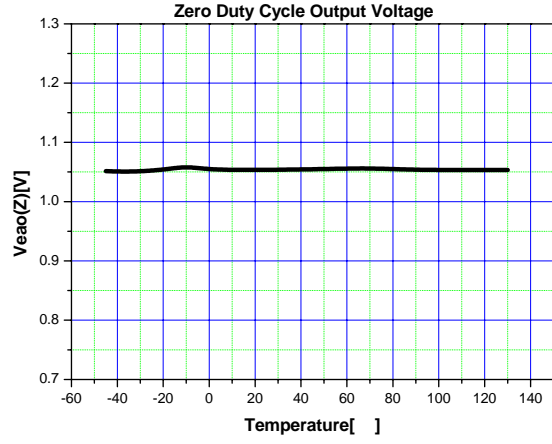


Figure 17. Zero Duty Output Voltage vs. Temp.

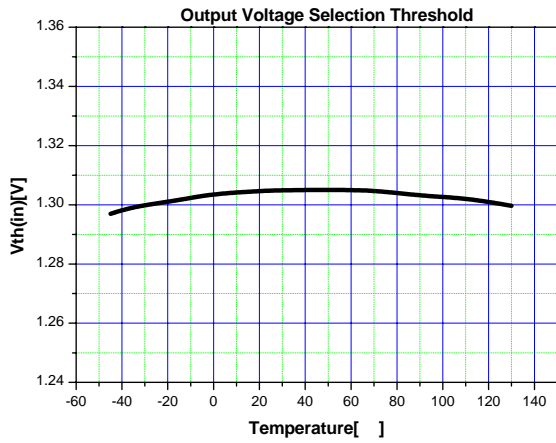


Figure 18. Output Select Threshold vs. Temp.

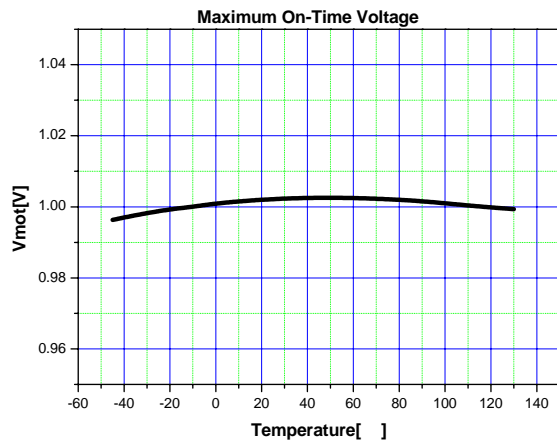


Figure 19. MOT pin Voltage vs. Temp.

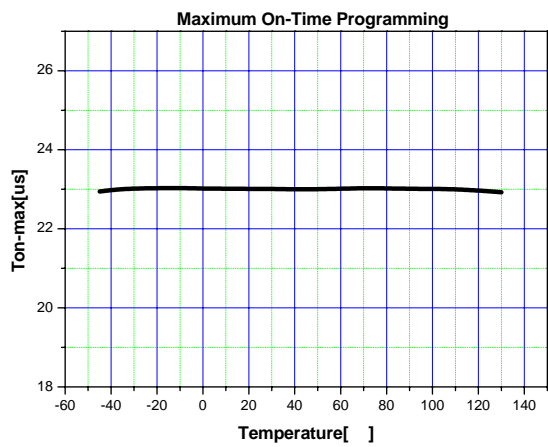


Figure 20. Maximum On-time vs. Temp.

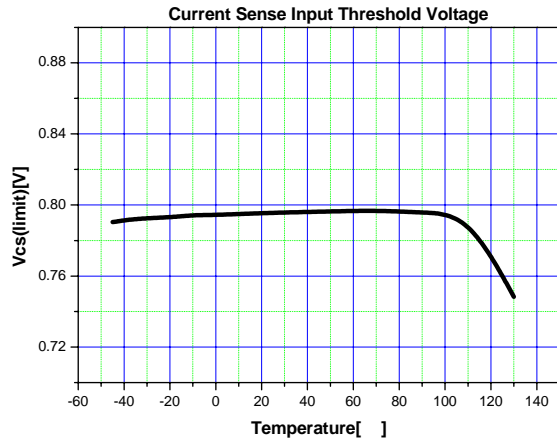


Figure 21. Current Limit vs. Temp.

## Typical Performance Characteristics (Continued)

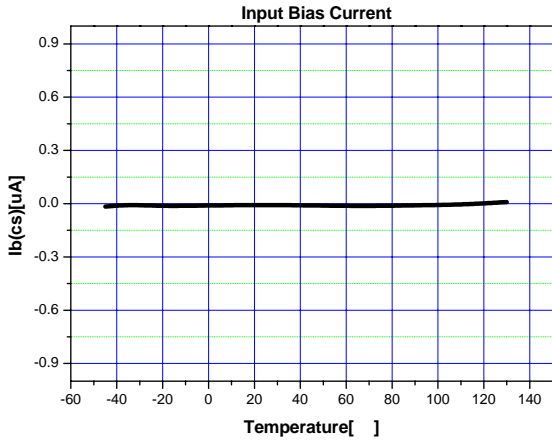


Figure 22. CS Input Bias Current vs. Temp.

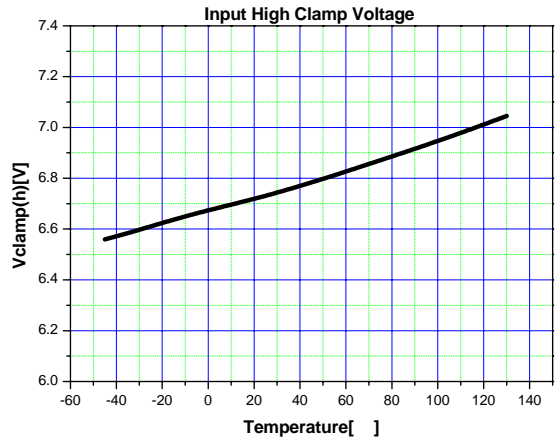


Figure 23. ZCD Input High Clamp vs. Temp.

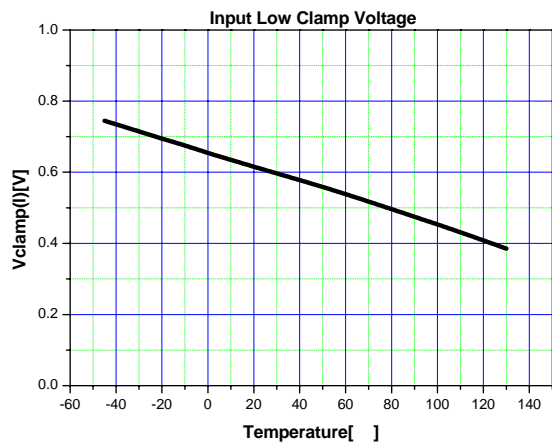


Figure 24. ZCD Input Low Clamp vs. Temp.

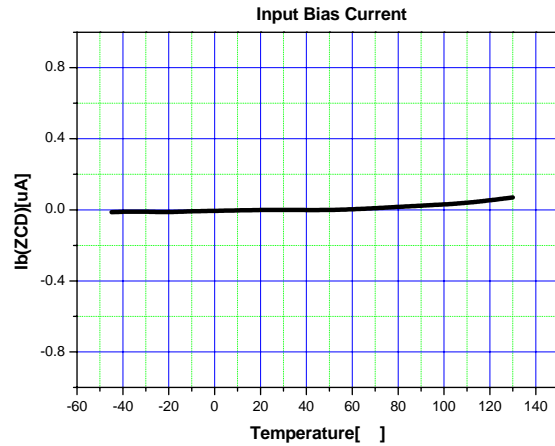


Figure 25. ZCD Input Bias Current vs. Temp.

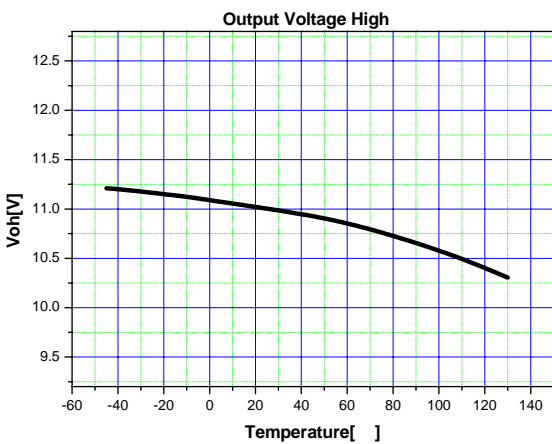


Figure 26. Output Voltage High vs. Temp.

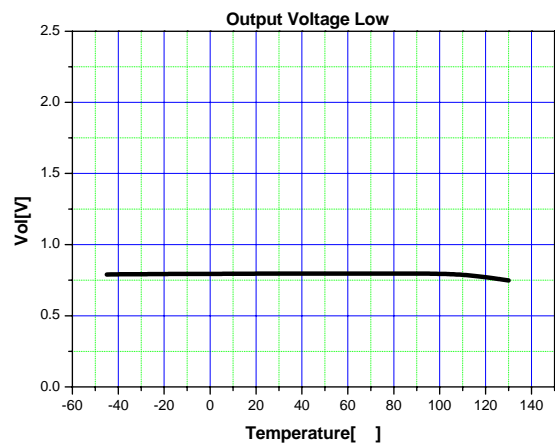


Figure 27. Output Voltage Low vs. Temp.

### Typical Performance Characteristics (Continued)

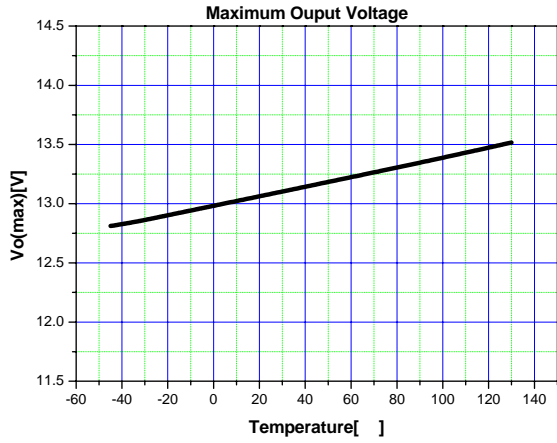


Figure 28. Maximum Output Voltage vs. Temp.

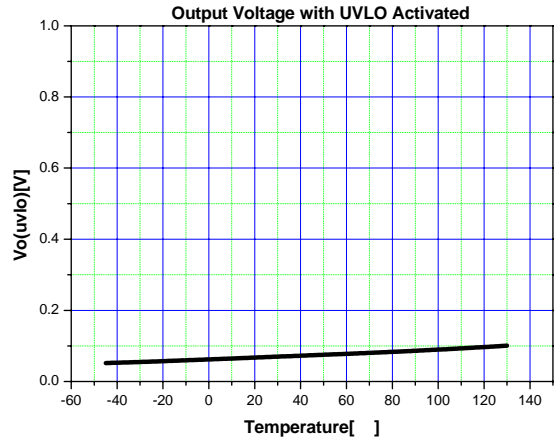


Figure 29. Output Voltage when UVLO vs. Temp.

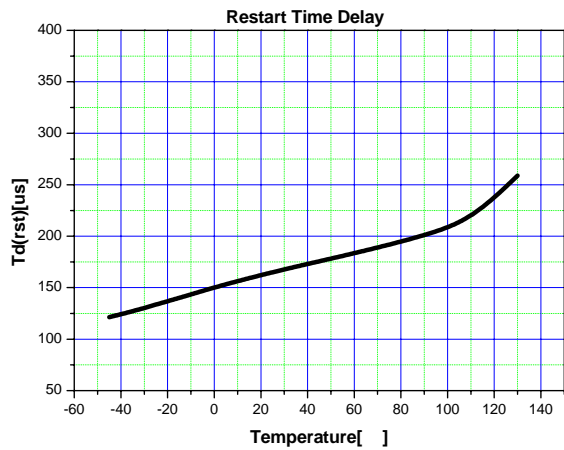


Figure 30. Restart Timer Delay vs. Temp.

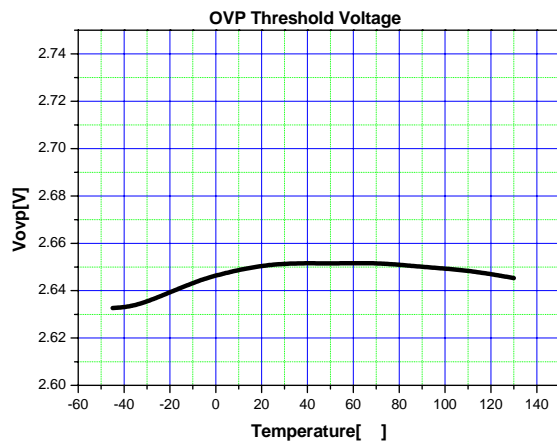


Figure 31. Over Voltage Protection vs. Temp.

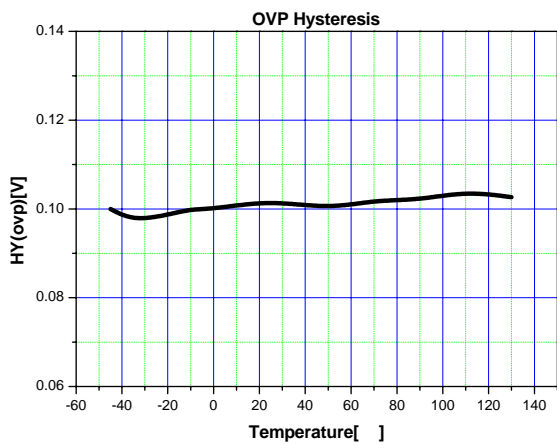


Figure 32. OVP Hysteresis vs. Temp.

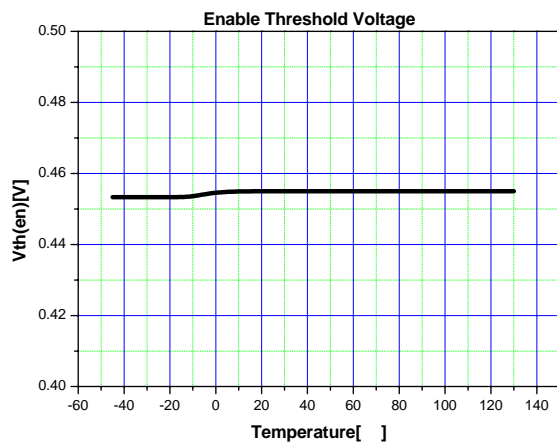


Figure 33. Enable Threshold Voltage vs. Temp.

Typical Performance Characteristics (Continued)

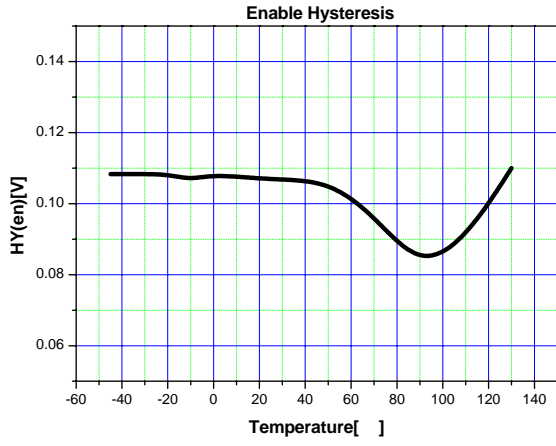


Figure 34. Enable Hysteresis vs. Temp.

## Applications Information

### 1. Error Amplifier Block

The error amplifier block has several functions such as dual output function, over voltage protection function and disable function.

#### 1.1 Dual Output Function

Unlike conventional CRM PFC controllers, the FAN7528 has the dual output control function according to the AC line voltage without sensing the rectified AC line voltage. Because the output voltage of the boost converter is proportional to the peak voltage of the input AC line voltage before the boost converter starts switching, the INV pin voltage represents the peak AC line voltage. When the AC line is connected to the boost converter, Vcc voltage starts to increase from zero voltage. If the Vcc voltage reaches 8.5V, the dual output reference generator compares the INV pin voltage with 1.3V reference and if the INV pin voltage is lower than 1.3V the dual output reference generator sets the reference voltage of the error amplifier to be 1.5V. If the INV pin voltage is higher than 1.3V, the reference voltage is set to be 2.5V. That means if the output voltage of the boost converter is set to be 400V at high line, the output voltage is 240V(400V\*1.5/2.5) at low line. If the output voltage is set to be 390V at high line, the output voltage is 234V at low line. Because this block does not need the input voltage sensing network, the power loss and cost related with the sensing network can be saved. The reference voltage of the error amplifier is not reset until the Vcc voltage goes below 4.5V.

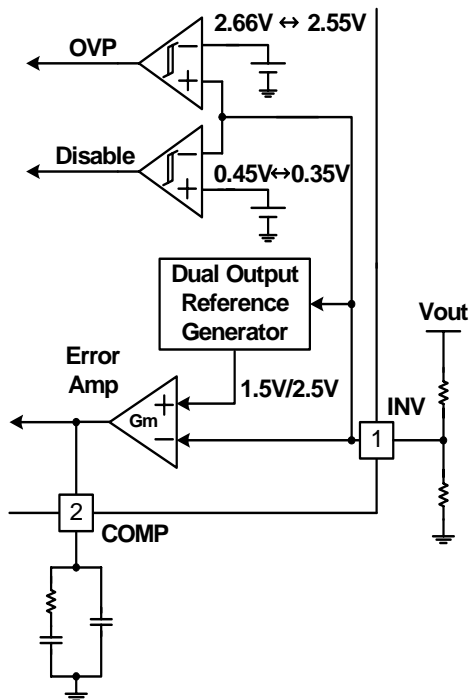


Figure 35. Error amplifier block

#### 1.2 Over Voltage Protection Function

The control speed of the PFC converter is very slow, therefore the over voltage protection of the output voltage is very important. The FAN7528 provides a precise OVP function that shuts down the drive circuit when the INV pin voltage exceeds 2.66V, and there is 0.11V hysteresis.

#### 1.3 Disable Function

If the INV pin voltage is lower than 0.45V, most of the internal block is disabled and the operating current is reduced to be 65uA, and there is 0.1V hysteresis in the comparator.

#### 1.4 Error Amplifier

The error amplifier is a transconductance type amplifier. The output current of the amplifier is proportional to the voltage difference between the inverting input and the non inverting input of the amplifier. Some resistors and capacitors should be connected to the error amplifier output pin, the COMP pin, for the output voltage loop compensation.

### 2. Zero Current Detection Block

The zero current detector(ZCD) generates the turn-on signal of the MOSFET when the boost inductor current reaches zero using an auxiliary winding coupled with the inductor. If the voltage of the ZCD pin goes higher than 1.5V then the ZCD comparator waits until the voltage goes below 1.4V. If the voltage goes below 1.4V, the zero current detector turns on the MOSFET. The ZCD pin is protected internally by two clamps, 6.7V high clamp and 0.6V low clamp. The 160us timer generates a MOSFET turn-on signal if the drive output has been low for more than 160us from the falling edge of the drive output.

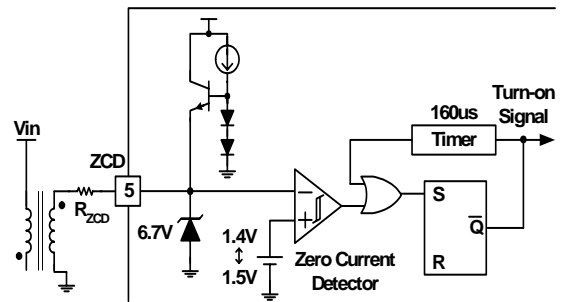
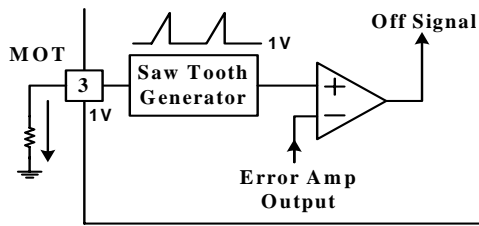


Figure 36. Zero current detector block

### 3. Saw Tooth Generator Block

The output of the error amplifier and the output of the saw tooth generator are compared to determine the MOSFET turn-off instance. The slope of the saw tooth is determined by an external resistor connected to the MOT pin. The voltage of the MOT pin is 1V and the slope is proportional to the current flowing out of the MOT pin. The internal ramp signal has 1V offset, therefore the drive output is shut down if the voltage of the COMP pin is lower than 1V. The MOSFET on-time is maximum when the COMP pin voltage is 5V. According to the slope of the internal ramp, the maximum on-time can be programmed. The necessary maximum on-time depends on the boost inductor, lowest

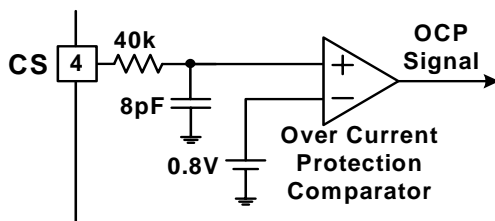
AC line voltage and maximum output power. The resistor value should be designed properly.



**Figure 37. Zero current detector block**

#### 4. Over Current Protection Block

The MOSFET current is sensed using an external sensing resistor for the over current protection. If the CS pin voltage is higher than 0.8V, the over current protection comparator generates a protection signal. An internal RC filter is included to filter switching noise.



**Figure 38. Over current protection block**

#### 5. Switch Drive Block

The FAN7528 contains a single totem-pole output stage designed for a direct drive of power MOSFET. The drive output is capable of up to 400mA peak current with a typical rise and fall time of 50ns with 1nF load. The output voltage is clamped to be 13V to protect MOSFET gate even if the Vcc voltage is higher than 20V.

#### 6. Under Voltage Lock Out Block

If the Vcc voltage reaches 12V, the IC's internal blocks are enabled and start operation. If the Vcc voltage drops below 8.5V, most of the internal blocks are disabled to reduce the operating current. Vcc voltage should be higher than 8.5V under normal conditions.

### Typical application circuit

Application	Output power	Input voltage	Output voltage
Adapter	100W	Universal input (90~264Vac)	389V/232V

#### Features

- High efficiency (>90% at 90Vac input)
- Low THD(total harmonic distortion) (<10% at 264Vac input)
- Dual output control

#### Key Design Notes

- Diode D4 is used to prevent IC malfunction that can happen if the CS pin voltage is lower than -0.3V.
- Important Component s for low THD are R2, R5 and C11.

#### 1. Schematic

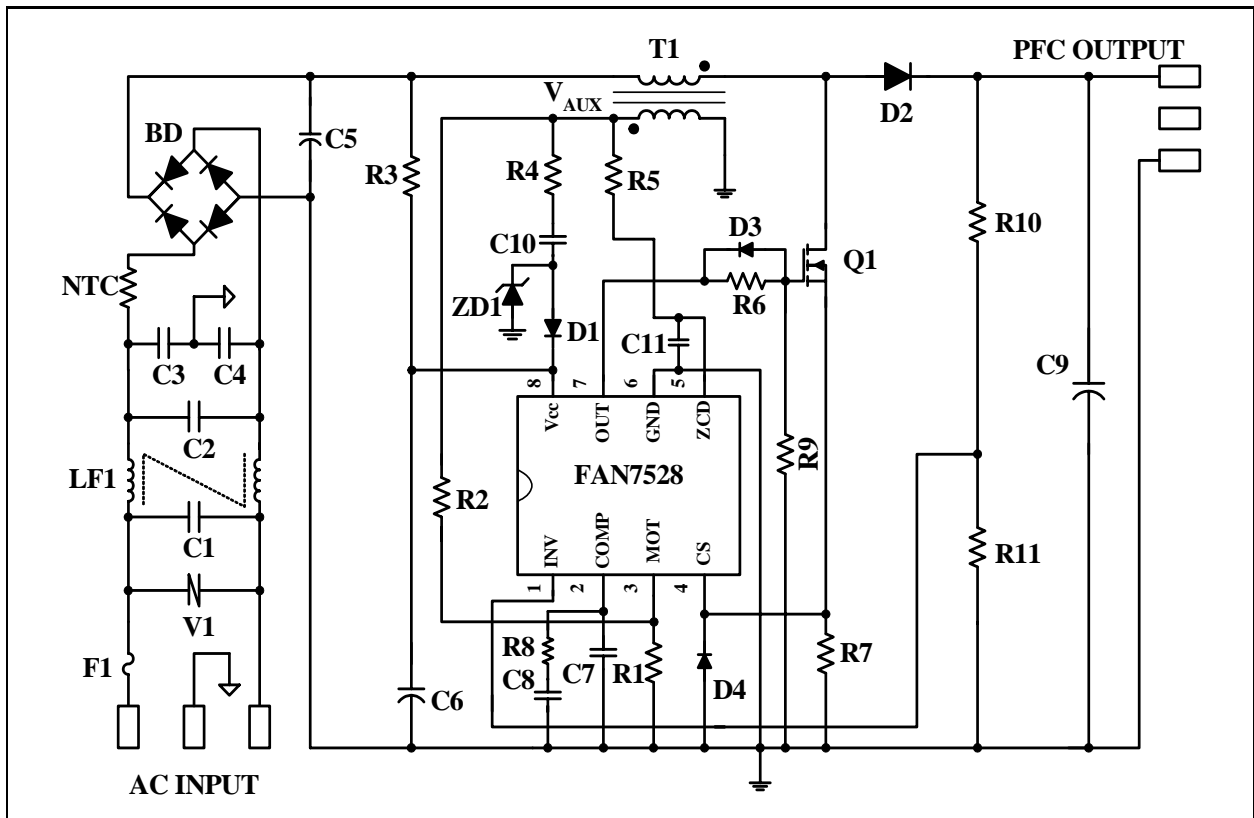


Figure 39. Schematic

## 2. Inductor Schematic Diagram

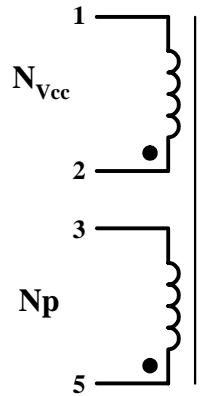


Figure 40. Inductor Schematic Diagram

## 3. Winding Specification

No	Pin (s→f)	Wire	Turns	Winding Method
$N_{Vcc}$	2 → 1	$0.2^\phi \times 1$	5	Solenoid Winding
Insulation: Polyester Tape $t = 0.050\text{mm}$ , 4Layers				
$N_p$	5 → 3	$0.2^\phi \times 10$	44	Solenoid Winding
Outer Insulation: Polyester Tape $t = 0.050\text{mm}$ , 4Layers				
Air Gap: 0.6mm for each leg				

## 4. Electrical Characteristics

	Pin	Specification	Remarks
Inductance	3 - 5	$400\mu\text{H} \pm 10\%$	100kHz, 1V

## 5. Core & Bobbin

- Core : EI 3026
- Bobbin : EI3026
- $A_e(\text{mm}^2)$  : 111



**6.Demo Circuit Part List**

Part	Value	Note	Part	Value	Note
<b>Fuse</b>			<b>Inductor</b>		
F1	3A/250V		T1	400uH	EI3026
<b>NTC</b>					
NTC	10D-9		<b>MOSFET</b>		
<b>Resistor</b>			Q1	FQPF13N50C	Fairchild
R1	10k	1/4W			
R2	300k	1/4W	<b>Diode</b>		
R3	330k	1/2W	D1	1N4148	Fairchild
R4	100	1/4W	D2	BYV26C	600V, 1A
R5	20k	1/4W	D3	1N5819	Fairchild
R6	10	1/4W	D4	1N5819	Fairchild
R7	0.22	1/2W	ZD1	1N4746	18V
R8	10k	1/4W			
R9	10k	1/4W	<b>Bridge Diode</b>		
R10	2M	1/4W	BD	KBL406	600V/4A
R11	12.9k	1/4W			
			<b>Line Filter</b>		
<b>Capacitor</b>			LF1	40mH	Wire 0.4mm
C1	150nF/275VAC	Box Capacitor			
C2	330nF/275VAC	Box Capacitor	<b>IC</b>		
C3	2.2nF/3kV	Ceramic Capacitor	IC1	FAN7528	Fairchild
C4	2.2nF/3kV	Ceramic Capacitor			
C5	100nF/630V	Film Capacitor	<b>TNR</b>		
C6	47uF/25V	Electrolytic Capacitor	V1	471	470V
C7	220nF/50V	Ceramic Capacitor			
C8	1uF	MLCC			
C9	100uF/450V	Electrolytic Capacitor			
C10	12nF/100V	Film Capacitor			
C11	56pF/50V	Ceramic Capacitor			

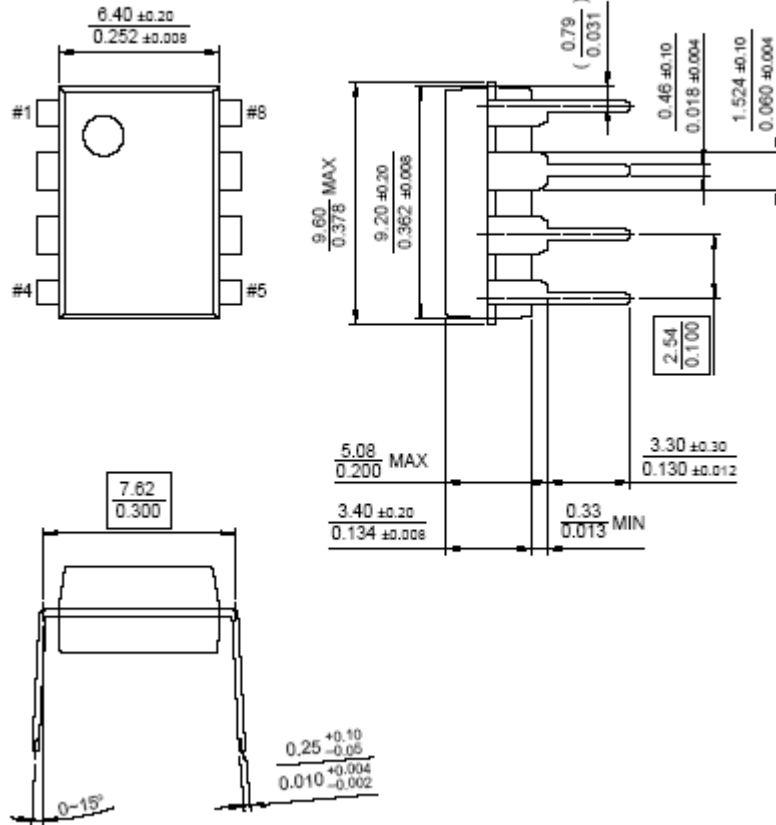


Mechanical Dimensions

Package

Unit : mm

8-DIP

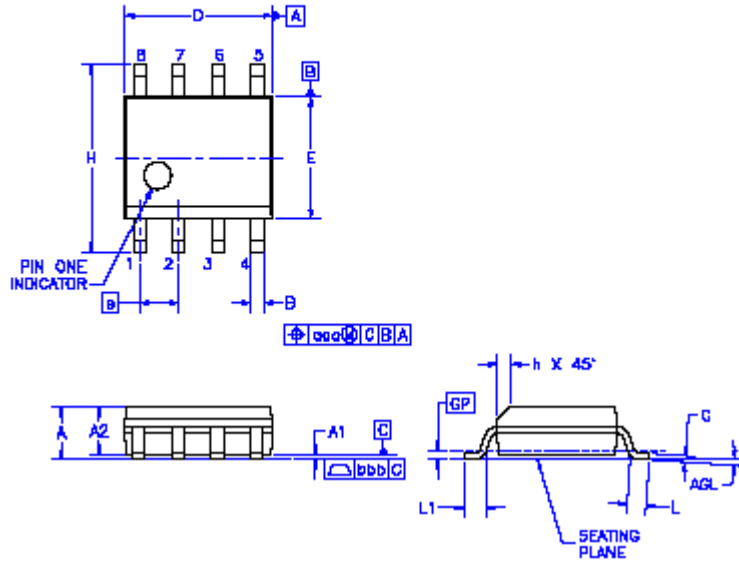


## Mechanical Dimensions

Package

Unit : mm

### 8-SOP



Symbol	Min	Nom	Max
A	-	-	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.50
B	0.35	0.37	0.51
C	0.19	0.20	0.25
D	4.80	4.90	5.00
E	3.80	3.90	4.00
e	1.27BSC		
H	5.79	5.99	6.20
h	0.25	-	0.50
L	0.50	0.70	0.90
GP	0.36 BSC		
q	0	-	8
aaa	-	-	0.25
bbb	-	-	0.10

**TRADEMARKS**

The following are registered and unregistered trademarks Fairchild Semiconductor owns or is authorized to use and is not intended to be an exhaustive list of all such trademarks.

ACEx™	FAST®	ISOPLANAR™	PowerSaver™	SuperSOT™-8
ActiveArray™	FASTr™	LittleFET™	PowerTrench®	SyncFET™
Bottomless™	FPS™	MICROCOUPLER™	QFET®	TinyLogic®
Build it Now™	FRFET™	MicroFET™	QS™	TINYOPTO™
CoolFET™	GlobalOptoisolator™	MicroPak™	QT Optoelectronics™	TruTranslation™
CROSSVOLT™	GTO™	MICROWIRE™	Quiet Series™	UHC™
DOME™	HiSeC™	MSX™	RapidConfigure™	UltraFET®
EcoSPARK™	I <sup>2</sup> C™	MSXPro™	RapidConnect™	UniFET™
E <sup>2</sup> CMOS™	i-Lo™	OCX™	μSerDes™	VCX™
EnSigna™	ImpliedDisconnect™	OCXPro™	SILENT SWITCHER®	Wire™
FACT™	IntelliMAX™	OPTOLOGIC®	SMART START™	
FACT Quiet Series™		OPTOPLANAR™	SPM™	
Across the board. Around the world.™		PACMAN™	Stealth™	
The Power Franchise®		POP™	SuperFET™	
Programmable Active Droop™		Power247™	SuperSOT™-3	
		PowerEdge™	SuperSOT™-6	

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

Rev. 116