For new designs use part CY7C374i

CY7C374

UltraLogic™ 128-Macrocell Flash CPLD

Features

- **128 macrocells in eight logic blocks**
- **64 I/O pins**
- **6 dedicated inputs including 4 clock pins**
- **Bus Hold capabilities on all I/Os and dedicated inputs**
- **No hidden delays**
- **High speed**
  - **— f_{MAX} = 100 MHz**
  - **— t_{PD} = 12 ns**
  - **— t_S = 6 ns**
  - **— t_{CO} = 7 ns**
- **Electrically Alterable Flash technology**
- **Available in 84-pin PLCC, 84-pin CLCC, 100-pin TQFP, and 84-pin PGA packages**
- **Pin compatible with the CY7C373**

Functional Description

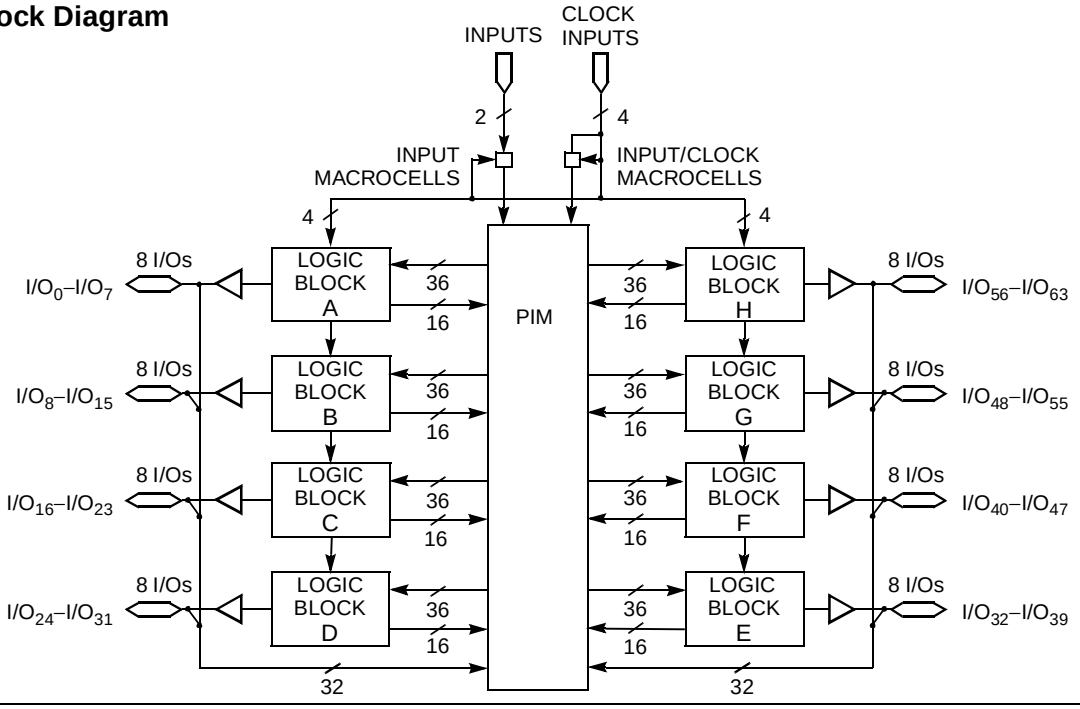
The CY7C374 is a Flash erasable Complex Programmable Logic Device (CPLD) and is part of the FLASH370™ family of high-density, high-speed CPLDs. Like all members of the FLASH370 family, the CY7C374 is designed to bring the ease of use and high performance of the 22V10 to high-density CPLDs.

The 128 macrocells in the CY7C374 are divided between eight logic blocks. Each logic block includes 16 macrocells, a 72 x 86 product term array, and an intelligent product term allocator.

The logic blocks in the FLASH370 architecture are connected with an extremely fast and predictable routing resource—the Programmable Interconnect Matrix (PIM). The PIM brings flexibility, routability, speed, and a uniform delay to the interconnect.

The CY7C374 is a register intensive 128-Macrocell CPLD. Every two macrocells in the device feature an associated I/O pin, resulting in 64 I/O pins on the CY7C374. In addition, there are two dedicated inputs and four input/clock pins.

Logic Block Diagram



Selection Guide

		7C374-100	7C374-83	7C374-66	7C374L-66
Maximum Propagation Delay t_{PD} (ns)		12	15	20	20
Minimum Set-Up, t_S (ns)		6	8	10	10
Maximum Clock to Output, t_{CO} (ncs)		7	8	10	10
Maximum Supply Current, I_{CC} (mA)	Commercial	300	300	300	150
	Military/Industrial		370	370	