Features

- AVR® Microcontroller-based Function Controller
- Fully Programmable USB Low-/Full-speed Function with Five Endpoints
- High Performance and Low Power 1.5/12/24 MIPs AVR RISC Microcontroller
- 120 Powerful Instructions – Most with 83 ns Execution Cycle Times
- 24 KB Masked ROM Program Memory
- 1 KB Internal SRAM
- 32 x 8 General-purpose Working Registers
- 19 Programmable I/O Port Pins
- 12 Channels 10-bit A-to-D Converter
- Programmable SPI Serial Interface
- One 8-bit Timer Counter with Separate Pre-scaler
- One 16-bit Timer Counter with Separate Pre-scaler and Two PWMs
- External and Internal Interrupt Sources
- Programmable Watchdog Timer
- Low Power Idle and Power-down Modes
- 6 MHz Crystal Oscillator with PLL
- 5V Operation with On-chip 3.3V Regulators
- 48-lead LQFP Package
- Binary-compatible with the AT43USB355

Description

The Atmel AT43USB351M is a USB AVR-based microcontroller that is configurable as a low-speed or full-speed USB device. Its program memory is a 24-Kbyte mask programmable ROM and its data memory is 1-Kbyte SRAM. The on-chip peripherals consists of 19 general-purpose I/O ports, two timer-counters, SPI serial interface, a PWM and a 10-bit AD converter with 12 input channels.

The MCU of the AT43USB351M is a high performance 8-bit AVR RISC that operates at a clock frequency of 1.5 MHz, 12 MHz or 24 MHz. The A-to-D converter has a minimum conversion time of 12 µs that together with the 12 input channel should cover even the most demanding game controllers such as gamepads, joysticks and racing wheels. The two PWM outputs can be programmed for 8-, 9- or 10-bit resolution for applications requiring force feedback. The 19 general-purpose programmable I/O pins provide generous inputs for the various buttons and switches and LED indicators that are being used in increasing numbers in today's game controllers.

The USB function has one control endpoint and four additional programmable endpoints, each with their own FIFOs. Two of the endpoints have a 64-byte FIFO each, while the other two have 8-byte FIFOs. The USB hardware supports the physical and link layers of the USB protocol while the transaction layer function must be implemented in the MCU's firmware. The AVR architecture was developed to be programmed in C efficiently and without loss in performance.

The AT43USB351M is binary-compatible with the AT43USB355. Program development and debugging for the AT43USB351M uses the AT43DK355 and all its tools and libraries.

Full-speed/ Low-speed USB Microcontroller with ADC and PWM

AT43USB351M

Summary

Rev. 3302BS–USB–09/02

Pin Configuration

Figure 1. AT43USB351M 48-lead LQFP

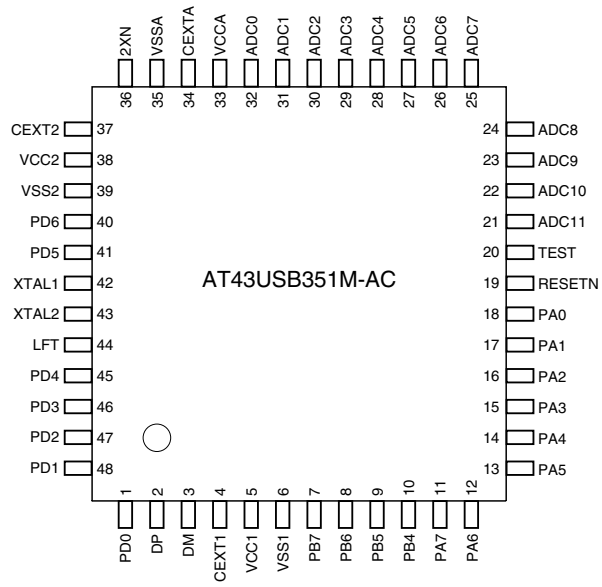
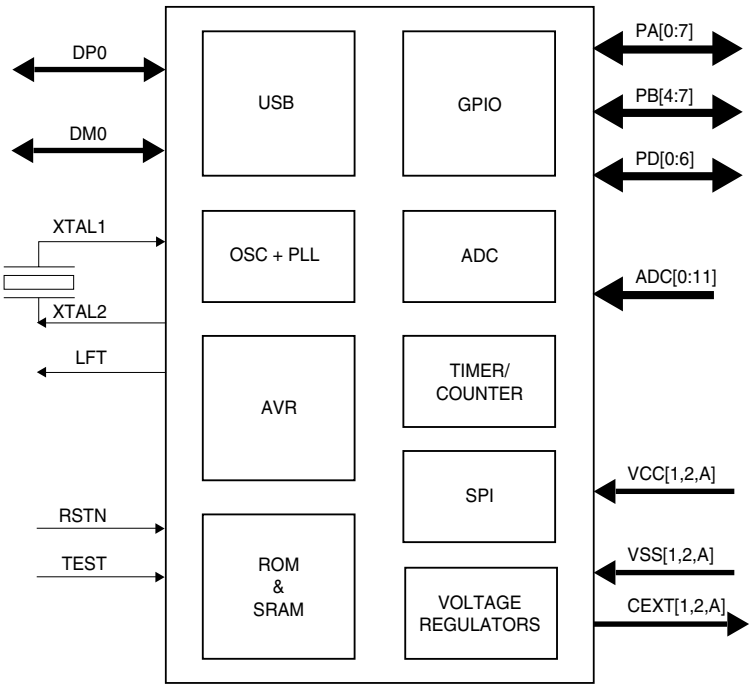


Figure 2. Low-/Full-speed USB Microcontroller with ADC and PWM



Pin Assignment

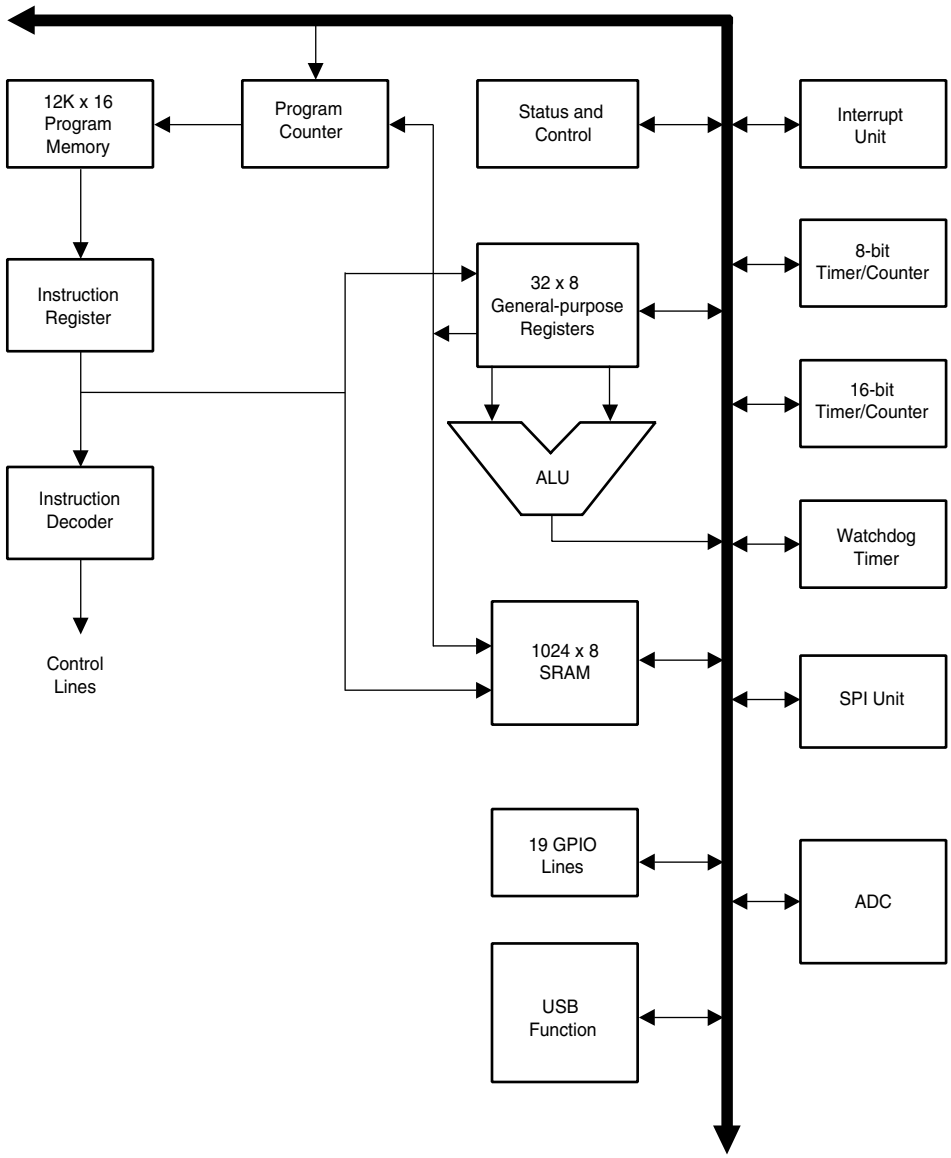
Pin#	Signal	Type
1	PD0	Bi-directional
2	DP	Bi-directional
3	DM	Bi-directional
4	CEXT1	Power Supply/Ground
5	VCC1	Power Supply/Ground
6	VSS1	Power Supply/Ground
7	PB7	Bi-directional
8	PB6	Bi-directional
9	PB5	Bi-directional
10	PB4	Bi-directional
11	PA7	Bi-directional
12	PA6	Bi-directional
13	PA5	Bi-directional
14	PA4	Bi-directional
15	PA3	Bi-directional
16	PA2	Bi-directional
17	PA1	Bi-directional
18	PA0	Bi-directional
19	RESETN	Input
20	TEST	Input
21	ADC11	Input
22	ADC10	Input
23	ADC9	Input
24	ADC8	Input

Pin#	Signal	Type
25	ADC7	Input
26	ADC6	Input
27	ADC5	Input
28	ADC4	Input
29	ADC3	Input
30	ADC2	Input
31	ADC1	Input
32	ADC0	Input
33	VCCA	Power Supply/Ground
34	CEXTA	Power Supply/Ground
35	VSSA	Power Supply/Ground
36	2XN	Input
37	CEXT2	Power Supply/Ground
38	VCC2	Power Supply/Ground
39	VSS2	Power Supply/Ground
40	PD6	Bi-directional
41	PD5	Bi-directional
42	XTAL1	Input
43	XTAL2	Output
44	LFT	Output
45	PD4	Bi-directional
46	PD3	Bi-directional
47	PD2	Bi-directional
48	PD1	Bi-directional

Signal Description

Name	Type	Function
$V_{CC1, 2}$	Power Supply/Ground	**5V Digital Power Supply**
V_{CCA}	Power Supply/Ground	**5V Power Supply for the ADC**
$V_{SS1, 2}$	Power Supply/Ground	**Digital Ground**
V_{SSA}	Power Supply/Ground	**Ground for the ADC**
CEXT1,2	Power Supply/Ground	**External Capacitors for Power Supplies** – High quality 2.2 µF capacitors must be connected to V331 and V332 for proper operation of the chip.
CEXT	Power Supply/Ground	**External Capacitor for Analog Power Supply** – A high quality 0.33 µF capacitor must be connected to V33A for proper operation of the chip.
XTAL1	Input	**Oscillator Input** – Input to the inverting oscillator amplifier.
XTAL2	Output	**Oscillator Output** – Output of the inverting oscillator amplifier.
LFT	Input	**PLL Filter** – For proper operation of the PLL, this pin should be connected through a 0.01 µF capacitor in parallel with a 100Ω resistor in series with a 0.1 µF capacitor to ground (VSS). Both capacitors must be high quality ceramic.
DPO	Bi-directional	**Upstream Plus USB I/O** – This pin should be connected to CEXT1 through an external 1.5 kΩ.
DMO	Bi-directional	**Upstream Minus USB I/O**
PA[0:7]	Bi-directional	**Port A[0:7]** – Bi-directional 8-bit I/O port with 2 mA drive strength and a programmable pull-up resistor.
PB[4:7]	Bi-directional	**Port B[4:7]** – Bi-directional 8-bit I/O port with 2 mA drive strength and a programmable pull-up resistor. PB[4:7] have dual functions as shown below: **Port Pin** — **Alternate Function** PB4 — SSN, SPI Slave Port Select or SCL, I2C Serial Bus Clock PB5 — MOSI, SPI Slave Port Select Input PB6 — MISO, SPI Master Data In, Slave Data Out PB7 — SCK, SPI Master Clock Out, Slave Clock In
PD[0:6]	Bi-directional	**Port D[0:6]** – Bi-directional I/O ports with 2 mA drive strength and a programmable pull-up resistor. PortD[2:6] have dual functions as shown below: **Port Pin** — **Alternate Function** PD2 — INT0, External Interrupt 0 PD4 — ICP, Timer/Counter, Input Capture PD3 — INT1, External Interrupt 1 PD5 — OC1A Timer/Counter1 Output Compare A PD6 — OC1B Timer/Counter1 Output Compare B
ADC[0:11]	Input	**ADC Input[0:11]** – 12-bit input pins for the ADC.
TEST	Input	**Test Pin** – This pin should be tied to ground.
RESETN	Input	**Reset** – Active Low.

Figure 3. The AT43USB351M Enhanced RISC Architecture



Architectural Overview

The AT43USB351M is binary-compatible with the AT43USB355 compound device. Firmware developed for the AT43USB355 will run on the AT43USB351M.

The peripherals and features of the AT43USB351M microcontroller are similar to those of the AT90S8515, with the exception of the following modifications:

- No EEPROM
- No External Data Memory Accesses
- No UART
- Idle Mode not Supported
- USB Function
- On-chip ADC

The embedded USB hardware of the AT43USB351M is a USB function with an 8-byte control endpoint and four additional programmable endpoints with separate FIFOs. Two of the FIFOs are 64 bytes deep and the other two are 8 bytes deep.

Depending on the USB speed and the state of 2XN input signal, device pin 36, the MCU runs at 1.5 MHz, 12 MHz or 24 MHz. The clock that operates the MCU is generated by the USB hardware. While at 12 MHz, the nominal and average period of the clock is 83.3 ns, it may have single cycles that deviate by ±20.8 ns during a phase adjustment by the SIE's clock/data separator of the USB hardware. Similarly at 1.5 MHz, the MCU clock runs 8 times slower and at 24 MHz, two times faster than the 12 MHz mode. The clock frequencies of the various modules of the AT43USB351M is summarized in the following table:

USB Mode	2XN Pin	MCU Clock	Timer/Counter Clock	ADC Clock	SPI Clock	WDT Clock
Full Speed	0	24 MHz	12 MHz	1 MHz	24 MHz	1 MHz
Full Speed	1	12 MHz	12 MHz	1 MHz	12 MHz	1 MHz
Low Speed	0	24 MHz	12 MHz	1 MHz	24 MHz	1 MHz
Low Speed	1	1.5 MHz	1.5 MHz	1 MHz	1.5 MHz	1 MHz

The microcontroller shares most of the control and status registers of the megaAVR Microcontroller Family. The registers for managing the USB operations are mapped into its SRAM space. Please refer to the Atmel AVR manual for more information.

The fast-access register file concept contains 32 x 8-bit general-purpose working registers with a single clock cycle access time. This means that during one single clock cycle, one Arithmetic Logic Unit (ALU) operation is executed. Two operands are output from the register file, the operation is executed, and the result is stored back in the register file – in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing - enabling efficient address calculations. One of the three address pointers is also used as the address pointer for look-up tables in program memory. These added function registers are the 16-bit X-, Y- and Z-registers.

The ALU supports arithmetic and logic operations between registers or between a constant and a register. Single register operations are also executed in the ALU. Figure 3 on page 5 shows the AT43USB351M AVR Enhanced RISC microcontroller architecture.

In addition to the register operation, the conventional memory addressing modes can be used on the register file as well. This is enabled by the fact that the register file is assigned the 32 lowest Data Space addresses ($00 - $1 F), allowing them to be accessed as though they were ordinary memory locations.

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, Timer/Counters, and other I/O functions. The I/O Memory can be accessed directly, or as the Data Space locations following those of the register file, $20 - $5F.

The AVR uses a Harvard architecture concept – with separate memories and buses for program and data. The program memory is executed with a single-level pipelining. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is a downloadable SRAM or a mask programmed ROM.

With the relative jump and call instructions, the whole 24K address space is directly accessed. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

During interrupts and subroutine calls, the return address Program Counter (PC) is stored on the stack. The stack is effectively allocated in the general data SRAM, and consequently, the stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the Stack Pointer (SP) in the reset routine (before subroutines or interrupts are executed). The 10-bit SP is read/write accessible in the I/O space.

The 1-Kbyte data SRAM can be easily accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps. A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the status register. All interrupts have a separate interrupt vector in the interrupt vector table at the beginning of the program memory. The interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.

Development Support

The AT43USB351M uses the same program and development tools as the AT43USB355 and other Atmel AVR microcontrollers, including: C compilers, macro assemblers, program debuggers/simulators and in-circuit emulators. The AT43DK355 development kit is also available, including firmware source code for the most common USB applications.

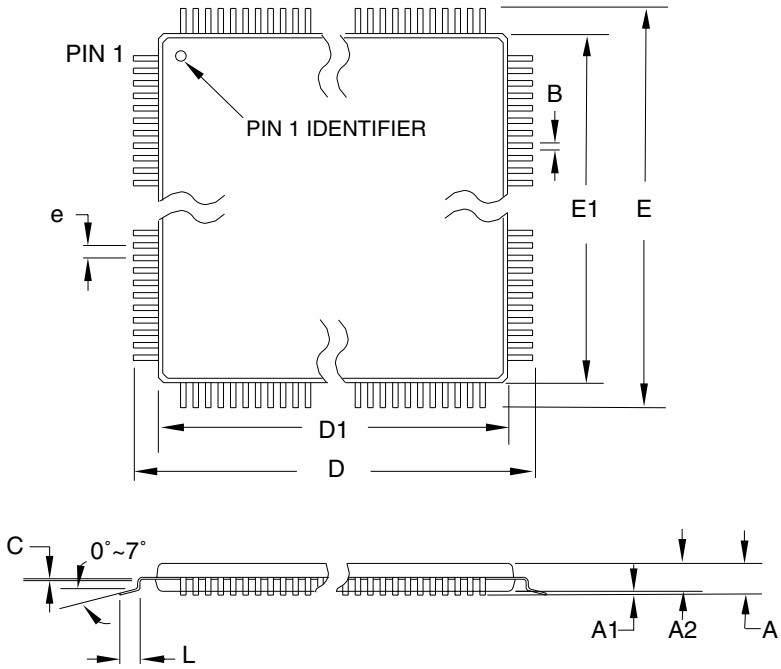
Ordering Information

Program Memory	Ordering Code	Package	Operation Range
Mask ROM	AT43USB351M-AC	48 LQFP	Commercial (0°C to 70°C)

Package Type	
48AA	48-lead, 7 x 7 mm Body Size, Low Profile Plastic Quad Flat Package (LQFP)

Package Information

48AA – LQFP



COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.60	
A1	0.05	–	0.15	
A2	1.35	1.40	1.45	
D	8.75	9.00	9.25	
D1	6.90	7.00	7.10	Note 2
E	8.75	9.00	9.25	
E1	6.90	7.00	7.10	Note 2
B	0.17	–	0.27	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.50 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation BBC.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.08 mm maximum.

10/5/2001

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**48AA,** 48-lead, 7 x 7 mm Body Size, 1.4 mm Body Thickness, 0.5 mm Lead Pitch, Low Profile Plastic Quad Flat Package (LQFP)	48AA	C

Atmel Headquarters

Corporate Headquarters
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 487-2600

Europe
Atmel Sarl
Route des Arsenaux 41
Case Postale 80
CH-1705 Fribourg
Switzerland
TEL (41) 26-426-5555
FAX (41) 26-426-5500

Asia
Room 1219
Chinachem Golden Plaza
77 Mody Road Tsimshatsui
East Kowloon
Hong Kong
TEL (852) 2721-9778
FAX (852) 2722-1369

Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
TEL (81) 3-3523-3551
FAX (81) 3-3523-7581

Atmel Operations

Memory
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

Microcontrollers
2325 Orchard Parkway
San Jose, CA 95131
TEL 1(408) 441-0311
FAX 1(408) 436-4314

La Chantrerie
BP 70602
44306 Nantes Cedex 3, France
TEL (33) 2-40-18-18-18
FAX (33) 2-40-18-19-60

ASIC/ASSP/Smart Cards
Zone Industrielle
13106 Rousset Cedex, France
TEL (33) 4-42-53-60-00
FAX (33) 4-42-53-60-01

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Scottish Enterprise Technology Park
Maxwell Building
East Kilbride G75 0QR, Scotland
TEL (44) 1355-803-000
FAX (44) 1355-242-743

RF/Automotive
Theresienstrasse 2
Postfach 3535
74025 Heilbronn, Germany
TEL (49) 71-31-67-0
FAX (49) 71-31-67-2340

1150 East Cheyenne Mtn. Blvd.
Colorado Springs, CO 80906
TEL 1(719) 576-3300
FAX 1(719) 540-1759

Biometrics/Imaging/Hi-Rel MPU/
High Speed Converters/RF Datacom
Avenue de Rochepleine
BP 123
38521 Saint-Egreve Cedex, France
TEL (33) 4-76-58-30-00
FAX (33) 4-76-58-34-80

e-mail
literature@atmel.com

Web Site
http://www.atmel.com

3302BS–USB–09/02 xM