

#### Features

- High-speed access times  
Com'l: 10, 12 and 15 ns  
Ind'l: 12 and 15 ns
- Low power operation (typical)
  - PDM41024SA  
Active: 450 mW  
Standby: 50 mW
  - PDM41024LA  
Active: 400 mW  
Standby: 25mW
- Single +5V ( $\pm 10\%$ ) power supply
- TTL-compatible inputs and outputs
- Packages
  - Plastic SOJ (300 mil) - TSO
  - Plastic SOJ (400 mil) - SO
  - Plastic TSOP (I)- T

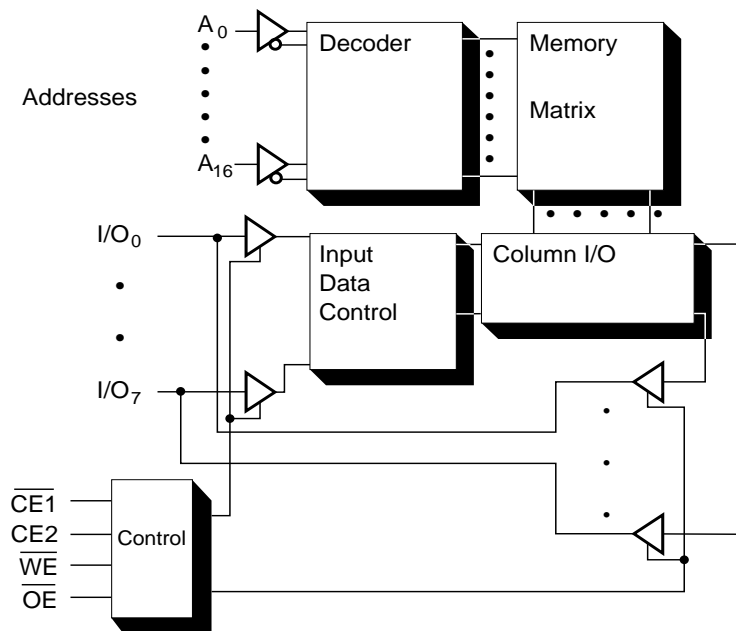
#### Description

The PDM41024 is a high-performance CMOS static RAM organized as 131,072 x 8 bits. Writing is accomplished when the write enable ( $\overline{WE}$ ) and the chip enable ( $\overline{CE1}$ ) inputs are both LOW and CE2 is HIGH. Reading is accomplished when  $\overline{WE}$  and CE2 remain HIGH and  $\overline{CE1}$  and  $\overline{OE}$  are both LOW.

The PDM41024 operates from a single +5V power supply and all the inputs and outputs are fully TTL-compatible. The PDM41024 comes in two versions: the standard power version (SA) and the low power version (LA). The two versions are functionally the same and differ only in their power consumption.

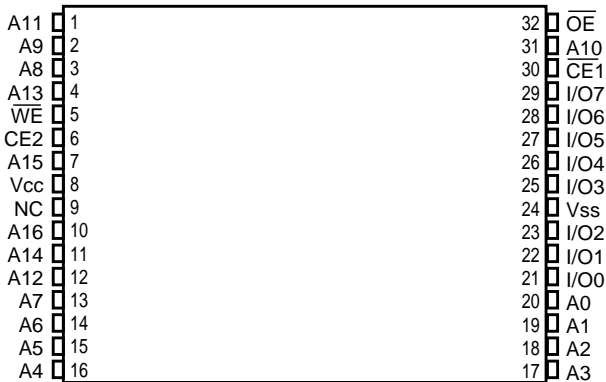
The PDM41024 is available in a 32-pin plastic TSOP (I), and a 300-mil and 400-mil plastic SOJ.

#### Functional Block Diagram

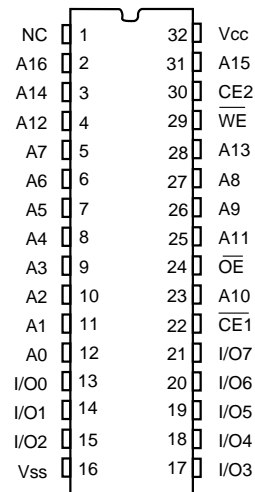


Pin Configuration

TSOP (I)



SOJ



Pin Description

Name	Description
A16-A0	Address Inputs
I/O7-I/O0	Data Inputs/Outputs
OE	Output Enable Input
WE	Write Enable Input
CE1, CE2	Chip Enable Inputs
NC	No Connect
VCC	Power (+5V)
VSS	Ground

Truth Table<sup>(1)</sup>

OE	WE	CE1	CE2	I/O	MODE
X	X	H	X	Hi-Z	Standby
X	X	X	L	Hi-Z	Standby
L	H	L	H	D <sub>OUT</sub>	Read
X	L	L	H	D <sub>IN</sub>	Write
H	H	L	H	Hi-Z	Output Disable

NOTE: 1. H = V<sub>IH</sub>, L = V<sub>IL</sub>, X = DON'T CARE

Absolute Maximum Ratings<sup>(1)</sup>

Symbol	Rating	Com'l.	Ind.	Unit
V <sub>TERM</sub>	Terminal Voltage with Respect to V <sub>SS</sub>	-0.5 to +7.0	-0.5 to +7.0	V
T <sub>BIAS</sub>	Temperature Under Bias	-55 to +125	-65 to +135	°C
T <sub>STG</sub>	Storage Temperature	-55 to +125	-65 to +150	°C
P <sub>T</sub>	Power Dissipation	1.0	1.0	W
I <sub>OUT</sub>	DC Output Current	50	50	mA
T <sub>j</sub>	Maximum Junction Temperature <sup>(2)</sup>	125	145	°C

NOTE: 1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

2. Appropriate thermal calculations should be performed in all cases and specifically for those where the chosen package has a large thermal resistance (e.g., TSOP). The calculation should be of the form:  $T_j = T_a + P * \theta_{ja}$  where  $T_a$  is the ambient temperature, P is average operating power and  $\theta_{ja}$  the thermal resistance of the package. For this product, use the following  $\theta_{ja}$  values:

SOJ: 72° C/W  
 TSOP: 95° C/W

### Recommended DC Operating Condition

Symbol	Parameter	Min.	Typ.	Max.	Unit
V <sub>CC</sub>	Supply Voltage	4.5	5.0	5.5	V
V <sub>SS</sub>	Supply Voltage	0	0	0	V
Industrial	Ambient Temperature	-40	25	85	°C
Commercial	Ambient Temperature	0	25	70	°C

### DC Electrical Characteristics (V<sub>CC</sub> = 5.0V ± 10%)

Symbol	Parameter	Test Conditions		PDM41024SA		PDM41024LA		Unit
				Min.	Max.	Min.	Max.	
I <sub>LI</sub>	Input Leakage Current	V <sub>CC</sub> = MAX., V <sub>IN</sub> = V <sub>SS</sub> to V <sub>CC</sub>	Com'l/ Ind.	-5	5	-1	1	µA
I <sub>LO</sub>	Output Leakage Current	V <sub>CC</sub> = MAX., CE1 = V <sub>IH</sub> and CE2 = V <sub>IL</sub> , V <sub>OUT</sub> = V <sub>SS</sub> to V <sub>CC</sub>	Com'l/ Ind.	-5	5	-1	1	µA
V <sub>IL</sub>	Input Low Voltage			-0.5 <sup>(1)</sup>	0.8	-0.5 <sup>(1)</sup>	0.8	V
V <sub>IH</sub>	Input High Voltage			2.2	6.0	2.2	6.0	V
V <sub>OL</sub>	Output Low Voltage	I <sub>OL</sub> = 8 mA, V <sub>CC</sub> = Min. I <sub>OL</sub> = 10 mA, V <sub>CC</sub> = Min.		—	0.4 0.5	—	0.4 0.5	V V
V <sub>OH</sub>	Output High Voltage	I <sub>OH</sub> = -4 mA, V <sub>CC</sub> = Min.		2.4	—	2.4	—	V

NOTE: 1. V<sub>IL</sub>(min) = -3.0V for pulse width less than 20 ns

### Power Supply Characteristics

Symbol	Parameter	Power	-10		-12		-15	
			Com'l.	Ind.	Com'l.	Ind.	Com'l.	Ind.
I <sub>CC</sub>	Operating Current CE1 = V <sub>IL</sub> and CE2 = V <sub>IH</sub>  f = f <sub>MAX</sub> = 1/t <sub>RC</sub> V <sub>CC</sub> = Max. I <sub>OUT</sub> = 0 mA	SA	250	230	240	185	195	
		LA	230	210	220	165	175	
I <sub>SB</sub>	Standby Current CE1 = V <sub>IH</sub> and CE2 = V <sub>IL</sub>  f = f <sub>MAX</sub> = 1/t <sub>RC</sub> V <sub>CC</sub> = Max.	SA	80	70	70	55	55	
		LA	75	65	65	50	50	
I <sub>SB1</sub>	Full Standby Current CE1 ≥ V <sub>HC</sub> and CE2 ≤ V <sub>LC</sub>  f = 0 V <sub>CC</sub> = Max. V <sub>IN</sub> ≥ V <sub>CC</sub> - 0.2V or ≤ 0.2V	SA	20	20	25	10	15	
		LA	10	10	10	5	10	

SHADED AREAS = PRELIMINARY DATA

NOTES: All values are maximum guaranteed values.

V<sub>LC</sub> ≤ 0.2V, V<sub>HC</sub> ≥ V<sub>CC</sub> - 0.2V

**Capacitance<sup>(1)</sup>** ( $T_A = +25^\circ\text{C}$ ,  $f = 1.0\text{ MHz}$ )

Symbol	Parameter	Max.	Unit
$C_{IN}$	Input Capacitance	8	pF
$C_{OUT}$	Output Capacitance	8	pF

NOTE:1. This parameter is determined by device characterization but is not production tested.

**AC Test Conditions**

Input pulse levels	$V_{SS}$ to 3.0V
Input rise and fall times	3 ns
Input timing reference levels	1.5V
Output reference levels	1.5V
Output load	See Figures 1 and 2

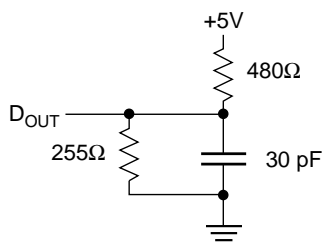


Figure 1. Output Load Equivalent

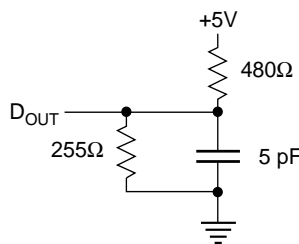


Figure 2. Output Load Equivalent  
(for  $t_{LZCE}$ ,  $t_{HZCE}$ ,  $t_{LZWE}$ ,  $t_{HZWE}$ ,  $t_{LZOE}$ ,  $t_{HZOE}$ )

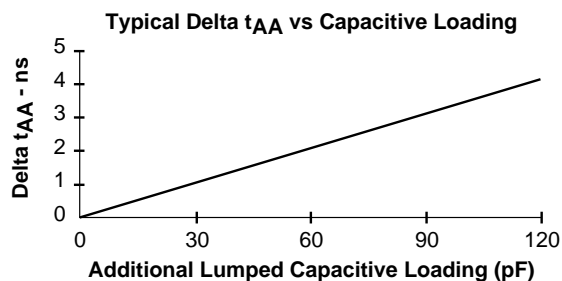
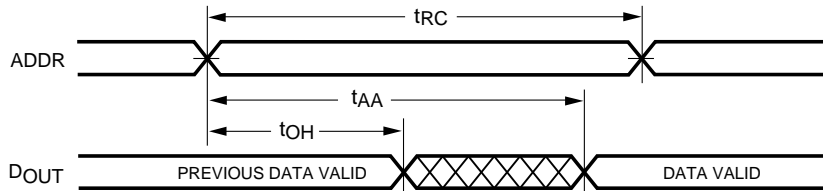
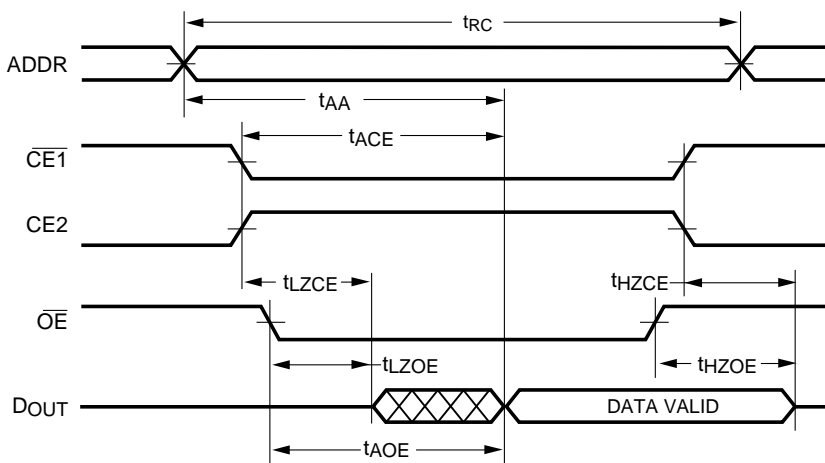


Figure 3.

**Read Cycle No. 1(4, 5)**



**Read Cycle No. 2(2, 4, 6)**



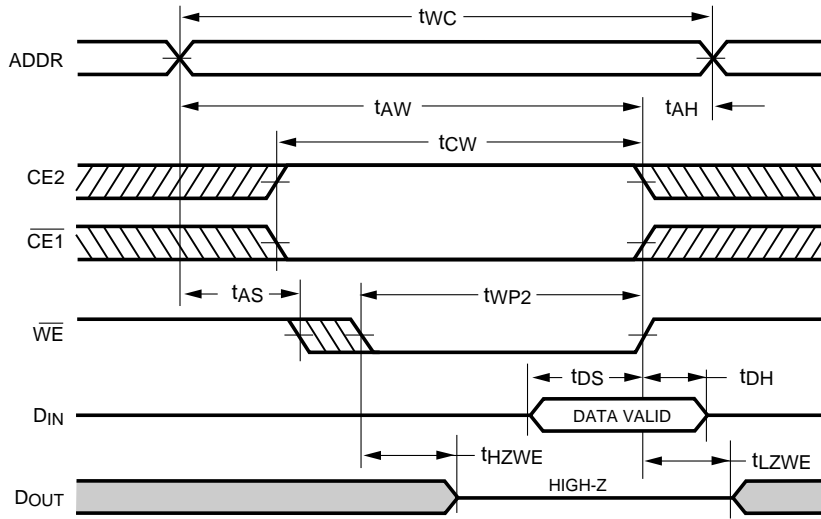
**AC Electrical Characteristics**

Description		-10 <sup>(7)</sup>		-12 <sup>(7)</sup>		-15		
READ Cycle	Sym	Min.	Max.	Min.	Max.	Min.	Max.	Units
READ cycle time	t <sub>RC</sub>	10		12		15		ns
Address access time	t <sub>AA</sub>		10		12		15	ns
Chip enable access time	t <sub>ACE</sub>		10		12		15	ns
Output hold from address change	t <sub>OH</sub>	3		3		3		ns
Chip enable to output in low Z <sup>(1,3)</sup>	t <sub>LZCE</sub>	5		5		5		ns
Chip disable to output in high Z <sup>(1,2,3)</sup>	t <sub>HZCE</sub>		6		6		7	ns
Chip enable to power up time <sup>(3)</sup>	t <sub>PU</sub>	0		0		0		ns
Chip disable to power down time <sup>(3)</sup>	t <sub>PD</sub>		10		12		15	ns
Output enable access time	t <sub>AOE</sub>		6		6		6	ns
Output enable to output in low Z <sup>(1,3)</sup>	t <sub>LZOE</sub>	0		0		0		ns
Output disable to output in high Z <sup>(1,3)</sup>	t <sub>HZOE</sub>		6		6		6	ns

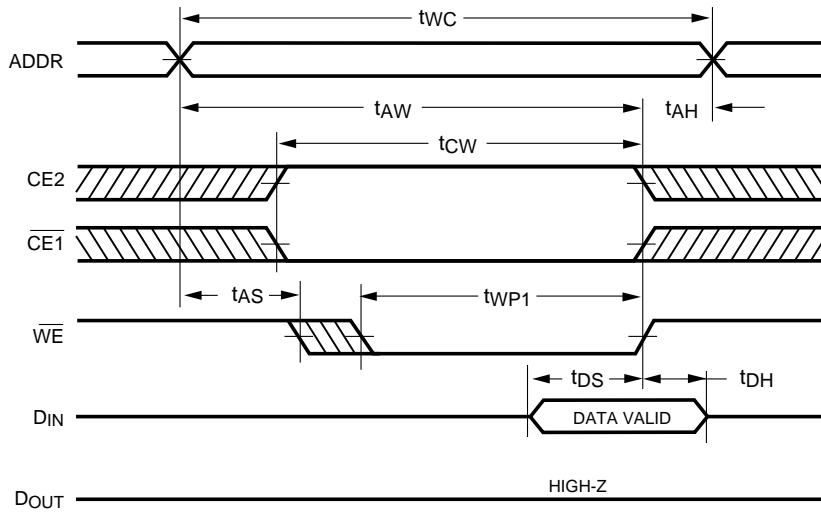
SHADED AREA = PRELIMINARY DATA

Notes referenced are after Data Retention Table.

**Write Cycle No. 1 (Write Enable Controlled)**

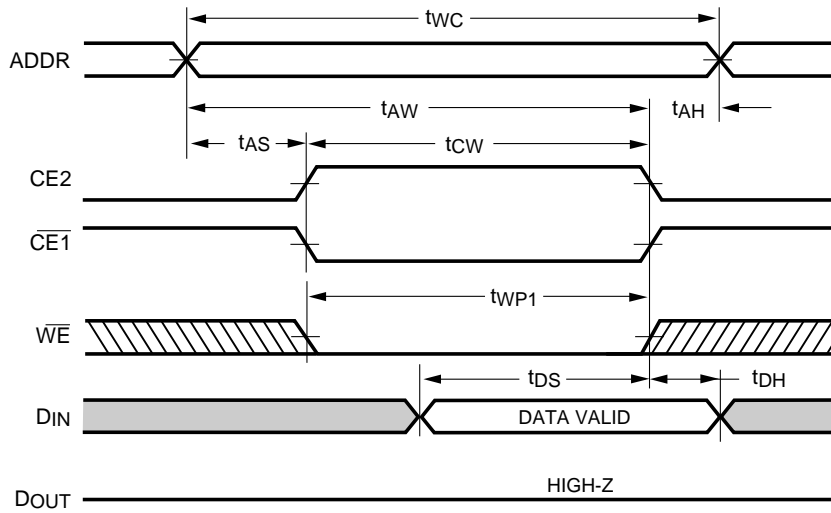


**Write Cycle No. 2 (Write Enable Controlled)**



NOTE: Output Enable ( $\overline{OE}$ ) is inactive (high)

**Write Cycle No. 3 (Chip Enable Controlled)**



NOTE: Output Enable ( $\overline{OE}$ ) is inactive (high)

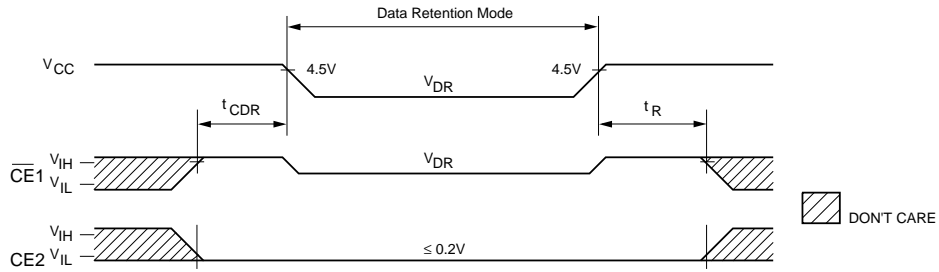
**AC Electrical Characteristics**

Description		-10 <sup>(7)</sup>		-12 <sup>(7)</sup>		-15		
WRITE Cycle	Sym	Min.	Max.	Min.	Max.	Min.	Max.	Units
WRITE cycle time	$t_{WC}$	10		12		15		ns
Chip enable active time	$t_{CW}$	10		10		11		ns
Address valid to end of write	$t_{AW}$	10		10		11		ns
Address setup time	$t_{AS}$	0		0		0		ns
Address hold from end of write	$t_{AH}$	0		0		0		ns
Write pulse width	$t_{WP1}$	8		8		11		ns
Write pulse width	$t_{WP2}$	8		8		12		ns
Data setup time	$t_{DS}$	7		7		7		ns
Data hold time	$t_{DH}$	0		0		0		ns
Write disable to output in low $Z^{(1,3)}$	$t_{LZWE}$	0		0		0		ns
Write enable to output in high $Z^{(1,3)}$	$t_{HZWE}$		7		7		7	ns

SHADED AREA = PRELIMINARY DATA

Notes referenced are after Data Retention Table

### Low V<sub>CC</sub> Data Retention Waveform



### Data Retention Electrical Characteristics (LA Version Only) for JEDEC Version

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>DR</sub>	V <sub>CC</sub> for Retention Data		2	—	—	V
I <sub>CCDR</sub>	Data Retention Current	$\overline{CE1} \geq V_{CC} - 0.2V$ or $\overline{CE2} \leq V_{SS} + 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $\leq 0.2V$	$V_{CC} = 2V$ $V_{CC} = 3V$	—	500 750	$\mu A$ $\mu A$
t <sub>CDR</sub>	Chip Deselect to Data Retention Time		0	—	—	ns
t <sub>R</sub> <sup>(3)</sup>	Operation Recovery Time		t <sub>RC</sub>	—	—	ns

NOTES: (For three previous Electrical Characteristics tables)

1. The parameter is tested with CL = 5 pF as shown in Figure 2. Transition is measured ±200 mV from steady state voltage.
2. At any given temperature and voltage condition, t<sub>HZCE</sub> is less than t<sub>LZCE</sub>.
3. This parameter is sampled.
4.  $\overline{WE}$  is high for a READ cycle.
5. The device is continuously selected. All the Chip Enables are held in their active state.
6. The address is valid prior to or coincident with the latest occurring Chip Enable.
7. V<sub>CC</sub> = 5V ± 5%.

### Ordering Information

