Electrical Characteristics Over the Operating Range[3]

Parameter	Description	Test Conditions		7B136-15 7B146-15		7B136-20 7B146-20		Unit
				Min.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	I_{OL} = 4.0 mA			0.4		0.4	V
		I_{OL} = 16.0 mA[4]			0.5		0.5	
V_{IH}	Input HIGH Voltage			2.2		2.2		V
V_{IL}	Input LOW Voltage				0.8		0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–10	+10	–10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–10	+10	–10	+10	µA
I_{CC}	V_{CC} Operating Supply Current	$\overline{CE}$ = V_{IL}, Outputs Open, f = f_{MAX}[5]	Com'l		260		240	mA
			Ind				300	
I_{SB1}	Standby Current Both Ports, TTL Inputs	$\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{IH}, f = f_{MAX}[5]	Com'l		110		100	mA
			Ind				105	
I_{SB2}	Standby Current One Port, TTL Inputs	$\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{IH}, Active Port Outputs Open, f = f_{MAX}[5]	Com'l		165		155	mA
			Ind				180	
I_{SB3}	Standby Current Both Ports, CMOS Inputs	Both Ports $\overline{CE}_L$ and $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, f = 0	Com'l		15		15	mA
			Ind				30	
I_{SB4}	Standby Current One Port, CMOS Inputs	One Port $\overline{CE}_L$ or $\overline{CE}_R$ ≥ V_{CC} – 0.2V, V_{IN} ≥ V_{CC} – 0.2V or V_{IN} ≤ 0.2V, Active Port Outputs Open, f = f_{MAX}[5]	Com'l		160		150	mA
			Ind				170	

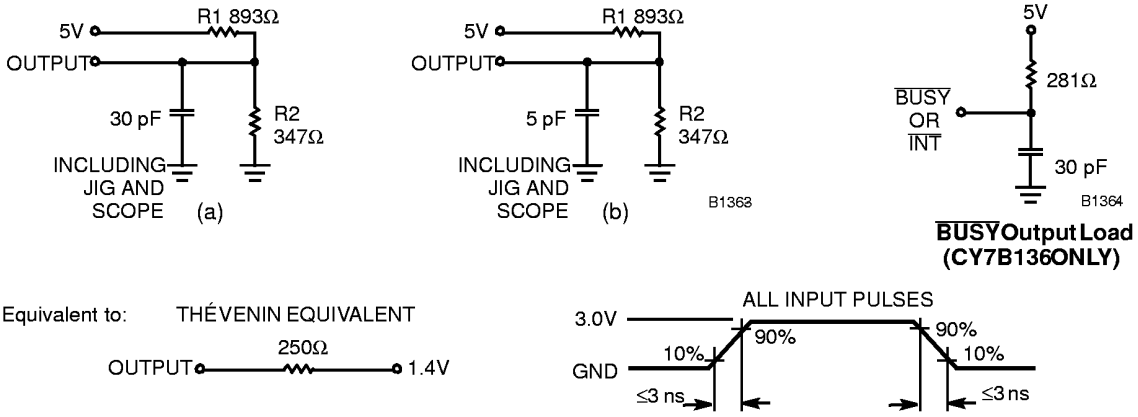
Notes:
3. See the last page of this specification for Group A subgroup testing information.
4. $\overline{BUSY}$ and $\overline{INT}$ pins only.
5. At f=f_{MAX}, address and data inputs are cycling at the maximum frequency of read cycle of $1/t_{rc}$ and using AC Test Waveforms input levels of GND to 3V.

Capacitance[6]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
6. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms



Switching Characteristics Over the Operating Range[3, 7]

Parameter	Description	7B136-15 7B146-15		7B136-20 7B146-20		Unit
		Min.	Max.	Min.	Max.	
READ CYCLE						
t_{RC}	Read Cycle Time	15		20		ns
t_{AA}	Address to Data Valid[8]		15		20	ns
t_{OHA}	Data Hold from Address Change	3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid[8]		15		20	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid[8]		10		13	ns
t_{LZOE}	$\overline{OE}$ LOW to Low Z[9]	3		3		ns
t_{HZOE}	$\overline{OE}$ HIGH to High Z[9,10]		10		13	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[9]	3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[9,10]		10		13	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		15		20	ns
WRITE CYCLE[11]						
t_{WC}	Write Cycle Time	15		20		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	12		15		ns
t_{AW}	Address Set-Up to Write End	12		15		ns
t_{HA}	Address Hold from Write End	2		2		ns
t_{SA}	Address Set-Up to Write Start	0		0		ns
t_{PWE}	R/$\overline{W}$ Pulse Width	12		15		ns
t_{SD}	Data Set-Up to Write End	10		13		ns

Notes:

7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH}, and 30-pF load capacitance.
8. AC test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
9. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
10. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE}, and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
12. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
13. CY7B146 only.
14. For information on port-to-port delay through RAM cells, from writing port to reading port, refer to the Read Timing with Port-to-Port Delay timing diagram.

Switching Characteristics Over the Operating Range[3, 7] (Continued)

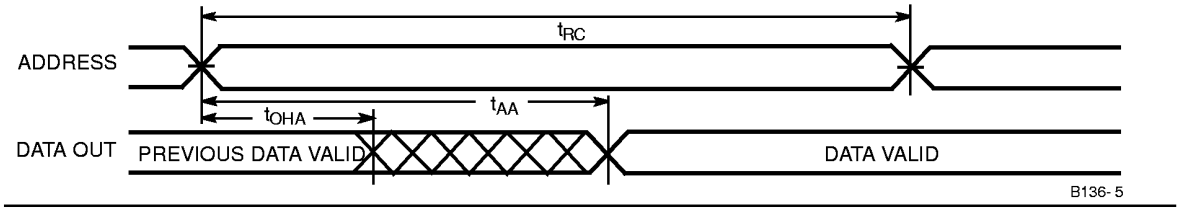
Parameter	Description	7B136-15 7B146-15		7B136-20 7B146-20		Unit
		Min.	Max.	Min.	Max.	
t_{HD}	Data Hold from Write End	0		0		ns
t_{HZWE}	R/$\overline{W}$ LOW to High Z		10		13	ns
t_{LZWE}	R/$\overline{W}$ HIGH to Low Z	3		3		ns
BUSY/INTERRUPT TIMING						
t_{BLA}	$\overline{BUSY}$ LOW from Address Match		15		20	ns
t_{BHA}	$\overline{BUSY}$ HIGH from Address Mismatch[12]		15		20	ns
t_{BLC}	$\overline{BUSY}$ LOW from $\overline{CE}$ LOW		15		20	ns
t_{BHC}	$\overline{BUSY}$ HIGH from $\overline{CE}$ HIGH[12]		15		20	ns
t_{PS}	Port Set Up for Priority	5		5		ns
t_{WB}[13]	R/$\overline{W}$ LOW after $\overline{BUSY}$ LOW	0		0		ns
t_{WH}	R/$\overline{W}$ HIGH after $\overline{BUSY}$ HIGH	13		20		ns
t_{BDD}	$\overline{BUSY}$ HIGH to Valid Data		15		20	ns
t_{DDD}	Write Data Valid to Read Data Valid[14]		25		30	ns
t_{WDD}	Write Pulse to Data Delay[14]]		30		40	ns
INTERRUPT TIMING						
t_{WINS}	R/$\overline{W}$ to $\overline{INTERRUPT}$ Set Time		15		20	ns
t_{EINS}	$\overline{CE}$ to $\overline{INTERRUPT}$ Set Time		15		20	ns
t_{INS}	Address to $\overline{INTERRUPT}$ Set Time		15		20	ns
t_{OINR}	$\overline{OE}$ to $\overline{INTERRUPT}$ Reset Time[12]		15		20	ns
t_{EINR}	$\overline{CE}$ to $\overline{INTERRUPT}$ Reset Time[12]		15		20	ns
t_{INR}	Address to $\overline{INTERRUPT}$ Reset Time[[12]		15		20	ns

Notes:

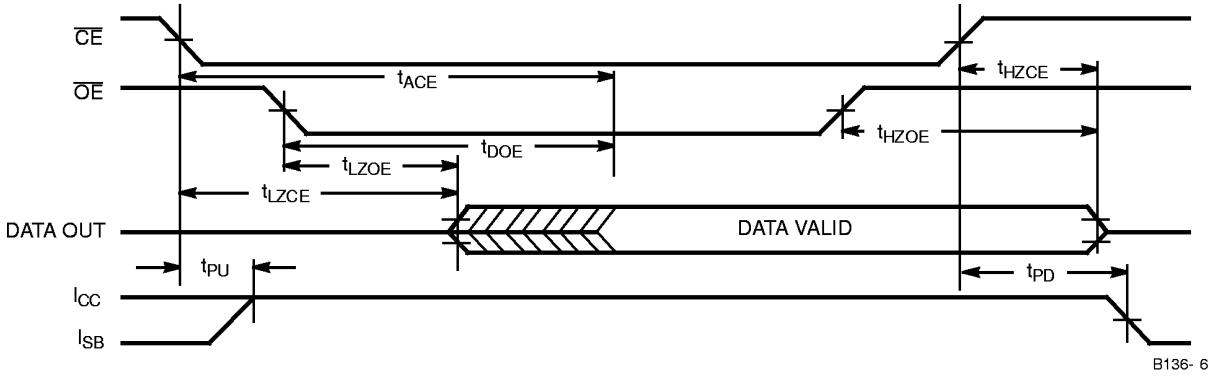
7. Test conditions assume signal transition times of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
8. AC test conditions use V_{OH} = 1.6V and V_{OL} = 1.4V.
9. At any given temperature and voltage condition for any given device, t_{HZCE} is less than t_{LZCE} and t_{HZOE} is less than t_{LZOE}.
10. t_{LZCE}, t_{LZWE}, t_{HZOE}, t_{LZOE}, t_{HZCE}, and t_{HZWE} are tested with C_L = 5pF as in part (b) of AC Test Loads. Transition is measured ±±500 mV from steady-state voltage.
11. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and R/$\overline{W}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input setup and hold timing should be referenced to the rising edge of the signal that terminates the write.
12. These parameters are measured from the input signal changing, until the output pin goes to a high-impedance state.
13. CY7B146 only.
14. For information on port-to-port delay through RAM cells, from writing port to reading port, refer to the Read Timing with Port-to-Port Delay timing diagram.

Switching Waveforms

Read Cycle No. 1 (Either Port-Address Access) [15,16]

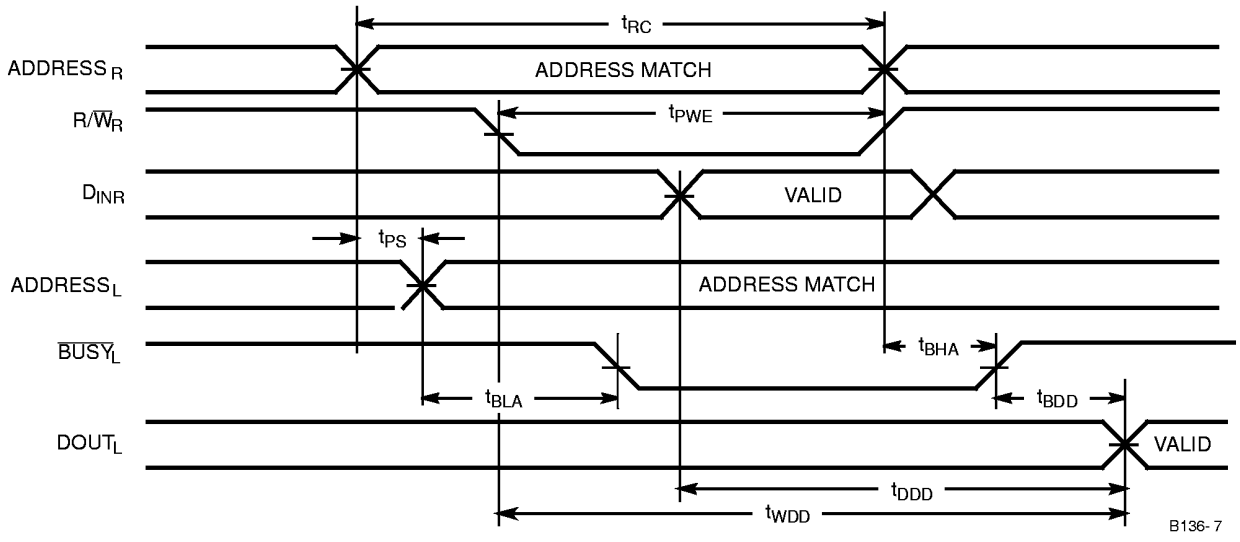


Read Cycle No. 2 (Either Port-CE/OE) [15,17]



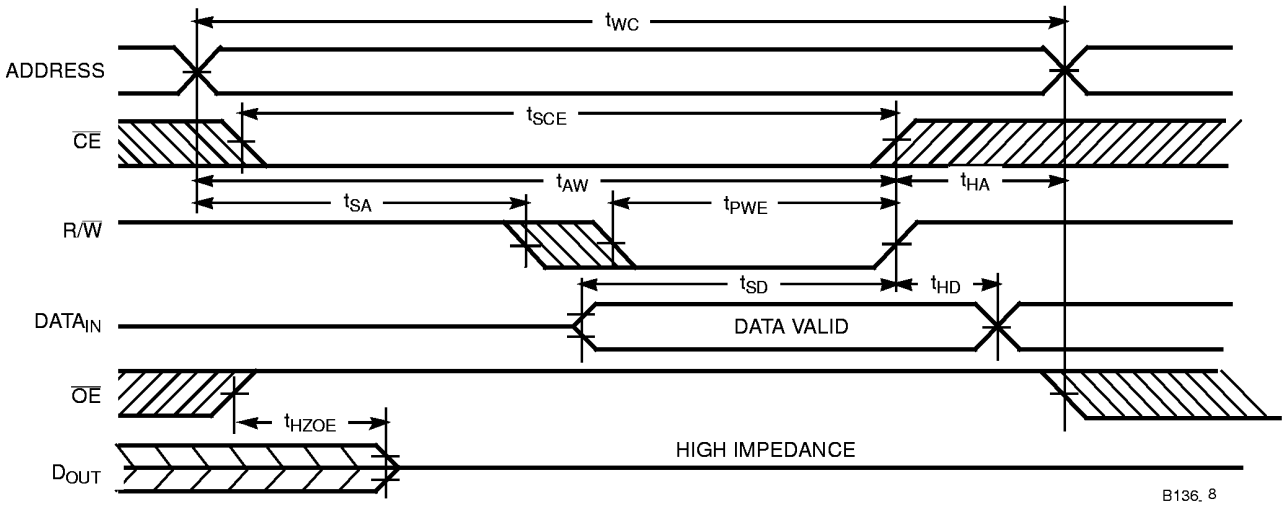
Notes:
15. R/$\overline{W}$ is HIGH for read cycle.
16. Device is continuously selected, $\overline{CE} = V_{IL}$ and $\overline{OE} = V_{IL}$.
17. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Read Cycle No.3 (Read with $\overline{BUSY}$ Master: CY7B136)



Switching Waveforms (Continued)

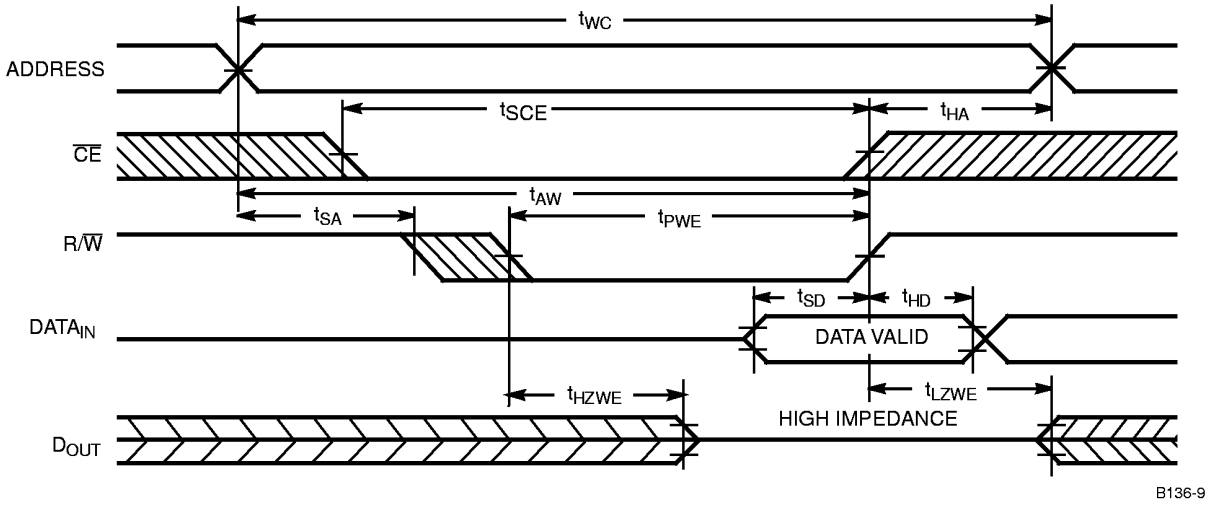
Write Cycle No. 1(OE Three-States Data I/Os-Either Port)[11,18]



Notes:

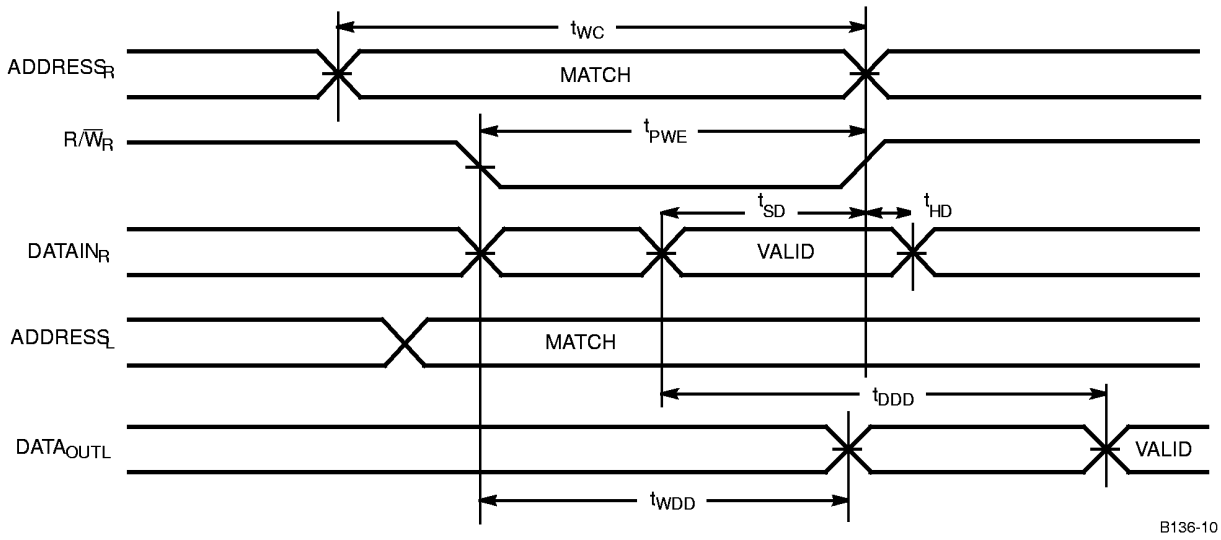
18. If $\overline{OE}$ is LOW during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{PWE} or $t_{HZWE} + t_{SD}$ to allow the data I/O pins to enter high impedance and for data to be placed on the bus for the required t_{SD}.

Write Cycle No. 2 (R/$\overline{W}$ Three-States Data I/Os — Either Port)[11, 19]



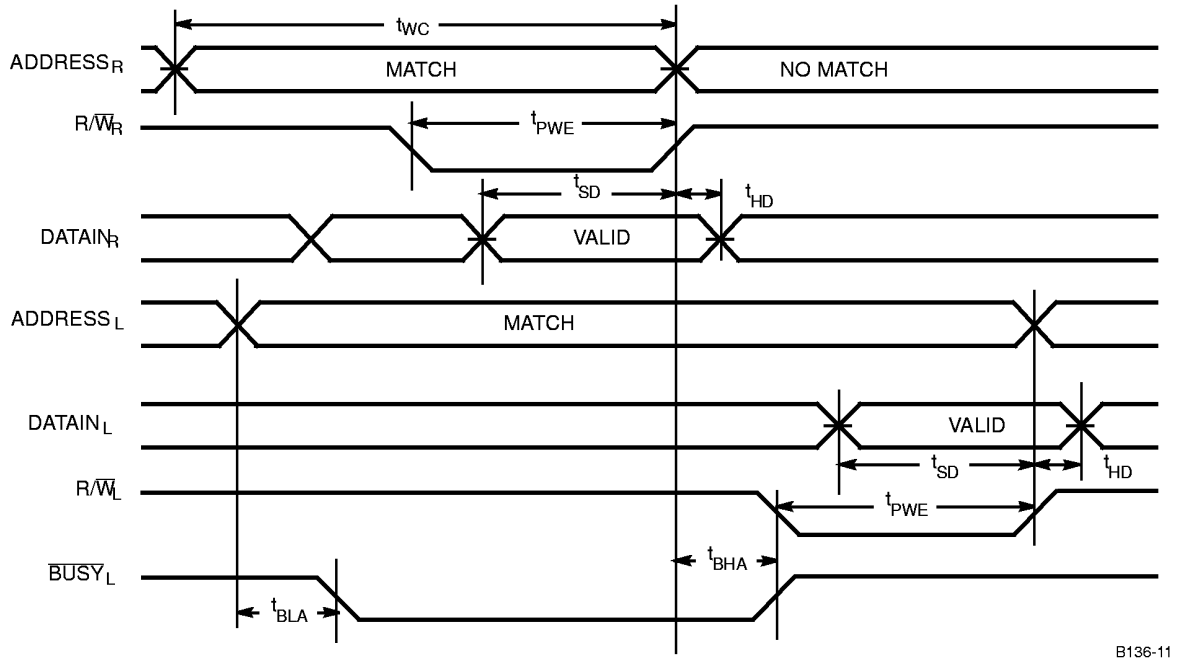
Switching Waveforms (Continued)

Read Timing with Port-to-Port Delay ($\overline{CE}_L$=$\overline{CE}_R$=LOW, $\overline{BUSY}$=HIGH for the Writing Port)



Notes:
19. If the $\overline{CE}$ LOW transition occurs simultaneously with or after the R/$\overline{W}$ LOW transition, the outputs remain in a high-impedance state.

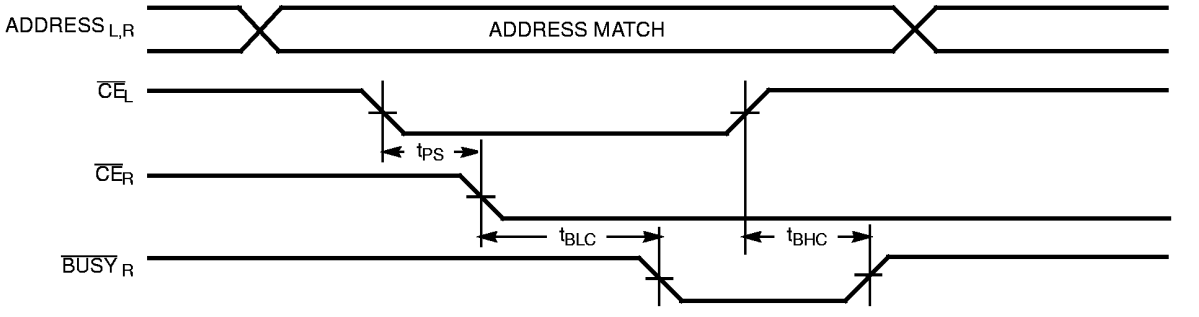
Write Timing with Port–to–Port Delay ($\overline{CE}_L$ + $\overline{CE}_R$ = LOW)



Switching Waveforms (Continued)

Busy Timing Diagram No. 1 ($\overline{CE}$ Arbitration)

$\overline{CE}_L$ Valid First:



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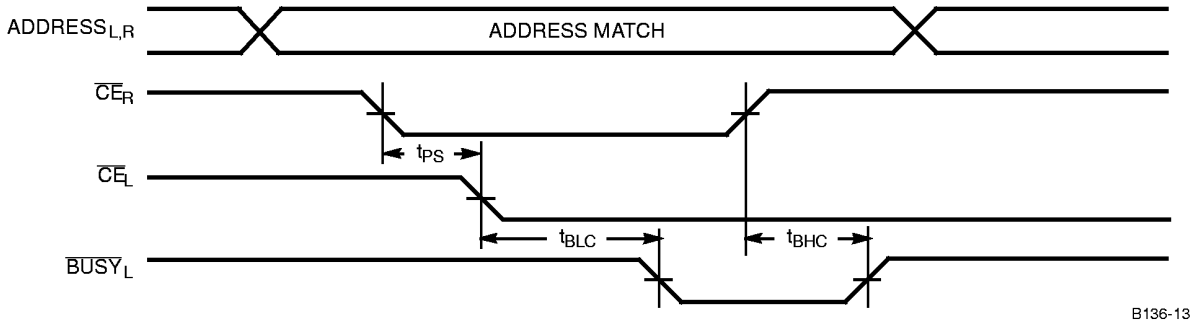
$\overline{CE}_R$ Valid First:

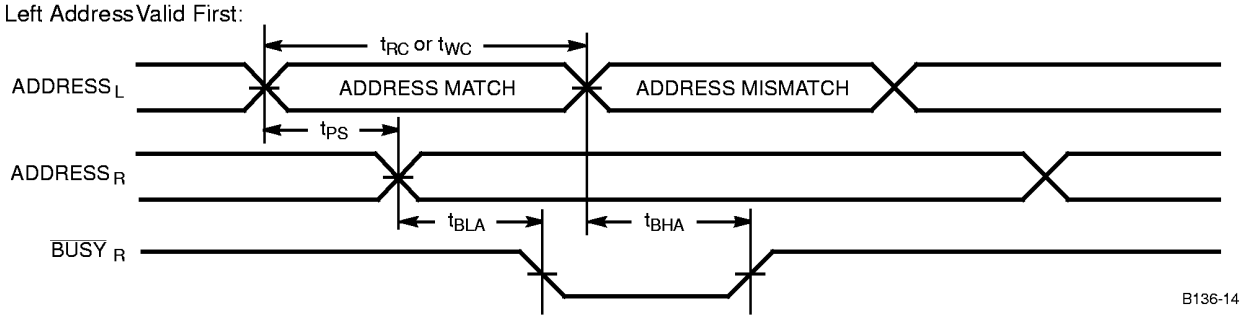


B136-13

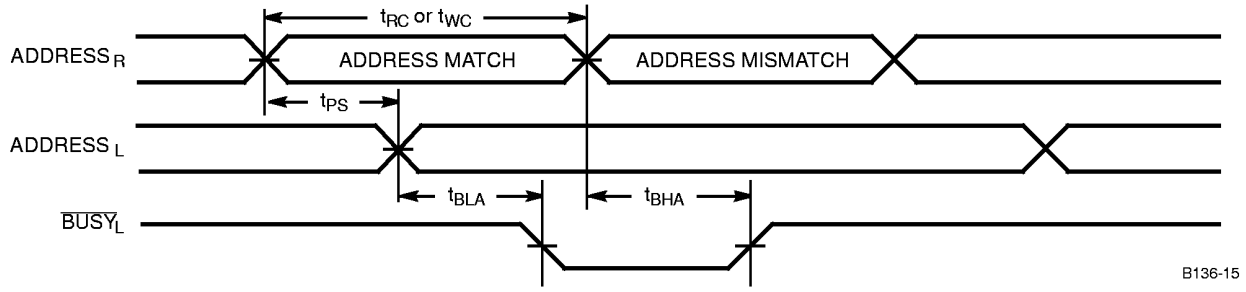
Switching Waveforms (Continued)

Busy Timing Diagram No.2 (AddressArbitration)

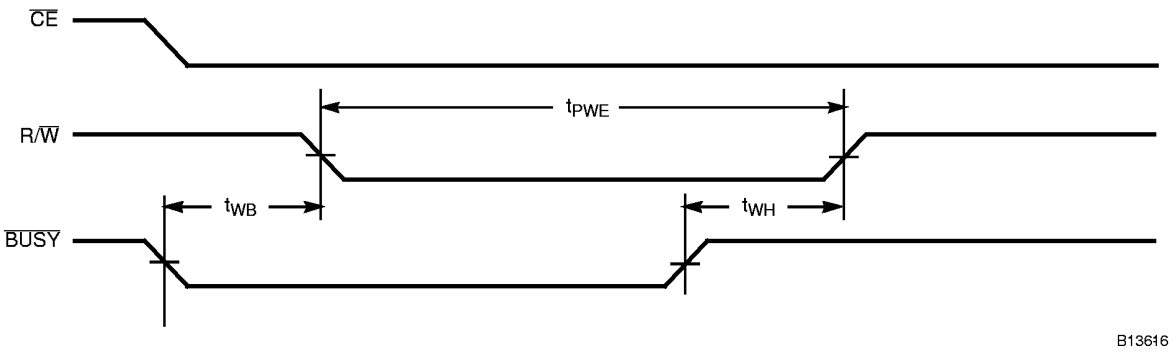
Left AddressValid First:



Right AddressValid First:

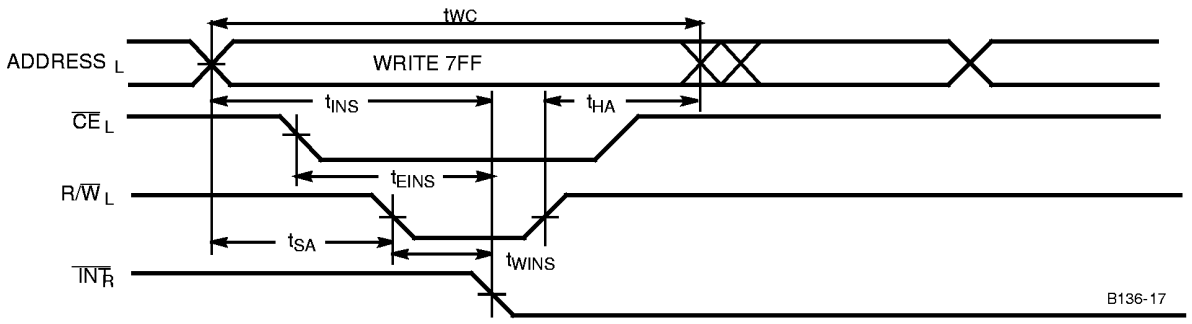


Busy Timing Diagram No.3 (Write with $\overline{BUSY}$, Slave:CY7B146)

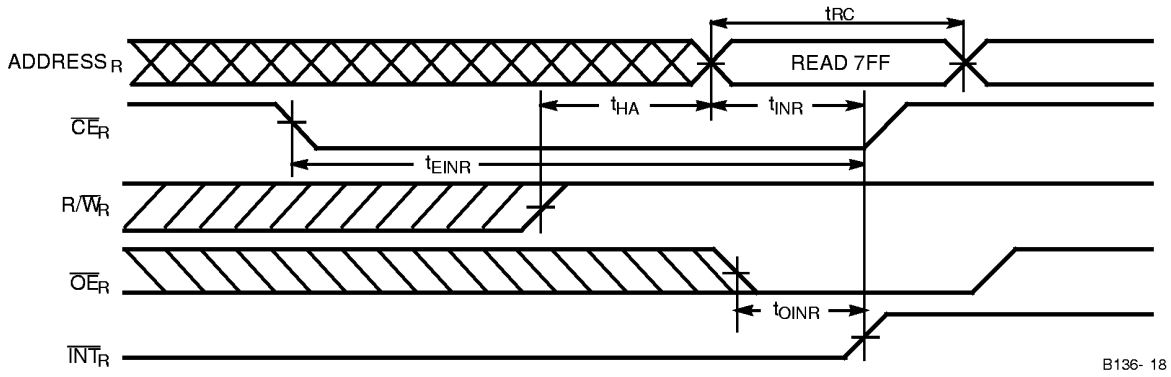


Interrupt Timing Diagrams

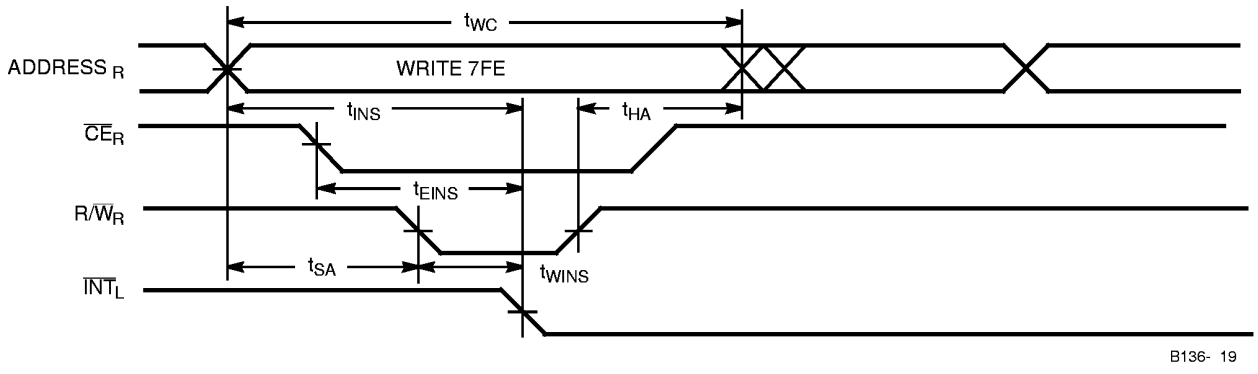
Left Side Sets $\overline{INT}_R$:



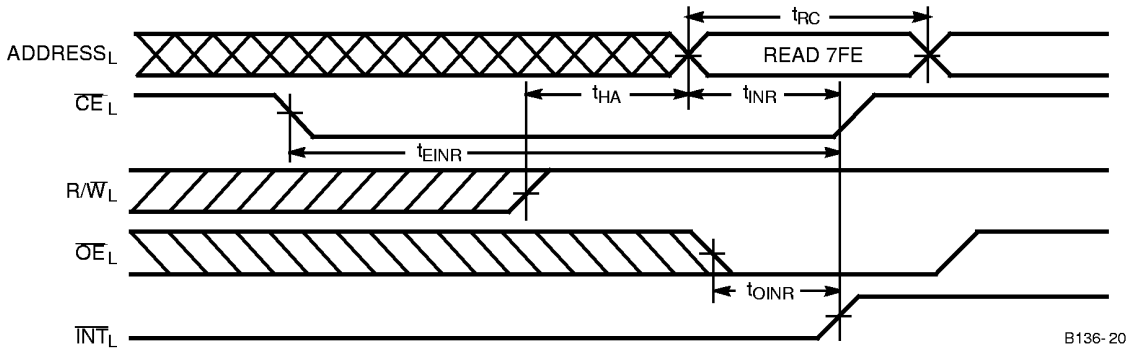
Right Side Clears $\overline{INT}_R$:



Right Side Sets $\overline{INT}_L$:



Left Side Clears $\overline{INT}_L$:



Architecture

The CY7B136 (master) and CY7B146 (slave) are 2048-byte deep dual-port RAMs, with two independent sets of address signals, common I/O data signals, and control signals. By convention, the two ports are called the left port and the right port. The subscript R or L on the signal name identifies the port.

The upper two memory locations (7FF, 7FE) are special locations and may be used as "mailboxes" for passing messages between the ports. Location 7FF is the mailbox for the right port and location 7FE is the mailbox for the left port. When one port writes to the other port's mailbox, an interrupt is generated to the owner of the mailbox. When the owner reads the mailbox, the interrupt is reset.

The address and control signals provide independent, asynchronous, random access to any location in the memory. It is possible that both ports may attempt to access the same memory location at the same time. If this contention occurs, a circuit in the master called an arbiter decides which port temporarily "owns" the memory location. The losing port receives a BUSY signal, which notifies it that the memory location is owned by the other port and that the operation it attempted to perform may not be successful.

The two BUSY signals are outputs from the master and inputs to the slave.

Contention, Arbitration and Resolution— The Significance of BUSY

When contention occurs, the arbiter decides which port wins (owns) the memory location and which port loses. The decision is on a "first-come-first-served" basis. In order for contention to occur, both ports must address the same memory location and have their respective chip enables active. If one port precedes the other by an amount of time greater than or equal to t_{PS} (port set-up for priority;equal to five nanoseconds) it is guaranteed to win the arbitration. If contention occurs within the t_{PS} interval, it is not possible to predict which port will win, but one will win and the other will lose.

There are two ports and each may be either reading or writing, and each may win or lose, so there are eight combinations. They are listed in *Table 1.* and identified as cases one through eight. In cases one and two, both ports are reading, the losing port receives a BUSY, the read is allowed to occur, and the data read by both ports is valid. In case three, the left port wins and reads valid data, and the write attempted by the right port is inhibited. In cases four and five, when the winning port is writing, the write is completed, but the data read by the losing port may be invalid. Case six is similar to case three; the right port successfully reads and the write attempt by the left port is inhibited. In cases seven and eight the winning port successfully writes and the attempted write by the losing port is inhibited.

In cases four and five, where the losing port is reading, if the port signals are asynchronous to each other, the data read may be the old data, the new data, or some random combination of the two sets of data. In cases seven and eight the losing port is prevented from writing. The commonality between these four cases is that the losing port receives a busy signal, which tells it that either (1) the operation it attempted was not successful, or (2) that the data it read may not be valid. In either situation, the operation should be repeated after the busy signal becomes inactive.

Flow-Through Operation

The CY7B136/146 have a flow-through architecture that facilitates repeating (actually extending) an operation when a BUSY is received by a losing port. The BUSY signal should be interpreted as a NOT READY. If a BUSY to a port is active, the port should wait for BUSY to go inactive, and then extend the operation it was performing for another cycle. The timing diagram titled, "Read Timing with Port-to-Port Delay" illustrates the case where the right port is writing to an address and the left port reads the same address. The data that the right port has just written flows through to the left, and is valid either t_{WDD} after the falling edge of the write strobe of the left port, or t_{DDD} after the data being written becomes stable.

The timing diagram titled, "Write Timing with Port-to-Port Delay" illustrates the case where the right port is writing to an address and the left port wants to write to the same address. If the left port extends its write strobe for a minimum time of t_{PWE} after the BUSY signal to it goes inactive, its write will be successful; it writes over the data just written by the right port.

Data Bus Width Expansion Using Slaves

One master and as many slaves as necessary may be connected in parallel to expand the data bus width in byte increments.

Two masters must not be connected in parallel because, if the time interval between which they address the same location is less than t_{PS}, both could end up waiting for the other to release the BUSY to it.

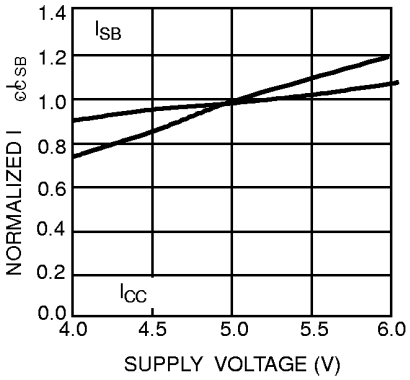
Therefore, only one master must arbitrate, and it can drive as many slaves as required. The write strobe to the slaves must be delayed an amount of time equal to at least t_{BLA}. This insures that the slave is not inadvertently written to before the outcome of the arbitration is determined.

Table 1. Operation.

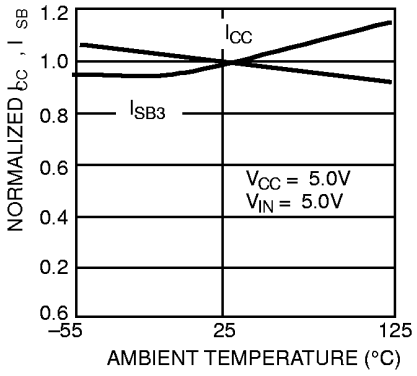
Case	Operation Port		Winning Port	Result
	L	R		
1	R	R	L	Both Read
2	R	R	R	Both Read
3	R	W	L	L Reads OK, R Write Inhibited
4	R	W	R	R Writes OK L Data May Be Invalid
5	W	R	L	L writes OK R Data May Be Invalid
6	W	R	R	R Reads OK L Write Inhibited
7	W	W	L	L Writes OK R Write Inhibited
8	W	W	R	R Writes OK L Write Inhibited

Typical DC and AC Characteristics

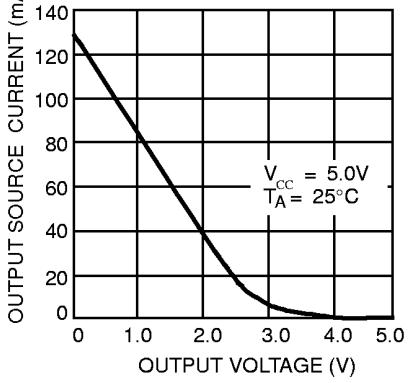
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



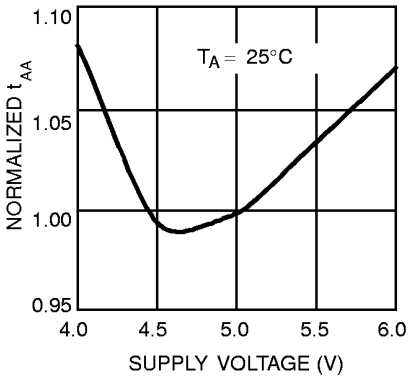
NORMALIZED SUPPLY CURRENT vs. AMBIENT TEMPERATURE



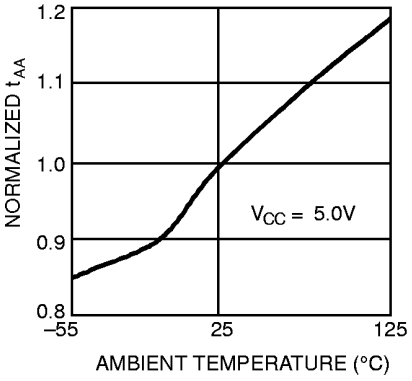
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



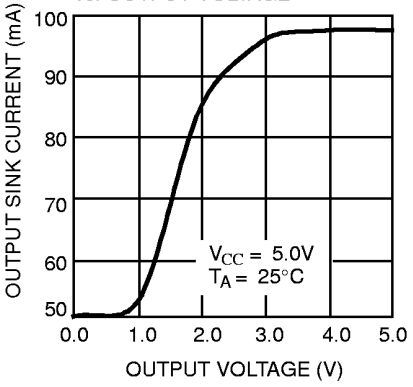
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



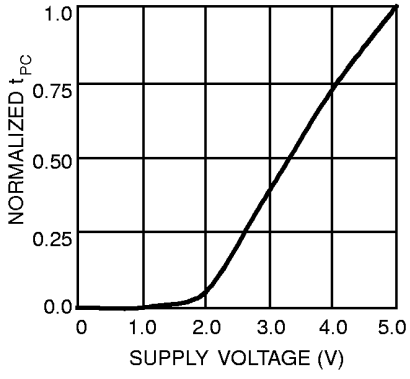
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



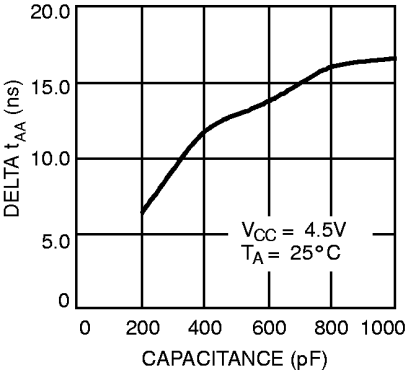
OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



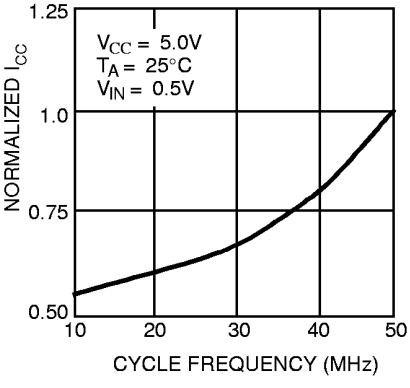
TYPICAL POWER- ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED ICC vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B136-15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
20	CY7B136-20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B136-20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
15	CY7B146-15JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
20	CY7B146-20JC	J69	52-Lead Plastic Leaded Chip Carrier	Commercial
	CY7B146-20JI	J69	52-Lead Plastic Leaded Chip Carrier	Industrial

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Package Diagram

52-Lead Plastic Leaded Chip Carrier J69