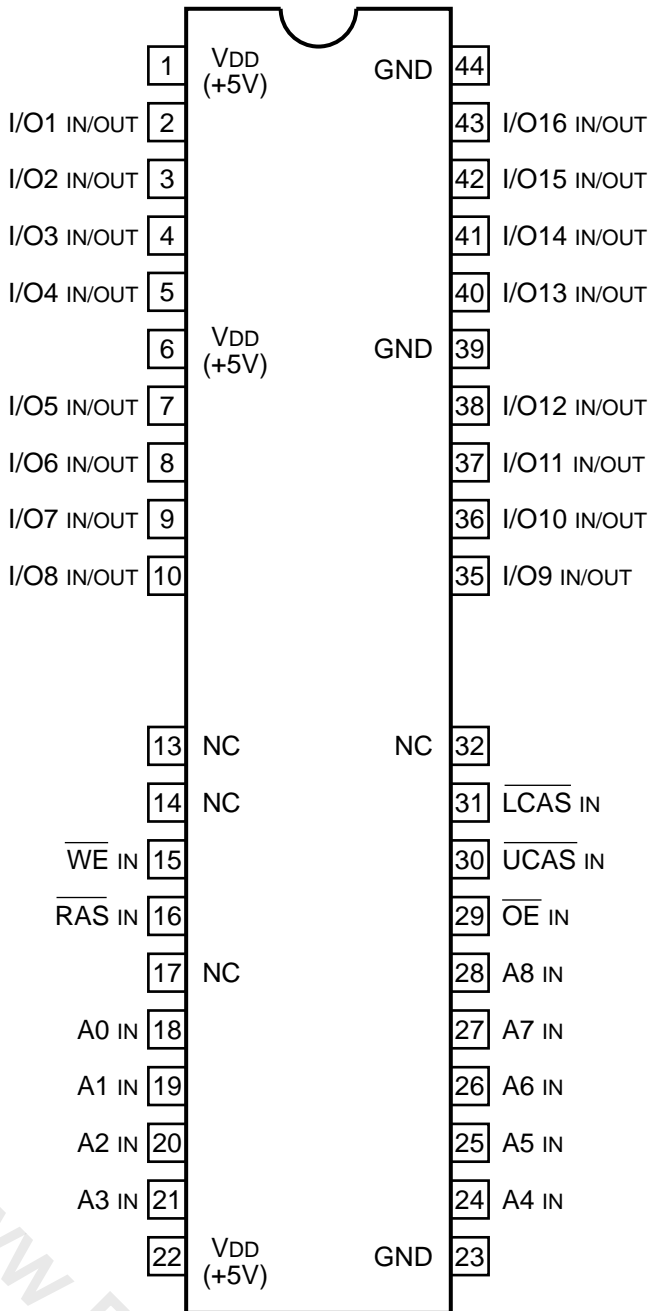

C-MOS 4M (262,144 x 16) BIT DYNAMIC RAM
-TOP VIEW-



18	A0	I/O1	2
19	A1	I/O2	3
20	A2	I/O3	4
21	A3	I/O4	5
24	A4	I/O5	7
25	A5	I/O6	8
26	A6	I/O7	9
27	A7	I/O8	10
28	A8	I/O9	35
		I/O10	36
		I/O11	37
16	RAS	I/O12	38
30	UCAS	I/O13	40
31	LCAS	I/O14	41
15	WE	I/O15	42
29	OE	I/O16	43

- A0-8 ; ADDRESS INPUTS
- I/O1-16 ; DATA INPUTS/OUTPUTS
- $\overline{\text{RAS}}$; ROW ADDRESS STROBE INPUT
- $\overline{\text{UCAS}}$; COLUMN ADDRESS STROBE (UPPER) INPUT
- $\overline{\text{LCAS}}$; COLUMN ADDRESS STROBE (LOWER) INPUT
- $\overline{\text{WE}}$; WRITE ENABLE INPUT
- $\overline{\text{OE}}$; OUTPUT ENABLE INPUT

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