37–39 GHz GaAs MMIC Power Amplifier

AA038P5-00

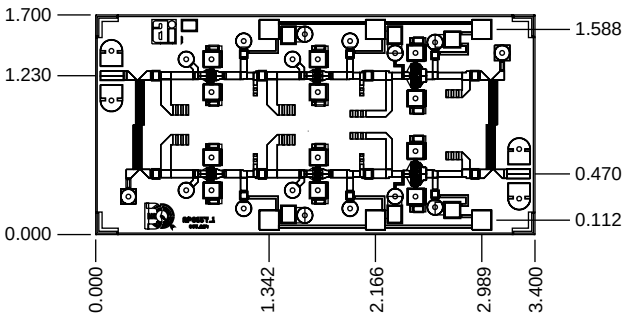
Features

- Single Bias Supply Operation (5.5 V)
- 18 dB Typical Small Signal Gain
- 19 dBm Typical $P_{1\ dB}$ Output Power at 39 GHz
- 0.25 µm Ti/Pd/Au Gates
- 100% On-Wafer RF and DC Testing
- 100% Visual Inspection to MIL-STD-883 MT 2010

Description

Alpha's three-stage reactively-matched Ka band GaAs MMIC amplifier has a typical $P_{1\ dB}$ of 19 dBm with 17 dB associated gain over the band 37–39 GHz. The chip uses Alpha's proven 0.25 µm MESFET technology, and is based upon MBE layers and electron beam lithography for the highest uniformity and repeatability. The FETs employ surface passivation to ensure a rugged, reliable part with through-substrate via holes and gold-based backside metallization to facilitate an epoxy die attach process. All chips are screened for small signal S-parameters and power characteristics prior to shipment for guaranteed performance. A broad range of applications exist in both the high reliability and commercial areas where power and gain are required.

Chip Outline



Dimensions indicated in mm.
All DC (V) pads are 0.1 x 0.1 mm and RF In, Out pads are 0.07 mm wide.
Chip thickness = 0.1 mm.

Absolute Maximum Ratings

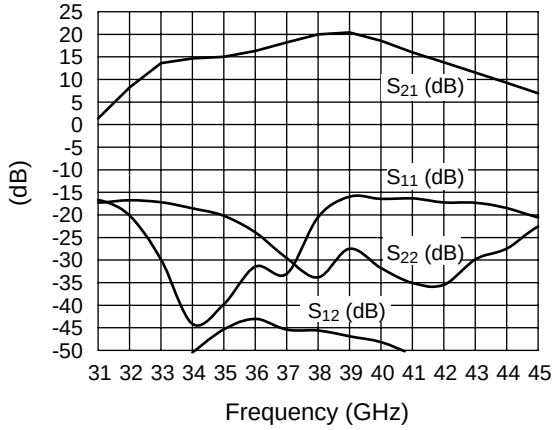
Characteristic	Value
Operating Temperature (T_C)	-55°C to +90°C
Storage Temperature (T_{ST})	-65°C to +150°C
Bias Voltage (V_D)	7 V_{DC}
Power In (P_{IN})	19 dBm
Junction Temperature (T_J)	175°C

Electrical Specifications at 25°C (V_{DS} = 5.5 V)

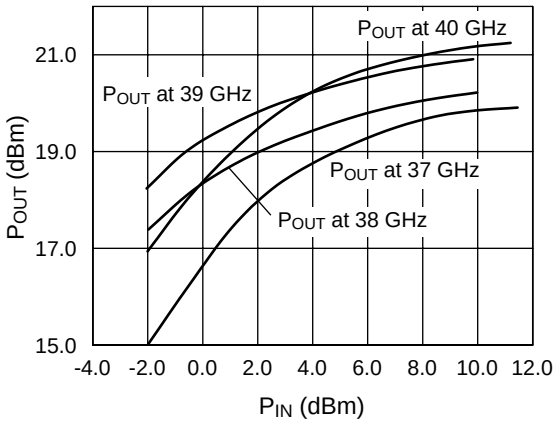
Parameter	Condition	Symbol	Min.	Typ.	Max.	Unit
Drain Current (at Saturation)		I_{DS}		200	370	mA
Small Signal Gain	F = 37–39 GHz	G	16	18		dB
Input Return Loss	F = 37–39 GHz	RL_I		-13	-10	dB
Output Return Loss	F = 37–39 GHz	RL_O		-20	-10	dB
Output Power at 1 dB Gain Compression	F = 39 GHz	$P_{1\ dB}$	16	19		dBm
Saturated Output Power	F = 39 GHz	P_{SAT}	19	21		dBm
Gain at Saturation	F = 39 GHz	G_{SAT}		15		dB
Thermal Resistance[1]		Θ_{JC}		51		°C/W

1. Calculated value based on measurement of discrete FET.

Typical Performance Data

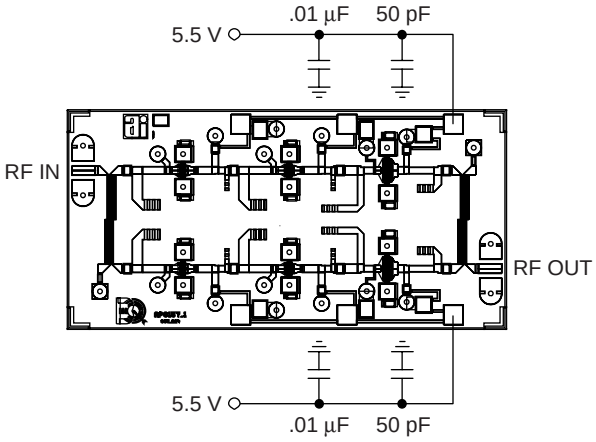


Typical S-Parameters



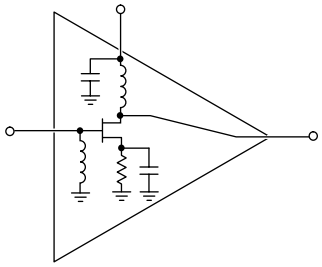
Typical Power Sweep

Bias Arrangement



For biasing on, adjust V_{DS} from zero to the desired value (5.5 V recommended). For biasing off, reverse the biasing on procedure.

Circuit Schematic



Detail A