

Preliminary Data Sheet

VSC7923

SONET/SDH 2.5Gb/s Laser Diode Driver

Features

- Rise Times Less Than 100ps
- High Speed Operation (Up to 2.4Gb/s NRZ Data)
- Single-Ended or Differential Input Operation
- Single Power Supply
- Direct Access to Modulation and Bias FETs
- Data Density Monitors

Applications

- SONET/SDH at 622Mb/s, 1.244Gb/s, 2.488Gb/s, 3.125Gb/s
- Full-Speed Fibre Channel (1.062Gb/s)

General Description

The VSC7923 is a single 5V supply, 2.4 Gb/s laser diode driver with direct access to the laser modulation and bias FET's. Laser bias and modulation currents are set by external components allowing precision monitoring and setting of the current levels. Data inputs accept ECL levels. Data density outputs are provided to allow the user to adjust the laser bias in high unbalanced data applications.

VSC7923 Block Diagram

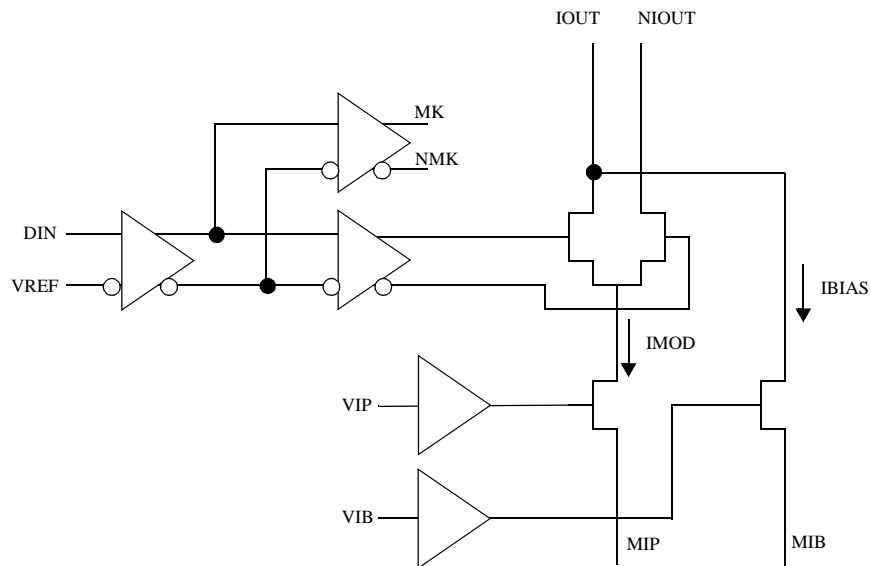


Table 1: Signal Pin Reference

<i>Signal</i>	<i>Type</i>	<i>Level</i>	<i># Pins</i>	<i>Description</i>
DIN	In	ECL	1	Data Input
MK, NMK	Out	ECL	2	Data Density Differential Outputs
NIOUT	Out		1	Laser Modulation Current Output (Complementary)
IOUT	Out		1	Laser Modulation Current Output (To Laser Cathode))
VSS	Pwr	Pwr	5	Negative Voltage Rail
GND	Pwr	Pwr	9	Positive Voltage Rail
VIP	In	DC	1	Modulation Gate Node
MIP	In	DC	1	Modulation Source Node
VIB	In	DC	1	Bias Gate Node
MIB	In	DC	1	Bias Source Node
VREF	In	DC	1	Data Input Reference
Total Pins			24	

Table 2: Absolute Maximum Ratings

<i>Symbol</i>	<i>Rating</i>	<i>Limit</i>
V _{SS}	Negative Power Supply Voltage	V _{CC} to -6.0V
T _J	Maximum Junction Temperature	-55°C to +125°C
T _{STG}	Storage Temperature	-65°C to +150°C

Table 3: Recommended Operating Conditions

<i>Symbol</i>	<i>Parameter</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>	<i>Conditions</i>
GND	Positive Voltage Rail	—	0	—	V	
VSS	Negative Voltage Rail	-5.5	-5.2	-4.9	V	
T _{Cl}	Operational Temperature ⁽¹⁾	-40	—	85 ⁽²⁾	°C	Power dissipation = 1.25W
T _J	Junction Temperature	—	—	125	°C	

NOTES: (1) Lower limit of specification is ambient temperature and upper limit is case temperature. (2) See section "Calculation of the Maximum Case Temperature" for detailed maximum temperature calculations.

Table 4: ECL Input and Outputs

<i>Symbol</i>	<i>Parameter</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>	<i>Conditions</i>
V _{IN}	Input Voltage Swing	300	—	800	mV	Peak-to-peak, V _{REF} = -2.0V
V _{OH}	ECL Output High Voltage	-1200	—	—	mV	50Ω to -2.0V
V _{OL}	ECL Output Low Voltage	—	—	-1600	mV	50Ω to -2.0V

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Table 5: Power Dissipation

<i>Symbol</i>	<i>Parameter</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>	<i>Conditions</i>
I_{VSS}	Power Supply Current (VSS)	—	—	220	mA	$V_{SS} = -5.5V, I_{MOD} = I_{BIAS} = 0mA$
P_D	Total Power Dissipation	—	—	1210	mW	$V_{SS} = -5.5V, I_{MOD} = I_{BIAS} = 0mA,$ $R_{LOAD} = 25\Omega$ to GND
P_{DMAX}	Maximum Power Dissipation	—	—	1815	mW	$V_{SS} = -5.5V, I_{MOD} = 60mA,$ $I_{BIAS} = 50mA, I_{OUT} = 0V$

Table 6: Laser Driver DC Electrical Specifications

<i>Symbol</i>	<i>Parameter</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>	<i>Conditions</i>
I_{BIAS}	Programmable Laser Bias Current	2	—	50	mA	—
I_{MOD}	Programmable Modulation Current	2	—	60	mA	—
V_{IB}	Laser Bias Control Voltage	—	—	$V_{SS} + 2.1$	V	$I_{BIAS} = 50mA$
V_{IP}	Laser Modulation Control Voltage	—	—	$V_{SS} + 2.1$	V	$I_{MOD} = 60mA$
V_{OCM}	Output Voltage Compliance	GND - 2.2V	—	—	V	$V_{SS} = -5.2V$

Table 7: Laser Driver AC Electrical Specifications

<i>Symbol</i>	<i>Parameter</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>	<i>Conditions</i>
t_R, t_F	Output Rise and Fall Times	—	—	100	ps	25 Ω load, 20%-80%, 15mA < I_{MOD} < 60mA, $I_{BIAS} = 20mA$

Table 8: Package Thermal Specifications

<i>Symbol</i>	<i>Parameter</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Units</i>	<i>Conditions</i>
θ_{JCC}	Thermal Resistance from Junction-to-Case	—	25	—	$^{\circ}C/W$	Ceramic Package
θ_{JCMG}	Thermal Resistance from Junction-to-Case	—	32	—	$^{\circ}C/W$	Metal Glass Package

Calculation of the Maximum Case Temperature

The VSC7923 is designed to operate with a maximum junction temperature of 125°C. The rise from the case to junction is determined by the power dissipation of the device. The power dissipation is determined by the V_{SS} current plus the operating I_{MOD} and I_{BIAS} currents.

The power of the chip is determined by the following formula:

$$P_D = (-V_{SS} * I_{SS}) + ((V_{IOUT} - V_{SS}) * I_{MOD}) + ((V_{IBIAS} - V_{SS}) * I_{BIAS})$$

For example with:

$$\begin{aligned} V_{SS} &= -5.2V \\ I_{MOD} &= 40mA \\ I_{BIAS} &= 20mA \\ V_{IBIAS} &= -2.0V \\ V_{IOUT} &= -2.0V \end{aligned}$$

$$P_D = 5.2 * 220mA + ((5.2 - 2.0) * 40mA) + ((5.2 - 2.0) * 20mA)$$

$$P_D = 1144mW + 128mW + 64mW = 1.336W$$

The thermal rise from junction to case is $\theta_{JC} * P_D$. For the metal glass package, $\theta_{JC} = 32 \text{ } ^\circ\text{C/W}$. Thus the thermal rise is:

$$32^\circ\text{C/W} * 1.336W = 42.7^\circ\text{C}$$

The maximum case temperature is:

$$125^\circ\text{C} - 42.7^\circ\text{C} = 82.3^\circ\text{C}$$

The absolute maximum power dissipation of the device is at:

$$\begin{aligned} V_{SS} &= -5.5V \\ I_{MOD} &= 60mA \\ I_{BIAS} &= 50mA \\ V_{IBIAS} &= 0V \\ V_{IOUT} &= 0V \end{aligned}$$

$$P_D = (5.5 * 220mA) + (5.5 * 60mA) + (5.5mA * 50mA)$$

$$P_D = 1.815W$$

This will net a maximum junction to case thermal rise of: $1.815W * 32^\circ\text{C/W} = 58^\circ\text{C}$

This situation will allow maximum case temperature of: $125^\circ\text{C} - 58^\circ\text{C} = 67^\circ\text{C}$

Input Termination Schemes

Figure 1: Input Structure

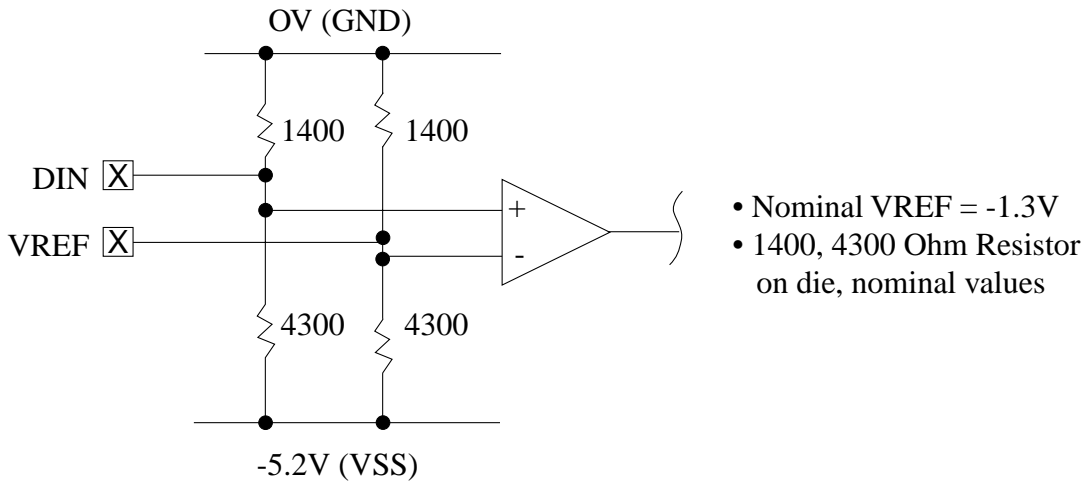


Figure 2: Single Ended AC Coupled

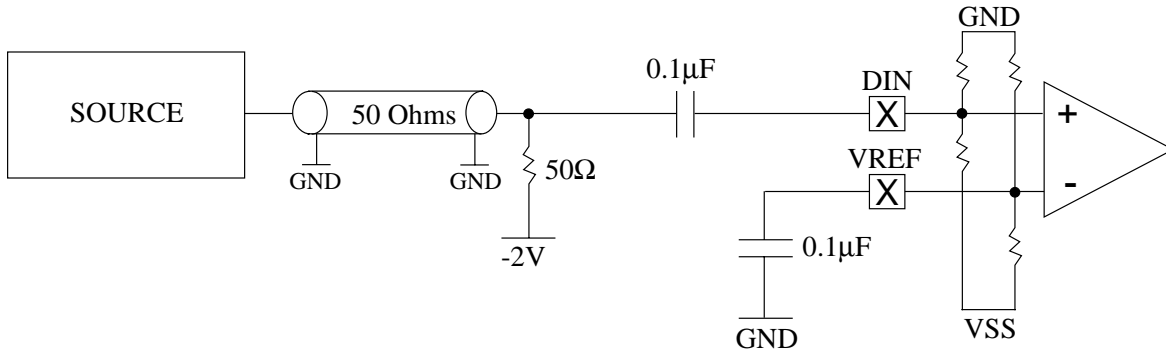


Figure 3: Differential AC Coupled

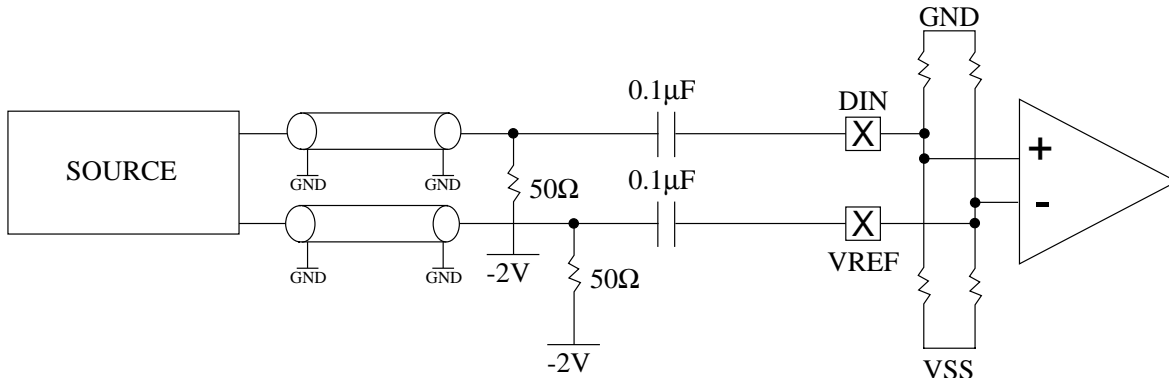


Figure 4: Differential DC Coupled

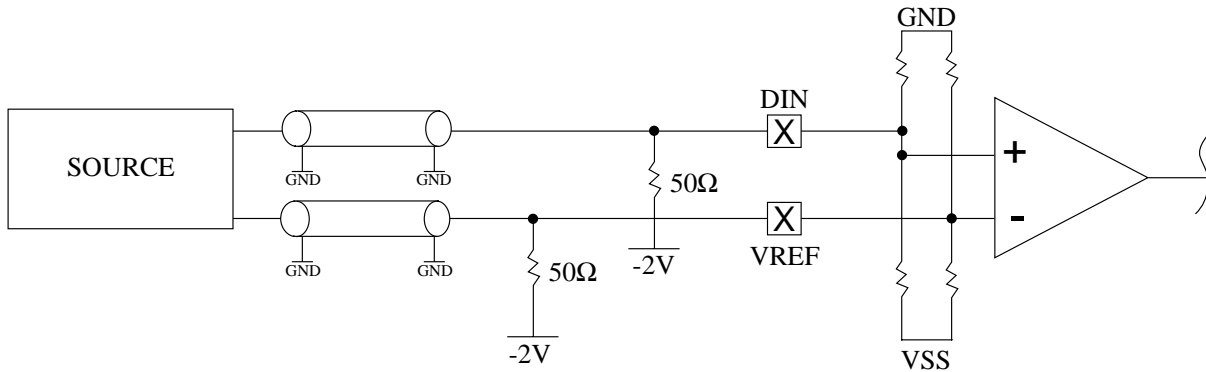
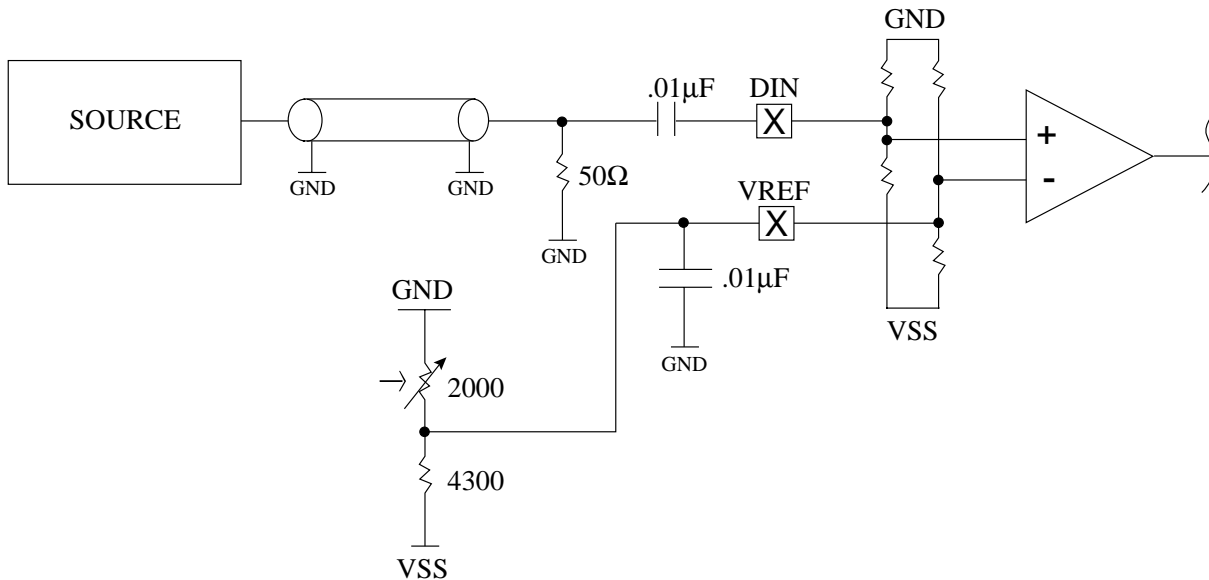


Figure 5: Single Ended AC Coupled with Offset Adjust

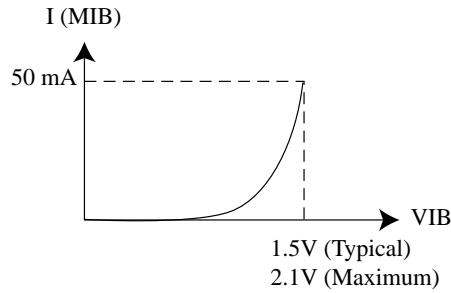


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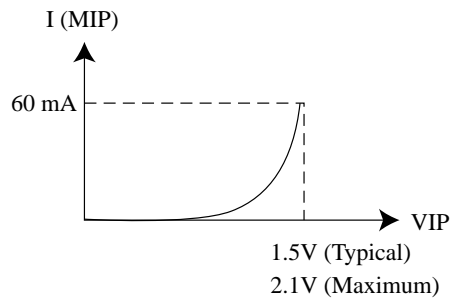
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Figure 6: Control Signals VIP and VIB



Typical Bias Current v.s. Bias Voltage



Typical Modulation Current v.s. Modulation Voltage

Figure 7: Simplified Output Structure

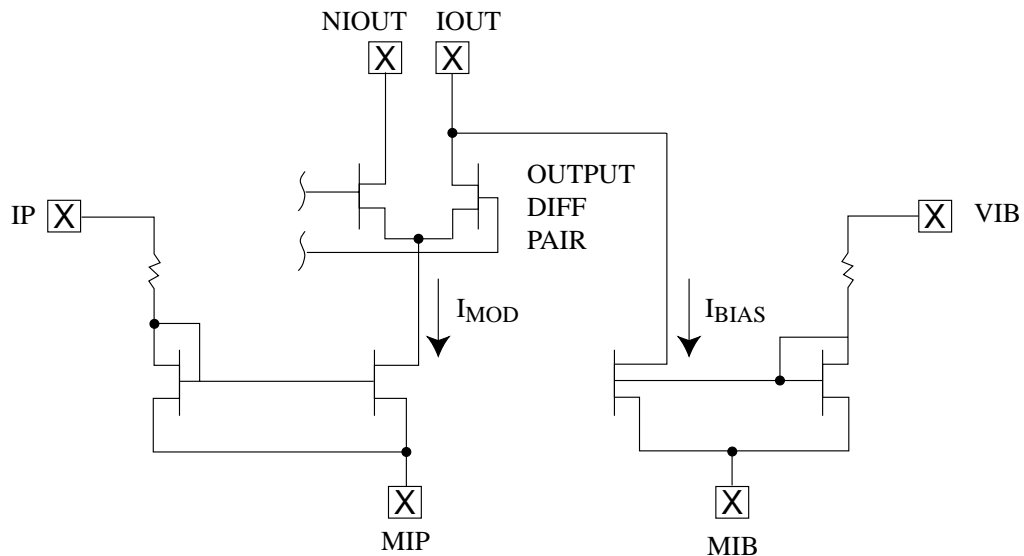
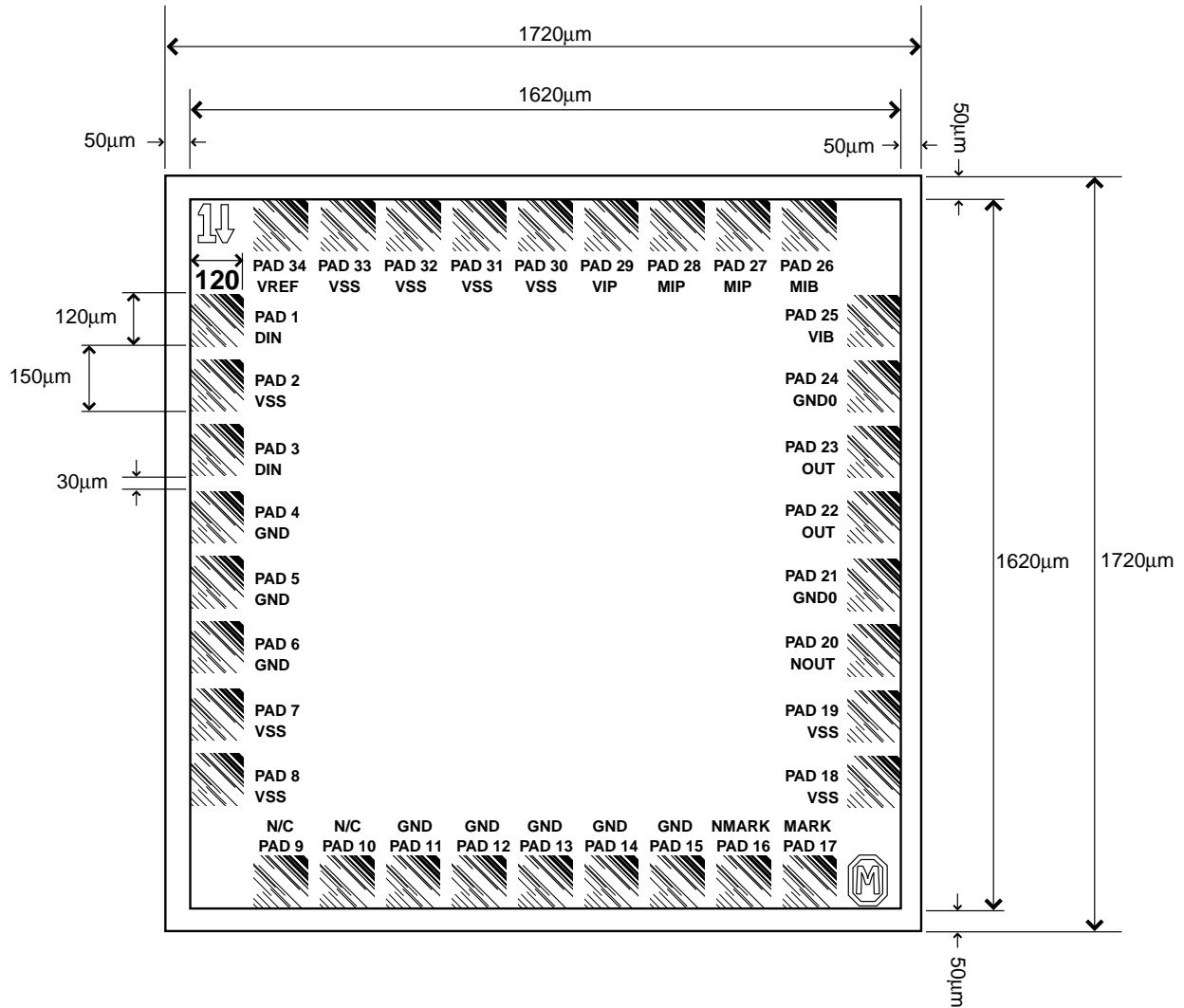


Figure 8: Pad Assignments for VSC7923 Die



NOTES:

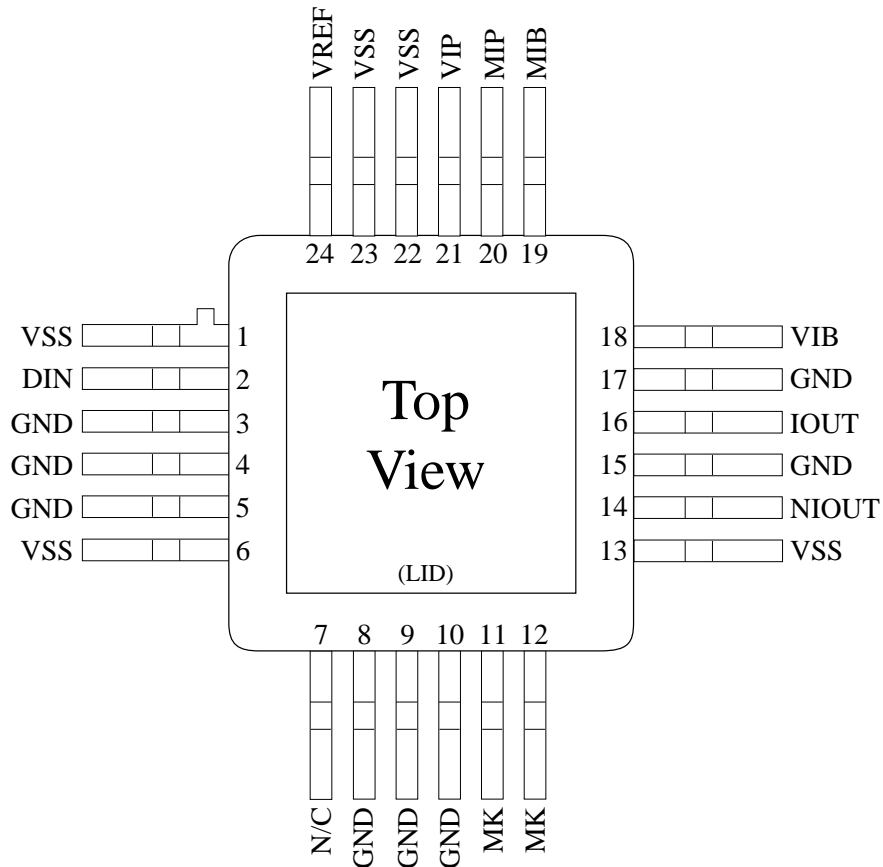
- 1) Die size = 1620µm x 1620µm
- 2) Actual die size = 1720µm x 1720µm (after die are cut up)
- 3) Pad size = 120µm x 120µm
- 4) Pad pitch = 150µm
- 5) Space between pads = 30µm

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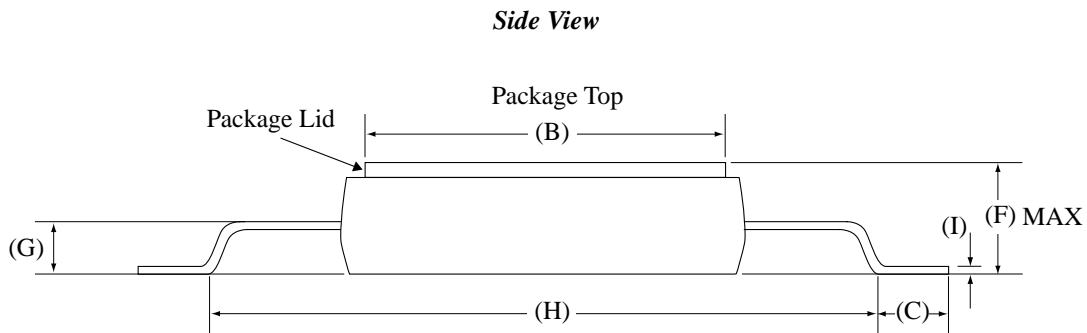
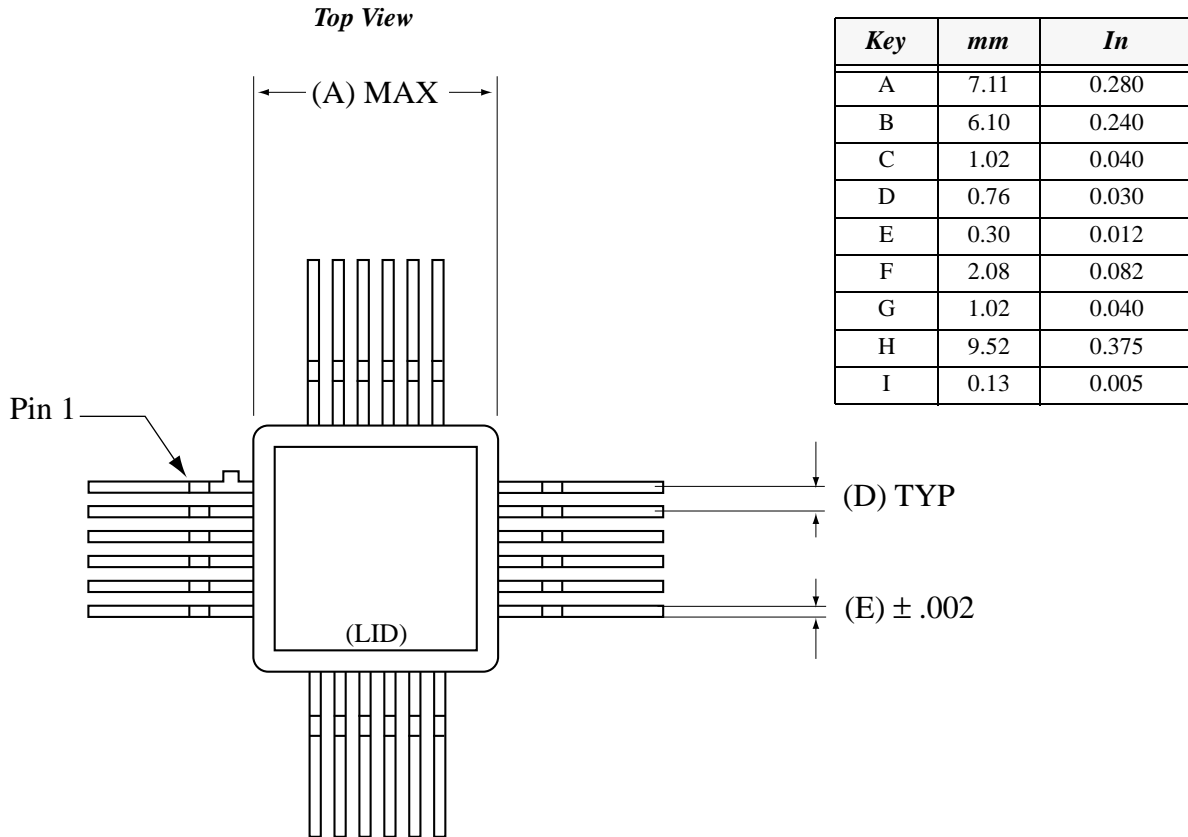
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Pin Diagram for 24 Pin Metal-Glass Package



Note: *Package bottom plate is connected to GND within the package.
Package lid is electrically unconnected.*

Package Information - 24 Pin Metal-Glass Package



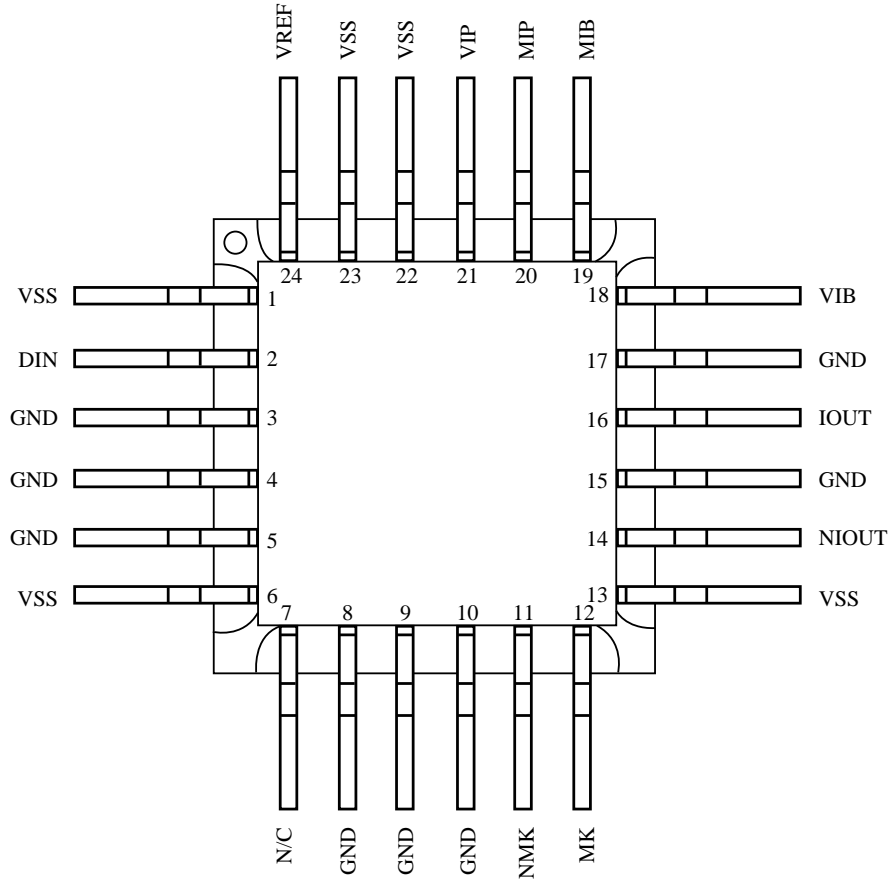
NOTES: Drawing not to scale.
 Package #: 101-291-8 Issue #: 1
 Lid #: 101-292-3 Issue #: 1

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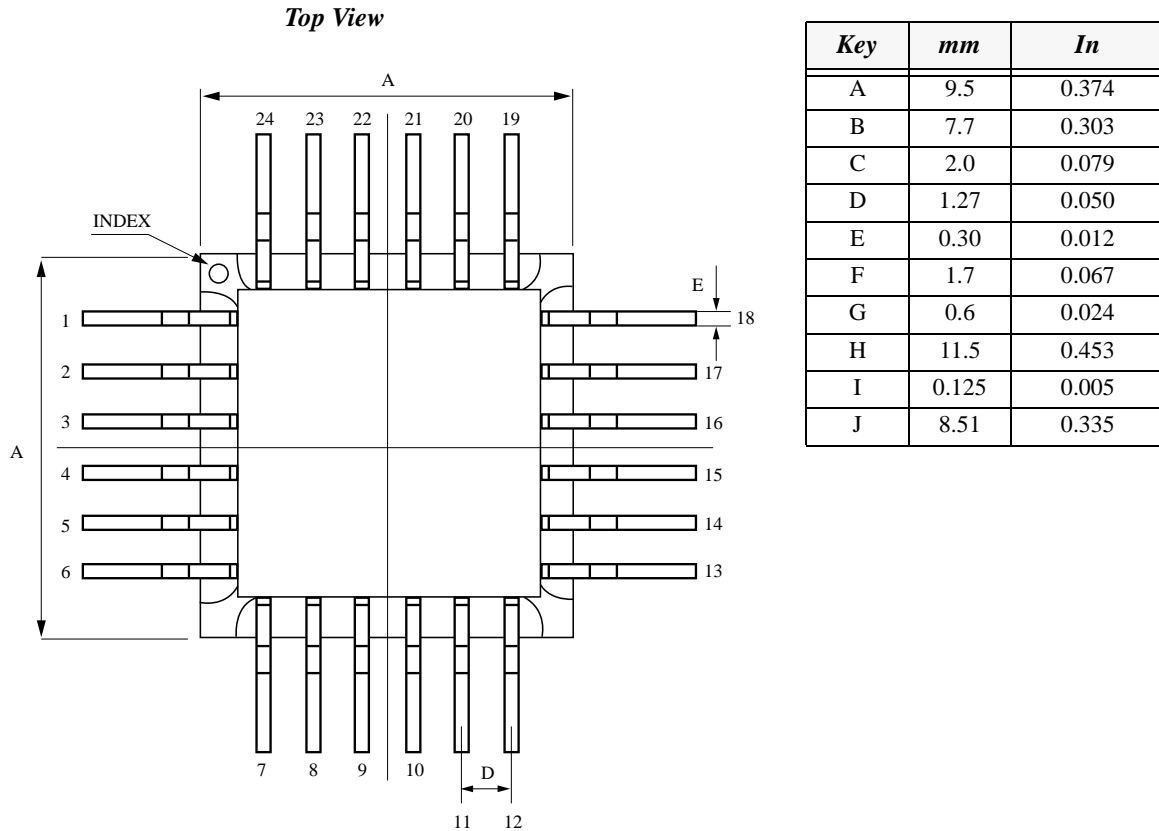
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Pin Diagram for 24 Pin Ceramic Package



Note: Package bottom plate is connected to GND within the package.
Package lid is electrically unconnected.

Package Information - 24 Pin Ceramic Package



NOTES: Drawing not to scale.
 Package #: 101-312-0 Issue #:1
 L id #: 101-303-1 Issue #:1

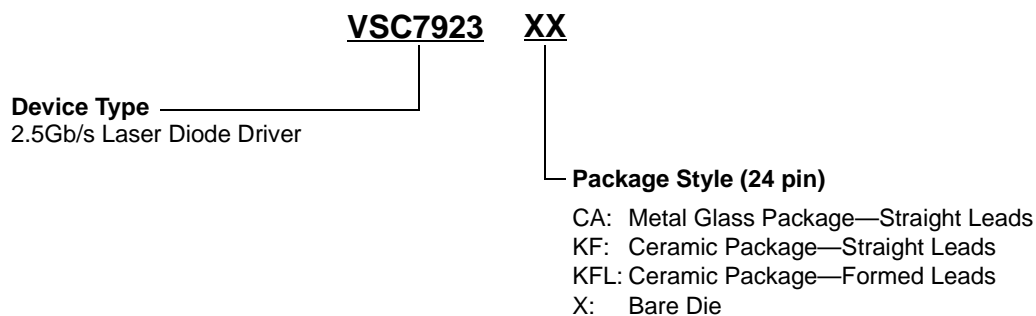
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Ordering Information

The order number for this product is formed by a combination of the device number, and package style.



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