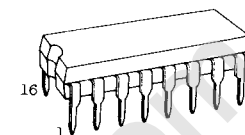
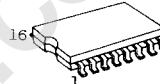


TC4518BP/TC4518BF DUAL BCD UP COUNTER
TC4520BP/TC4520BF DUAL BINARY UP COUNTER

TC4518BP/BF and TC4520BP/BF are up counters of BCD or 4 bit binary.
Since both of TC4518BP/BF and TC4520BP/BF contain two independent circuits of counters with the same functions in one package, counting or frequency division of two BCD digits or eight binary bits can be achieved with one IC. The counters can be reset to "0" (Q0~Q3="L") by giving "H" level signal to RESET input regardless of other inputs. The counting condition is changed by the rising edge of CLOCK input if ENABLE="H" or by the falling edge of ENABLE if CLOCK="L".



DIP16(3D16A-P)



MFP16(F16GC-P)

ABSOLUTE MAXIMUM RATINGS

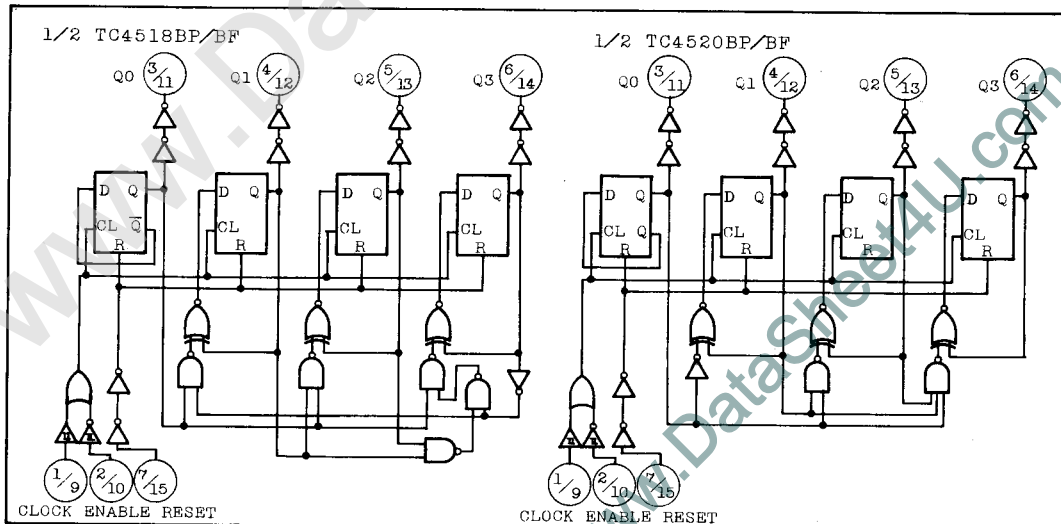
CHARACTERISTIC	SYMBOL	RATING	UNIT
DC Supply Voltage	V _{DD}	V _{SS} -0.5 ~ V _{SS} +20	V
Input Voltage	V _{IN}	V _{SS} -0.5 ~ V _{DD} +0.5	V
Output Voltage	V _{OUT}	V _{SS} -0.5 ~ V _{DD} +0.5	V
DC Input Current	I _{IN}	±10	mA
Power Dissipation	P _D	300(DIP)/180(MFP)	mW
Operating Temperature Range	T _A	-40 ~ 85	°C
Storage Temperature Range	T _{stg}	-65 ~ 150	°C
Lead Temp./Time	T _{sol}	260°C • 10sec	

PIN ASSIGNMENT

CLOCK A	1	16	V _{DD}
ENABLE A	2	15	RESET B
Q0 A	3	14	Q3 B
Q1 A	4	13	Q2 B
Q2 A	5	12	Q1 B
Q3 A	6	11	Q0 B
RESET A	7	10	ENABLE B
V _{SS}	8	9	CLOCK B

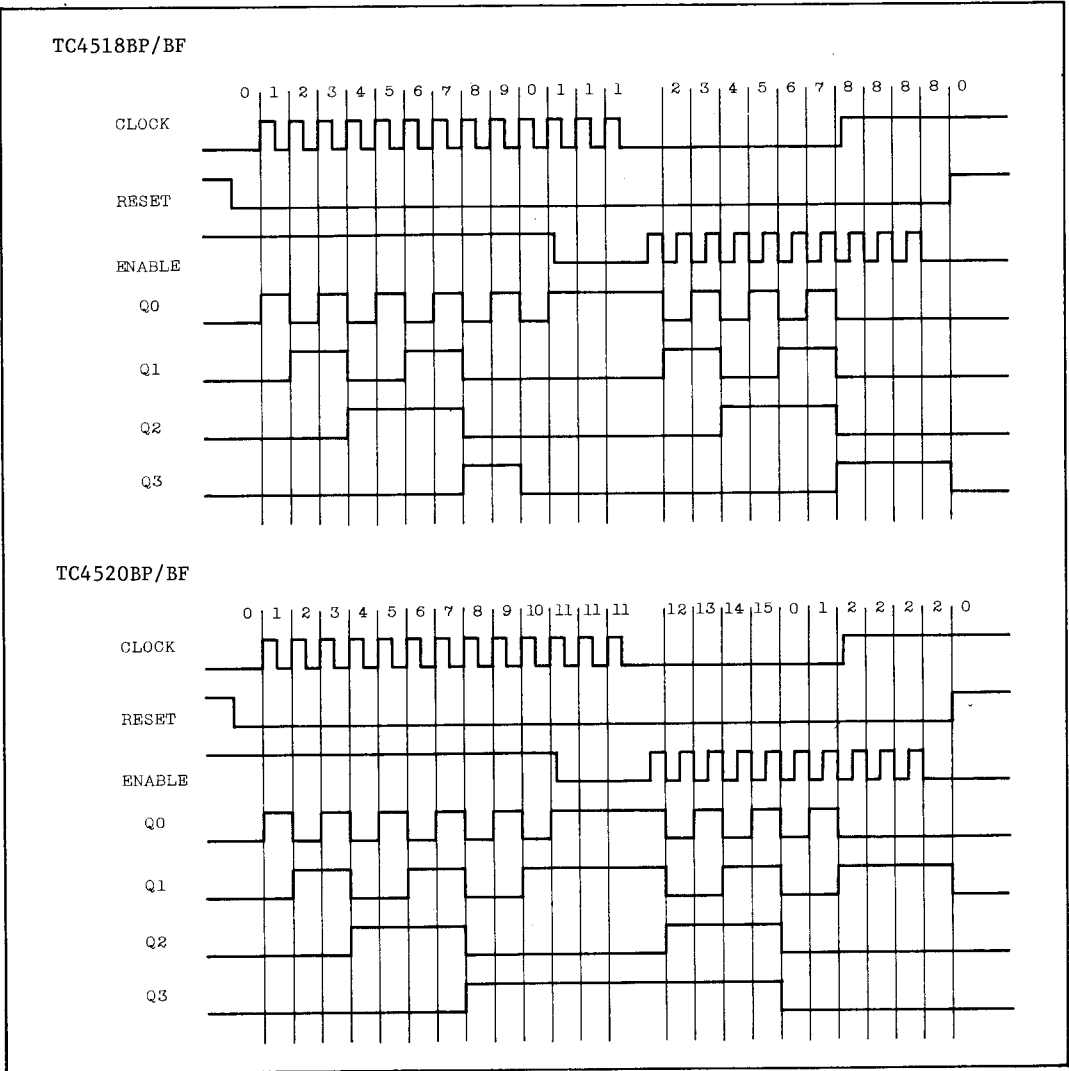
(TOP VIEW)

LOGIC DIAGRAM



TC4518BP/BF, TC4520BP/BF

TIMING CHART



RECOMMENDED OPERATING CONDITIONS (V_{SS}=0V)

CHARACTERISTIC	SYMBOL		MIN.	TYP.	MAX.	UNIT
DC Supply Voltage	V _{DD}		3	-	18	V
Input Voltage	V _{IN}		0	-	V _{DD}	

STATIC ELECTRICAL CHARACTERISTICS ($V_{SS}=0V$)

CHARACTERISTIC		SYMBOL	TEST CONDITION	V _{DD} (V)	-40°C		25°C			85°C		UNIT
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
High-Level Output Voltage		V _{OH}	I _{OUT} <1μA V _{IN} =V _{SS} , V _{DD}	5	4.95	-	4.95	5.00	-	4.95	-	V
				10	9.95	-	9.95	10.00	-	9.95	-	
				15	14.95	-	14.95	15.00	-	14.95	-	
Low-Level Output Voltage		V _{OL}	I _{OUT} <1μA V _{IN} =V _{SS} , V _{DD}	5	-	0.05	-	0.00	0.05	-	0.05	
				10	-	0.05	-	0.00	0.05	-	0.05	
				15	-	0.05	-	0.00	0.05	-	0.05	
Output High Current		I _{OH}	V _{OH} =4.6V	5	-0.61	-	-0.51	-1.0	-	-0.42	-	mA
			V _{OH} =2.5V	5	-2.5	-	-2.1	-4.0	-	-1.7	-	
			V _{OH} =9.5V	10	-1.5	-	-1.3	-2.2	-	-1.1	-	
			V _{OH} =13.5V	15	-4.0	-	-3.4	-9.0	-	-2.8	-	
			V _{IN} =V _{SS} , V _{DD}									
Output Low Current		I _{OL}	V _{OL} =0.4V	5	0.61	-	0.51	1.2	-	0.42	-	
			V _{OL} =0.5V	10	1.5	-	1.3	3.2	-	1.1	-	
			V _{OL} =1.5V	15	4.0	-	3.4	12.0	-	2.8	-	
			V _{IN} =V _{SS} , V _{DD}									
Input High Voltage		V _{IH}	V _{OUT} =0.5V, 4.5V	5	3.5	-	3.5	2.75	-	3.5	-	V
			V _{OUT} =1.0V, 9.0V	10	7.0	-	7.0	5.5	-	7.0	-	
			V _{OUT} =1.5V,13.5V	15	11.0	-	11.0	8.25	-	11.0	-	
			I _{OUT} <1μA									
Input Low Voltage		V _{IL}	V _{OUT} =0.5V, 4.5V	5	-	1.5	-	2.25	1.5	-	1.5	
			V _{OUT} =1.0V, 9.0V	10	-	3.0	-	4.0	3.0	-	3.0	
			V _{OUT} =1.5V,13.5V	15	-	4.0	-	6.75	4.0	-	4.0	
			I _{OUT} <1μA									
Input Current	"H" Level	I _{IH}	V _{IH} =18V	18	-	0.1	-	10 ⁻⁵	0.1	-	1.0	μA
	"L" Level	I _{IL}	V _{IL} =0V	18	-	-0.1	-	-10 ⁻⁵	-0.1	-	-1.0	
Quiescent Device Current		I _{DD}	V _{IN} =V _{SS} , V _{DD} *	5	-	5	-	0.005	5	-	150	
				10	-	10	-	0.010	10	-	300	
				15	-	20	-	0.015	20	-	600	

* All valid input combinations.

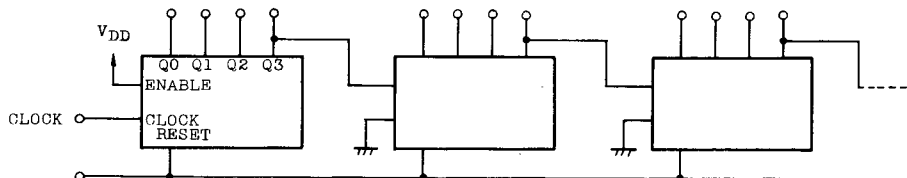
TC4518BP/BF, TC4520BP/BF

DYNAMIC ELECTRICAL CHARACTERISTICS (Ta=25°C, VSS=0V, CL=50pF)

CHARACTERISTIC	SYMBOL	TEST CONDITION	V _{DD} (V)	MIN.	TYP.	MAX.	UNIT	
Output Transition Time	t _{TLH}		5	–	70	200	ns	
	t _{THL}		10	–	35	100		
			15	–	30	80		
Propagation Delay Time (CLOCK, ENABLE – Q)	t _{pLH}		5	–	160	560		
	t _{pHL}		10	–	75	230		
			15	–	60	160		
Propagation Delay Time (RESET – Q)	t _{pHL}		5	–	110	560		
			10	–	55	230		
			15	–	40	160		
Max. Clock Frequency	f _{CL}		5	1.5	6	–	MHz	
			10	3	14	–		
			15	4	18	–		
Max. Clock Input Rise/ Fall Time	t _{rCL}		5	No Limit			μs	
	t _{fCL}		10					
			15					
Max. Input Rise/Fall Time (ENABLE)	t _r		5	No Limit				
	t _f		10					
			15					
Min. Clock Pulse Width	t _W		5	–	30	200	ns	
			10	–	15	100		
			15	–	10	70		
Min. Pulse Width (ENABLE)	t _W		5	–	35	250		
			10	–	20	110		
			15	–	15	80		
Min. Pulse Width (RESET)	t _{WH}		5	–	45	250		
			10	–	20	110		
			15	–	15	80		
Min. Removal Time	t _{rem}		5	–	–	0		
			10	–	–	0		
			15	–	–	0		
Input Capacitance	C _{IN}			–	5	7.5	pF	

The timing diagram illustrates the relationship between the RESET, ENABLE, and CLOCK signals and the output Q. The RESET signal has a pulse width of 20ns, with 90%, 50%, and 10% level markers. The ENABLE signal has a pulse width of t_{WH} and a delay of t_{rem} from the end of the RESET pulse. The CLOCK signal is a square wave with a period of 20ns. The output Q shows a propagation delay t_{PHL} from the falling edge of the CLOCK signal to the 50% level.

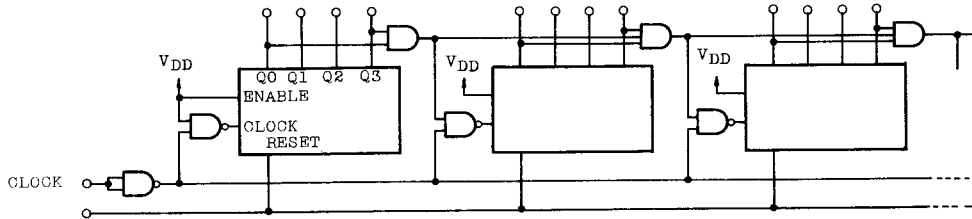
(1) RIPPLE CARRY UP COUNTER



APPLICATION CIRCUIT (Continued)

(2) PARALLEL CARRY UP COUNTER

TC4518BP/BF



TC4520BP/BF

