M37260M6-XXXSP/FP
M37260E6-XXXSP/FP, M37260E6SP/FP

SINGLE-CHIP 8-BIT CMOS MICROCOMPUTER with ON-SCREEN DISPLAY CONTROLLER

DESCRIPTION

The M37260M6-XXXSP/FP is a single-chip microcomputer designed with CMOS silicon gate technology. It is housed in a 52-pin shrink plastic molded DIP or a 64-pin plastic molded QFP. This single-chip microcomputer is useful for the high-tech on-screen display system for TVs.

In addition to their simple instruction sets, the ROM, RAM, and I/O addresses are placed on the same memory map to enable easy programming.

The features of the M37260E6-XXXSP/FP and the M37260E6SP/FP are similar to those of the M37260M6-XXXSP/FP except that these chips have a built-in PROM which can be written electrically. Accordingly, the following descriptions will be for the M37260MF-XXXSP/FP unless otherwise noted.

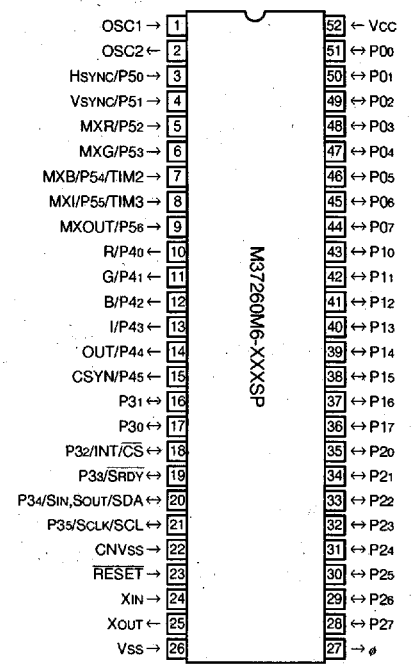
FEATURES

- Number of basic instructions 69
- Memory size ROM ..... 24 K bytes
  - RAM ..... 320 bytes
  - ROM for display ..... 20 K bytes
  - RAM for display ..... 280 bytes
- The minimum instruction execution time ..... 0.5μs (at 8MHz oscillation frequency)
- Power source voltage ..... 5V ± 10%
- Power dissipation ..... 110mW (at 4MHz frequency, V_{CC} = 5.5V, at CRT display)
- Subroutine nesting ..... 96 levels (Max.)
- Interrupts ..... 11 types, 11 vectors
- 8-bit timers 4
- Programmable I/O ports (Ports P0, P1, P2, P3) 30
- Output port (Port P4) 6
- Input port (Port P5) 7
- Serial I/O ..... maximum 64-bit × 1 channel
- CRT display function
  - Display characters ..... 40 characters × 3 lines (25 lines max.)
  - Character kinds ..... 510 kinds
  - Dot structure ..... 12 × 20 dots or 16 × 20 dots
  - Character size ..... 30 kinds (minimum dot width is 1/2 scanning line)
  - Character color kinds (It can be specified by the character) max. 15 kinds (R, G, B, I)
  - Character background color (It can be specified by the block) max. 15 kinds (R, G, B, I)
  - Raster color (max. 15 kinds)
  - Display layout
    - Horizontal ..... 256 levels
    - Vertical ..... 1024 levels
  - Bordering (horizontal and vertical)

APPLICATION

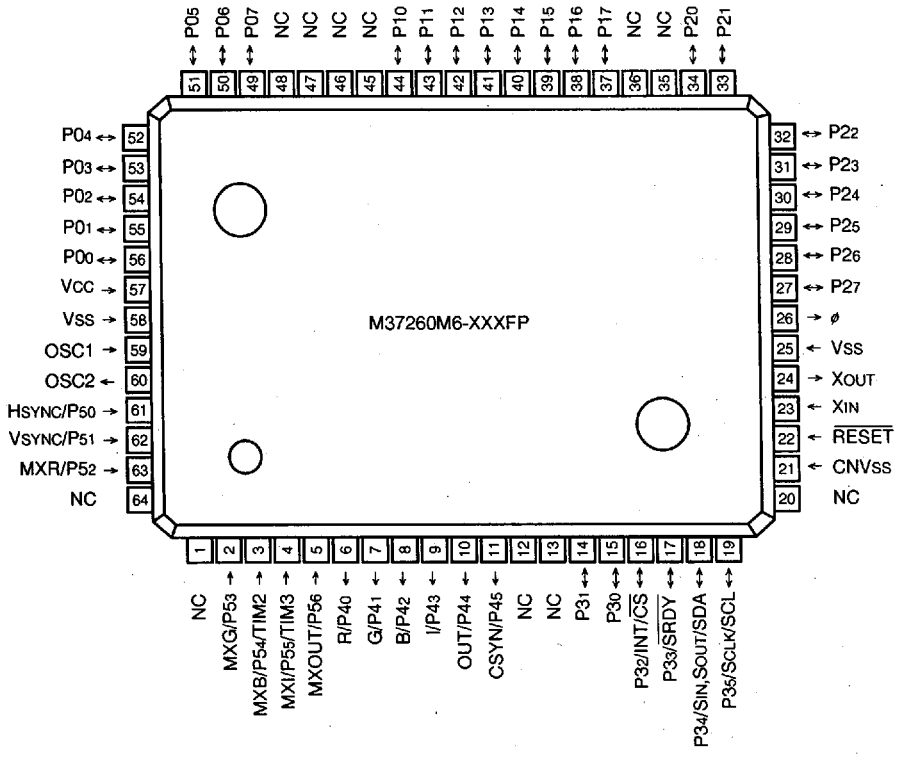
TV

PIN CONFIGURATION (TOP VIEW)



Outline 52P4B

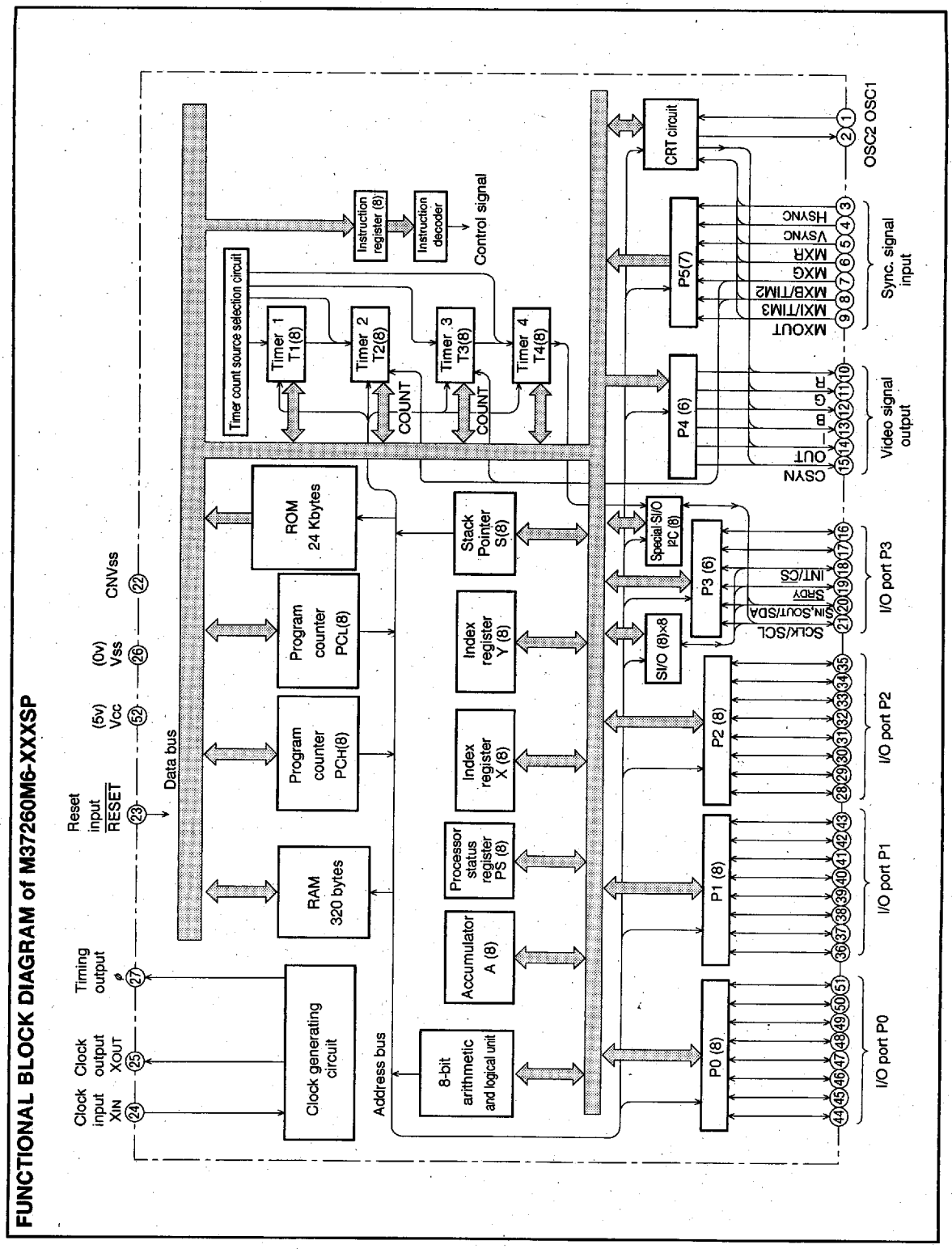
PIN CONFIGURATION (TOP VIEW)



Outline 64P6W-B

NC : No connect

FUNCTIONAL BLOCK DIAGRAM of M37260M6-XXXSP



FUNCTIONS

Parameter			Functions
Number of basic instructions			69
Instruction execution time			0.5μs (The minimum instruction execution time, at 8MHz oscillation frequency)
Clock frequency			8MHz (maximum)
Memory size	ROM		24 K bytes
	RAM		320 bytes
	CRT ROM		20 K bytes
	CRT RAM		280 bytes
Input/Output ports	P0, P1, P2	I/O	8-bit × 3 (CMOS output)
	P30, P31	I/O	2-bit × 1 (CMOS output)
	P32 – P35	I/O	4-bit × 1 (can be used as serial I/O pins and external interrupt pin) (N-channel open drain output)
	P4	Output	6-bit × 1 (can be used as R, G, B, I, OUT, and CSYN pins) (CMOS output)
	P5	Input	7-bit × 1 (can be used as HSYNC, VSYNC, MXR, MXG, MXB, MXI, and MXOUT pins)
Serial I/O			64-bit (maximum) × 1, Special serial I/O (8-bit) × 1
Timers			8-bit timer × 4
Subroutine nesting			96 levels (maximum)
Interrupt			One external interrupt, eight internal interrupts, one software interrupt
CRT display function	Display characters		40 characters × 3 lines (maximum 25 lines in program)
	Dot structure		12 × 20 dots or 16 × 20 dots
	kinds of characters		510 types
	Character size		30 types (mimimum dot width is 1/2 scanning line)
	kinds of color		Max, 15 types (R, G, B, I)
	Display layout		Holizontal 256 levels, Vs, Vertical 1024 levels
Clock generating circuit			Two built-in circuits (externally connected a ceramic resonator or a quartz-crystal oscillator)
Power source voltage			5V ± 10%
Power dissipation	at CRT display ON		110mW (at 4MHz oscillation frequency V_{CC} = 5.5V, Typ.)
	at CRT display OFF		55mW (at 4MHz oscillation frequency V_{CC} = 5.5V, Typ.)
	at stop mode		1.65mW (maximum)
Memory expansion			Possible
Operating temperature range			−10 to 70°C
Device structure			CMOS silicon gate process
Package			52-pin shrink plastic molded

PIN DESCRIPTION

Pin	Name	Input/ Output	Functions
V_{CC}, V_{SS}	Power source		Apply voltage of 5V ± 10% to V_{CC}, and 0V to V_{SS}.
CNV_{SS}	CNV_{SS}		This is connected to V_{SS}.
$\overline{RESET}$	Reset input	Input	To enter the reset state, the reset input pin must be kept at a "L" for 2μs or more (under normal V_{CC} conditions). If more time is needed for the crystal oscillator to stabilize, this "L" condition should be maintained for the required time.
X_{IN}	Clock input	Input	This chip has an internal clock generating circuit. To control generating frequency, an external ceramic resonator or a quartz-crystal oscillator is connected between X_{IN} and X_{OUT} pins. If an external clock is used, the clock source should be connected the X_{IN} pin and the X_{OUT} pin should be left open.
X_{OUT}	Clock output	Output	
ø	Timing output	Output	This is a timing output pin.
$P0_0$ – $P0_7$	I/O port P0	I/O	Port P0 is an 8-bit I/O port with direction register allowing each I/O bit to be individually programmed as input or output. At reset, this port is set to input mode. The output structure is CMOS output.
$P1_0$ – $P1_7$	I/O port P1	I/O	Port P1 is an 8-bit I/O port and has basically the same functions as port P0.
$P2_0$ – $P2_7$	I/O port P2	I/O	Port P2 is an 8-bit I/O port and has basically the same functions as port P0.
$P3_0$ – $P3_5$	I/O port P3	I/O	Port P3 is a 6-bit I/O port and has basically the same functions as port P0, but the output structure of $P3_0$ and $P3_1$ is CMOS output and the output structure of $P3_2$ – $P3_5$ is N-channel open drain. $P3_2$ is in common with external interrupt input pin INT. When serial I/O is used, $P3_2$, $P3_3$, $P3_4$, and $P3_5$ work as $\overline{CS}$, $\overline{SRDY}$, $SIN/SOUT$, and $SCLK$ pins, respectively. When special serial I/O is used, $P3_4$, and $P3_5$ work as SDA and SCL pins, respectively.
OSC1	Clock input for CRT display	Input	There are I/O pins of the clock generating circuit for the CRT display function.
OSC2	Clock output for CRT display	Output	
H_{SYNC}	H_{SYNC} input	Input	This is a horizontal synchronizing signal input for CRT display. This pin is in common with input Port $P5_0$.
V_{SYNC}	V_{SYNC} input	Input	This is a vertical synchronizing signal input for CRT display. This pin is in common with input Port $P5_1$.
MXR, MXG, MXB, MXI, MXOUT	Video signal input for mixing	Input	These are video signal input pins. MXR, MXG, MXB, MXI, and MXOUT are in common with $P5_2$, $P5_3$, $P5_4$, $P5_5$, and $P5_6$. Also $P5_4$ and $P5_5$ are in common with external clock input pins TIM2 and TIM3.
R, G, B, I, OUT	CRT output	Output	This is a 5-bit output pin for CRT display. The output structure is CMOS output. R, G, B, I, and OUT are in common with $P4_0$, $P4_1$, $P4_2$, $P4_3$, and $P4_4$.
CSYN	Composite sync signal output	Output	This is a composite sync signal output pin, and in common with output port $P4_5$.

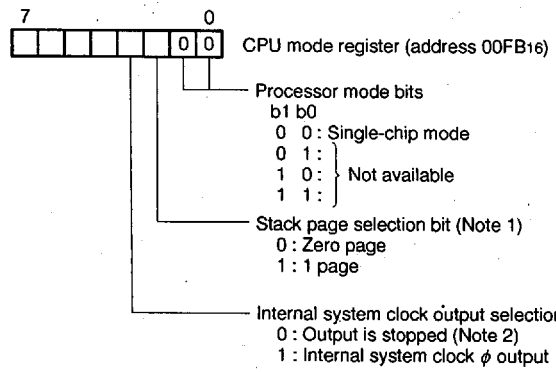
FUNCTIONAL DESCRIPTION
Central Processing Unit (CPU)

The M37260M6-XXXSP/FP uses the standard 740 family instruction set. Refer to the table of 740 family addressing modes and machine instructions or the SERIES 740 ⟨Software⟩ User's Manual for details on the instruction set.

Machine-resident 740 family instructions are as follows:
The FST, SLW, MUL and DIV instruction cannot be used.
The WIT and STP instruction can be used.

CPU Mode Register

The CPU mode register is allocated at address 00FB16. The CPU mode register contains the stack page selection bit and the internal system clock output selection bit.



Notes 1: Please beware of this bit when programming because it is set to "1" after the reset release.
2: The internal system clock φ stoppes at "H."

Fig. 1 Structure of CPU mode register

MEMORY

Special Function Register (SFR) Area

The special function register (SFR) area in the zero page contains control registers such as I/O ports and timers.

RAM

RAM is used for data storage and for stack area of subroutine calls and interrupts.

ROM

ROM is used for storing user programs as well as the interrupt vector area.

RAM for Display

RAM for display is used for specifing the character codes and colors to display.

ROM for Display

ROM for display is used for storing character data.

Interrupt Vector Area

The interrupt vector area contains reset and interrupt vectors.

Zero Page

The 256 bytes from addresses 0000_{16} to $00FF_{16}$ are called the zero page area. The internal RAM and the special function registers (SFR) are allocated to this area.

The zero page addressing mode can be used to specify memory and register addresses in the zero page area. Access to this area with only 2 bytes is possible in the zero page addressing mode.

Special Page

The 256 bytes from addresses $FF00_{16}$ to $FFFF_{16}$ are called the special page area. The special page addressing mode can be used to specify memory addresses in the special page area. Access to this area with only 2 bytes is possible in the special page addressing mode.

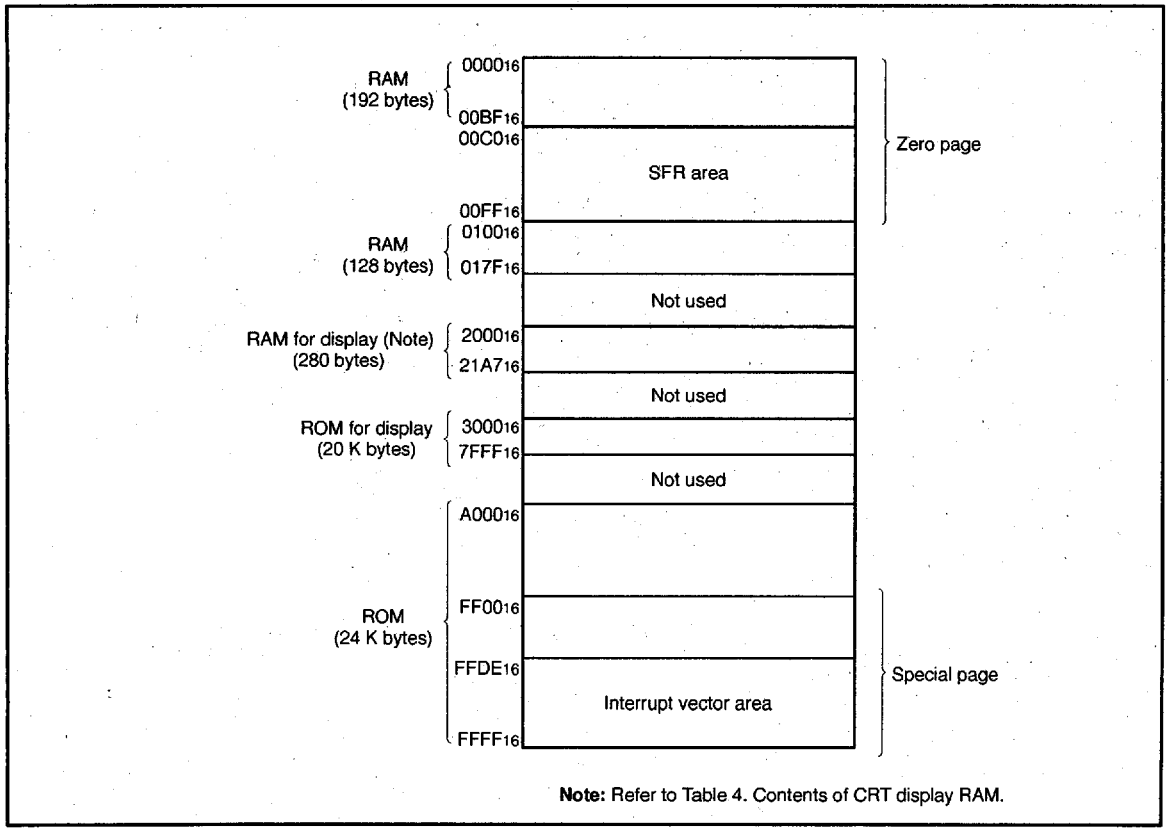


Fig. 2 Memory map

00C016	Port P0
00C116	Port P0 direction register
00C216	Port P1
00C316	Port P1 direction register
00C416	Port P2
00C516	Port P2 direction register
00C616	Port P3
00C716	Port P3 direction register
00C816	Port P4
00C916	Port P4 control register
00CA16	Port P5
00CB16	
00CC16	
00CD16	Serial I/O mode register 1
00CE16	Serial I/O mode register 2
00CF16	Serial I/O register 0
00D016	Serial I/O register 1
00D116	Serial I/O register 2
00D216	Serial I/O register 3
00D316	Serial I/O register 4
00D416	Serial I/O register 5
00D516	Serial I/O register 6
00D616	Serial I/O register 7
00D716	Character size register 1 (block 1)
00D816	Character size register 2 (block 2)
00D916	Character size register 3 (block 3)
00DA16	Blank control register 1 (block 1)
00DB16	Blank control register 2 (block 2)
00DC16	Blank control register 3 (block 3)
00DD16	Block 1 interrupt occurrence position control register
00DE16	Block 2 interrupt occurrence position control register
00DF16	Block 3 interrupt occurrence position control register

00E016	Horizontal position register
00E116	Vertical position register 1 (block 1)
00E216	Vertical position register 2 (block 2)
00E316	Vertical position register 3 (block 3)
00E416	Vertical position register 4 (block 1 to 3)
00E516	Mixing circuit control register
00E616	
00E716	
00E816	CRT input polarity register
00E916	Sync. generater control register
00EA16	CRT control register
00EB16	Display block counter
00EC16	CRT output polarity register
00ED16	Wipe mode register
00EE16	Wipe start register
00EF16	
00F016	Timer 1
00F116	Timer 2
00F216	Timer 3
00F316	Timer 4
00F416	Timer 12 mode register
00F516	Timer 34 mode register
00F616	Special serial I/O register
00F716	Special mode register 1
00F816	Special mode register 2
00F916	
00FA16	
00FB16	CPU mode register
00FC16	Interrupt request register 1
00FD16	Interrupt request register 2
00FE16	Interrupt control register1
00FF16	Interrupt control register2

Fig. 3 Memory map of special function register (SFR)

INTERRUPTS

Interrupts can be caused by 10 different sources consisting of two external, seven internal, and one software, and reset.

Interrupts are vectored interrupts with priorities shown in Table 1. Reset is also included in the table because its operation is similar to an interrupt.

When an interrupt is accepted, the registers are pushed, interrupt disable flag I is set, and the program jumps to the address specified in the vector table. The interrupt request bit is cleared automatically. The reset can never be disabled. Other interrupts are disabled when the interrupt disable flag is set.

All interrupts except the BRK instruction interrupt have an interrupt request bit and an interrupt enable bit. The interrupt request bits are in interrupt request registers 1 and 2 and the interrupt enable bits are in interrupt control registers 1 and 2. Figure 4 shows the structure of the interrupt request registers 1 and 2 and interrupt control registers 1 and 2.

Interrupts other than the BRK instruction interrupt and reset are accepted when the interrupt enable bit is "1", interrupt request bit is "1", and the interrupt disable flag is "0". The interrupt request bit can be cleared with a program, but not set. The interrupt enable bit can be set and cleared with a program.

Reset is treated as a non-maskable interrupt with the highest priority. Figure 5 shows interrupts control.

Interrupt Causes

(1) VSYNC and CRT interrupts

The VSYNC interrupt is an interrupt request synchronized with the vertical synchronization signal.

The CRT interrupt is generated after character block display to the CRT is completed.

(2) INT interrupt

With an external interrupt input, the system detects that the level of a pin changes from "L" to "H" or from "H" to "L", and generates an interrupt request. The input active edge can be selected by bit 5 of the CRT input active edge register (address $00E8_{16}$) : when this bit is "0", a change from "L" to "H" is detected; when it is "1", a change from "H" to "L" is detected. Note that all bits are cleared to "0" at reset.

(3) Timer 1, 2, 3 and 4 interrupts

An interrupt is generated by an overflow of timer 1, 2, 3 or 4.

(4) Serial I/O interrupt

This is an interrupt request from the clock-synchronized serial I/O function.

Note that serial I/O or special serial I/O is selected by bit 3 of the serial I/O mode register 2 (address $00CE_{16}$).

(5) 1 ms interrupt

This interrupt is generated regularly with a 1024μs period. When the XIN clock is 4MHz, set bits 7 and 4 of the sync generator control register to "0". When the XIN clock is 8MHz, set bit 7 of the sync generator control register to "0" and bit 4 to "1"

(6) BRK instruction interrupt

This software interrupt has the least significant priority. It does not have a corresponding interrupt enable bit, and it is not affected by the interrupt disable flag (non-maskable).

Table 1. Interrupt vector addresses and priority

Interrupt sources	Priority	Vector addresses	Remarks
Reset	1	$FFFF_{16}$, $FFFE_{16}$	Non-maskable
CRT interrupt	2	$FFFD_{16}$, $FFFC_{16}$	
INT interrupt	3	$FFFB_{16}$, $FFFA_{16}$	Active edge selectable
Serial I/O interrupt	4	$FFF9_{16}$, $FFF8_{16}$	
1 ms interrupt (Note)	5	$FFF7_{16}$, $FFF6_{16}$	
Timer 4 interrupt	6	$FFF5_{16}$, $FFF4_{16}$	
VSYNC interrupt	7	$FFF3_{16}$, $FFF2_{16}$	Active edge selectable
Timer 3 interrupt	8	$FFF1_{16}$, $FFF0_{16}$	
Timer 2 interrupt	9	$FFEF_{16}$, $FFEE_{16}$	
Timer 1 interrupt	10	$FFED_{16}$, $FFEC_{16}$	
BRK instruction interrupt	11	$FFDF_{16}$, $FFDE_{16}$	Non-maskable software interrupt

Note: Refer to "(5) 1 ms interrupt."

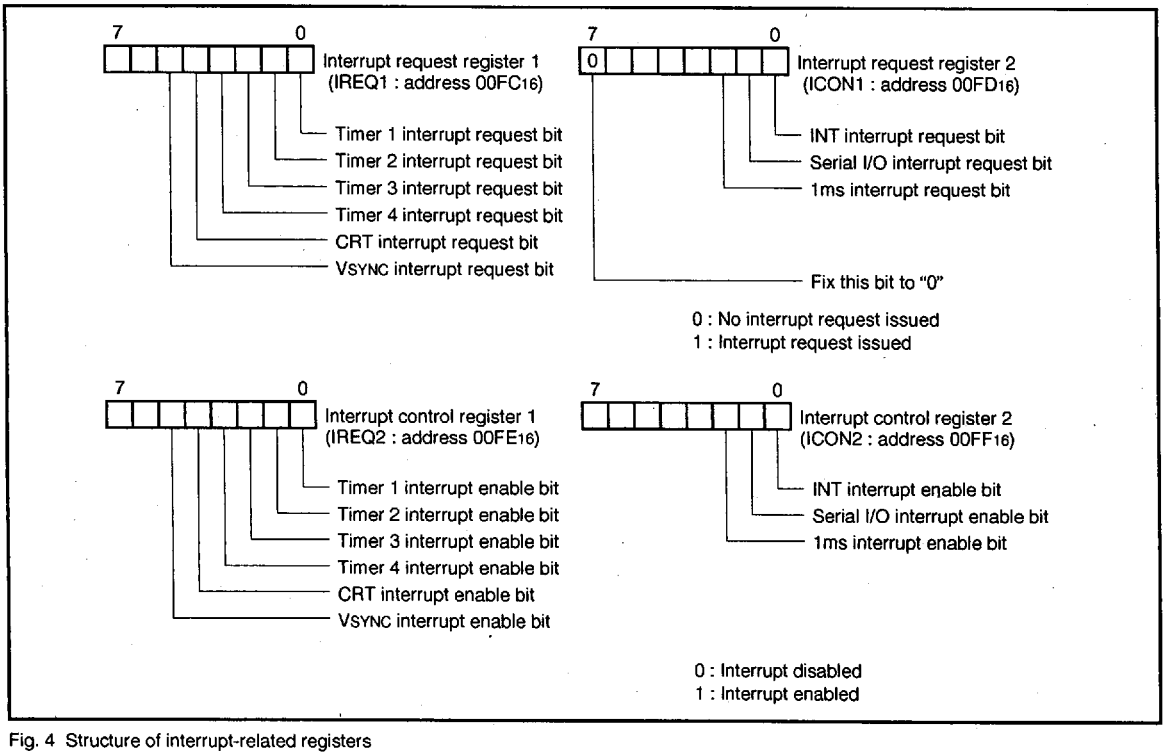


Fig. 4 Structure of interrupt-related registers

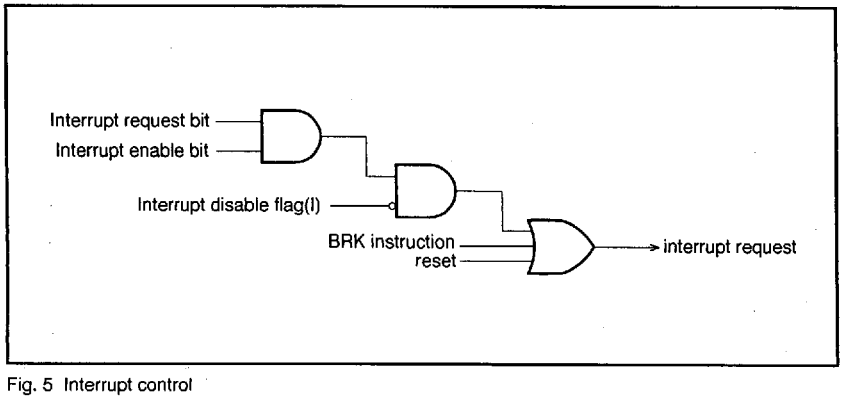


Fig. 5 Interrupt control

TIMER

The M37260M6-XXXSP has four timers ; timer 1, timer 2, timer 3 and timer 4. All of timers are 8-bit structure and have 8-bit latches.

A block diagram of timer 1 through 4 is shown in Figure 7.

All of the timers are down count timers and their divide ratio are 1/(n + 1), where n is the contents of timer latch.

The same value is set to timer by writing the count value to the latch (addresses 00F0$_{16}$ to 00F3$_{16}$: timer 1 to timer 4).

When a timer reaches "00$_{16}$" and the next count pulse is input to a timer, a value which is the contents of the reload latch are loaded into the timer. The timer interrupt request bit is set at the next count pulse after the timer reaches "00$_{16}$".

The contents of each timer is shown in following.

(1) Timer 1

Either f (XIN) divided by 16 or a 1024μs clock can be selected as the count source of timer 1.

(When the XIN clock is 4MHz, set bits 7 and 4 of the sync generator control register (address 00E9$_{16}$) to "0".

When the XIN clock is 8MHz, set bit 7 of the sync generator control register to "0" and bit 4 to "1".) When bit 0 of the timer 12 mode register (address 00F4$_{16}$) is "0", f (XIN) divided by 16 is selected ; when it is "1", the 1024μs clock is selected.

Timer 1 interrupt request is occurred with timer 1 overflow.

(2) Timer 2

f (XIN) divided by 16, timer 1 overflow signal, or an external clock input from P54/MXB/TIM2 pin can be selected as the count source of timer 2 by specifying bit 4 and 1 of the timer 12 mode register (address 00F4$_{16}$).

Timer 2 interrupt request is occurred with timer 2 overflow.

(3) Timer 3

Either f (XIN) divided by 16 or an external clock input from P55/MXI/TIM3 pin can be selected as the count source of timer 3 by specifying bit 0 of the timer 34 mode register (address 00F5$_{16}$).

Timer 3 interrupt request is occurred with timer 3 overflow.

(4) Timer 4

f (XIN) divided by 16, f (XIN) divided by 2, or timer 3 overflow signal can be selected as the count source of timer 4 by specifying bit 4 and 1 of the timer 34 mode register (address 00F5$_{16}$).

Timer 4 interrupt reguest is occurred with timer 4 overflow. And the timer 4 overflow signal can be used as the clock source of special serial I/O.

At reset, timers 3 and 4 are connected by hardware and "FF$_{16}$" is automatically set in timer 3; "07$_{16}$" in timer 4. The f(XIN)/16 is selected as the timer 3 count source. The internal reset is released by timer 4 overflow at these state, the internal clock is connected.

At execution of the STP instruction, timers 3 and 4 are connected by hardware and "FF$_{16}$" is automatically set in timer 3; "07$_{16}$" in timer 4. However, the f(XIN)/16 is not selected as the timer 3 count source. So set bit 0 of the timer 34 mode register (address 00F5$_{16}$) to "0" before the execution of the STP instruction (f(XIN)/16 is selected as the timer 3 count source). The internal STP state is released by timer 4 overflow at these state, the internal clock is connected.

Because of this, the program starts with stable clock.

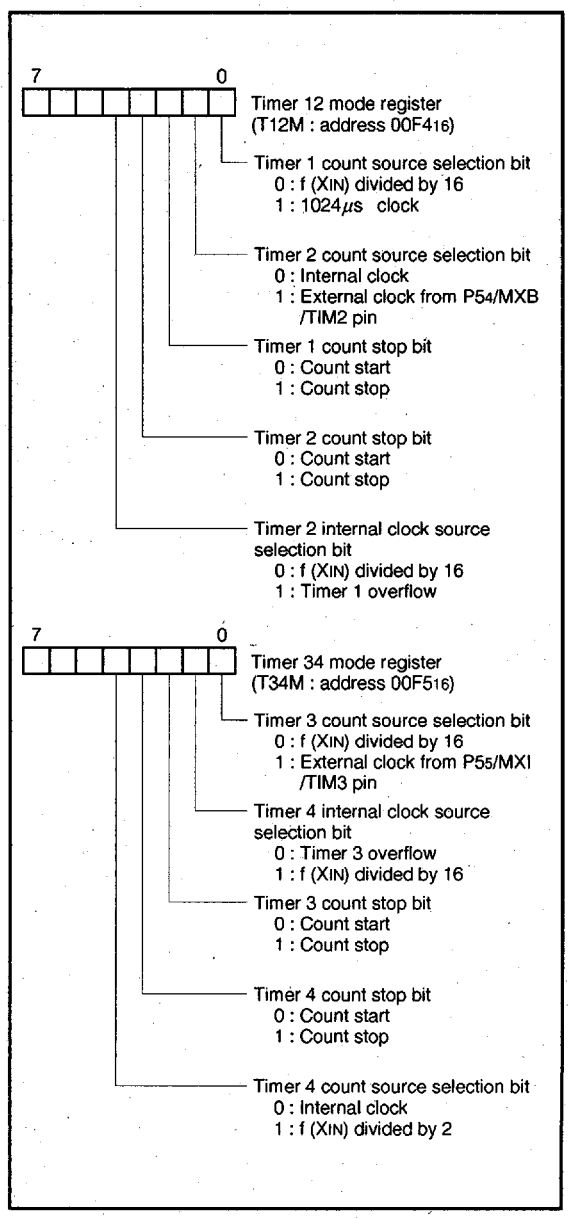
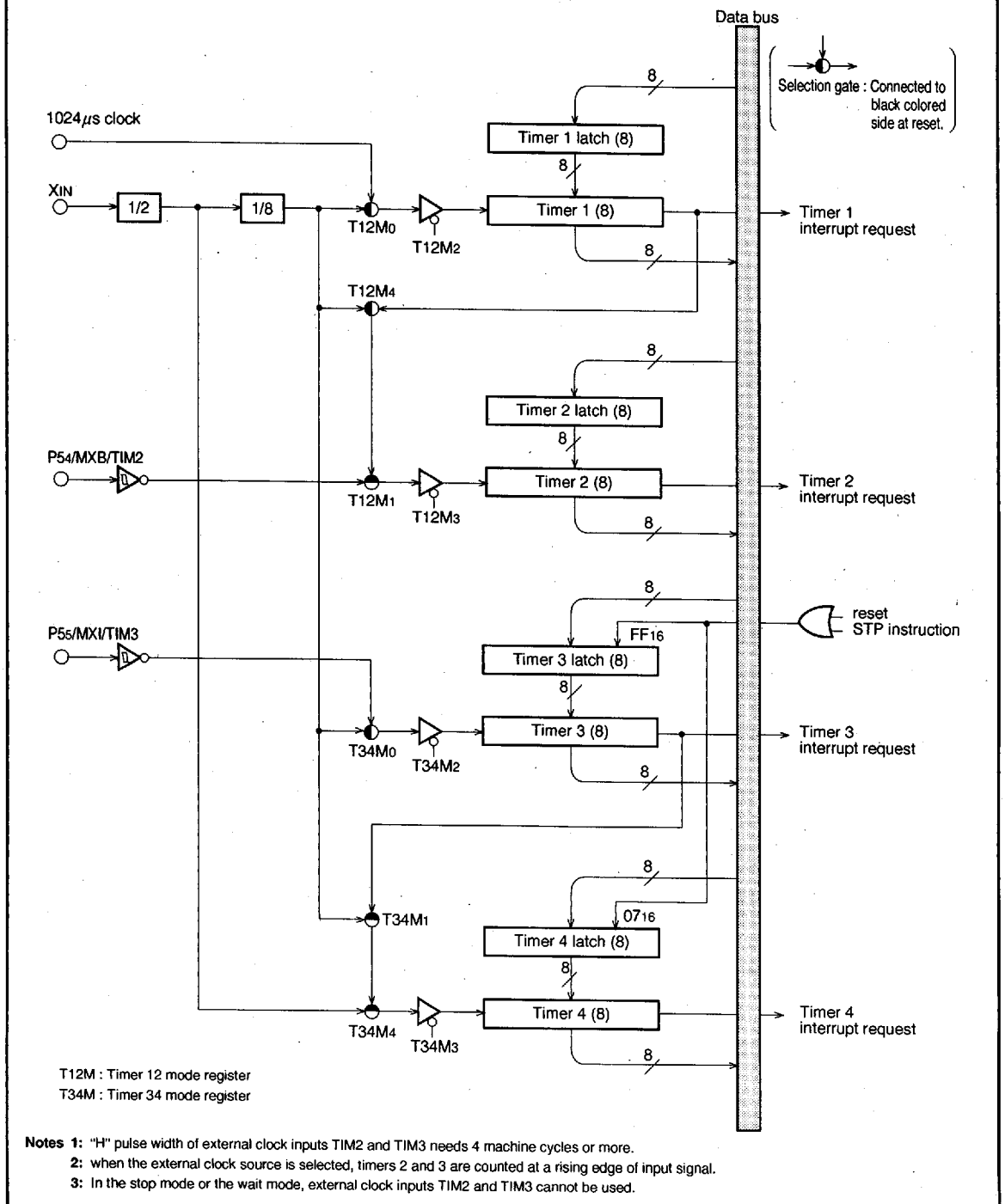


Fig. 6 Structure of timer 12 mode register and timer 34 mode register



T12M : Timer 12 mode register
T34M : Timer 34 mode register

Notes 1: "H" pulse width of external clock inputs TIM2 and TIM3 needs 4 machine cycles or more.
2: when the external clock source is selected, timers 2 and 3 are counted at a rising edge of input signal.
3: In the stop mode or the wait mode, external clock inputs TIM2 and TIM3 cannot be used.

Fig. 7 Timer block diagram

SERIAL I/O

The M37260M6-XXXSP has a built-in serial I/O function that can either transmit or receive up to 64-bits of serial data in clock-synchronized form. The serial I/O function can transfer up to 64 bits of data in 8-bit units according to the setting of the serial I/O shift register.

A block diagram of the serial I/O function is shown in Fig.8. The serial I/O receive enabled signal pin ($\overline{SRDY}$), syn chronization clock I/O pin (SCLK), and data I/O pins (SOUT and SIN) also function as the P3 port.

Bit 2 of the serial I/O mode register 1 (address 00CD16) selects whether the synchronizaion clock is supplied internally or externally (from the SCLK pin) and, if the internal clock is selected, bits 1 and 0 select whether f (XIN) is divided by 8,16,32, or 64. Bits4 and 3 select whether port P3 is used for serial I/O. Bits 2, 1,and 0 of the serial I/O mode register 2 select the count of the transfer clock at which the serial I/O interrupt request is generated. The operation of the serial I/O function is described below.

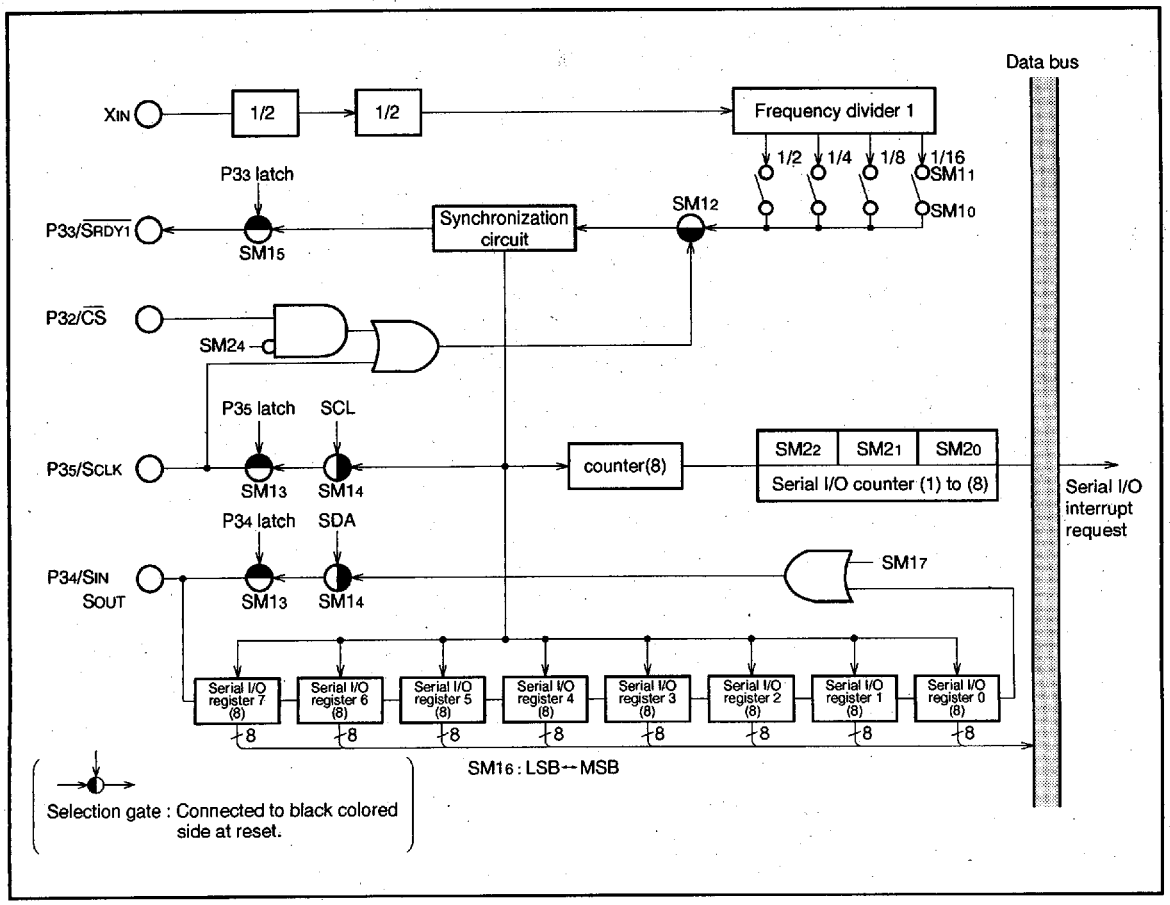


Fig. 8 Serial I/O block diagram

If the serial I/O register 0 (address 00CF16) is written to, the $\overline{SRDY}$ signal is at "H" during the write cycle ; it then goes "L" when the write cycle ends to indicate reception enabled status. If the serial I/O register's transfer clock goes "L" even once the $\overline{SRDY}$ signal goes "H". During the write cycle to the serial I/O register 0, the value set in the serial I/O mode register 2 is set in the serial I/O counter, and the serial I/O register's transfer clock is forced to "H". After the write cycle ends, the data in each register is shifted one bit in sequence from serial I/O register 0 to serial I/O register 1, serial I/O register 2, serial I/Q register 3, serial I/O register 4, serial I/O register 5, serial I/O register 6, to serial I/O register 7 until it is finally output from the SOUT pin, each time the transfer clock changes from "H" to "L". Bit 6 of the serial I/O mode register selects whether transfer is from the lowest bit of each serial I/O register, or from the highest bit.

During reception, data is fetched from the SIN pin each time the transfer clock changes from "L" to "H" and, at the same time, the data in each register is shifted one bit in sequence from serial I/O register 7 to serial I/O register 6, serial I/O register 5, serial I/O register 4, serial I/O register 3, serial I/O register 2, serial I/O register 1, to serial I/O register 0.

If the transfer clock is the count value set in the serial I/O mode register 2, when the serial I/O counter reaches "0", the transfer clock stops at "H" and the corresponding interrupt request bit is set.

If an external clock is selected as the clock, source, it must be controlled externally because the transfer clock does not stop, even when the interrupt request bit is set. Use a clock of no more that 1MHz with a duty cycle of 50% as the external clock.

Serial I/O timing is shown in Fig. 9. If an external clock is used for the transfer, the external clock must be "H" when the serial I/O counter is initialized. If the internal clock is switched to an external clock, make sure that it is switched while no transfer is in progress, and make sure that the serial I/O counter is initialized after the switch.

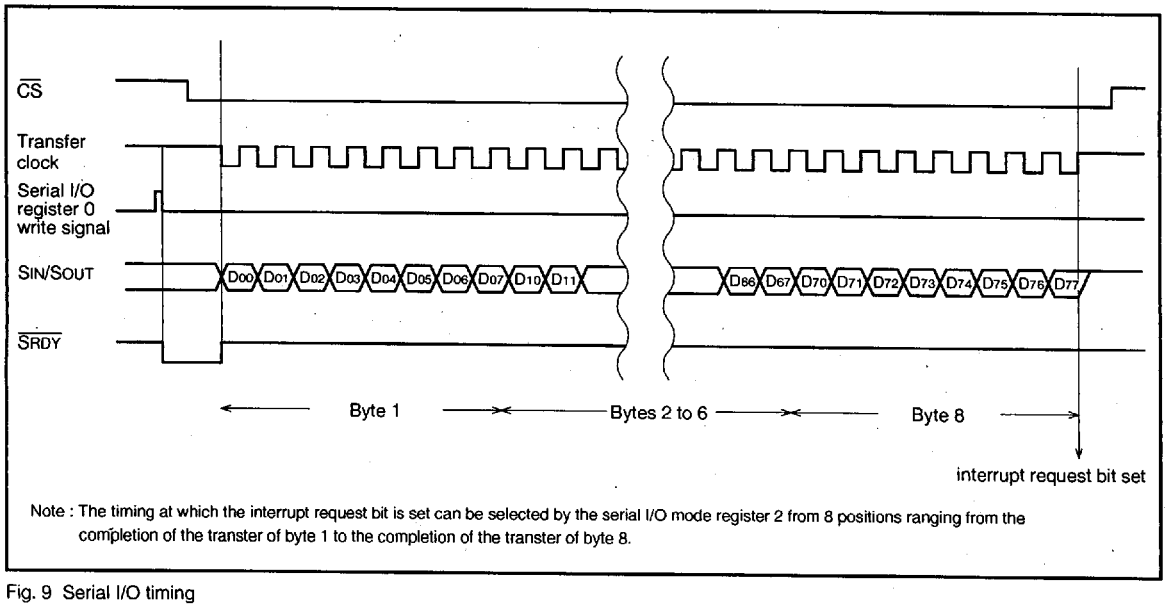
A connection example for transferring data from one M37260M6-XXXSP to another is shown in Fig. 10. If P32 is used as the $\overline{CS}$ pin, set the P32 direction register to input ("0") and set bit 4 of the serial I/O mode register 2 to "0".

This setting ensures that the transfer clock is fixed at "H" when the P32 input signal is "H", and data is not shifted. If the P32 input signal goes "L", data will be shifted according to the clock input from the P35/SCLK pin. Note that if bit 4 of the serial I/O mode register 2 is set to "1", the data will be shifted according to the clock input from the P35/SCLK pin, regardless of the P32 input signal.

Notes1 : When writing programs, remember that the serial I/O counter will also be set by using bit manipulation instructions such as SEB and CLB to write to the serial I/O register 0.

2 : When writing data to serial I/O registers 0 to 7, make sure that serial I/O register 0 is the last one written to.

3 : When an external clock is used as the synchronizing clock, write transmit data to the serial I/O register at "H" of the transfer clock input level.



Note : The timing at which the interrupt request bit is set can be selected by the serial I/O mode register 2 from 8 positions ranging from the completion of the transter of byte 1 to the completion of the transter of byte 8.

Fig. 9 Serial I/O timing

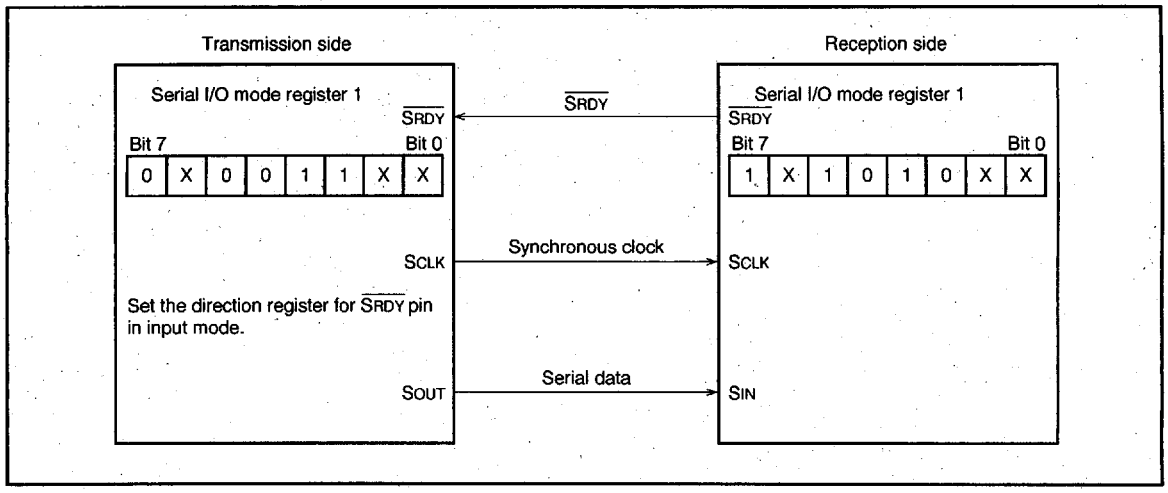


Fig. 10 Example of serial I/O connection

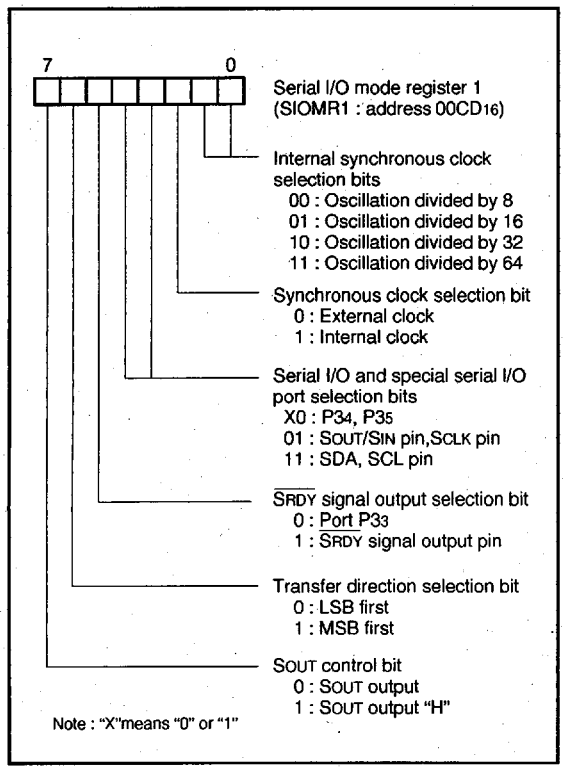


Fig. 11 Structure of serial I/O mode register 1

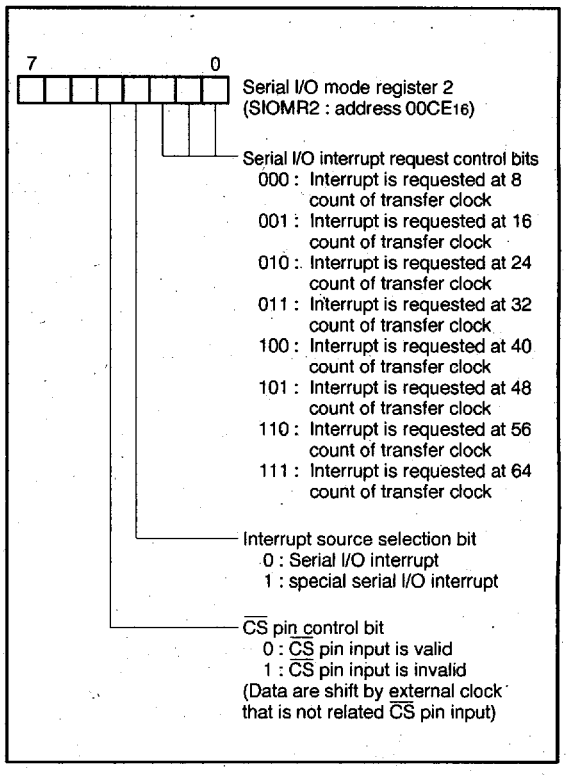


Fig. 12 Structure of serial I/O mode register 2

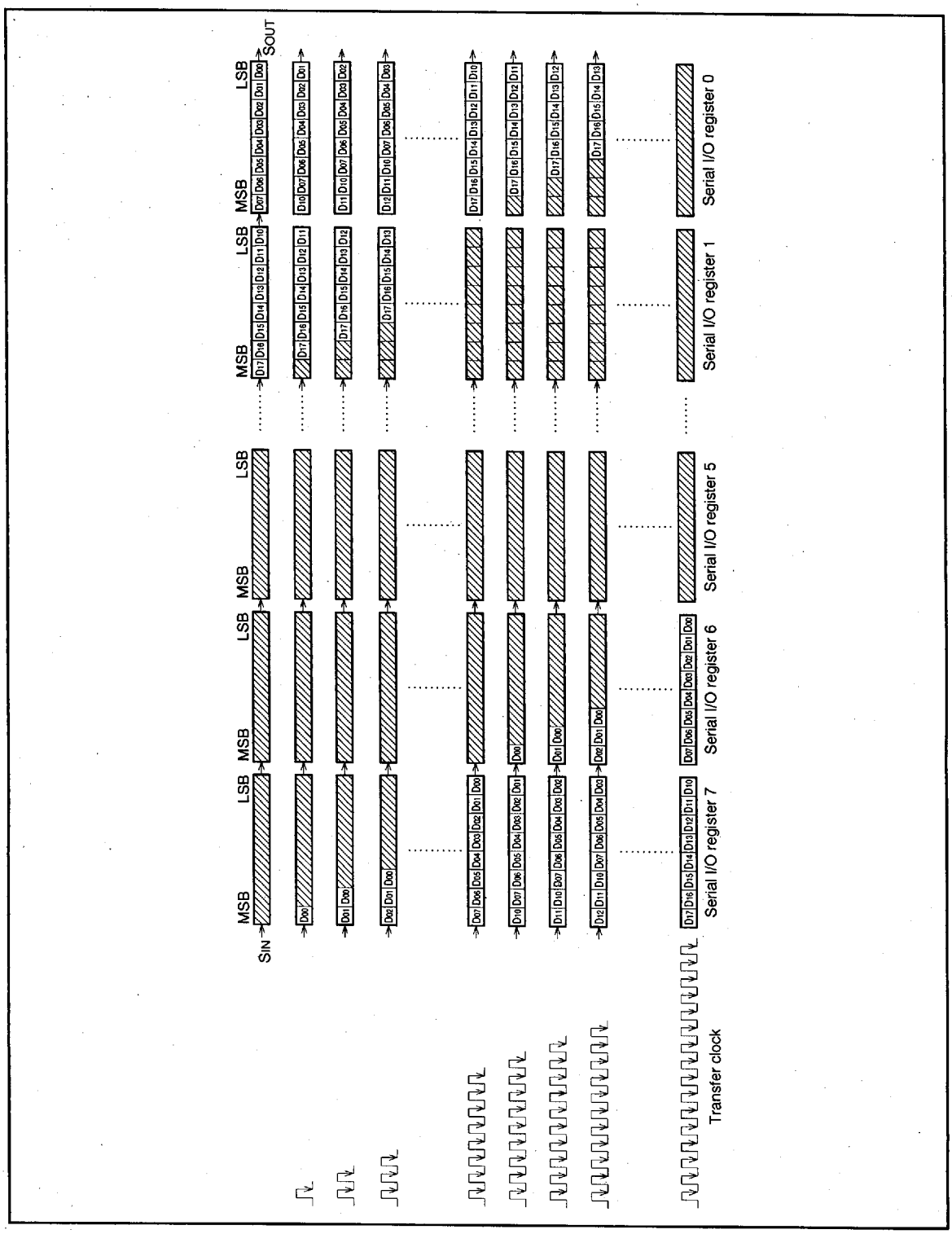


Fig. 13 Serial I/O register state during transmission of 2-byte date

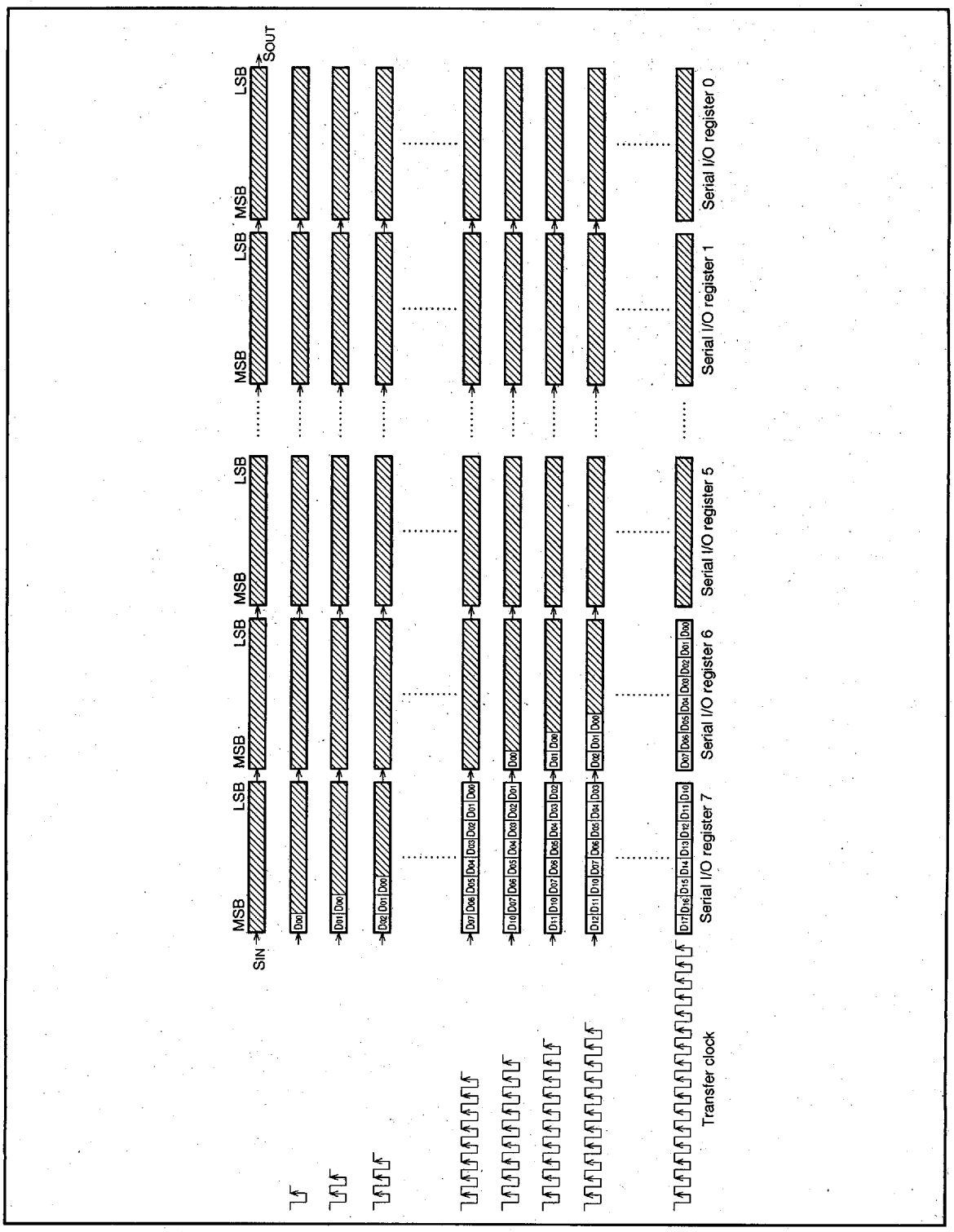


Fig. 14 Serial I/O register state during reception of 2-byte date

SPECIAL MODE (I^2C BUS MODE*)

M37260M6-XXXSP has a special serial I/O circuit that can be reception or transmission of serial data in conformity with I^2C (inter IC) bus format.

I^2C bus is a two line directional serial bus developed by Philips to transfer and control data among internal ICs of a machinery.

M37260M6-XXXSP's special serial I/O is not included the clock synchronisation function and the arbitration detectable function at multimaster.

Operations of master transmission and master reception with special serial I/O explained in the following:

(1) Master Transmission

① To generate an interrupt at the end of transmission, set bit 3 of serial I/O mode register 2 (address $00CE_{16}$) to "1" so as to special serial I/O interrupt is selected.

② Then set bit 1 of interrupt control register 2 (address $00FF_{16}$) to "1" so as to special serial I/O interrupt is enabled. Clear the interrupt disable flag I to, "0" by using the CLI instruction.

③ The output signals of master transmission SDA and SCL are output from ports $P3_4$ and $P3_5$. Set all bits (bits 4 and 5) corresponding to $P3_4$ and $P3_5$ of the port P3 register (address $00C6_{16}$) and the port P3 direction register(address $00C7_{16}$)to "1".

④ Set the transmission clock. The transmission clock uses the overflow signal of timer 4. Set appropriate value in timer 4 and timer 34 mode register. (For instance, if f (X_{IN}) /2 is selected as the clock source of timer 4 and 9 is set in timer 4 when f (X_{IN}) is 4MHz, the master transmission clock frequency is 100kHz.)

⑤ Set contents of the special mode register 2 (address $00F8_{16}$). (Usually, the vaule is "03_{16}".)

⑥ Set the bits 3 and 4 of serial I/O mode register 1(address $00CD_{16}$) so as the port $P3_4$ and $P3_5$ is specified to SDA and SCL. After that set the special mode register 1 (address $00F7_{16}$). Figure 18 shows the stucture of special mode registers 1 and 2.
Initial setting is completed by the above procedure.

⑦ Clear bits 0 and 1 of special mode register 2 (to "0") to make both SDA and SCL output to "L". This is for arbitration. Immediately after this, write data to be transmitted in the special serial I/O register (address $00F6_{16}$). The start signal has been completed.
The hardware automatically sends out data of 9-clock cycle. The 9th clock is for ACK reception and the output level becomes "H" at this clock. If other master outputs the start signal to transmit data simultaneously with this 9th clock, it is not detected as an arbitrationlost.
When the ACK bit has been transmitted, bit 1 of the interrupt request register 2 is set to "1" (issue of interrupt request), notifying the end of data transmission.

⑧ To transmit data successively, write data to be sent to the special serial I/O register, and set the interrupt enabled state again. By repeating this procedure, unlimited number of bytes can be transmitted.

⑨ To terminate data transfer, clear bits 0 and 1 of the special mode register 2 to "0".

⑩ Set bit 1 clock SCL to "1".

⑪ Then set bit 0 data SDA to "1". This procedure transmits the stop signal.
Figure 16 shows master transmission timing explained above.(the numbers in this figure are correspond to above explained numbers.)

(2) Master Reception

Master reception is carried out in the interrupt routine after data is transferred by master transmission. For master transmission and interrupt thereafter, see the preceding section (1) Master transmission (the process until ⑦ in Figure 16.)

⑫ In the interrupt routine, set master reception ACK provided (22_{16}) in the special mode register 1 (address $00F7_{16}$).

⑬ Write "FF_{16}" in the special serial I/O register (address $00F6_{16}$). This sets data line SDA to "H" and to perform 8-clock master reception. Then, a clock of "L" is transmitted to data line SDA for ACK receiving. In the ACK provided mode, the above ACK is automatically sent out.

⑭ Repeat the above receiving operation for a necessary number of times. Then return to the master transmission mode and transmit the stop signal by the same procedure for the master transmission (the process from ⑨ to ⑪ in Figure 16.)
Figure 17 shows master reception timing.

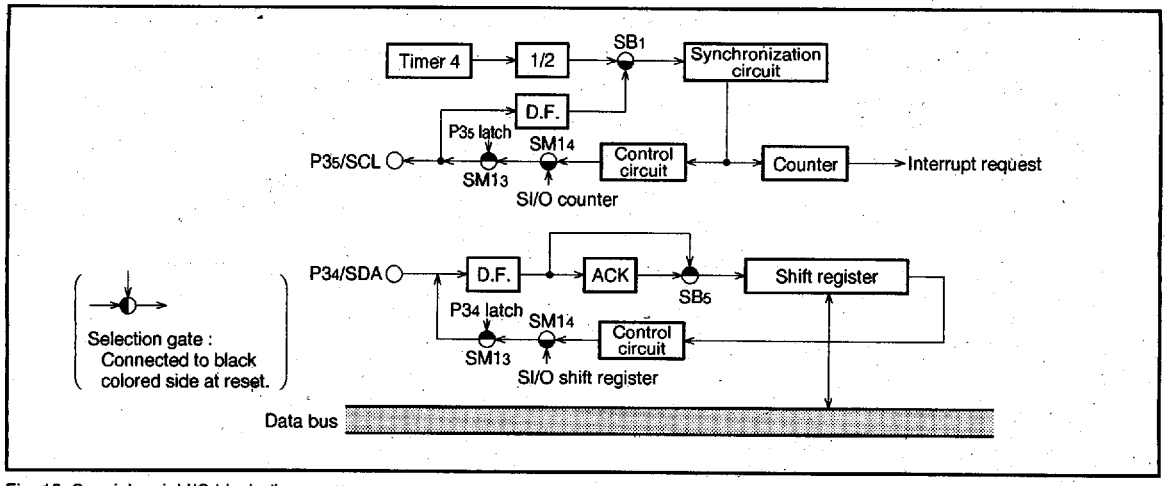


Fig. 15 Special serial I/O block diagram

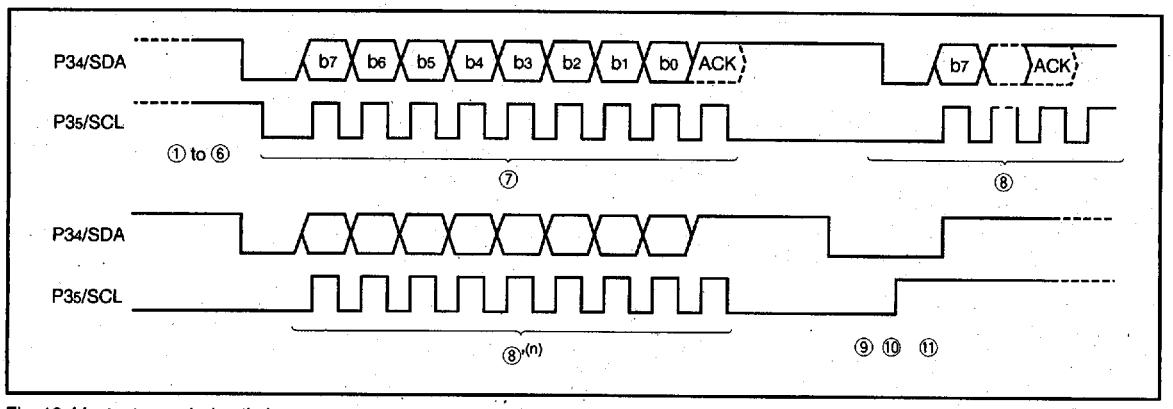


Fig. 16 Master transmission timing

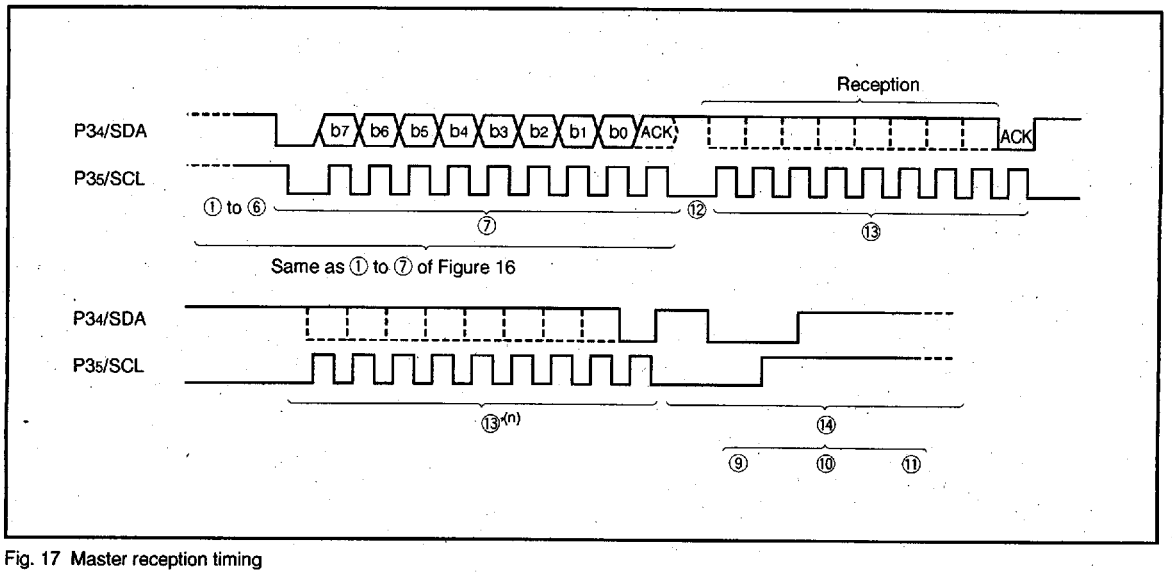


Fig. 17 Master reception timing

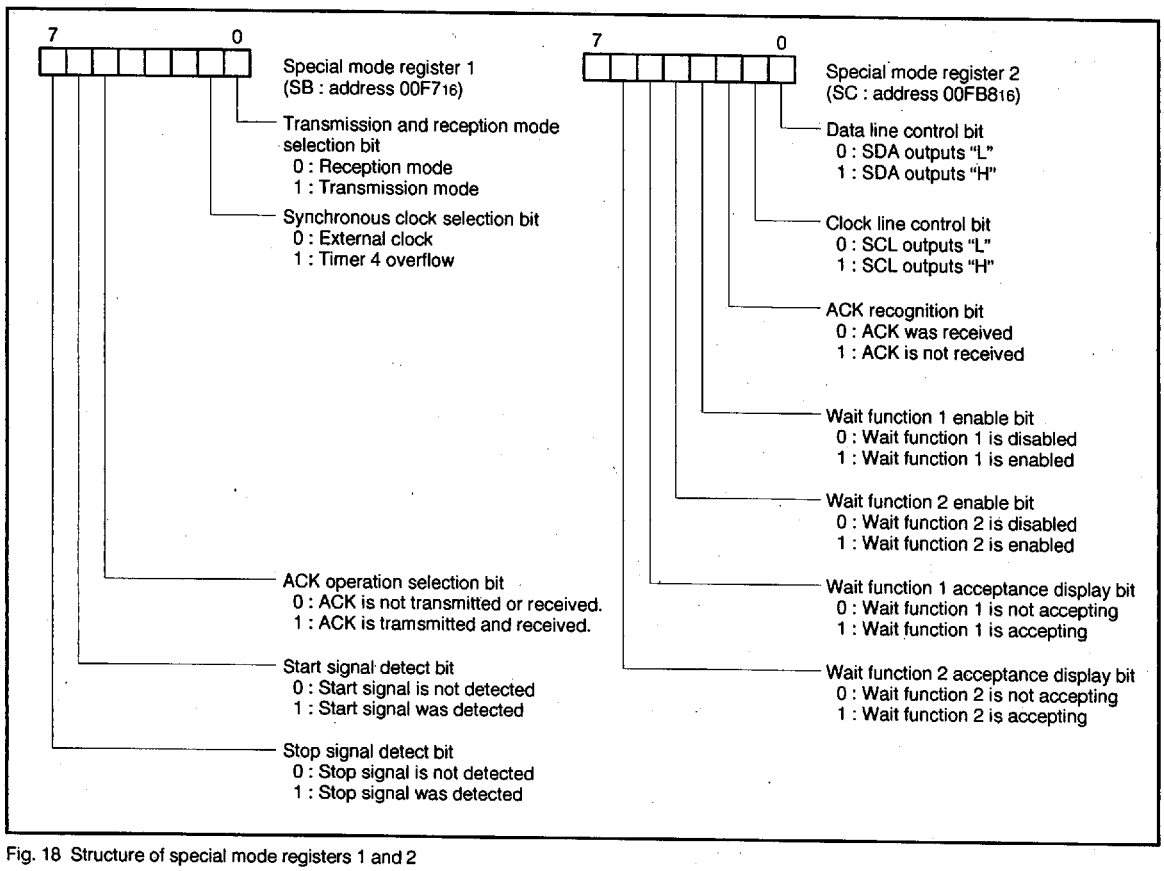


Fig. 18 Structure of special mode registers 1 and 2

(3) Wait Functions

Wait function 1 holds the SCL line at "L" after the 8th clock falls in special mode. Wait function 2 holds the SCL line at "L" after the 9th clock falls in the same way.

When one of the wait functions operates, the internal counter that counts the clock must be reset after bit 3 or 4 of the special mode register 2 is set to "1", to enable the corresponding wait function 1 or 2 to operate, Reset the internal counter by writing data to the special serial I/O register (address 00F616), or by setting the START signal detection bit to "1". Reset the internal counter for each byte before data transfer.

The wait functions can be released by setting the corresponding bit 5 or 6 of the special mode register 2 to "1".

Notes 1 : Clear the START signal detection bit (bit 6) and the STOP signal detection bit (bit 7) of the special mode register 1 by writing "1" to bit 6 or bit 7.

2 : If the special serial I/O function is operating, change the value of bit 4 of the sync generator control register (address 00E916) to suit the frequency of the system clock (XIN).

CRT DISPLAY FUNCTIONS

Table 2 outlines the CRT display functions of the M37260M6-XXXSP. The M37260M6-XXXSP incorporates a 40 columns × 3 lines CRT display control circuit. CRT display is controlled by the CRT display control register.

Up to 510 kinds of characters can be displayed, and colors can be specified for each character. A combination of up to 15 colors can be obtained by using each output signal (R, G, B, and I).

Table 2. Outline of CRT display functions

Parameter		Functions
Display characters		40 characters × 3 lines (maximum 25 lines)
Character configuration		12 × 20 or 16 × 20 dots (refer to Figure19)
Kinds of character		510 kinds
Character size		30 kinds
Color	Kinds of color	1 screen: 15 kinds, maximum 15 kinds
	Coloring unit	A character
Display expansion		Possible (multiline display)
Raster coloring		Possible (maximum 15 kinds)
Character background coloring		Possible (A block unit, 1 screen 3 kinds, maximum 15 kinds)

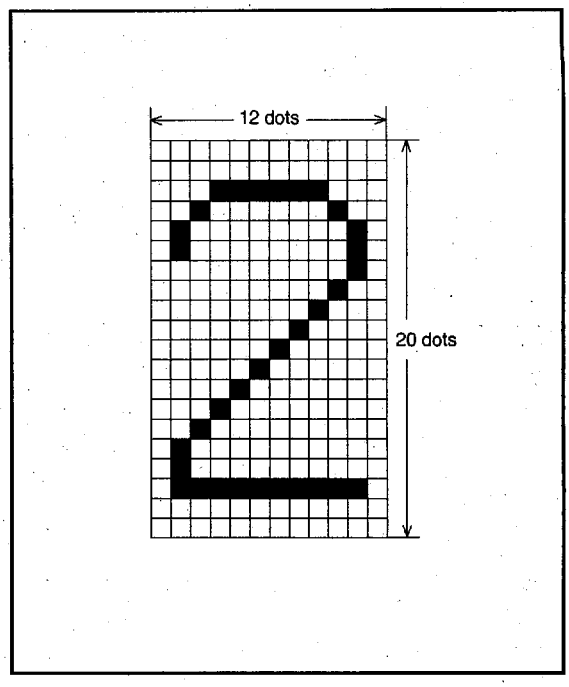


Fig. 19 CRT display character configuration

Characters are displayed in a 12 × 20 or 16 × 20 dots configuration to obtain smooth character patterns. (See Figure 19)

The following shows the procedure how to display characters on the CRT screen.

① Write the display character code to the display RAM.
② Write the color code to the display RAM.
③ Specify the vertical position and character size by using the vertical position register and the character size register.
④ Specify the horizontal position by using the horizontal position register.
⑤ Write the display enable bit to the designated block display flag of the CRT control register. When this is done, the CRT starts operation according to the input of the VSYNC signal.

The CRT display circuit has an extended display mode.

This mode allows multiple lines (more than 4 lines) to be displayed on the screen by interrupting the display each time one line is displayed and rewriting data in the block for which display is terminated by software.

Figure 20 shows a block diagram of the CRT display control circuit. Figure 21 shows the structure of the CRT display control register.

And the mixing circuit is built-in that can be output the signal mixed external color signals with internal color signals, so that the CRT display can be controlled by the 2-chip constructed system.

The sync generator that generates the synchronous signal can be output each synchronous signal as NTSC or PAL with/without interlacing.

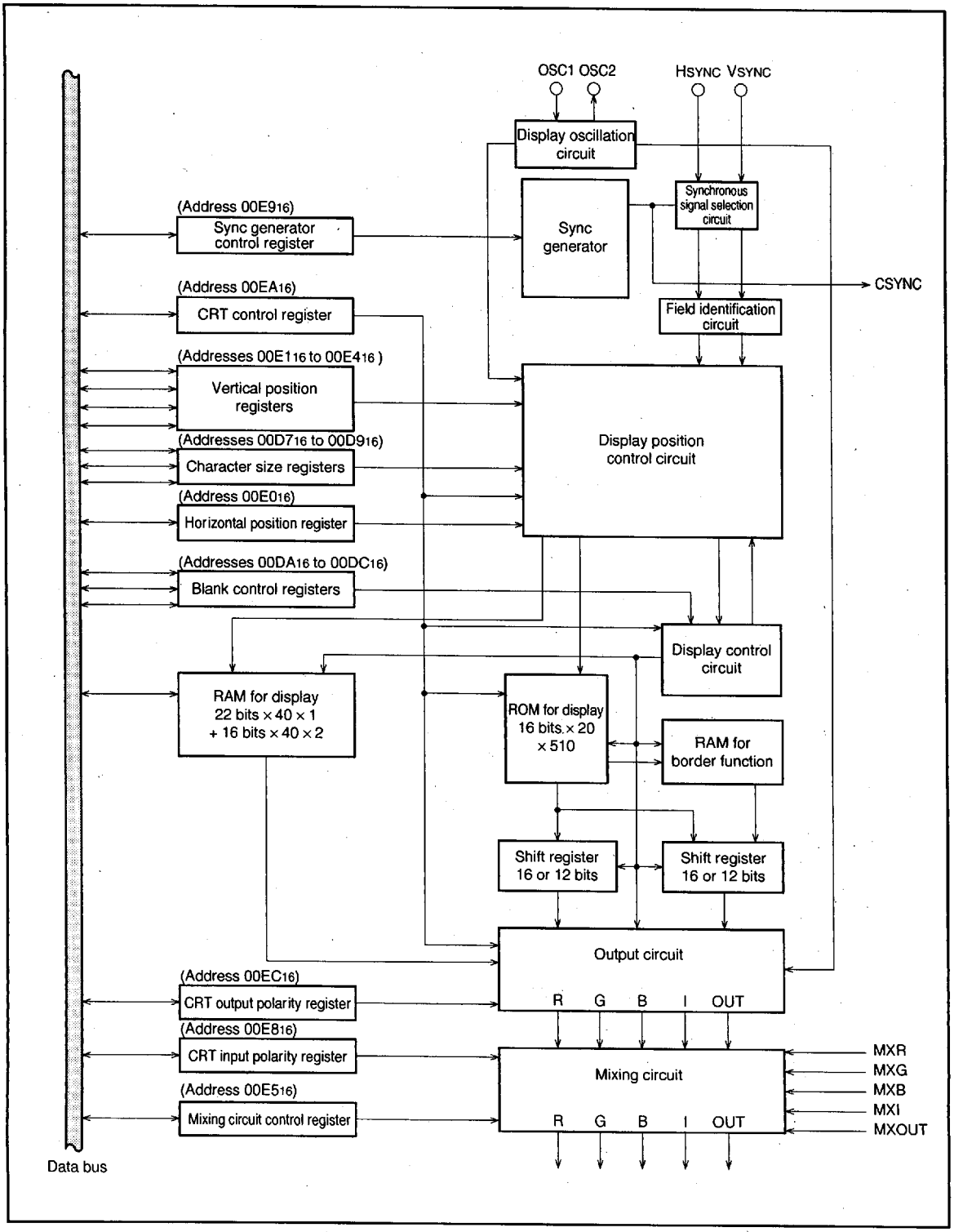


Fig. 20 CRT display control circuit block diagram

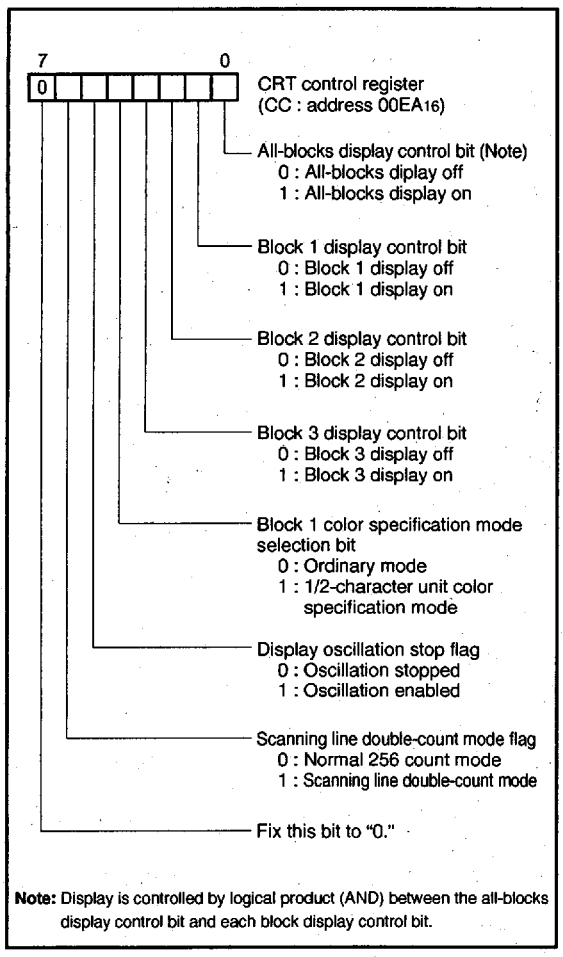


Fig. 21 Structure of CRT control register

(1) Display Position

Character display position is specified in units called blocks. There are three blocks – block 1 to block 3 – and each block can hold up to 40 characters (for details, refer to the previous section (3) Memory for Display).

The display position of each block can be set horizontally and vertically by software.

Horizontal positions can be selected for all blocks in common from 256-steps in 4Tc units (Where Tc : display oscillation period).

Vertical display positions can be selected for each block from 1024-steps in single scanning line units.

If a display start position is superimposed on another block ((b) in Figure 23), the block with the smallest number (1 to 3) is displayed.

If the display position of a block comes while another block is displayed ((c) in Figure 23), the second block is displayed.

Vertical positions for each block can be set in 1024 steps (where each step is one scanning line) as values 0016 to FF16 in vertical position registers 1 to 3 (addresses 00E116 to 00E316)and values 0016 to 3F16 in bits 0 to 5 of vertical position register 4. The structures of the vertical position registers are shown in Figure 22.

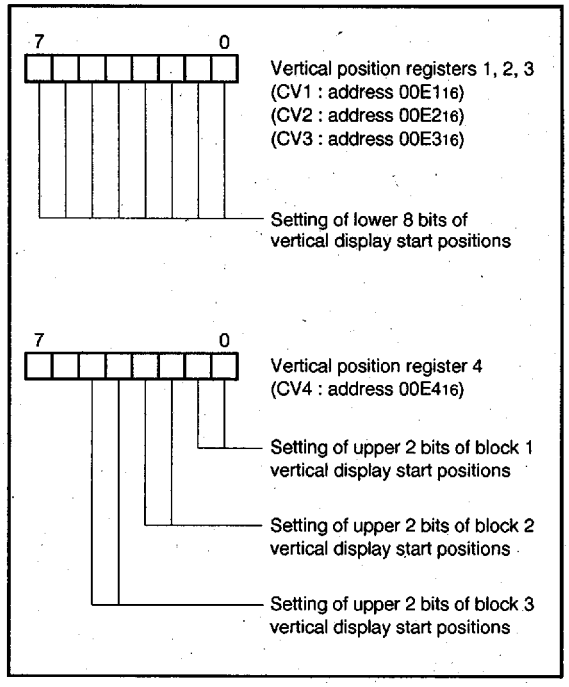
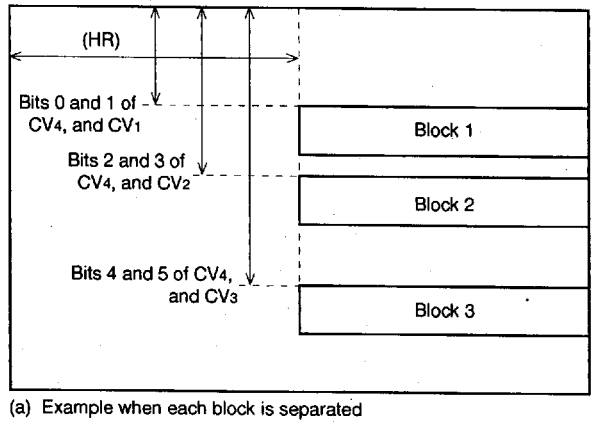
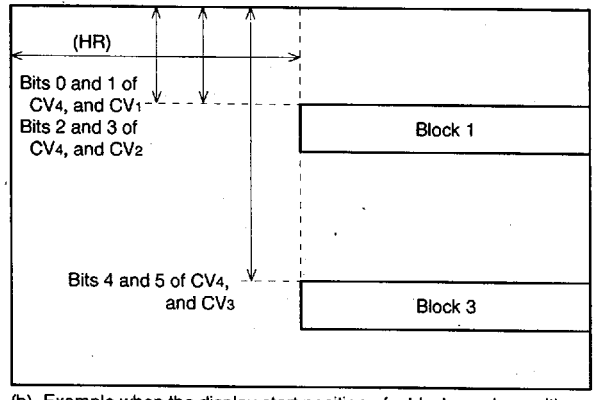


Fig. 22 Structure of vertical position registers

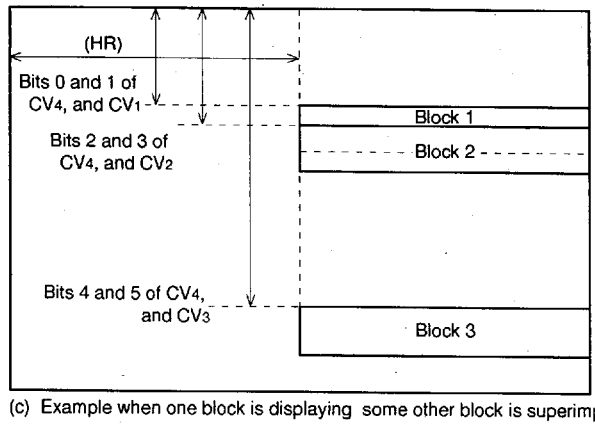
The horizontal position is common to all blocks, and can be set in 256 steps (where one step is 4Tc, Tc being the display oscillation period) as values 0016 to FF16 in the horizontal position register (address 00E016). The structure of the horizontal position register is shown in Figure 24.



(a) Example when each block is separated



(b) Example when the display start position of a block overlaps with some other block



(c) Example when one block is displaying some other block is superimposed.

Fig. 23 Display position and value of vertical position registers CVx (x : 1 to 4)

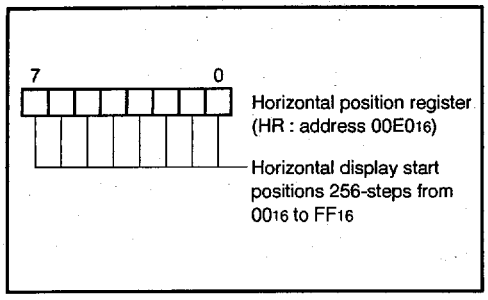


Fig. 24 Structure of horizontal position register

(2) Character Size

The size of characters to be displayed can be selected from 30 types, by combining 5 vertical types and 6 horizontal types in block units. Set the size with the character size registers (addresses 00D716 to 00D916). Either of two character font configurations, 12 dots wide × 20 dots high or 16 dots wide × 20 dots high, can be selected for each block.

The configuration of the character ROM font is shown in Figure 26. The display start position in the horizontal direction is the same, regardless of changes in character size, but it does differ if the character font configuration is changed. The display start position in the horizontal direction for 16 dots wide × 20 dots high characters is 4Tc to the right of that for 12 dots wide × 20 dots high characters.

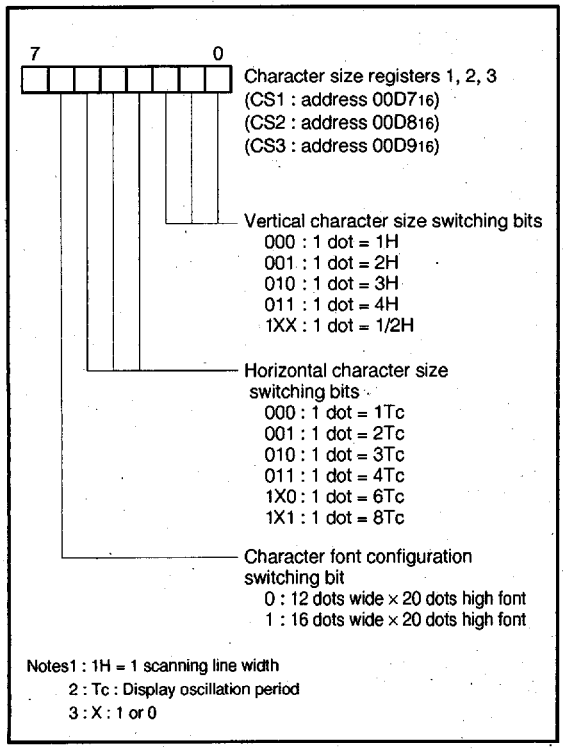


Fig. 25 Structure of character size registers

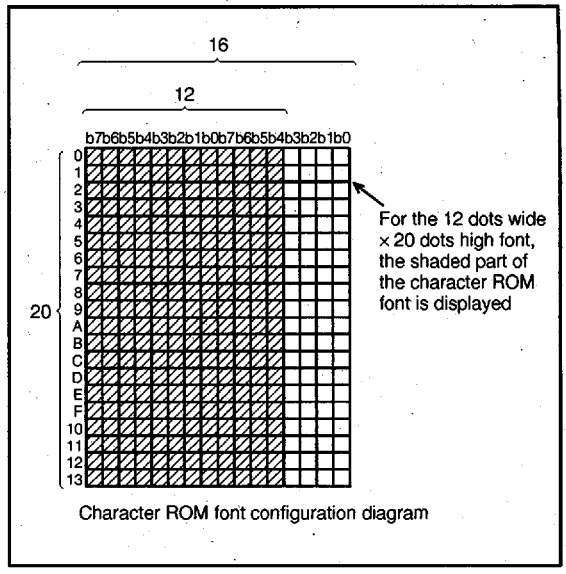


Fig. 26 Character ROM font for 12 dots wide × 20 dots high font

The 1 dot = 1/2 scanning line display function differentiates between odd-numbered and even-numbered fields from differences in the waveform in the synchronization signals used by the interlace method, and displays one character font for both fields. Bit 6 of the sync generator control register (address 00E9$_{16}$) controls the active edge of the field identification flag, and the character font divided for each field can be selected.
The field identification flag can also be read out from bit 6 of the display block counter (address 00EB$_{16}$).

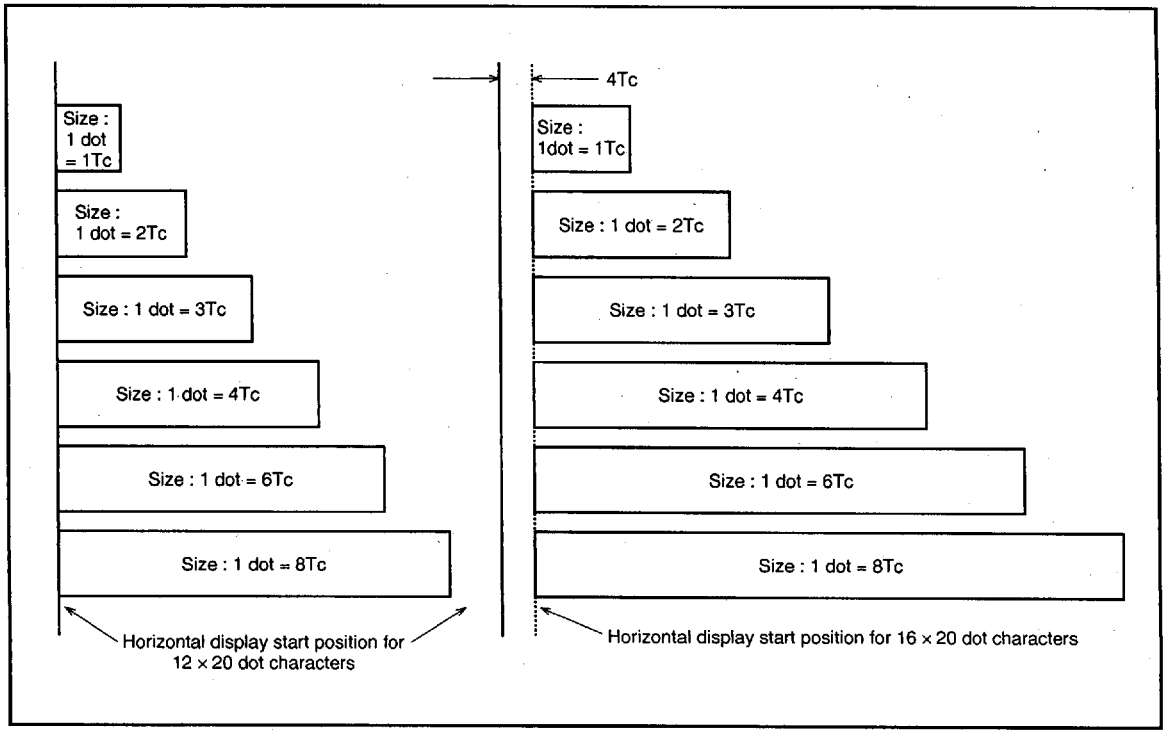


Fig. 27 Display start positions (horizontal) for each character size

The description below assumes that field identification is based on the case where the active edges of both the horizontal and vertical synchronization signals are negative.

Each field is identified as either odd or even by the hardware detecting the positions of the falling edges of the horizontal and vertical synchronization signals, and comparing them. Therefore, to ensure correct field identification, make sure that the two synchronization signals are input in accordance with the identification criteria given below.

Since the field identification is based on the system clock (XIN), make sure that the value of bit 4 of the sync generator control register (address 00E9$_{16}$) is changed in accordance with the frequency of the system clock.

Even-numbered field : The vertical synchronization signal falls within 2μs before or after the fall of the horizontal synchronization signal.

Odd-numbered field : The vertical synchronization signal falls within 2μs before or after a point 1/2 a cycle after the fall of the horizontal synchronization signal.

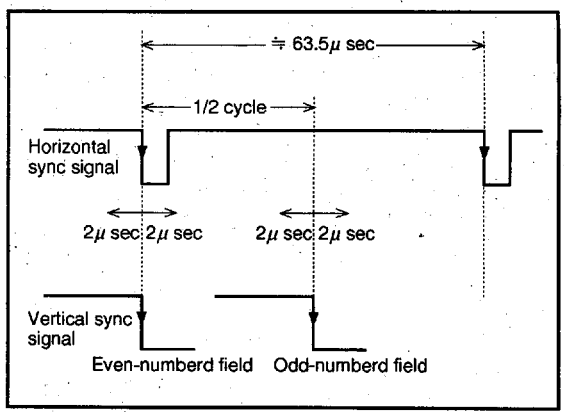
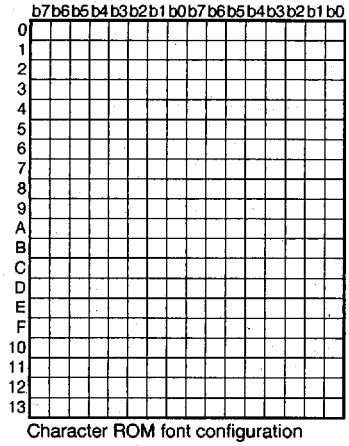


Fig. 28. Identification criteria for field identification

Field	Sync signal (Example : negative edge input)	Field identification flag active edge bit (bit 6 of the sync generator control register)	Field identification flag bit (bit 6 of the display block counter)	Display font
Odd-numbered field	Horizontal sync signal	0	1	□ part
	Vertical sync signal	1	0	□ part
Even-numbered field	Horizontal sync signal	0	0	□ part
	Vertical sync signal	1	1	□ part



Character ROM font configuration

Example : When the field identification flag active edge bit is 0, odd-numbered fields display the □ font and even-numbered fields display the □ font, Bit 6 of the display block counter can be read as the field identification flag : it is "1" for an odd-numbered field, "0" for an even-numbered field.

Note : The field identification flag changes at the fall of the vertical sync signal (negative edge input).

Fig. 29 Relationships between field identification flag and display font

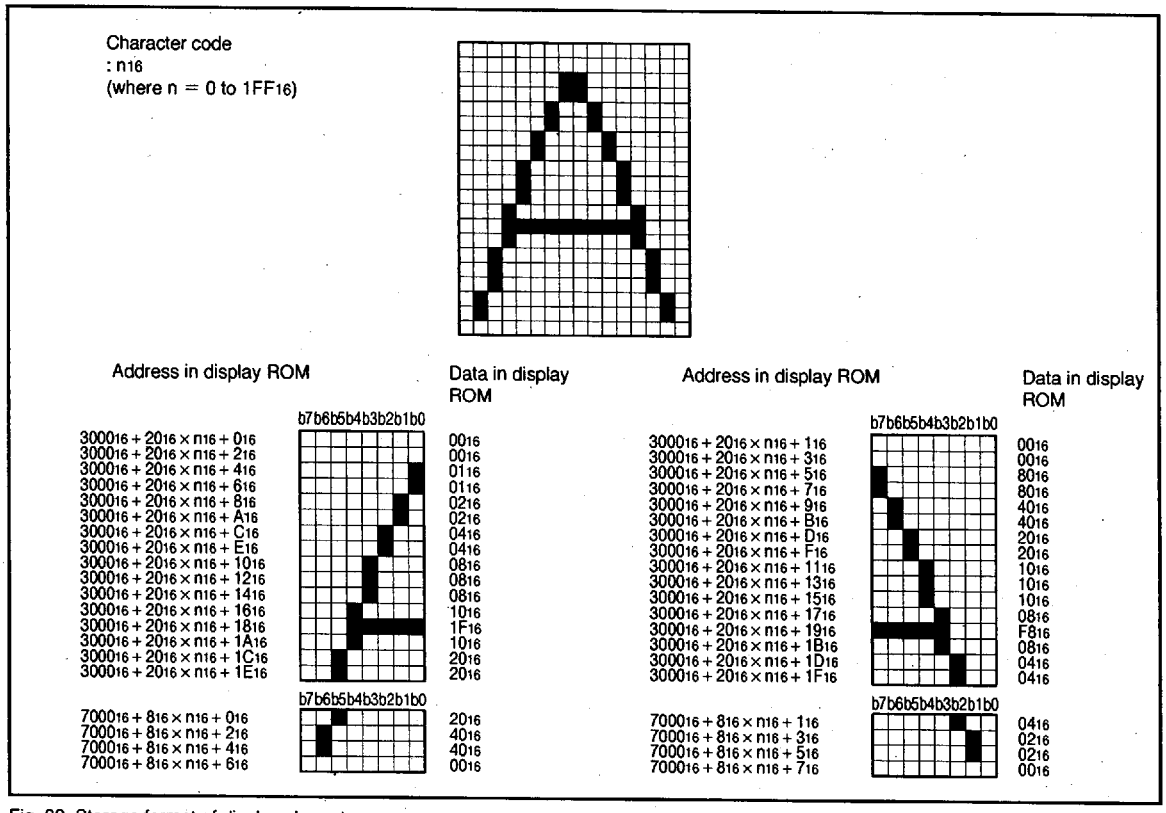


Fig. 30 Storage format of display characters

(3) Memory for Display

There are two types of memory for display : CRT display ROM (addresses 300016 to 7FFF16) which contains previously stored (masked) character dot data, and display RAM (addresses 200016 to 27FF16) which specifies characters and colors to be displayed. These memory types are described below.

① ROM for display(addresses 300016 to 7FFF16)

The CRT display ROM contains dot pattern data for display characters. To display these stored characters in operation, specify character codes (code determined based on addresses in CRT display ROM) that are specific to those characters, by writing them to the CRT display RAM.

Since the CRT display ROM has contains 20K bytes and the data for one character takes up 40 bytes, 512 characters can be stored. However, a two-character space is required for test purposes, so in practice 510 characters can be stored for display.

Within the CRT display ROM area, data for part of each character that is [upper 16 dots high] × [left-hand 8 dots wide] is stored at addresses 300X16 to 3FFX16 (where X = 0, 2, 4, 6, 8, A, C, E),data for part of each character that is [upper 16 dots high] × [right-hand 8 dots wide] is stored at 300Y16 to 3FFY16 (where Y = 1, 3, 5, 7, 9, B, D, F), data for part of each character that is [lower 4 dots high] × [left-hand 8 dots wide] is stored at addresses 700M16 to 7FFM16 (where M = 0, 2, 4, 6, 8, A, C, E), and data for part of each character that is [lower 4 dots high] × [right-hand 8 dots wide] is stored at 700N16 to 7FFN16 (where N = 1, 3, 5, 7, 9, B, D, F), as shown in Figure 30.

Table 3. Character Code Chart (Partially abbreviated)

Character code	Character data storage address			
	Left-hand 8 dots		Right-hand 8 dots	
	Upper 16 dots	Lower 4 dots	Upper 16 dots	Lower 4 dots
00₁₆	3000₁₆	7000₁₆	3001₁₆	7001₁₆
	3002₁₆	7002₁₆	3003₁₆	7003₁₆
	3004₁₆	7004₁₆	3005₁₆	7005₁₆
	3006₁₆	7006₁₆	3007₁₆	7007₁₆
	3008₁₆		3009₁₆	
	300A₁₆		300B₁₆	
	300C₁₆		300D₁₆	
	300E₁₆		300F₁₆	
	3010₁₆		3011₁₆	
	3012₁₆		3013₁₆	
	3014₁₆		3015₁₆	
	3016₁₆		3017₁₆	
	3018₁₆		3019₁₆	
	301A₁₆		301B₁₆	
	301C₁₆		301D₁₆	
	301E₁₆		301F₁₆	
01₁₆	3020₁₆	7008₁₆	3021₁₆	7009₁₆
	3022₁₆	700A₁₆	3023₁₆	700B₁₆
	3024₁₆	700C₁₆	3025₁₆	700D₁₆
	3026₁₆	700E₁₆	3027₁₆	700F₁₆
	3028₁₆		3029₁₆	
	302A₁₆		302B₁₆	
	302C₁₆		302D₁₆	
	302E₁₆		302F₁₆	
	3030₁₆		3031₁₆	
	3032₁₆		3033₁₆	
	3034₁₆		3035₁₆	
	3036₁₆		3037₁₆	
	3038₁₆		3039₁₆	
	303A₁₆		303B₁₆	
	303C₁₆		303D₁₆	
	303E₁₆		303F₁₆	
⋮	⋮	⋮	⋮	⋮
1FF₁₆	6FE0₁₆	7FF8₁₆	6FE1₁₆	7FF9₁₆
	6FE2₁₆	7FFA₁₆	6FE3₁₆	7FFB₁₆
	6FE4₁₆	7FFC₁₆	6FE5₁₆	7FFD₁₆
	6FE6₁₆	7FFE₁₆	6FE7₁₆	7FFF₁₆
	6FE8₁₆		6FE9₁₆	
	6FEA₁₆		6FEB₁₆	
	6FEC₁₆		6FED₁₆	
	6FEE₁₆		6FEF₁₆	
	6FF0₁₆		6FF1₁₆	
	6FF2₁₆		6FF3₁₆	
	6FF4₁₆		6FF5₁₆	
	6FF6₁₆		6FF7₁₆	
	6FF8₁₆		6FF9₁₆	
	6FFA₁₆		6FFB₁₆	
	6FFC₁₆		6FFD₁₆	
	6FFE₁₆		6FFF₁₆	

Each character code used when specifying display characters is defined as n₁₆ (where n = 0 to 1FF), and is determined based on the address in CRT display ROM that contains the data for that character (see the storage format of display character shown in Fig. 30). The character codes are listed in Table 3.

② RAM for display (addresses 2000₁₆ to 27FF₁₆)

The CRT display RAM is allocated at addresses 2000₁₆ to 27FF₁₆, and is divided into a display character code specification part and a display color code specififcation part for each block. The contents of this area are shown in Table 4.

For example, to display one character at the first character position (the left edge) of block 1, write the character code to bit 6 of address 20C0₁₆ and to address 2000₁₆, and write the color code to the lowermost 6 bits (bits 0 to 5) of address 20C0₁₆. For details of the color codes, see section (4) Color codes. The structure of the CRT display RAM is shown in Fig.31.

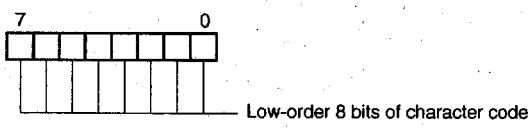
When generating a mask for the M37260M6-XXXSP, note that the character patterns of Table 6 and Table 7 must be written to the specified addresses as a test character pattern.

Table 4. Contents of CRT display RAM

Block	Display position (from left side)	Character code specification		Color code specification	1/2 character unit color code specification
		High-order 1 bit	Low-order 8 bit		
Block 1	1st character	$20C0_{16}$	2000_{16}	$20CO_{16}$	2180_{16}
	2nd character	$20C1_{16}$	2001_{16}	$20C1_{16}$	2181_{16}
	3rd character ⋮ 38th character	$20C2_{16}$ ⋮ $20E5_{16}$	2002_{16} ⋮ 2025_{16}	$20C2_{16}$ ⋮ $20E5_{16}$	2182_{16} ⋮ $21A5_{16}$
	39th character	$20E6_{16}$	2026_{16}	$20E6_{16}$	$21A6_{16}$
	40th character	$20E7_{16}$	2027_{16}	$20E7_{16}$	$21A7_{16}$
Not used		$20E8_{16}$ to $20FF_{16}$	2028_{16} to $203F_{16}$	$20E8_{16}$ to $20FF_{16}$	
Block 2	1st character	2100_{16}	2040_{16}	2100_{16}	
	2nd character	2101_{16}	2041_{16}	2101_{16}	
	3rd character ⋮ 38th character	2102_{16} ⋮ 2125_{16}	2042_{16} ⋮ 2065_{16}	2102_{16} ⋮ 2125_{16}	
	39th character	2126_{16}	2066_{16}	2126_{16}	
	40th character	2127_{16}	2067_{16}	2127_{16}	
Not used		2128_{16} to $213F_{16}$	2068_{16} to $207F_{16}$	2128_{16} to $213F_{16}$	
Block 3	1st character	2140_{16}	2080_{16}	2140_{16}	
	2nd character	2141_{16}	2081_{16}	2141_{16}	
	3rd character ⋮ 38th character	2142_{16} ⋮ 2165_{16}	2082_{16} ⋮ $20A5_{16}$	2142_{16} ⋮ 2165_{16}	
	39th character	2166_{16}	$20A6_{16}$	2166_{16}	
	40th character	2167_{16}	$20A7_{16}$	2167_{16}	
Not used		2168_{16} to $217F_{16}$	$20A8_{16}$ to $20BF_{16}$	2168_{16} to $217F_{16}$	

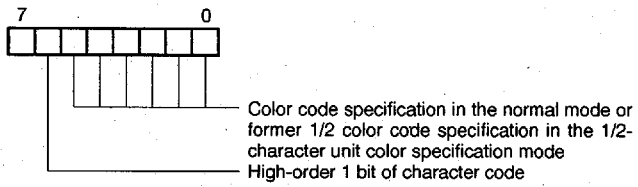
Block 1
[Character specification]

1st character : 200_{16}
to
40th character : 202_{16}

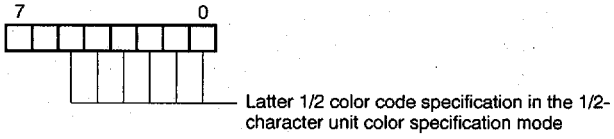


[Color and character specification]

1st character : $20C_{16}$
to
40th character : $20E_{16}$



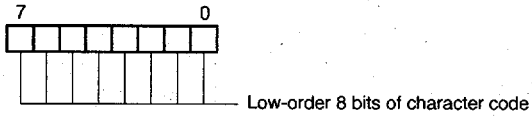
1st character : 218_{16}
to
40th character : $21A_{16}$



Block 2 and 3
[Character specification]

1st character : 204_{16}
to
40th character : 206_{16}

(Addresses 208_{16} to $20A_{16}$ in the case of block 3)



[Color and character specification]

1st character : 210_{16}
to
40th character : 212_{16}

(Addresses 214_{16} to 216_{16} in the case of block 3)

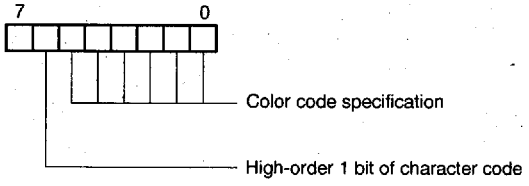


Fig. 31 Structure of CRT display RAM

③ Block overwriting function of display memory

Character codes or color codes for 40 characters can be written for each block in a batch by overwriting data at a specific address.

The addresses for block overwriting, the addresses in display memory overwritten by these addresses, and the contents of these addresses are listed in Table 5.

Table 5. Block overwriting of display memory

Address for block overwriting	Addresses in overwritten display memory	Memory contents
220016	200016 to 202716	Block 1 character code
220116	204016 to 206716	Block 2 character code
220216	208016 to $20A716$	Block 3 character code
220316	$20C016$ to $20E716$	Block 1 color code
220416	210016 to 212716	Block 2 color code
220516	214016 to 216716	Block 3 color code
220616	218016 to $21A716$	Block 1 color code 2

Note : After a write instruction is executed for a block overwriting address, wait at least 60 machine cycles before issuing a read or write instruction from the CPU for a block overwriting address or for display memory.

④ Notes on display RAM data access

If the display RAM is accessed (data read or write, block write) from the CPU during OSD display, make sure that the display RAM for each block is accessed after it has been confirmed that the block has been displayed, by an event such as a CRT interrupt.

RAM data can be destroyed if the display RAM for a block that is currently being displayed is accessed.

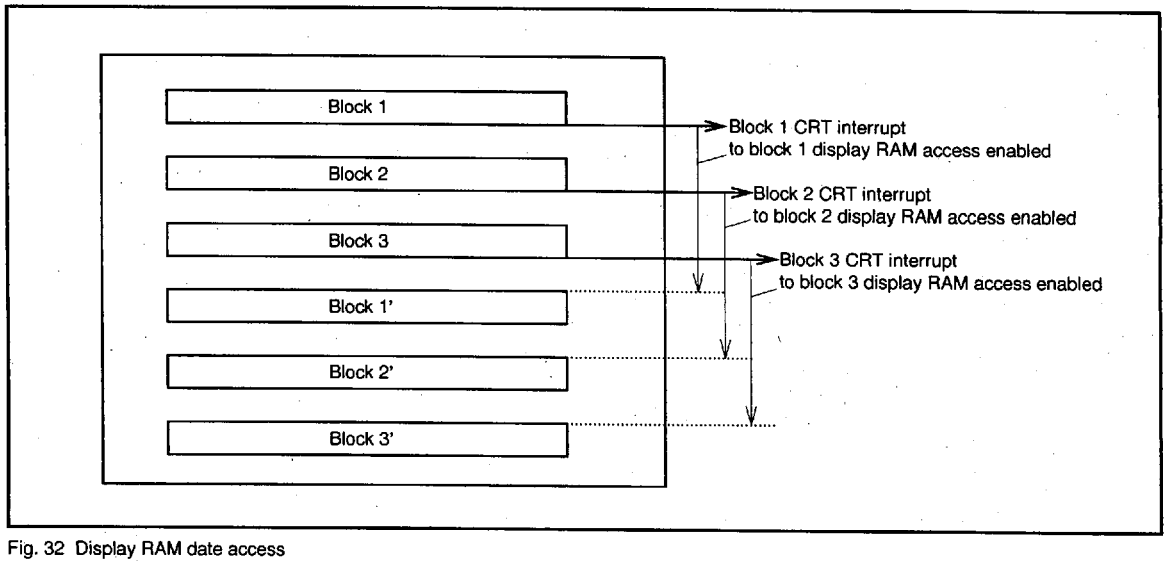


Fig. 32 Display RAM date access

Table 6. Test character pattern 1 settings

Address	Data	Address	Data
6FE0₁₆	00₁₆	6FF0₁₆	00₁₆
6FE1₁₆	00₁₆	6FF1₁₆	00₁₆
6FE2₁₆	00₁₆	6FF2₁₆	00₁₆
6FE3₁₆	00₁₆	6FF3₁₆	00₁₆
6FE4₁₆	00₁₆	6FF4₁₆	00₁₆
6FE5₁₆	00₁₆	6FF5₁₆	00₁₆
6FE6₁₆	00₁₆	6FF6₁₆	00₁₆
6FE7₁₆	00₁₆	6FF7₁₆	00₁₆
6FE8₁₆	00₁₆	6FF8₁₆	00₁₆
6FE9₁₆	00₁₆	6FF9₁₆	00₁₆
6FEA₁₆	00₁₆	6FFA₁₆	00₁₆
6FEB₁₆	00₁₆	6FFB₁₆	00₁₆
6FEC₁₆	00₁₆	6FFC₁₆	00₁₆
6FED₁₆	00₁₆	6FFD₁₆	00₁₆
6FEE₁₆	00₁₆	6FFE₁₆	00₁₆
6FEF₁₆	00₁₆	6FFF₁₆	00₁₆
7FF8₁₆	00₁₆	7FFC₁₆	00₁₆
7FF9₁₆	00₁₆	7FFD₁₆	00₁₆
7FFA₁₆	00₁₆	7FFE₁₆	00₁₆
7FFB₁₆	00₁₆	7FFF₁₆	00₁₆

Table 7. Test character pattern 2 settings

Address	Data	Address	Data
6FC0₁₆	88₁₆	6FD0₁₆	22₁₆
6FC1₁₆	11₁₆	6FD1₁₆	22₁₆
6FC2₁₆	00₁₆	6FD2₁₆	00₁₆
6FC3₁₆	00₁₆	6FD3₁₆	00₁₆
6FC4₁₆	00₁₆	6FD4₁₆	00₁₆
6FC5₁₆	00₁₆	6FD5₁₆	00₁₆
6FC6₁₆	00₁₆	6FD6₁₆	00₁₆
6FC7₁₆	00₁₆	6FD7₁₆	00₁₆
6FC8₁₆	44₁₆	6FD8₁₆	11₁₆
6FC9₁₆	44₁₆	6FD9₁₆	11₁₆
6FCA₁₆	00₁₆	6FDA₁₆	00₁₆
6FCB₁₆	00₁₆	6FDB₁₆	00₁₆
6FCC₁₆	00₁₆	6FDC₁₆	00₁₆
6FCD₁₆	00₁₆	6FDD₁₆	00₁₆
6FCE₁₆	00₁₆	6FDE₁₆	00₁₆
6FCF₁₆	00₁₆	6FDF₁₆	00₁₆
7FF0₁₆	08₁₆	7FF4₁₆	00₁₆
7FF1₁₆	88₁₆	7FF5₁₆	00₁₆
7FF2₁₆	00₁₆	7FF6₁₆	80₁₆
7FF3₁₆	00₁₆	7FF7₁₆	11₁₆

(4) Color Codes

The color each display character can be specified by specifying the four color outputs (R, G, B, and I) with the CRT display RAM. A color code can be specified for each character, and $2^4 = 16$ colors can be set.

The R, G, B, and I outputs are set by bits 0 to 3 of the color code, character or blank output is set by bit 4, and character output or blank output is specified by bit 5. The structure of the color code is shown in Figure 33.

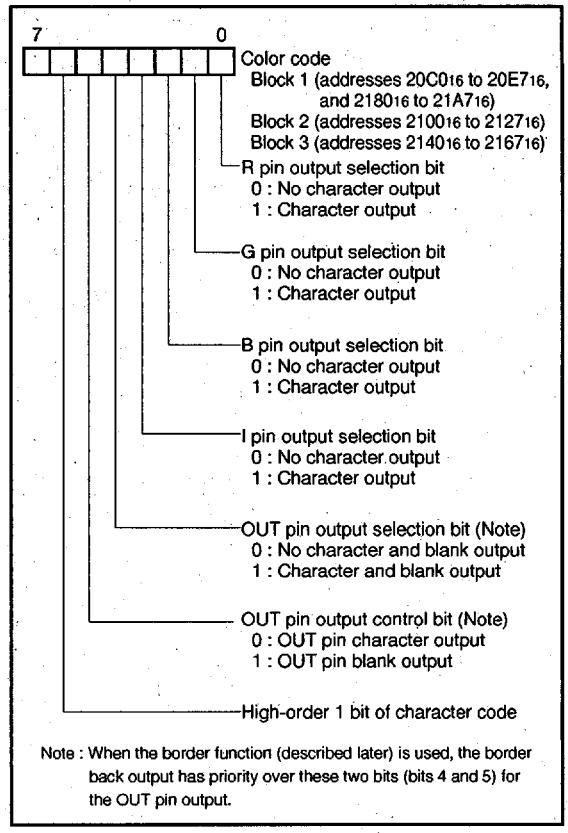


Fig. 33 Structure of color code

(5) 1/2-Character Unit Color Specification Mode

Colors can be specified in 1/2-characters units for the characters of block 1 alone, by setting bit 4 of the CRT control register (address 00EA16). In 1/2-character unit color specification mode, each half of a display character in block 1 is displayed as follows :

- Left-hand half : The color of the color code specified by bits 0 to 5 of color code specification addresses 20C016 to 20E716 in the CRT display RAM.
- Right-hand half : The color of the color code specified by bits 0 to 5 of color code specification addresses 218016 to 21A716 in the CRT display RAM.

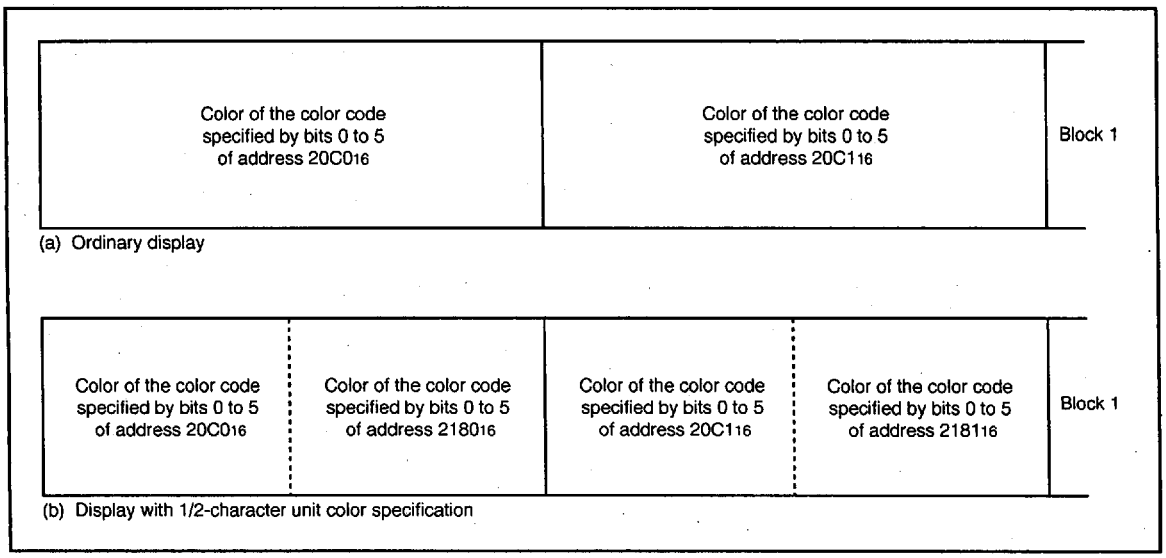


Fig. 34 Correspondence between ordinary color specification and 1/2-character unit color specification mode

(6) Multiline Display

The M37260M6-XXXSP can ordinarily display three lines of characters, in three blocks with different vertical positions.

In addition, up to 25 lines can be displayed by using CRT interrupts and the display block counter.

A CRT interrupt is a function that generates an interrupt for each block at the point at which the display of any desired number of dots has been completed. In other words, when a scanning line reaches the point of the display position (specified by the vertical and horizontal position registers) of a certain block, the character display of that block starts,and an interrupt is issued at the point at which the number of dots set by the interrupt position control register is exceeded.

If the lateral character size has been set to 1 dot = 1/2 scanning line width, the CRT interrupt position can be set to 10 steps in 1 block/2 dot units ; for all other scanning line widths it can be set to 20 steps in 1 block/1 dot units.

The display block counter counts the number of times the display of a block has been completed, and its contents are incremented by 1 each time the display of one block is completed.

To provide multiline display, enable CRT interrupts by clearing the interrupt disable flag to "0" and setting the CRT interrupt enable bit (bit 4 at address $00FE_{16}$) to "1".

The processing within the CRT interrupt processing routine is as follows.

① Read the value of the display block counter.
② The value of ① enables identification of a block whose display has completed (whether a CRT interrupt generation cause has occurred).
③ Read the interrupt position control register.
④ The value of ③ enables identification of the number of dots at which the CRT interrupt is to occur.
⑤ Write the display character code, color code, and vertical display position of that block into the character code, color code (CRT display RAM contents), and vertical display position (contents of vertical position register) to be displayed next.

The structure of the display block counter is shown in Figure 35.

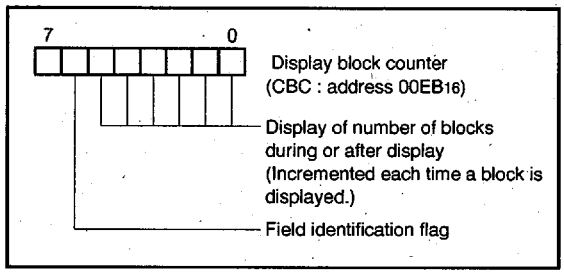


Fig. 35 Structure of display block counter

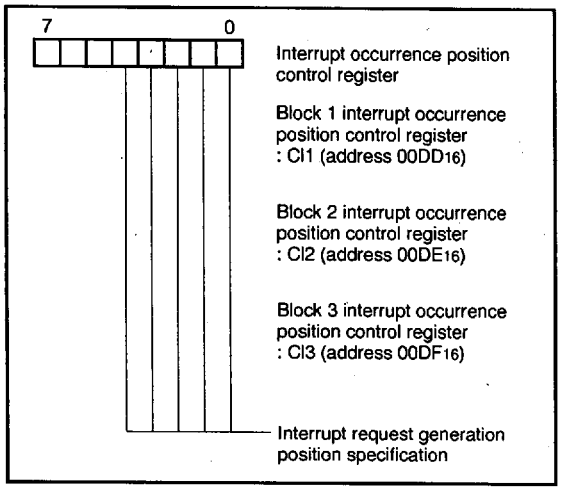


Fig. 36 Structure of interrupt position control register

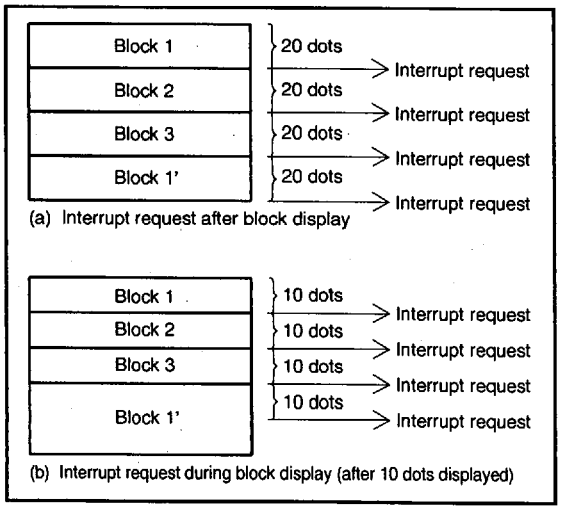


Fig. 37 Timing of CRT interrupts

(a) When lateral character size is not 1 dot = 1/2 scanning line width

Interrupt occurrence position control register					Timing of interrupt request generation
b4	b3	b2	b1	b0	
0	0	0	0	0	Interrupt after completion of 1-dot display
0	0	0	0	1	Interrupt after completion of 2-dot display
0	0	0	1	0	Interrupt after completion of 3-dot display
0	0	0	1	1	Interrupt after completion of 4-dot display
		:			:
		:			:
1	0	0	1	1	Interrupt after completion of 20-dot display
		:			} Interrupts disabled (no interrupt requests)
		:			
1	1	1	1	1	

(b) When lateral character size is 1 dot = 1/2 scanning line width

Interrupt occurrence position control register					Timing of interrupt request generation			
b4	b3	b2	b1	b0		Odd-numbered field	Even-numbered field	
0	0	0	0	×	Interrupt after completion of	1	2	dot display
0	0	0	1	×		3	4	
0	0	1	0	×		5	6	
0	0	1	1	×		7	8	
		:		×		:	:	
		:		×		:	:	
1	0	0	1	×		19	20	
		:		×	} Interrupts disabled (no interrupt requests)			
		:		×				
1	1	1	1	×				

Fig. 38 Timing of interrupt request generation with respect to values in interrupt position control register

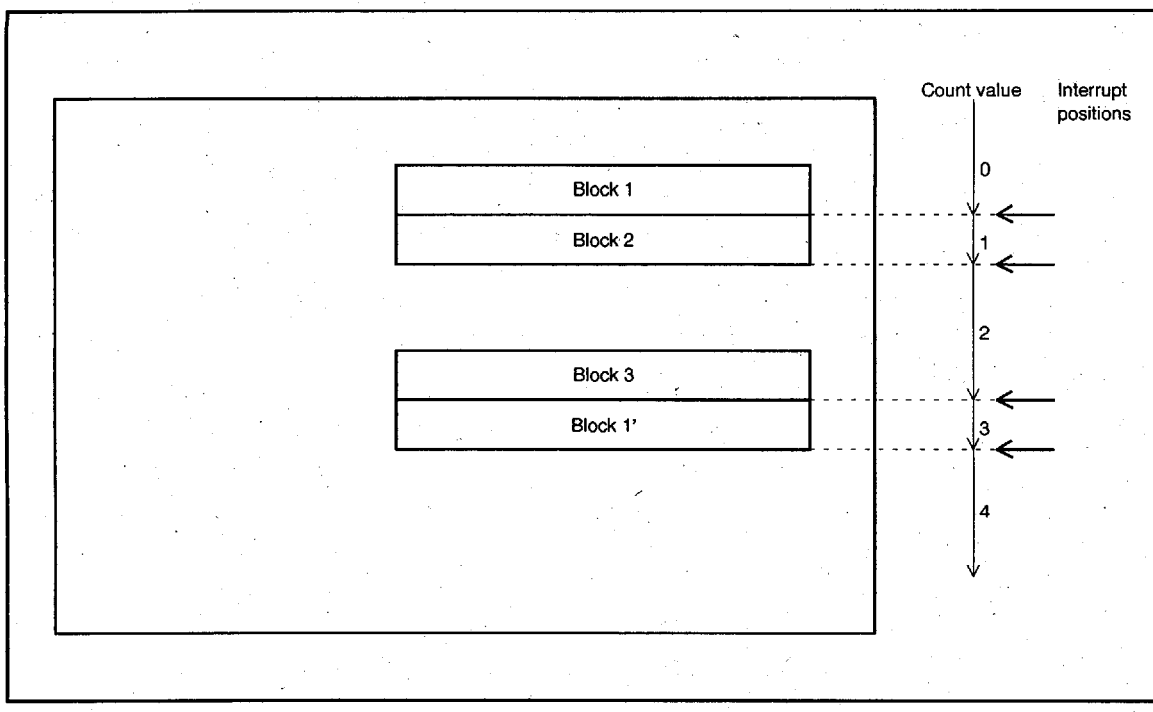


Fig. 39 Timing of CRT interrupts and values in display block counter

(7) Scanning Line Double-Count Mode

Scanning line double-count mode enables an increase in character size in the vertical direction to twice the normal size, and it can also double the display start position of the characters in the vertical direction by double-counting scanning lines. In other words, the vertical position register sets either a normal mode in which one step is one scanning line, or a scanning line double-count mode is which one step is two scanning lines.

Scanning line double-count mode can be specified by setting bit 6 of the CRT control register (address 00EA16) to "1".
Since this mode functions in screen units, a change in mode while a screen is being displayed is not validated until the next screen is displayed.

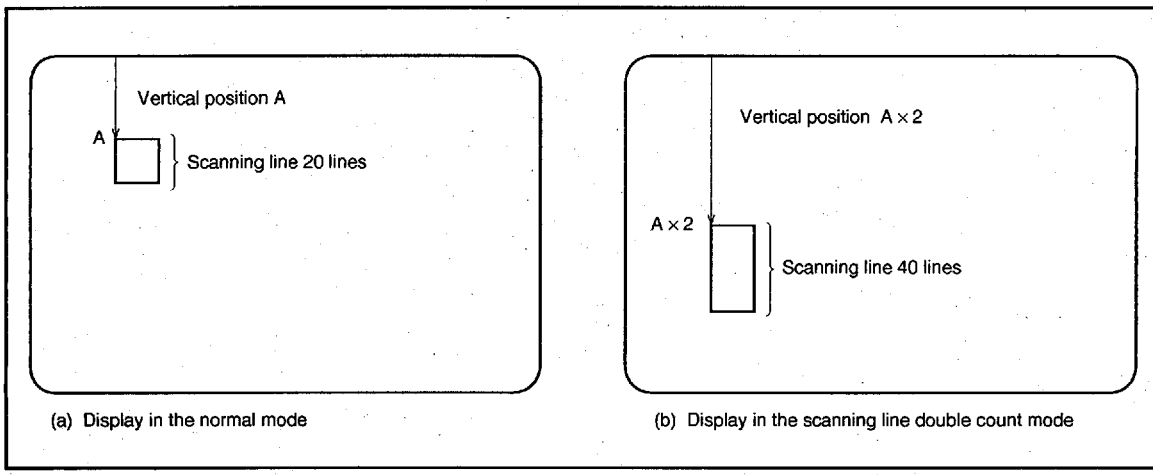


Fig. 40 Corresponding between normal mode display and scanning line double-count mode display

(8) Border Function

A one clock (one dot) border can be drawn around each character displayed, in both the horizontal and vertical directions.
This border is output from the OUT pin. In this case, bits 4 and 5 in the color code (the OUT pin output contents) are ignored, and the border output is output from the OUT pin.

The border can be set in block units by the blank control registers (addresses 00DA16 to 00DC16). The relationship between the settings of the blank control registers and the border function are listed in Table 8, and the structure of the blank control registers is shown in Fig.42.

Table 8. Corresponding between the blank control register value and border function

Blank control register		Function	Output example
BLn1	BLn0		
X	0	Ordinary	R, G, B, I output OUT output
0	1	Border including character	R, G, B, I output OUT output
1	1	Border excluding character	R, G, B, I output OUT output

X : 1 or 0

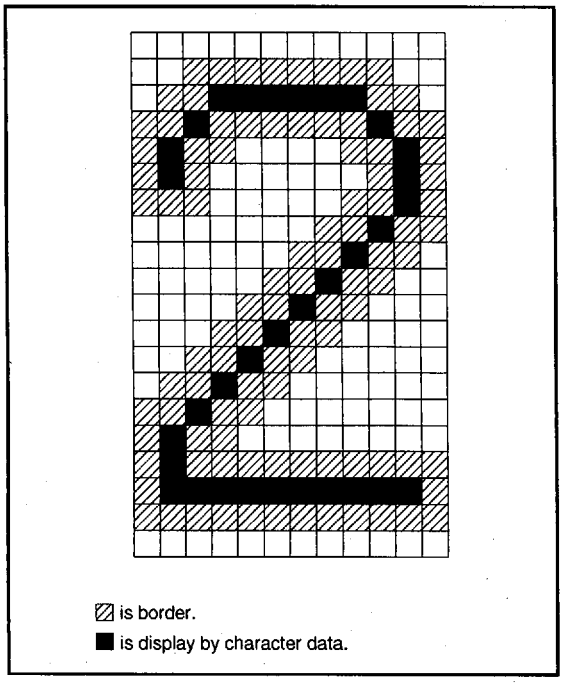


Fig. 41 Border example

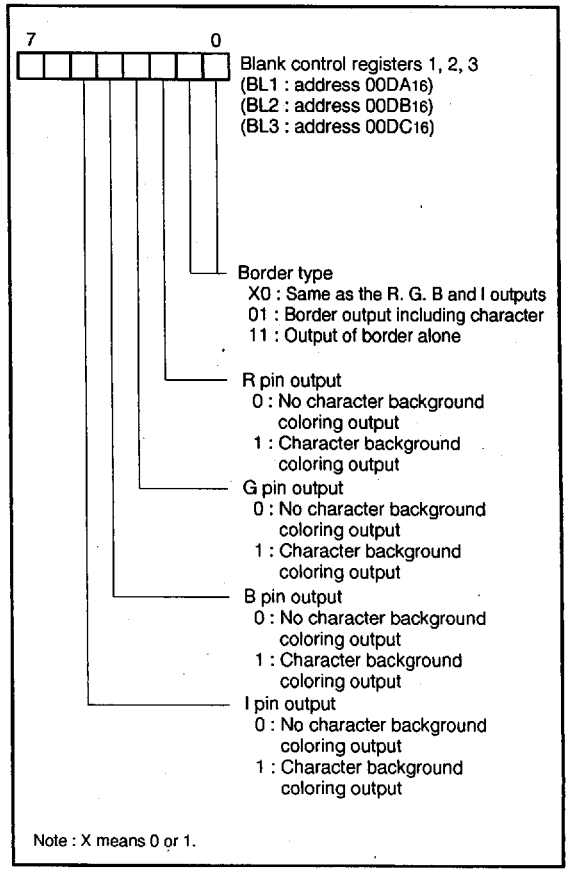
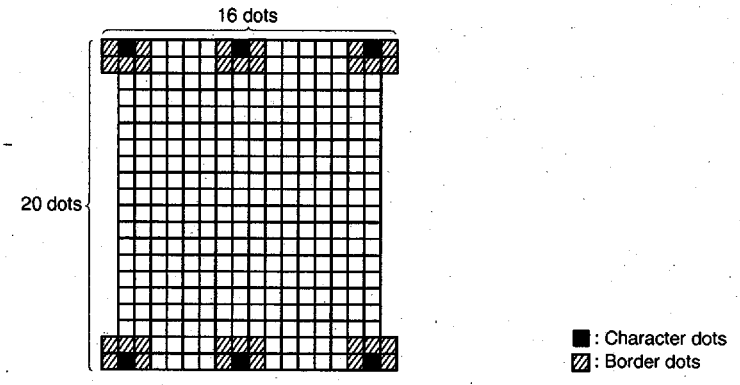


Fig. 42 Structure of blank control registers

(a) When vertical character size is not 1 dot = 1/2 scanning line width, borders avobe the uppermost dots and borders below the lowermost dots of the character font are not displayed.



(b) When vertical character size is 1 dot = 1/2 scanning line width, borders avobe and below the uppermost dots and borders below the lowermost dots of the character font are not displayed.

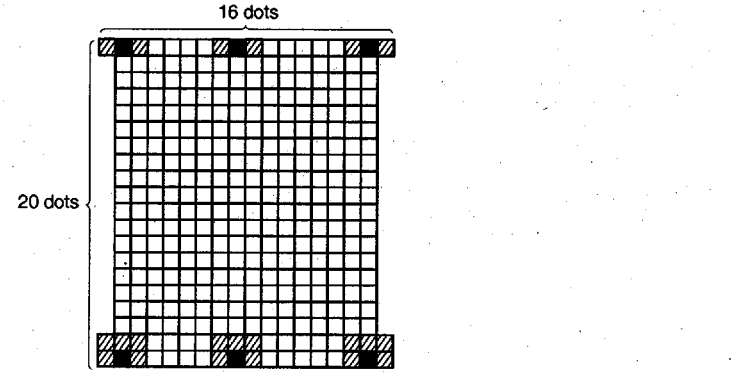


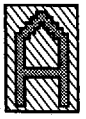
Fig. 43 Notice of border function

Character Background Color Function

character background of the 16 × 20 or 12 × 20 area of character (the blank part), excluding the character part of, or character border part can be colored. The background color can be selected from 16 colors set by bits 2, 3, and 5 of the blank control register. Since a background color can be set for each block, up to 15 background colors can be set for a screen when multi-line display is used.

Six character display types with background colors can be selected by combining bits 4 and 5 of the display memory color code with bits 0 and 1 of the blank control register.

Table 9. Display types

Display memory color code		Blank control register		OUT signal background coloring signal	Example of output signal	Example of character
BL2	BL1	BLn1	BLn0			
X	0	X	0	No OUT signal No background coloring signal	R, G, B, and I for character OUT R, G, B, and I for background	
0	1	X	0	OUT signal same as R,G,B,and I No background coloring signal	R, G, B, and I for character OUT R, G, B, and I for background	
X	X	0	1	Border including character Border coloring signal	R, G, B, and I for character OUT R, G, B, and I for background	
X	X	1	1	Border-only output Border coloring signal	R, G, B, and I for character OUT R, G, B, and I for background	
1	1	1	0	Blank output Background coloring (Note 1)	R, G, B, and I for character OUT R, G, B, and I for background	
1	1	0	0	Blank output Background coloring with border (Note 1, 2)	R, G, B, and I for character OUT R, G, B, and I for background	

Notes 1 : If there are no character R,G,B,and I outputs,the background R,G,B, and I signals become the same as the OUT output.

2 : When the characters (① and ③ in Figure 44) have the dots which are displayed adjoining a character (② in Figure 44) whose display type is the background coloring with border, the border of the adjoined characters (① and ③ in Figure 44) ; bear no relation to the display type ; are displayed in the background area (② in Figure 44).

O : 1 to 3
X : 0 or 1

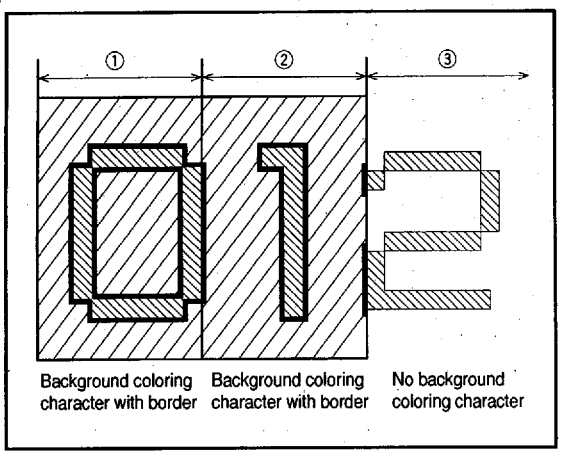


Fig. 44 Notice of character background color function

(10) Mixing Function

Color signals (MXR, MXG, MXB, MXI, and MXOUT) input from outside and color signals (R, G, B, I, and OUT) generated internally can be ORed and output as a mixed signal.

The mixing control register (address 00E516) can be used to turn on and off the mixing of the external and internal color signals, and also to specify which of the two signals has priority when they are combined.

The I pin can be switched to output an overlapped signal indicating the parts of the external color signals (MXR, MXG, MXB, MXI, and MXOUT) and internal color signals (R, G, B, I, and OUT) that are overlapped.

The MXB and MXI pins can also be used as external input pins for timer 2 and timer 3.

Examples of displays generated with an internal color signal for the letter "I" and an external color signal for the letter "O" are shown in Figure 46.

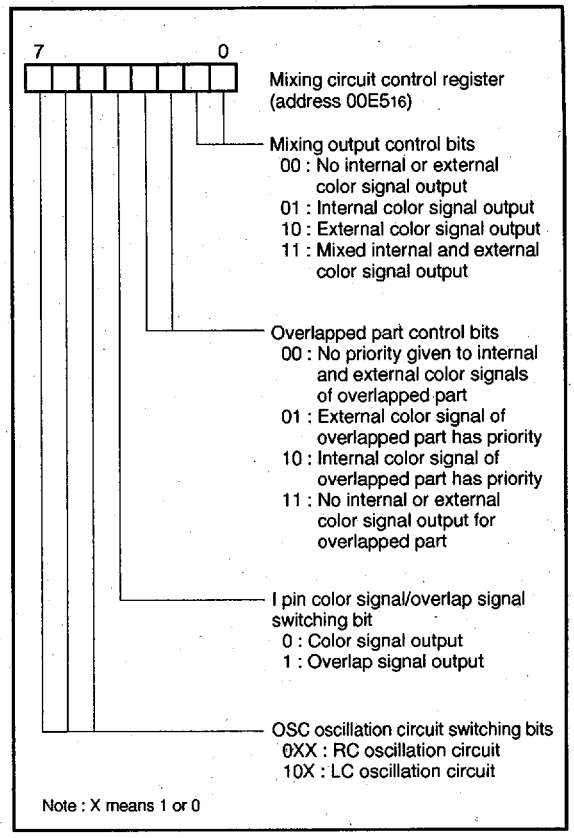


Fig. 45 Structure of mixing control register

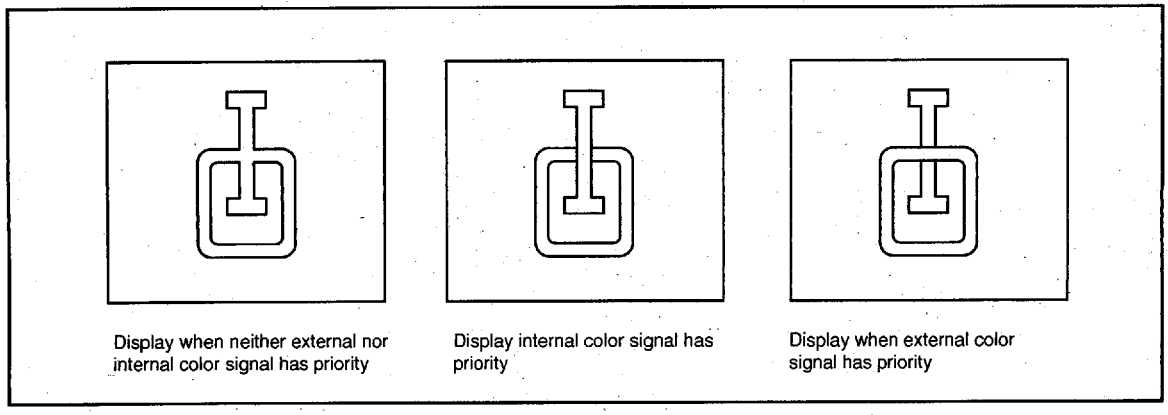


Fig. 46 Examples of display provided by mixing function

(11) CRT Output Pin Control

The CRT output pins R, G, B, I, and OUT and the syncgenerator output pin CSYN can also function as ports P40, P41, P42, P43, P44, and P45. Clear the corresponding bit of the port P4 control register (address 00C916) to "0" to specify these pins as CRT output pins, or set it to "1" to specify it as a general-purpose port P4 pins.

The input active edges of the HSYNC, VSYNC, MXR, MXG, MXB, MXI, and MXOUT signals can be specified with the bits of the CRT input polarity register (address 00E816), and the output active edges of the R, G, B, I, and OUT signals can be specified with the bits of the CRT output polarity register (address 00EC16). Clear a bit to "0" to specify positive active edge ; set it to "1" to specify negative active edge.The structure of the CRT output polarity register is shown in Fig.48 and that of the CRT input polarity register is shown in Fig.49.

(12) Raster Coloring Function

An entire screen (raster) can be colored by setting the upper 5 bits of the CRT output polarity register. Since each of the R, G, B, and I pins can be switched to raster coloring output, 15 raster colors can be obtained.

If the OUT pin has been set to raster coloring output, a raster coloring signal is always output during the horizontal scanning period. This setting is necessary for erasing a background TV image.

If the R, G, B, and I pins have been set to raster coloring output, a raster coloring signal is output during the horizontal scanning period whenever there is no other color character output. This ensures that character colors do not mix with the raster color.

An example in which a magenta letter "I" and a red letter "O" are displayed with blue raster coloring is shown in Fig.47.

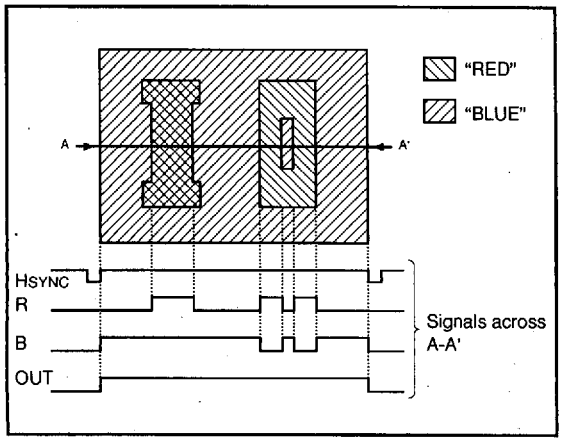


Fig. 47 Example of raster coloring

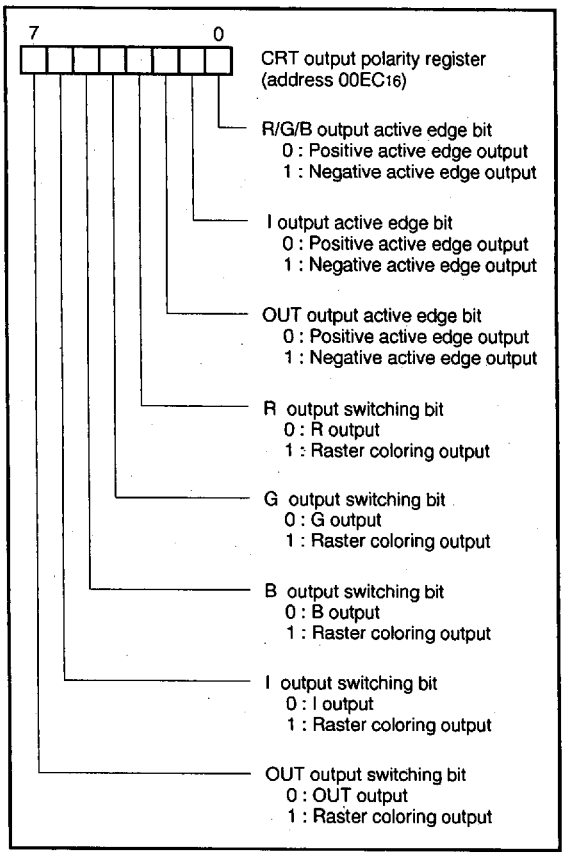


Fig. 48 Structure of CRT output polarity register

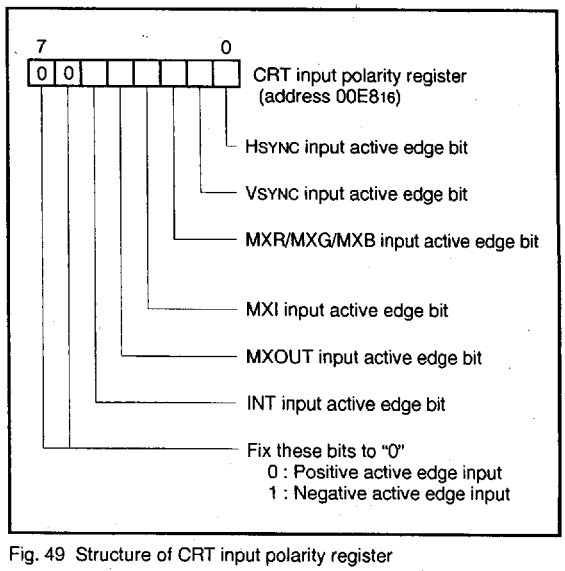


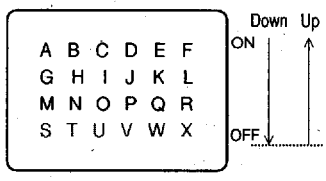
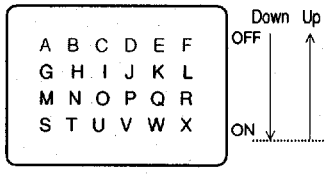
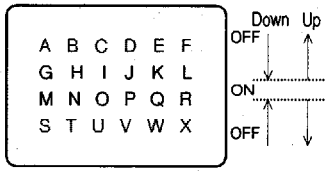
Fig. 49 Structure of CRT input polarity register

(13) Wipe Function

① Wipe mode

The M37260M6-XXXSP allows the display area to be gradually expanded or shrunk in the vertically direction in units of 1H (H : HSYNC signal). There are three modes for this wipe method. Each mode has Down and UP modes, providing a total of six modes.
Table 10 shows the contents of each wipe mode.

Table 10. Wipe operation in each mode and the values of wipe mode register

Mode		Wipe operation		Wipe mode register Bit 2	Bit 1	Bit 0
1	DOWN	Appear from upper side		0	0	1
	UP	Erase from lower side		1	0	1
2	DOWN	Erase from upper side		0	1	0
	UP	Appear from lower side		1	1	0
3	DOWN	Erase from both upper and lower side		0	1	1
	UP	Appear to both upper and lower side		1	1	1

② Wipe speed

The wipe speed is determined by the vertical synchronization (VSYNC) signal. For the NTSC interlace method, assuming that V = 16.7ms 262.5 HSYNC signals per screen

The wipe speed is shown in Table 11.
Wipe resolution varies with each wipe mode. In mode 1 and 2, one of three resolutions (1H, 2H, 4H) can be selected. In mode 3, wipe is done in units of 4H alone.

Table 11. Wipe speed (NTSC method with interlacing, H = 262.5)

Wipe resolution	Wipe speed (in all picture)
1 H unit	16.7 (ms) × 262.5 ÷ 1 ≒ 4 (s)
2 H unit	16.7 (ms) × 262.5 ÷ 2 ≒ 2 (s)
4 H unit	16.7 (ms) × 262.5 ÷ 4 ≒ 1 (s)

Table 12. Wipe mode and wipe resolution

Mode	Wipe resolution	Wipe speed
Mode1	1H Unit	about 4 second
Mode2	2H Unit	about 2 second
	4H Unit	about 1 second
Mode3	4H Unit	about 1 second

Table 13. Relationship between wipe speed and wipe resolution

Wipe resolution	Wipe speed (full screen)		
	NTSC method	PAL method	Bi-scan method (525H/flame)
1H (2H) unit	about 4 second	about 6 second	about 4 second
2H (4H) unit	about 2 second	about 3 second	about 2 second
4H (8H) unit	about 1 second	about 1.5 second	about 1 second

Note : Values in parentheses refer to resolutions for bi-scan method.
To perform a wipe with the bi-scan method, set bit 6 of the CRT control register to "1".

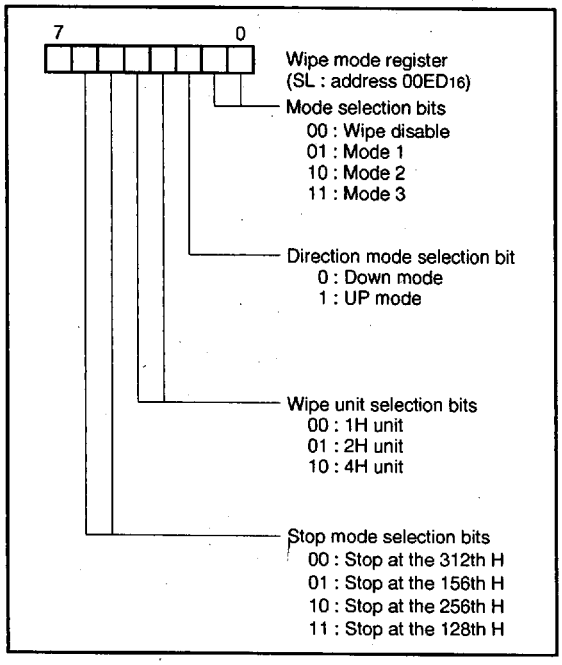


Fig. 50 Structure of wipe mode register

SYNC GENERATOR

The sync generator can output a total of six synchronization signals : NTSC method with interlacing, without interlacing, or bi-scan, and PAL method with interlacing, without interlacing, or bi-scan. Since the synchronization signal is output from the CSYN/P45 pin, set bit 5 of the port P4 mode register to "0".

Activate the sync generator by clearing bit 7 of the sync generator control register to "0" and setting bit 4 to match the XIN clock frequency.

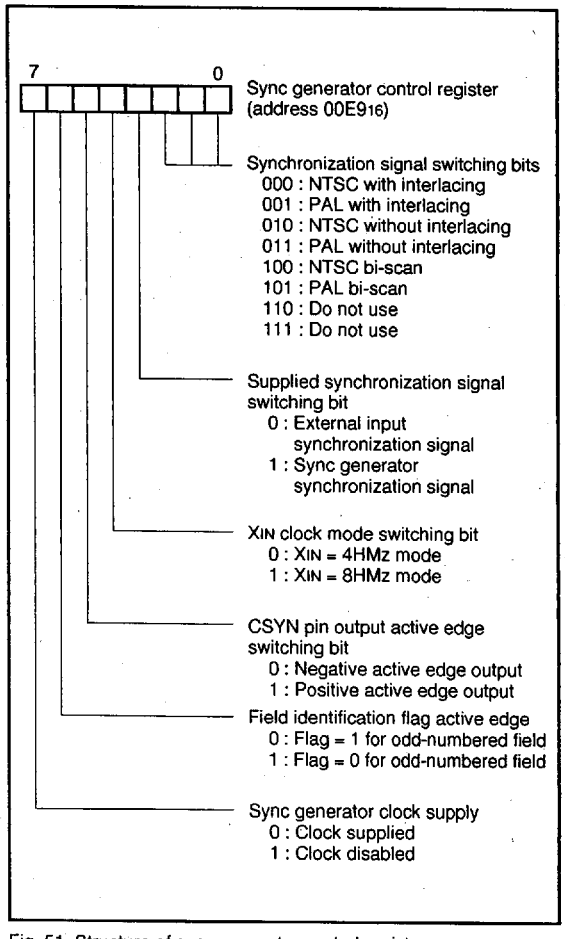


Fig. 51 Structure of sync generator control register

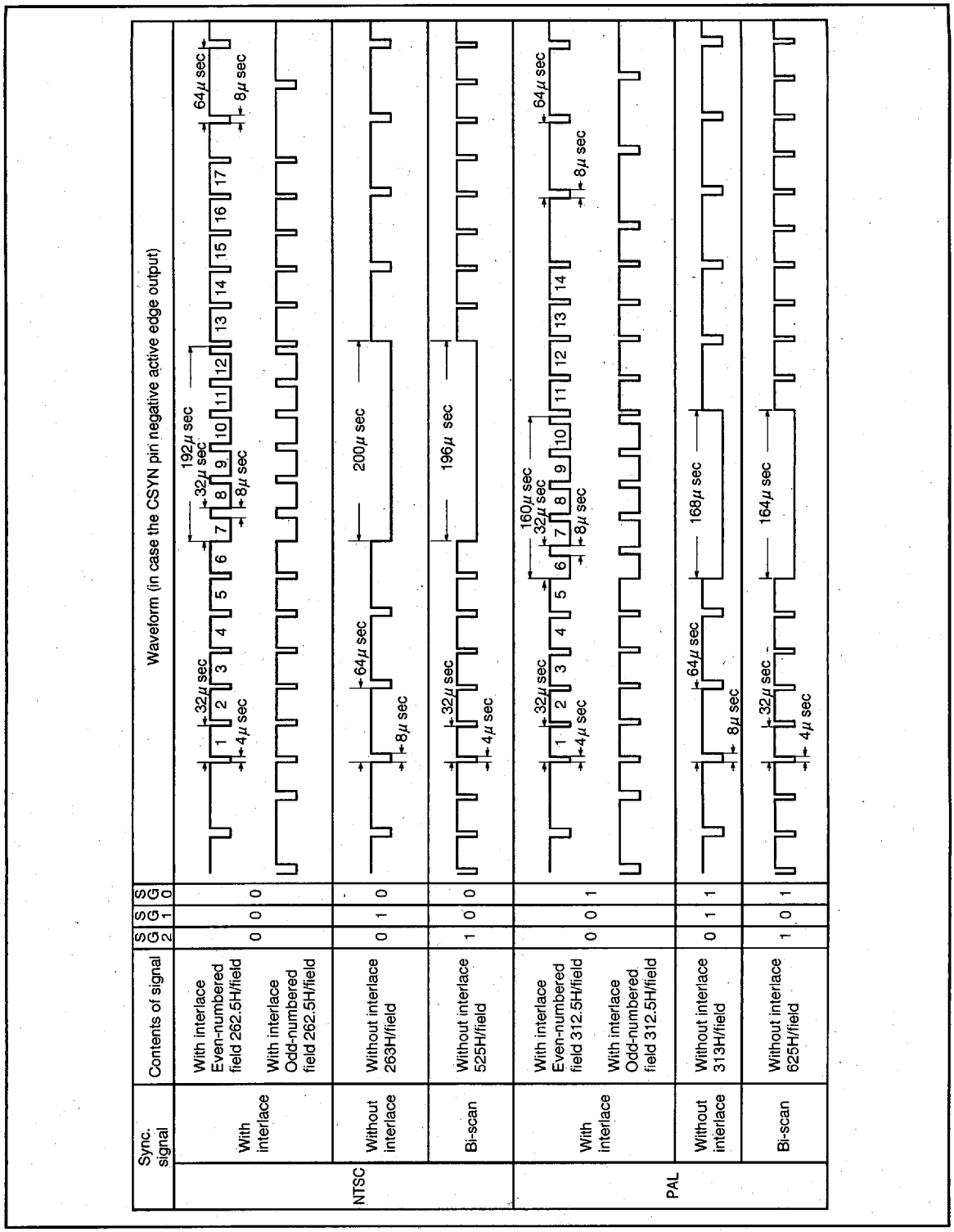
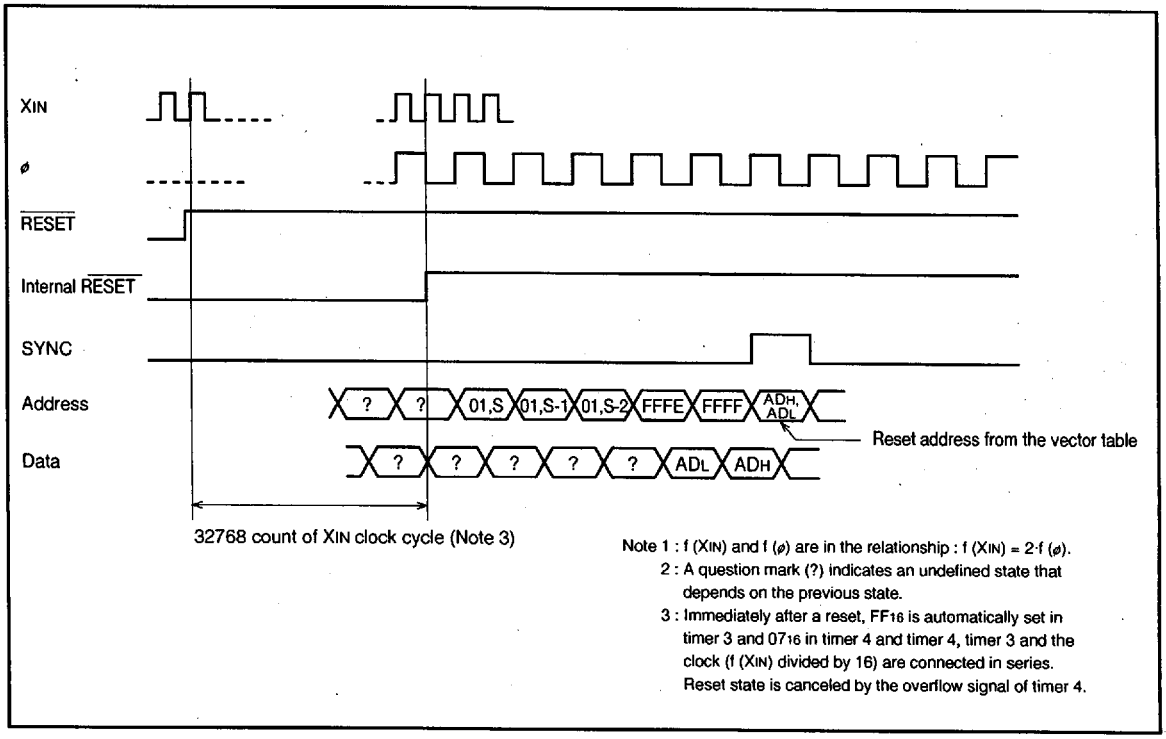


Fig. 52 Relation between the synchronization signals of sync generator and output waveform

RESET CIRCUIT

The M37260M6-XXXSP/FP is reset according to the sequence shown in Figure 53. It starts the program from the address formed by using the content of address FFFF16 as the high order address and the content of the address FFFE16 as the low order address, when the $\overline{\text{RESET}}$ pin is held at "L" level for no less than 2μs while the power voltage is 5V ± 10% and the crystal oscillator oscillation is stable and then returned to "H" level. The internal initializations following reset are shown in Figure 54.

An example of the reset circuit is shown in Figure 55.The reset input voltage must be kept below 0.6V until the supply voltage surpasses 4.5V.



Note 1 : f (XIN) and f (ø) are in the relationship : f (XIN) = 2·f (ø).
2 : A question mark (?) indicates an undefined state that depends on the previous state.
3 : Immediately after a reset, FF16 is automatically set in timer 3 and 0716 in timer 4 and timer 4, timer 3 and the clock (f (XIN) divided by 16) are connected in series. Reset state is canceled by the overflow signal of timer 4.

Fig. 53 Reset sequence

	Address	Contents of register
(1) Port P0 direction register	00C1 16	0016
(2) Port P1 direction register	00C3 16	0016
(3) Port P2 direction register	00C5 16	0016
(4) Port P3 direction register	00C7 16	××0000 0
(5) Port P4 control register	00C9 16	0016
(6) Serial I/O mode register 1	00CD 16	0016
(7) Serial I/O mode register 2	00CE 16	×××0000 0
(8) Character size register 1	00D7 16	×
(9) Character size register 2	00D8 16	×
(10) Character size register 3	00D9 16	×
(11) Blank control register 1	00DA 16	××
(12) Blank control register 2	00DB 16	××
(13) Blank control register 3	00DC 16	××
(14) Block 1 interrupt occurrence position control register	00DD 16	×××
(15) Block 2 interrupt occurrence position control register	00DE 16	×××
(16) Block 3 interrupt occurrence position control register	00DF 16	×××
(17) Horizontal position register	00E0 16	0016
(18) Vertical position register 4	00E4 16	××
(19) Mixing circuit control register	00E5 16	0016
(20) CRT input polarity register	00E8 16	0016
(21) Sync generator control register	00E9 16	0016
(22) CRT control register	00EA 16	0016
(23) Display block counter	00EB 16	×0000000
(24) CRT output polarity register	00EC 16	0016
(25) Wipe mode register	00ED 16	×0000000
(26) Timer 1	00F0 16	FF16
(27) Timer 2	00F1 16	0716
(28) Timer 3	00F2 16	FF16
(29) Timer 4	00F3 16	0716
(30) Timer 12 mode register	00F4 16	×××0000 0
(31) Timer 34 mode register	00F5 16	×××0000 0
(32) Special mode register 1	00F7 16	000××00 0
(33) Special mode register 2	00F8 16	×000000 0
(34) CPU mode register	00FB 16	1100
(35) Interrupt request register 1	00FC 16	××000000
(36) Interrupt request register 2	00FD 16	××××××00
(37) Interrupt control register 1	00FE 16	××000000
(38) Interrupt control register 2	00FF 16	××××××00
(39) Processor status register		1
(40) Program counter	PCH	Contents of address FFFF16
	PCL	Contents of address FFFE16

Note : The blank above, the contents of all other registers and RAM are undefined, so set their initial values.
At reset, "0" is read from the bits marked X.

Fig. 54 Internal state of microcomputer at reset

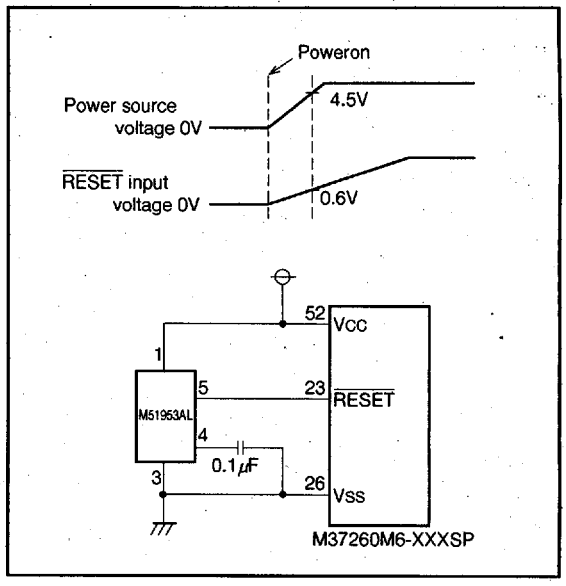


Fig. 55 Example of reset circuit

I/O PORTS

(1) Port P0

Port P0 is an 8-bit I/O port with CMOS output.

As shown in the memory map (Figure 3), port P0 can be accessed at zero page memory address $00C0_{16}$.

Port P0 has a direction register (address $00C1_{16}$) which can be used to program each individual bit as input ("0") or as output ("1"). If the pins are programmed as output, the output data is latched to the port register and then output. When data is read from the output port the output pin level is not read, only the latched data in the port register is read. This allows a previously output value to be read correctly even though the output voltage level is shifted up or down.

Pins set as input are in the floating state and the signal levels can thus be read. When data is written into the input port, the data is latched only to the port latch and the pin still remains in the floating state.

(2) Port P1

Port P1 has the same function as port P0.

(3) Port P2

Port P2 has the same function as port P0.

(4) Port P3

Port P3 is a 6-bit I/O port with function similar to port P0, but the output structure of $P3_0$, $P3_1$ is CMOS output, and $P3_2$-$P3_5$ is N-channel open drain.

$P3_2$ is in common with the external input pin INT and the serial I/O input pin $\overline{CS}$.

When a serial I/O function is selected, $P3_3$ to $P3_5$ work as $\overline{SRDY}$, SIN/SOUT, and SCLK pins.

When a special serial I/O function is selected, $P3_4$ and $P3_5$ work as SDA and SCL pins.

(5) OSC1, OSC2 pins

Clock input/output pins for CRT display function.

(6) HSYNC, VSYNC pins

HSYNC is a horizontal synchronizing signal input pin for CRT display.

VSYNC is a vertical synchronizing signal input pin for CRT display.

(7) R, G, B, I, OUT pins

This is a 5-bit output pin for CRT display and in common with $P4_0$–$P4_4$.

(8) CSYN pin

CSYN pin outputs the composite sync signal by the sync generator.

CSYN pin is in common with $P4_5$.

(9) MXR, MXG, MXB, MXI, MXOUT pins

These are video signal input pins for mixing function.

MXR, MXG, MXB, MXI, and MXOUT are in common with the input port $P5_2$, $P5_3$, $P5_4$, $P5_5$, $P5_6$. MXB and MXI are also in common with the external clock input pins TIM2 and TIM3.

(10) ϕ pin

The internal system clock (1/2 the frequency of the oscillator connected between the XIN and XOUT pins) is output from this pin. If an STP or WIT instruction is executed, output stops after going "H".

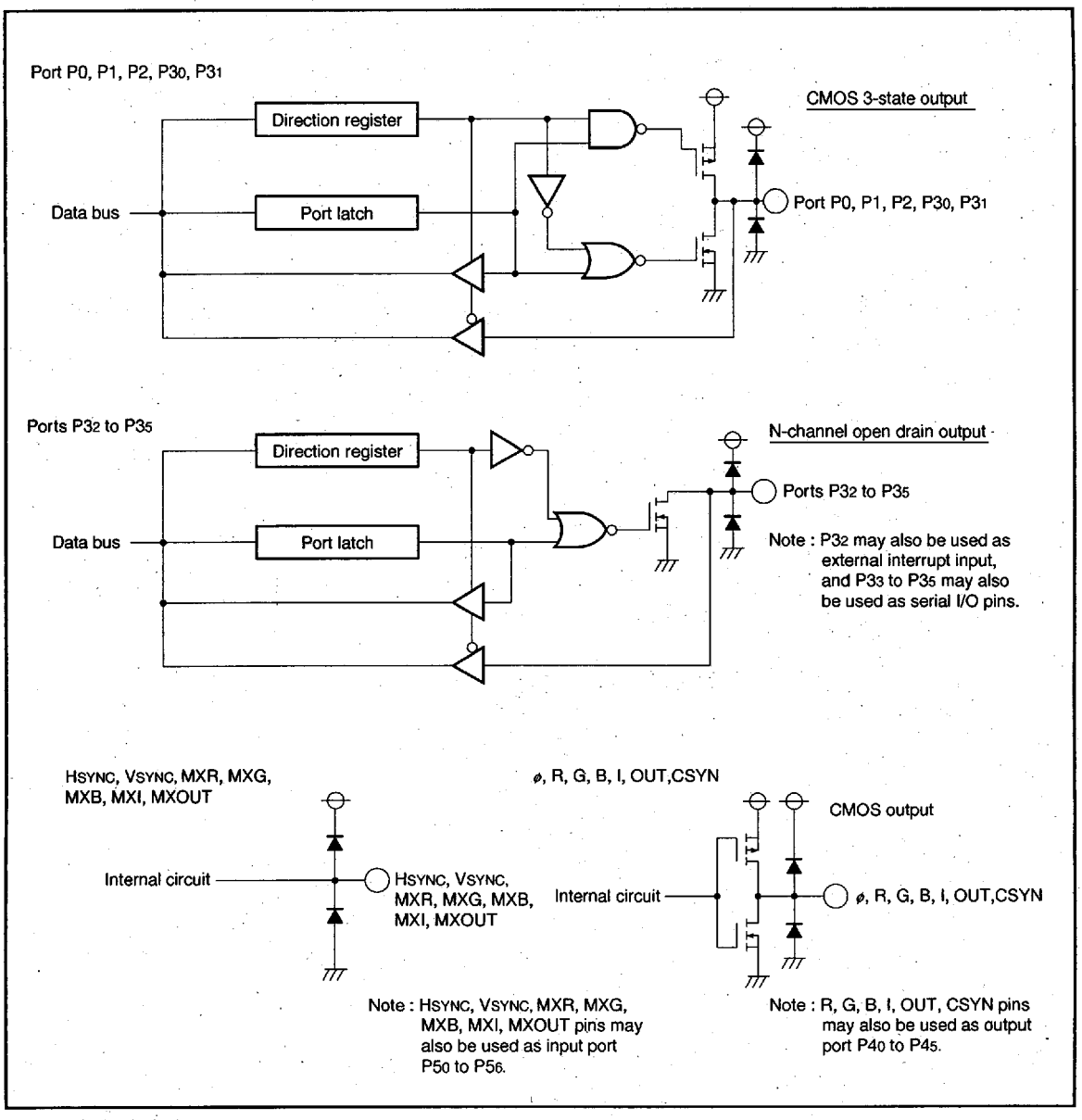


Fig. 56 I/O pin block diagram

Data-set timing of CPU mode register

The value of bit 0 and bit 1 in the CPU mode register is set at the second rising edge of the SYNC signal after the writing instruction is executed.
However the value of bit 2 and bit 3 is set at the first rising edge of the SYNC signal, just as in the other registers.

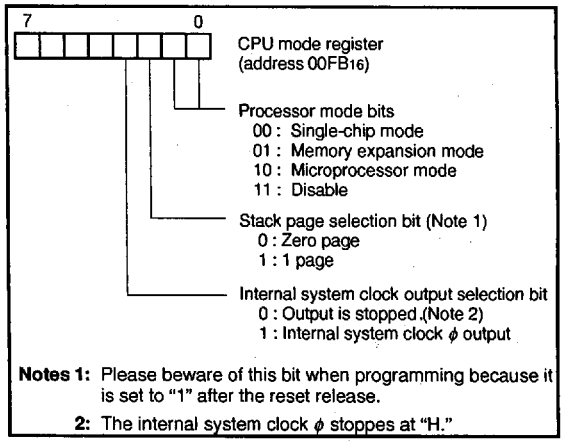


Fig. 57 Structure of CPU mode register

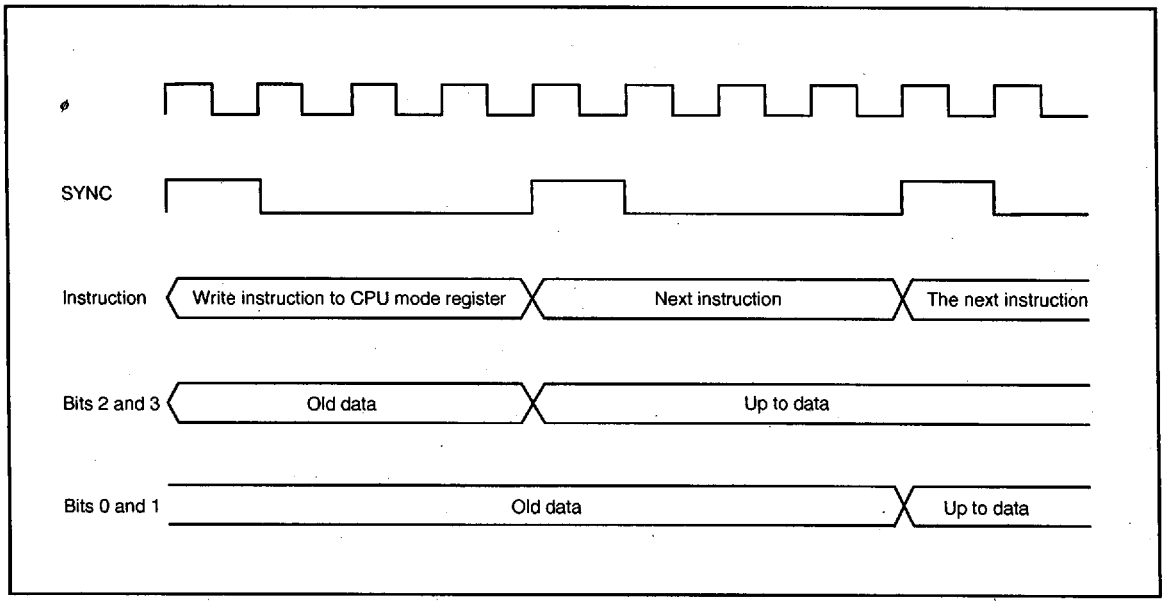


Fig. 58 Data-set timing of CPU mode register

Table 14. The value of CPU mode register at reset

CNVss pin	b7				CPU mode register			b0
Vss					1	1	0	0
Vcc					1	1	1	0

Note: High-order 4 bits are undefined.

CLOCK GENERATING CIRCUIT

The built-in clock generating circuit is shown in Figure 61.

When the STP instruction is executed, the internal clock ϕ stops oscillating at "H" level. At the same time, timers 3 and 4 are connected in hardware and "FF16" is set in the timer 3, "0716" is set in the timer 4. Select f(XIN)/16 as the timer 3 count source (set both bit 0 of the timer 34 mode register to "0" before the execution of the STP instruction). And besides, set the timer 3 and timer 4 interrupt enable bits to disabled ("0") before execution of the STP instruction.

The oscillator is restarted when an external interrupt is accepted. However, the internal clock ϕ keeps its "H" level until timer 4 overflows.

This is because the oscillator needs a set-up period if a ceramic resonator or a quartz-crystal oscillator is used.

When the WIT instruction is executed, the internal clock ϕ stops in the "H" level but the oscillator continues running.

This wait state is cleared when an interrupt is accepted (Note).

Since the oscillation does not stop, the next instructions are executed at once.

To return from the stop or the wait state, set the interrupt enable bit to "1" before executing the STP or the WIT instruction.

Note: In the wait mode, the following interrupts are invalid.

(1) VSYNC interrupt
(2) CRT interrupt
(3) Timer 2 interrupt using P54/MXB/TIM2 pin input as count source
(4) Timer 3 interrupt using P55/MXI/TIM3 pin input as count source
(5) 1ms interrupt
(6) Timer 4 interrupt using f(XIN)/2 as count source

The circuit example using a ceramic resonator (or a quartz-crystal oscillator) is shown in Figure 59.

Use the circuit constants in accordance with the resonator manufacturer's recommended values.

The example of external clock usage is shown in Figure 60 XIN is the input, and XOUT is open.

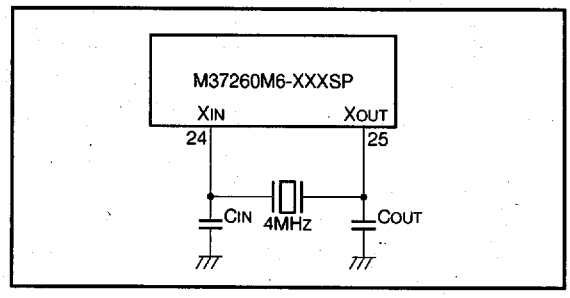


Fig. 59 Ceramic resonator circuit example

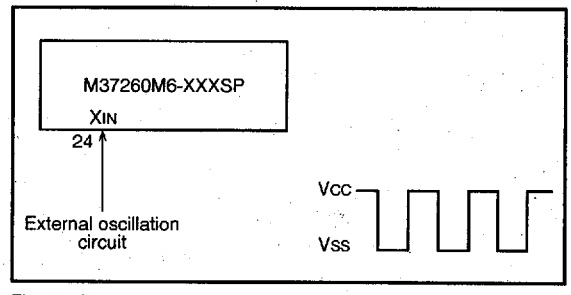


Fig. 60 External clock input circuit example

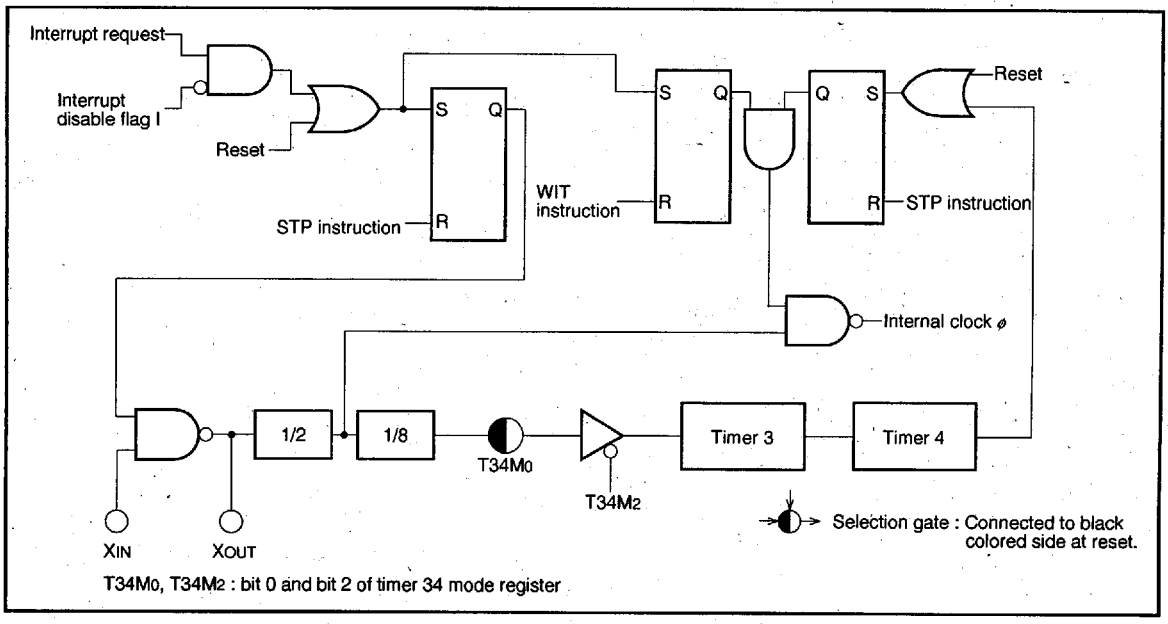


Fig. 61 Clock generating circuit block diagram

DISPLAY OSCILLATION CIRCUIT

The CRT display clock oscillation circuit has built-in RC and LC oscillation circuits, so that a clock can be obtained simply by connecting an RC or LC circuit between the OSC1 and OSC2 pins.
Select the RC or LC oscillation circuit by setting bits 6 and 7 of the mixing control register (see the structure of the mixing control register in Figure 45).

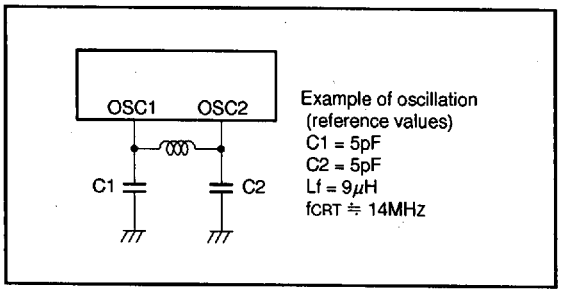
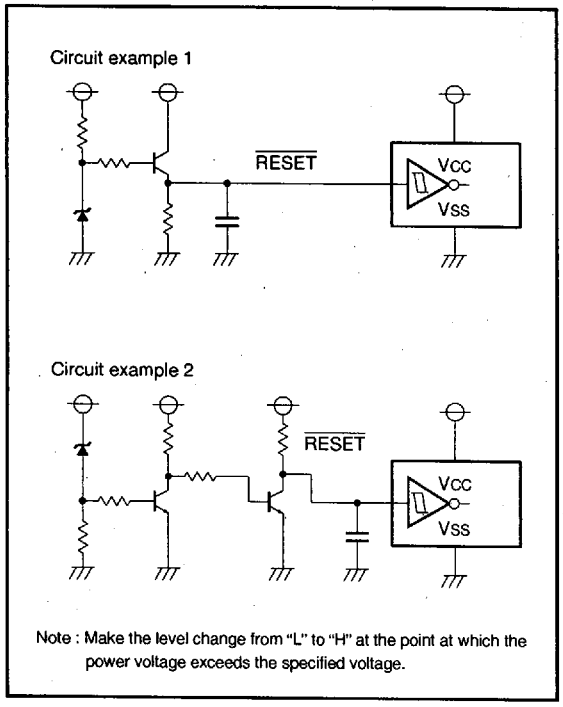


Fig. 62 Display oscillation circuit

AUTO CLAER CIRCUIT

When power is supplied, the auto-clear function can be performed by connecting the following circuit to reset pin.



Note : Make the level change from "L" to "H" at the point at which the power voltage exceeds the specified voltage.

Fig. 63 Auto clear circuit example

PROGRAMMING NOTES

(1) The divide ratio of the timer is 1/ (n+1).
(2) Even though the BBC and BBS instructions are executed immediately after the interrupt request bits are modified (by the program), those instructions are only valid for the contents before the modification. At least one instruction cycle is needed (such as an NOP) between the modification of the interrupt request bits and the execution of the BBC and BBS instructions.
(3) After the ADC and SBC instructions are executed (indecimal mode), one instruction cycle (such as an NOP) is needed before the SEC, CLC, or CLD instructions are executed.
(4) An NOP instruction is needed immediately after the execution of a PLP instruction.
(5) In order to avoid noise and latch-up, connect a bypass capacitor (≈ 0.1μF) directly between the Vcc pin and Vss pin using a thick wire.

DATA REQUIRED FOR MASK ORDERS

The following are necessary when ordering a mask ROM production:

(1) Mask ROM Order Confirmation Form
(2) Mark Specification Form
(3) Data to be written to ROM, in EPROM form(28-pin DIP type 27512, three identical copies)

PROM Programming Method

The built-in PROM of the blank One Time PROM version and built-in EPROM version can be read or programmed with a general-purpose PROM programmer using a special programming adapter.

Product	Name of Programming Adapter
M37260M6-XXXSP	PCA4736
M37260M6-XXXFP	PCA4737

The PROM of the blank One Time PROM version is not tested or screened in the assembly process and following processes. To ensure proper operation after programming, the procedure shown in Figure 64 is recommended to verify programming.

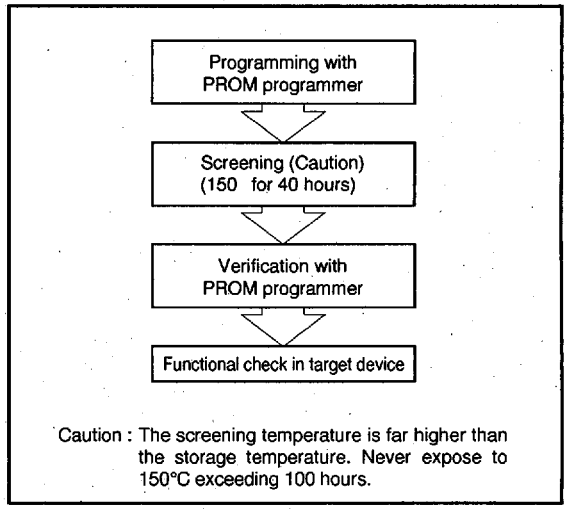


Fig. 64 Programming and testing of One Time PROM version

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Power source voltage	All voltages are based on V_{SS}. Output transistors are cut off.	– 0.3 to 6	V
V_I	Input voltage CNVss		– 0.3 to 6	V
V_I	Input voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_5$, MXR, MXG, MXB, MXI, MXOUT, HSYNC, VSYNC, $\overline{RESET}$		– 0.3 to V_{CC} + 0.3	V
V_O	Output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_5$, R, G, B, I, OUT, CSYN, X_{OUT}, OSC2		– 0.3 to V_{CC} + 0.3	V
I_{OH}	Circuit current R, G, B, I, OUT, CSYN, $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$, P31		0 to 1 (Note 1)	mA
I_{OL1}	Circuit current R, G, B, I, OUT, CSYN, $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_5$		0 to 2 (Note 2)	mA
Pd	Power dissipation	Ta = 25°C	550	mW
Topr	Operating temperature		– 10 to 70	°C
Tstg	Storage temperature		– 40 to 125	°C

RECOMMENDED OPERATING CONDITIONS (Ta = –10 to 70°C, V_{CC} = 5V ± 10% unless otherwise noted)

Symbol	Parameter	Limits			Unit
		Min.	Typ.	Max.	
V_{CC}	Power source voltage (Note 3) During the CPU and CRT operation	4.5	5.0	5.5	V
V_{SS}	Power source voltage	0	0	0	V
V_{IH}	"H" input voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, HSYNC, VSYNC, MXR, MXG, MXB, MXI, MXOUT, $\overline{RESET}$, X_{IN}, OSC1	0.8V_{CC}		V_{CC}	V
V_{IH}	"H" input voltage $P3_4$, $P3_5$	0.7V_{CC}		V_{CC}	V
V_{IL1}	"L" input voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$, $P3_1$, $P3_3$, MXR, MXG, MXOUT	0		0.4V_{CC}	V
V_{IL2}	"L" input voltage $P3_2$, $P3_4$, $P3_5$, HSYNC, VSYNC, $\overline{RESET}$, X_{IN}, OSC1, MXB, MXI	0		0.2V_{CC}	V
I_{OH}	"H" average output current (Note 1) R, G, B, I, OUT, CSYN, $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$, $P3_1$			1	mA
I_{OL}	"L" average output current (Note 2) R, G, B, I, OUT, CSYN, $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_5$			2	mA
f_{CPU}	Oscillation frequency (for CPU operation) (Note 4)	3.6	4.0	8.1	MHz
f_{CRT}	Oscillation frequency (for CRT display)	12.0	14.0	16.0	MHz
fhs	Input frequency INT, TIM2, TIM3, SCL			100	kHz
fhs	Input frequency SCLK			1	MHz

Notes 1: The total current that flows out of the IC should be 20mA (max.).
2: The total current shold be 30mA (max.).
3: Connect 0.022μF or more capacitor externally between the V_{CC} – V_{SS} power source pins so as to reduce power source noise.
Also connect 0.068μF or more capacitor externally between the V_{CC} – CNVss pins.
4: Use a quartz-crystal oscillator or a ceramic resonator for the CPU oscillation circuit.

ELECTRIC CHARACTERISTICS (V_{CC} = 5V ± 10%, V_{SS} = 0V, f (X_{IN}) = 4MHz, Ta = −10 to 70°C unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min.	Typ.	Max.	
I_{CC}	Power source current	V_{CC} = 5.5V, f (X_{IN}) = 4MHz CRT OFF		10	20	mA
		V_{CC} = 5.5V, f (X_{IN}) = 4MHz CRT ON		20	50	
		At stop mode			300	μA
V_{OH}	"H" output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$, $P3_1$, R, G, B, I, OUT, CSYN	V_{CC} = 4.5V I_{OH} = −0.5mA	2.4			V
V_{OL}	"L" output voltage $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_3$, R, G, B, I, OUT, CSYN	V_{CC} = 4.5V I_{OL} = 0.5mA			0.4	V
	"L" output voltage $P3_4$, $P3_5$	V_{CC} = 4.5V I_{OL} = 3mA			0.4	
V_{T+}–V_{T-}	Hysteresis $\overline{RESET}$	V_{CC} = 5.0V		0.5	0.7	V
	Hysteresis (Note) H_{SYNC}, V_{SYNC}, $P3_2$, $P3_4$, $P3_5$, MXB, MXI	V_{CC} = 5.0V		0.5	1.3	
I_{OZH}	"H" input leak current $\overline{RESET}$, $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_5$, H_{SYNC}, V_{SYNC}, MXR, MXG, MXB, MXI, MXOUT	V_{CC} = 5.5V V_O = 5.5V			5	μA
I_{OZL}	"L" input leak current $\overline{RESET}$, $P0_0$ – $P0_7$, $P1_0$ – $P1_7$, $P2_0$ – $P2_7$, $P3_0$ – $P3_5$, H_{SYNC}, V_{SYNC}, MXR, MXG, MXB, MXI, MXOUT	V_{CC} = 5.5V V_O = 0V			5	μA

Note : $P3_2$, MXB, MXI have the hysteresis when these pins are used as interrupt input pins or timer input pins.
$P3_4$, $P3_5$ have the hysteresis when these pins are used as serial I/O and special serial I/O ports.

Note 28. Self refresh sequence
Two refreshing ways should be used properly depending on the low pulse width (t_{RASS}) of $\overline{RAS}$ signal during self refresh period.

1. In case of $t_{RASS} < 300ms$
1.1 Distriduted refresh during Read/Write operation
(A) Timing Diagrams

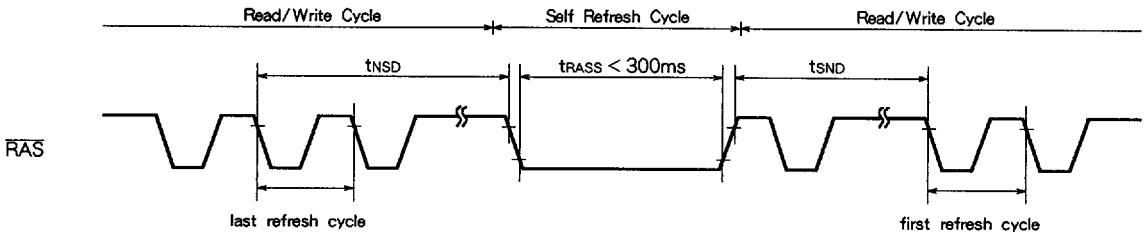


Table 2

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR distributed refresh	$t_{NSD} + t_{SND} \leqq 16.4ms$	
$\overline{RAS}$ only distributed refresh	$t_{NSD} \leqq 16\ \mu s$	$t_{SND} \leqq 16\ \mu s$

(B) Definition of refresh

Definition of CBR distributed refresh

The CBR distributed refresh performs more then 1024 discrete CBR cycles within 16.4 ms.

Definition of $\overline{RAS}$ only distributed refresh

All combination of ten row address signals (A_0~A_9) are selected during 1024 discrete $\overline{RAS}$ only refresh cycles within 16.4 ms.

1.1.1 CBR distributed Refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSD} (shown in table 2).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within t_{SND} (shown in table 2).

1.1.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSD} from the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16 μs.
- Switching from self refresh operation to read/write operation. The time interval t_{SND} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period should be set within 16 μs.

1.2 Burst refresh during Read/Write operation

(A) Timing diagram

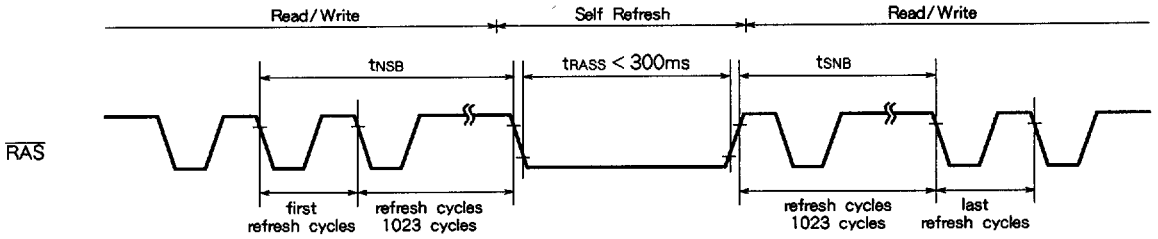


Table 3

Read/Write Cycle	Read/Write→ Self Refresh	Self Refresh→ Read/Write
CBR burst refresh	$t_{NSB} \leqq 16.4ms$	$t_{SNB} \leqq 16.4ms$
$\overline{RAS}$ only burst refresh	$t_{NSB} + t_{SNB} \leqq 16.4ms$	

(B) Definition of burst refresh

Definition of CBR burst refresh

The CBR burst refresh performs more then 1024 continuous CBR cycles within 16.4ms.

Definition of $\overline{RAS}$ only burst refresh

All combination of ten row address signals (A_0~A_9) are selected during 1024 continuous $\overline{RAS}$ only refresh cycles within 16.4 ms.

1.2.1 CBR distributed Refresh

- Switching from read/write operation to self refresh operation. The time interval t_{NSB} from the falling edge of $\overline{RAS}$ signal in the first CBR refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within 16.4 ms.
- Switching from self refresh operation to read/write operation. The time interval t_{SNB} from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last CBR refresh cycle during read /write operation period should be set within 16.4 ms.

1.2.2 $\overline{RAS}$ only distributed refresh

- Switching from read/write operation to self refresh operation. The time interval from the falling edge of $\overline{RAS}$ signal in the first $\overline{RAS}$ only refresh cycle during read/write operation period to the falling edge of $\overline{RAS}$ signal at the start of self refresh operation should be set within t_{NSB} (shown in table 3).
- Switching from self refresh operation to read/write operation. The time interval from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation to the falling edge of $\overline{RAS}$ signal in the last $\overline{RAS}$ only refresh cycle during read/ write operation period should be set within t_{SNB} (shown in table 3).

2. In case of $t_{RASS} \geqq 300ms$
(A) Timing diagram

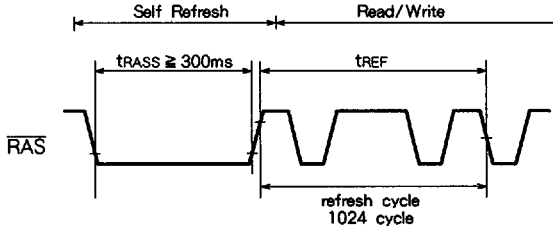


Table 4

Read/Write	Self Refresh→Read/Wirte
CBR distributed refresh $\overline{RAS}$ only distributed refresh CBR burst refresh $\overline{RAS}$ only burst refresh	$t_{REF} \leqq 16.4ms$

(B) Definition of refresh
The same as 1.1-(B) and 1.2-(B)

2.1
Regardless of the refresh (CBR distributed refresh, $\overline{RAS}$ only distributed refresh, CBR burst refresh, $\overline{RAS}$ only burst refresh) during Read/Write operation the minimum of 1024 cycles refresh should be preformed within 16.4 ms from the rising edge of $\overline{RAS}$ signal at the end of self refresh operation.