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ECL Products	

10130
Latch

Dual D-Type Latch

FEATURES

- **Typical propagation delay: 2.5ns**
- **Typical supply current ($-I_{EE}$): 30mA**

DESCRIPTION

The 10130 is a clocked Dual D-Type Latch. Each element can be clocked separately by holding the common clock in the Low-State and using the clock enable inputs for the clocking function. The outputs are latched when the level of the clock is High. All unused inputs must be tied to V_{IL} or V_{EE}.

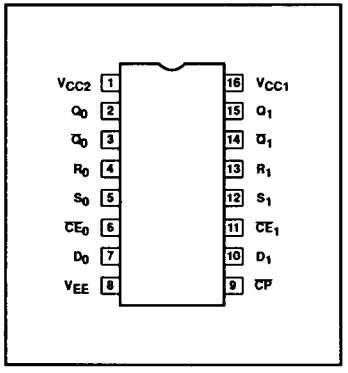
ORDERING INFORMATION

DESCRIPTION	ORDER CODE
16–Pin Plastic DIP	10130N
16–Pin Ceramic DIP	10130F

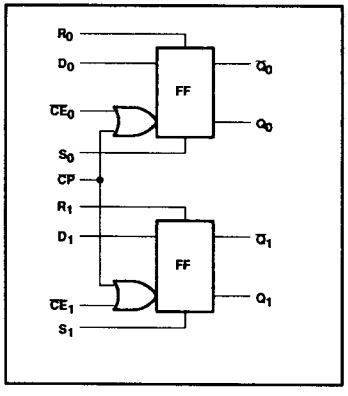
PIN DESCRIPTION

PINS	DESCRIPTION
D_0, D_1	Data Inputs
$\overline{CP}$	Clock Input
$\overline{CE}_0$, $\overline{CE}_1$	Clock Enable Inputs
S_0, S_1	Set Inputs
R_0, R_1	Reset Inputs
Q_0, Q_1, $\overline{Q}_0$, $\overline{Q}_1$	Data Outputs

PIN CONFIGURATION



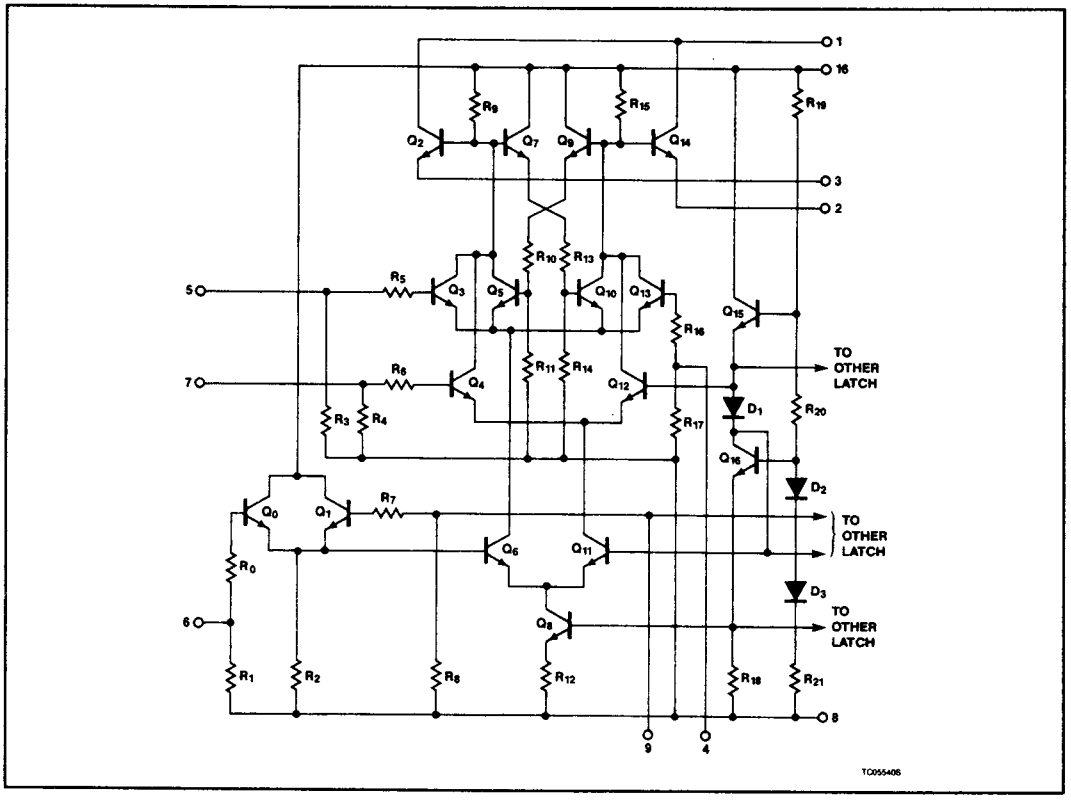
LOGIC DIAGRAM



Latch

10130

SIMPLIFIED SCHEMATIC



FUNCTION TABLES

SYNCHRONOUS OPERATION

INPUTS			OUTPUTS
D_n	$\overline{CP}$	$\overline{C}_E$	Q_{n+1}*
L	L	L	L
L	L	H	Q_n
L	H	L	Q_n
L	H	H	Q_n
H	L	L	H
H	L	H	Q_n
H	H	L	Q_n
H	H	H	Q_n

* R and S = Low

ASYNCHRONOUS OPERATION

INPUTS		OUTPUTS
R	S	Q_1
L	L	Q
L	H	H
H	L	L
H	H	N

$\overline{CP}$ or $\overline{C}_E$ = High
H = High voltage level
L = Low voltage level
N = Not allowed

ABSOLUTE MAXIMUM RATINGS

SYMBOL	PARAMETER		LIMITS	UNIT
V_{EE}	Supply voltage		–8.0 to 0	V
V_{IN}	Input voltage (V_{IN} should never be more negative than V_{EE})		0 to V_{EE}	V
I_O	Output source current (continuous)		–50	mA
T_S	Storage temperature range		–55 to +150	°C
T_J	Maximum junction temperature	Ceramic Package	+165	°C
		Plastic Package	+150	°C

NOTE:
Operation beyond the limits set forth in this table may impair the useful life of the device. Unless otherwise noted, these limits are specified over the operating ambient temperature range.

DC OPERATING CONDITIONS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			MIN.	NOM.	MAX.	
V_{CC1}, V_{CC2}	Circuit ground		0	0	0	V
V_{EE}	Supply voltage (negative)			–5.2		V
V_{IH}	High level input voltage	T_A = –30°C			–890	mV
		T_A = +25°C			–810	mV
		T_A = +85°C			–700	mV
V_{IHT}	High level input threshold voltage	T_A = –30°C	–1205			mV
		T_A = +25°C	–1105			mV
		T_A = +85°C	–1035			mV
V_{ILT}	Low level input threshold voltage	T_A = –30°C			–1500	mV
		T_A = +25°C			–1475	mV
		T_A = +85°C			–1440	mV
V_{IL}	Low level input voltage	T_A = –30°C	–1890			mV
		T_A = +25°C	–1850			mV
		T_A = +85°C	–1825			mV
T_A	Operating ambient temperature range		–30	+25	+85	°C

NOTE:
When operating at other than the specified V_{EE} voltage (–5.2V), the DC and AC Electrical Characteristics will vary slightly from specified values.

DC ELECTRICAL CHARACTERISTICS

$V_{CC1} = V_{CC2}$ = ground, $V_{EE} = -5.2V \pm 0.010V$, $T_A = -30°C$ to $+85°C$ output loading 50Ω to $-2.0V \pm 0.010V$ unless otherwise specified[1,3]

SYMBOL	PARAMETER		TEST CONDITIONS[2]		LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
V_{OH}	High level output voltage		$T_A = -30°C$	For Q_n output, apply V_{IHMAX} to each D_n input, one at	-1060		-890	mV
			$T_A = +25°C$	a time, with V_{ILMIN} applied to all other inputs.	-960		-810	mV
			$T_A = +85°C$	For $\overline{Q}_n$ output, apply V_{ILMIN} to all inputs.	-890		-700	mV
V_{OHT}	High level output threshold voltage		$T_A = -30°C$	For Q_n output, apply V_{IHT} to each D_n input, one at a	-1080			mV
			$T_A = +25°C$	time with V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ output, apply V_{ILT} to each D_n input, one at a time,	-980			mV
			$T_A = +85°C$	with V_{ILMIN} applied to all other inputs.	-910			mV
V_{OLT}	Low level output threshold voltage		$T_A = -30°C$	For Q_n output, apply V_{ILT} to each D_n input, one at a			-1655	mV
			$T_A = +25°C$	time with V_{ILMIN} applied to all other inputs. For $\overline{Q}_n$ output, apply V_{IHT} to each D_n input, one at a time,			-1630	mV
			$T_A = +85°C$	with V_{ILMIN} applied to all other inputs.			-1595	mV
V_{OL}	Low level output voltage		$T_A = -30°C$	For Q_n output, apply V_{ILMIN} to all inputs. For $\overline{Q}_n$	-1890		-1675	mV
			$T_A = +25°C$	output, apply V_{IHMAX} to each D_n input, one at a time,	-1850		-1650	mV
			$T_A = +85°C$	with V_{ILMIN} applied to all other inputs.	-1825		-1615	mV
I_{IH}	High level input current	$\overline{CE}_0$, $\overline{CE}_1$ inputs	$T_A = -30°C$	Apply V_{IHMAX} to each input under			360	µA
			$T_A = +25°C$	test, one at a time, with V_{ILMIN}			220	µA
			$T_A = +85°C$	applied to all other inputs.			220	µA
		$\overline{CP}$ input	$T_A = -30°C$	Apply V_{IHMAX} to $\overline{CP}$ input			425	µA
			$T_A = +25°C$	with V_{ILMIN} applied			265	µA
			$T_A = +85°C$	to all other inputs.			265	µA
		D_n inputs	$T_A = -30°C$	Apply V_{IHMAX} to each D_n input under			455	µA
			$T_A = +25°C$	test, one at a time with V_{ILMIN}			285	µA
			$T_A = +85°C$	applied to all other inputs.			285	µA
		R_n inputs	$T_A = -30°C$	Apply V_{IHMAX} to S_n and CP inputs and R_n			455	µA
			$T_A = +25°C$	input under test, one at a time with V_{ILMIN}			285	µA
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.			285	µA
		S_n inputs	$T_A = -30°C$	Apply V_{IHMAX} to R_n and CP inputs and S_n			455	µA
			$T_A = +25°C$	input under test, one at a time with V_{ILMIN}			285	µA
			$T_A = +85°C$	V_{ILMIN} applied to all other inputs.			285	µA
I_{IL}	Low level input current		$T_A = -30°C$	Apply V_{ILMIN} to each input under	0.5			µA
			$T_A = +25°C$	test, one at a time, with V_{IHMAX}	0.5			µA
			$T_A = +85°C$	applied to all other inputs.	0.3			µA
$-I_{EE}$	V_{EE} supply current		$T_A = -30°C$				38	mA
			$T_A = +25°C$			30	35	mA
			$T_A = +85°C$				38	mA

DC ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	TEST CONDITIONS[2]	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT
$\frac{\Delta V_{OH}}{\Delta V_{EE}}$	High level output voltage compensation	T_A = +25°C		0.016		V/V
$\frac{\Delta V_{OL}}{\Delta V_{EE}}$	Low level output voltage compensation			0.230		V/V
$\frac{\Delta V_{BB}}{\Delta V_{EE}}$	Reference bias voltage compensation			0.140		V/V

NOTES:
1. The specified limits represent the worst case values for the parameter. Since these worst case values normally occur at the supply voltage and temperature extremes, additional noise immunity can be achieved by decreasing the allowable operating condition ranges.
2. Conditions for testing shown in the tables are not necessarily worst case. For worst case testing guidelines, refer to DC Testing, Chapter 1, Section 3.
3. The specified limits shown in the DC Electrical Characteristics table can be met only after thermal equilibrium has been established. Thermal equilibrium is established by applying power for at least 2 minutes, while maintaining transverse airflow of 2.5 meters/sec (500 linear feet/min) over the device, mounted either in a test socket or on a printed circuit board. Test voltage values are given in the DC Operating Conditions table.

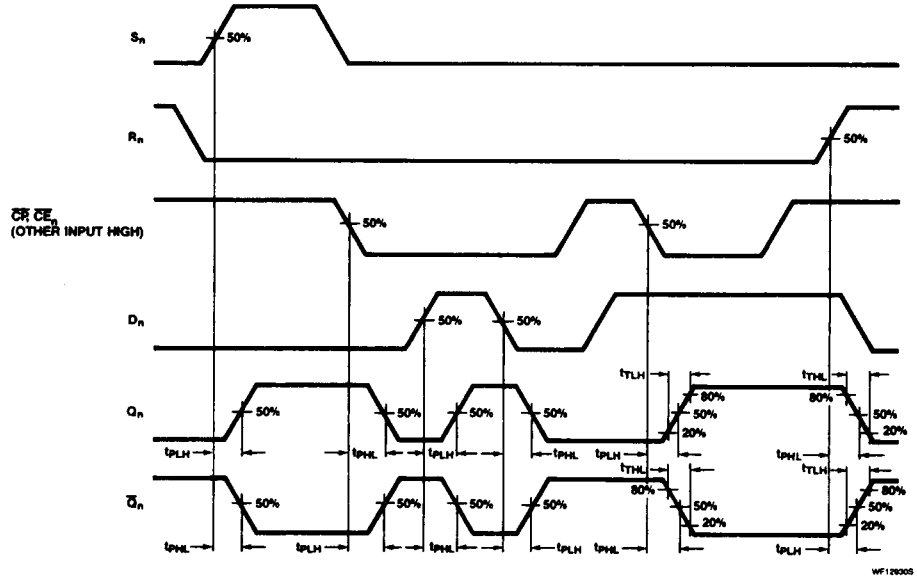
AC ELECTRICAL CHARACTERISTICS $V_{CC1} = V_{CC2}$ = ground, V_{EE} = –5.2V ± 0.010V

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS T_A = –30°C MIN.	LIMITS T_A = –30°C MAX.	LIMITS T_A = +25°C MIN.	LIMITS T_A = +25°C TYP.	LIMITS T_A = +25°C MAX.	LIMITS T_A = +85°C MIN.	LIMITS T_A = +85°C MAX.	UNIT
t_{PLH} t_{PHL}	Propagation delay D_n to Q_n, $\overline{Q}_n$	Waveform 1	1.00 1.00	3.60 3.60	1.00 1.00	2.50 2.50	3.50 3.50	1.00 1.00	3.80 3.80	ns ns
t_{PLH} t_{PHL}	Propagation delay R_n to Q_n, $\overline{Q}_n$		1.00 1.00	3.60 3.60	1.00 1.00	2.70 2.70	3.50 3.50	1.00 1.00	3.90 3.90	ns ns
t_{PLH} t_{PHL}	Propagation delay S_n to Q_n, $\overline{Q}_n$		1.00 1.00	3.60 3.60	1.00 1.00	2.70 2.70	3.50 3.50	1.00 1.00	3.90 3.90	ns ns
t_{PLH} t_{PHL}	Propagation delay $\overline{CP}$, $\overline{CE}_n$ to Q_n, $\overline{Q}_n$		1.00 1.00	4.30 4.30	1.00 1.00		4.00 4.00	1.00 1.00	4.10 4.10	ns ns
t_s	Setup time D_n to $\overline{CP}$, $\overline{CE}_n$	Waveform 2	2.50		2.50			2.50		ns
t_h	Hold time D_n to $\overline{CP}$, $\overline{CE}_n$		1.50		1.50			1.50		ns
t_{TLH} t_{THL}	Transition time 20% to 80%, 80% to 20%	Waveform 1	1.00 1.00	3.60 3.60	1.10 1.10	2.70 2.70	3.50 3.50	1.10 1.10	3.80 3.80	ns ns

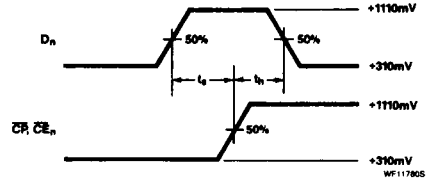
NOTE:
For AC test setup information, see AC Testing, Chapter 2, Section 3.

Latch 10130

AC WAVEFORMS



Waveform 1. Propagation Delay and Transition Times



Waveform 2. Setup and Hold Times