PLESSEY Semiconductors

T-79-07-10

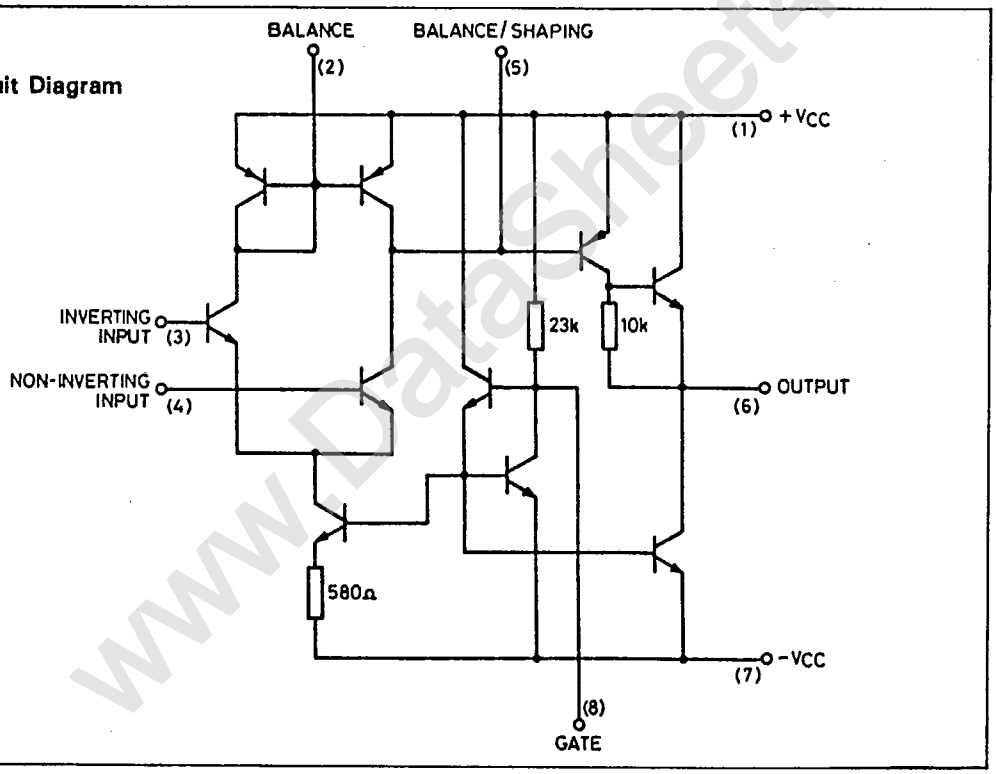
ZN424P

GATED LINEAR AMPLIFIER

FEATURES

- 86dB typical gain
- Very low open loop distortion
- Low noise ($e_n^2 = 4 \times 10^{-17}$ V²/Hz; 100Hz to 20kHz)
- 200kΩ input resistance
- 20kHz open loop bandwidth (−3dB)
- 0.1μs closed loop rise time
- Class A output stage
- 100V/μs slew rate (rising edge)
- Maximum output swing ±11V, ±17V at V_{CC} = ±18V
- Operation at 5V, TTL compatible
- Logic gate current drive capability
- Input-output isolation gating facility

Circuit Diagram



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GENERAL DESCRIPTION

The ZN424P is a versatile linear amplifier designed to satisfy the growing requirement for high quality signal processing. As a voltage amplifier the very low distortion and low noise performance makes the device ideally suited for audio applications. The gating facility, coupled with the ability to operate from a TTL supply, gives the device broad appeal in the instrumentation, computing and allied fields. The device is readily stabilised using an external capacitor, or capacitor/resistor combination.

PIN CONFIGURATIONS

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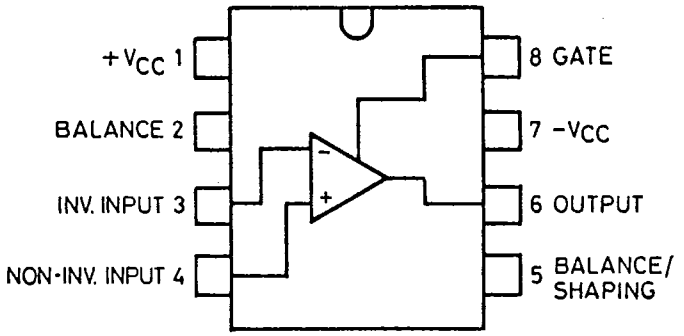


ZN424P
(8 lead Moulded Dual in-line)
Viewed from top

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation	250mW
Differential Input Voltage	5V
Storage Temperature Range	−65 to +125°C

RECOMMENDED RATINGS

Supply Voltage Range	±2 to ±18V
Operating Temperature Range	0 to +70°C

ELECTRICAL CHARACTERISTICS

($V_S = \pm 12V$, Load = 20kΩ, $T_{amb} = 25°C$ unless otherwise specified). T-79-07-10

Parameter	Min.	Typ.	Max.	Units
Input offset voltage		2	6	mV
Input current		0.5	1.2	μA
Input offset current		0.1	0.5	μA
Input offset voltage drift		5		μV/°C
Input current drift		2.0		nA/°C
Input offset current drift		0.4		nA/°C
Input resistance		200		kΩ
Output resistance		4		kΩ
Voltage gain	10,000	20,000		
Mutual conductance		5		A/V
Common mode range	±10	±11		V
Output voltage swing	±10	±11		V
Maximum negative output current (load = 1kΩ)		3.0		mA
Supply current		5.5	7.0	mA
Open loop bandwidth (−3dB)		20		kHz
Unity gain bandwidth (−3dB) (See Note 2)		1		MHz
Common mode rejection ratio	70	100		dB
Supply rejection ratio	80	85		dB
Unity gain rise time(slew rate 1.5V/μs, see Note 2)		0.35		μs
Unity gain overshoot (see Note 2)		10		%
Output leakage current (gated off)		5	30	nA
Voltage gain $V_S = \pm 2.5V$, 3.3kΩ between gating input and $+V_{CC}$, load = 10kΩ	5,000	12,000		
Slew rising edge		100		V/μs
Slew rate falling edge		12		V/μs
Open loop distortion (2V ptp swing)		<1.5		%T.H.D.
Open loop distortion (10V ptp swing)		6		%T.H.D.

OPERATING NOTES

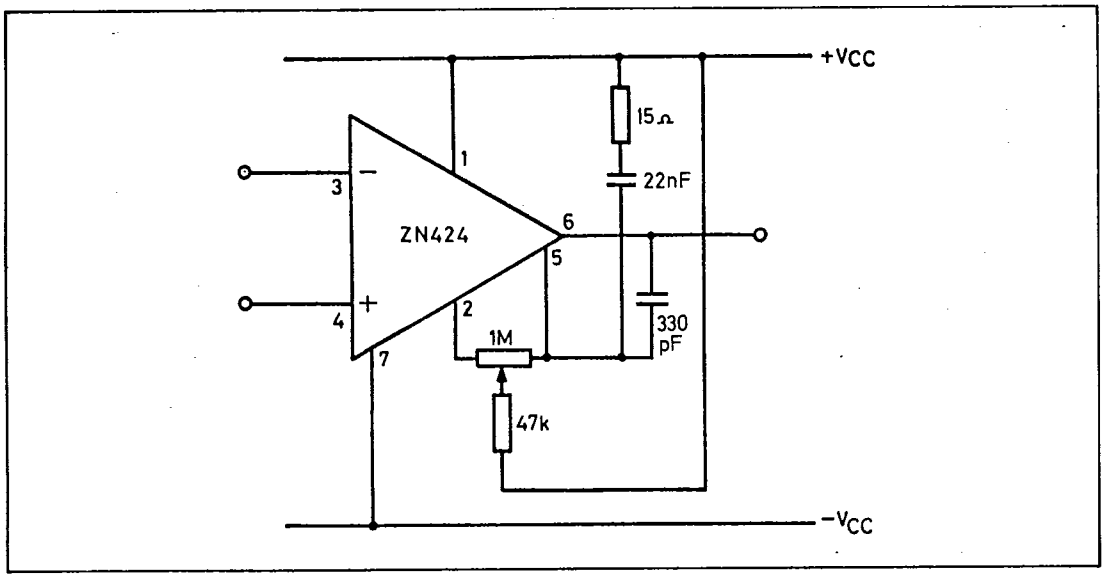
1. When operating with low supply voltages the output bias current may be maintained at about 3mA by connecting an external resistor between the gating input and $+V_{CC}$. Under these conditions the output current is given approximately by:

$$I_C = \frac{(V_{CC} - 1.4) \times 3}{R}$$

R is the parallel combination of the external and internal (23kΩ) resistors.

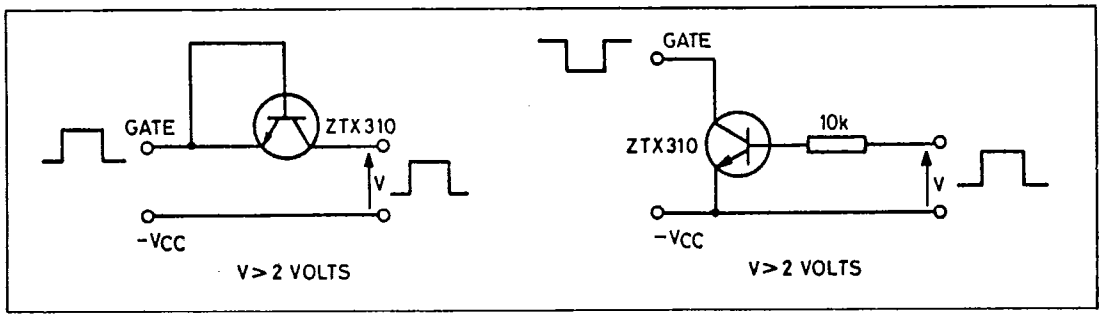
2. Unity frequency stability is achieved by connecting a 22nF capacitor and a 15 ohm resistor in series between 'shaping' and +Vcc. and 330pF between 'shaping' and output.

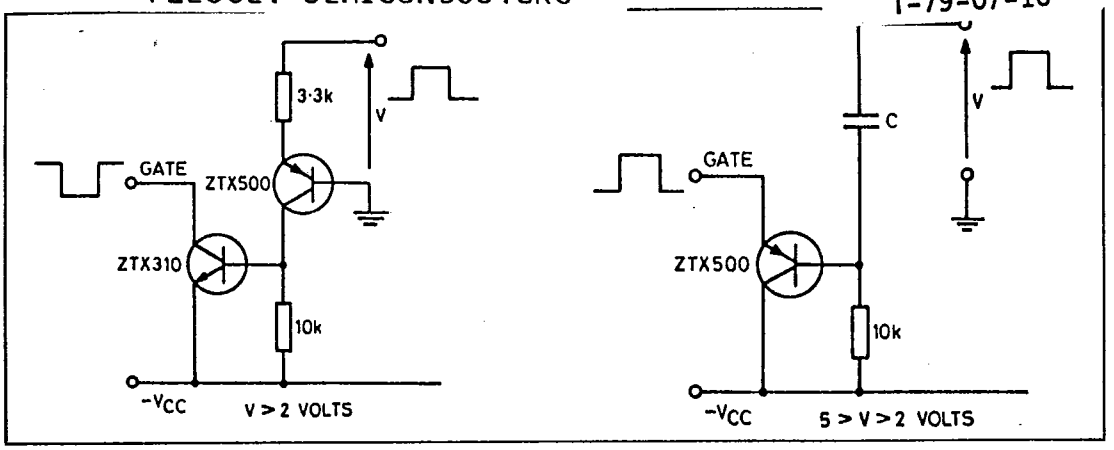
3. Input offset voltage is nullified by connecting a 1MΩ potentiometer between 'balance' and 'balance/shaping' with the wiper connected through a 47kΩ resistor to $+V_{CC}$.



Offset and Frequency Compensation Circuit

4. The ZN424P is gated 'off' by shunting the current source bias current to the negative rail. Four methods of gating the ZN424P are illustrated below, two of which require a drive voltage with respect to the negative rail (e.g. from another ZN424P or from logic, when using a single supply), and the other two allowing the drive pulse to be with respect to earth or another convenient point.



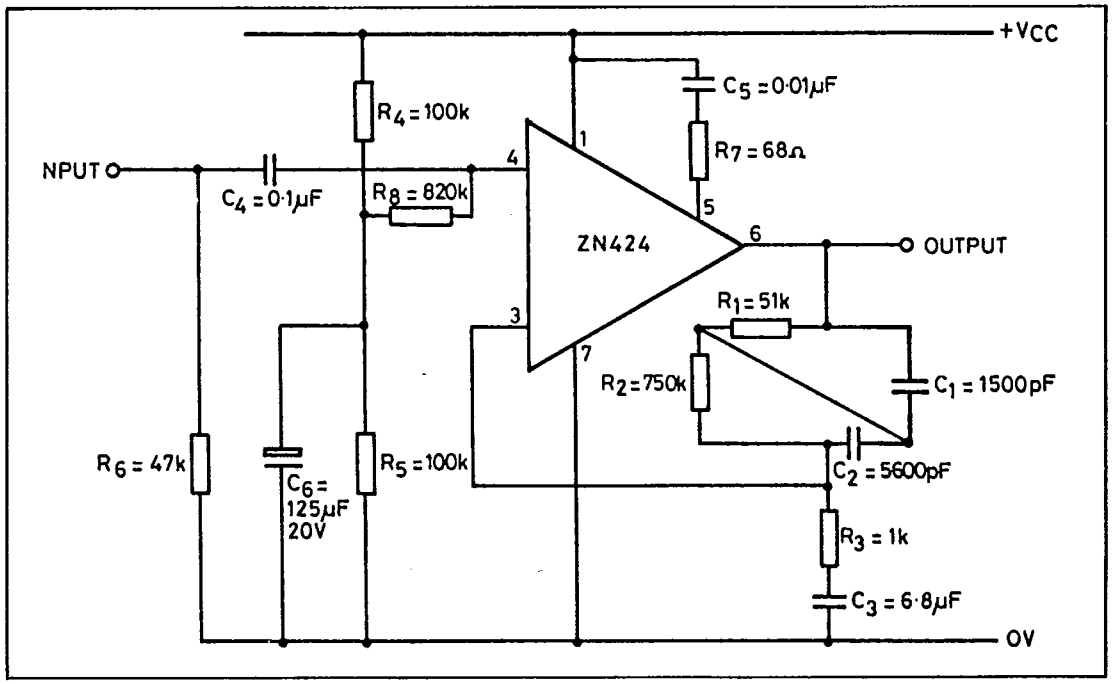


5. When gated off, the input-output coupling is representable by a 1pF capacitor.

APPLICATIONS

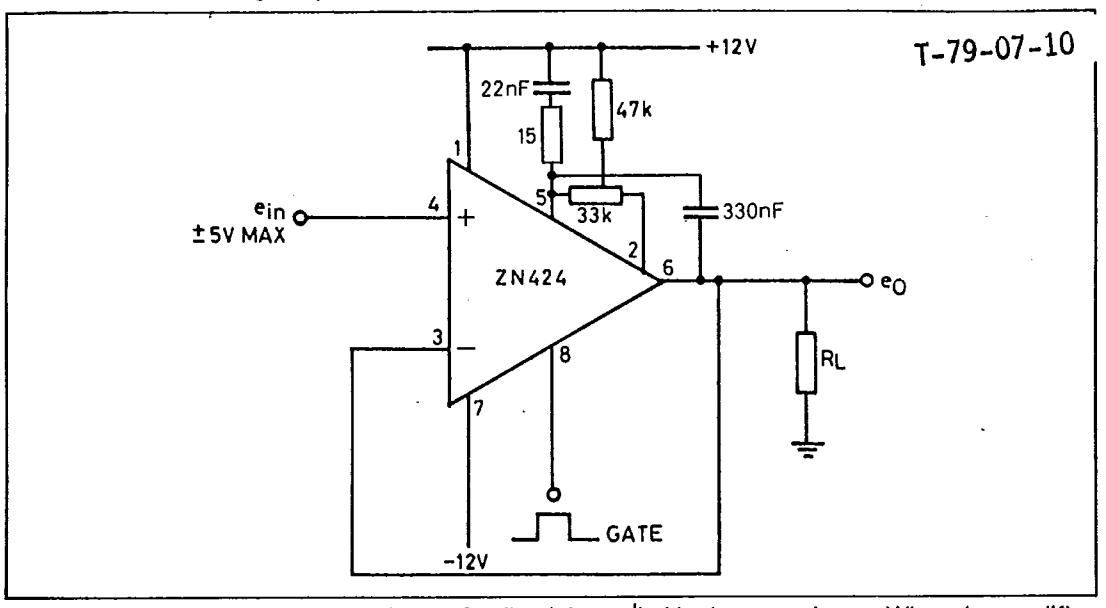
1. Magnetic Cartridge (R.I.A.A.) Preamplifier:

The open loop gain of the ZN424P is 20,000 (86dB) and the open loop distortion is typically, 1.5% corresponding to a 2 volt peak output swing (this is the maximum output ever likely to be encountered from a magnetic cartridge). To feed most power amplifiers a voltage gain, at 1kHz, of 50 (34dB) is necessary between cartridge and amplifier. Thus by applying 52dB of feedback (86dB to 34dB) the distortion figure at 1kHz becomes 0.004%. If more gain is required R_3 may be made smaller but C_3 must be increased proportionaly to avoid loss of bias. C_1, C_2, R_1, R_2 provide R.I.A.A. equlisation and, in addition, C_3 and R_3 provide an effective rumble filter. C_5 and R_7 provide stability for all supply voltages. Assuming a 30 volts supply the overload factor of the circuit is $\simeq$ 40dB referred to a 5mV input. The signal to noise ratio is better than 70dB below a 5mV input. The layout of the circuits is unimportant.



Magnetic Cartridge Preamplifier Circuit

2(a) X1 Non-Inverting Amplifier: PLESSEY SEMICONDUCTORS

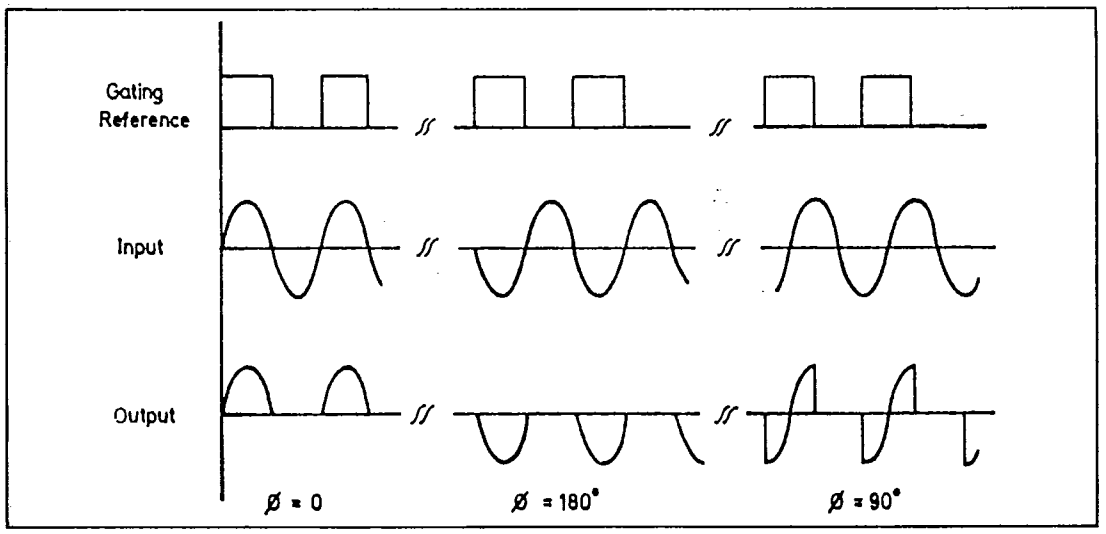


The circuit diagram is shown above. Feedback is applied in the normal way. When the amplifier is gated 'off' the input and output become open circuited as long as the maximum differential input voltage is not exceeded. This limits the input voltage range to ± 5V. This may be effectively increased by attenuating the input suitably and defining the gain of the amplifier to give an overall gain of unity. In order to obtain an overall gain of unity an attenuator comprising of $R_F = 47k\Omega$ and $R_S = 10k\Omega$ is required.

This method has the disadvantages of requiring four accurate resistors, giving a higher output offset voltage (unless an offset control is used) and lower input resistance (57kΩ). However, the settling time is reduced (see Table 1) since lower values of shaping capacitor can be used.

By applying a square wave to the gating point, an output may be obtained which is an amplified square wave modulated version of the input.

2(b) Rectification/Demodulation (no transformers ncessary):



The previous circuit may be used as a half-wave sensitive detector by applying a square wave reference voltage to the gating point and a phase related signal to the input. Typical waveforms are illustrated below for phase differences (ϕ) of 0, 90 and 180 degrees.

The mean d.c. output level is proportional to R cosϕ, where R is the input amplitude. For a half-wave detector with a gain of A:

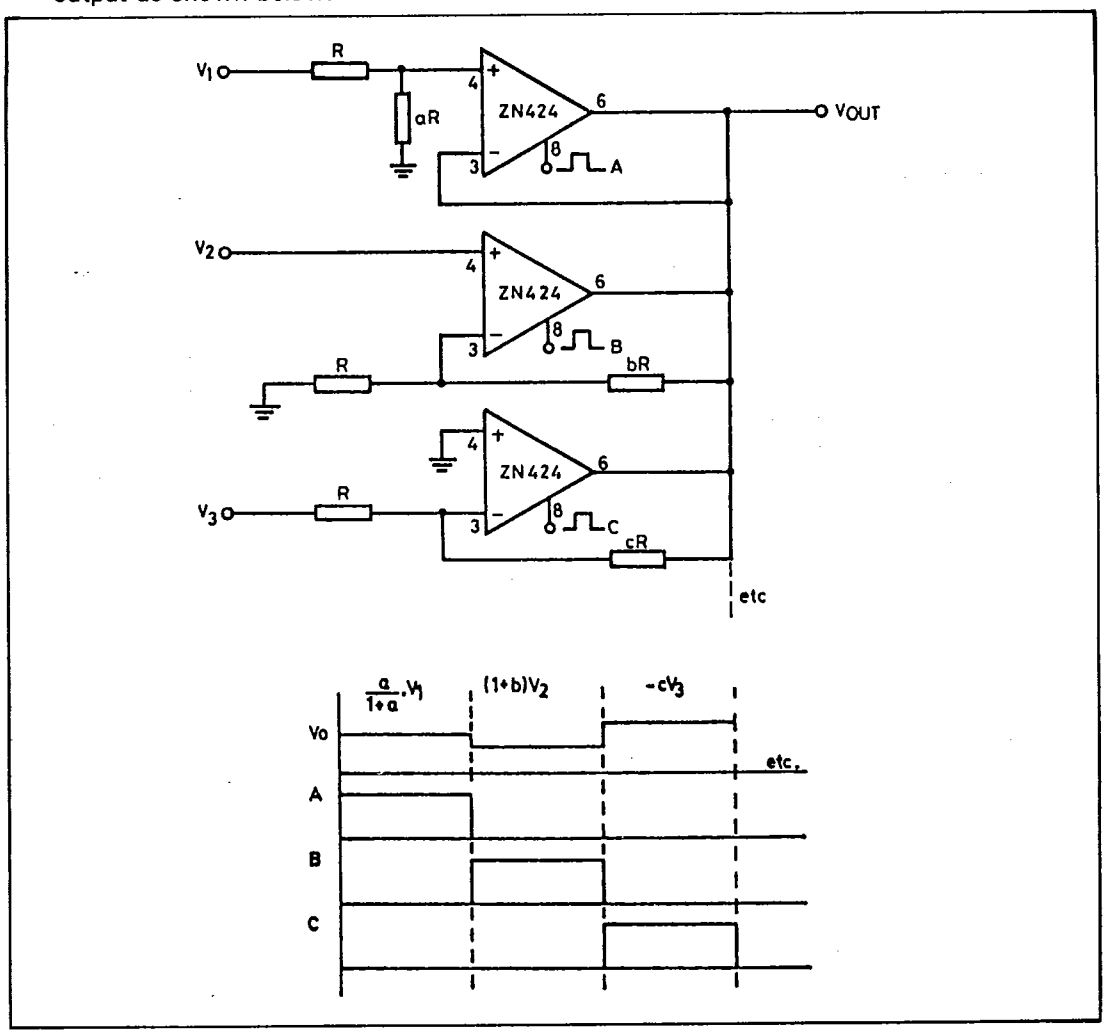
$$\overline{e_O} = \frac{AR}{\pi}\cos\phi$$

Using two phase sensitive detectors driven from square wave reference voltages 90 degrees out of phase, outputs proportional to Rcosϕ and Rsinϕ may be obtained. If these voltages are applied to the X and Y plates of a cathode ray tube the spot will describe the polar plot (R,ϕ). Nyquist plots may thus be obtained directly.

The square wave reference voltages may be generated using a ring counter.

3. Multiplexing:

A ring counter is used to provide a gating pulse to enable the ZN424P to give a multiplexed output as shown below.



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4. Sample and Hold Circuits:

A typical circuit is shown below. The output voltage, e_O, is determined by the choice of feedback resistor when the ZN424P is gated 'on'. When gated 'off', e_O is held for a time which is dependent on 'C', the leakage of the FET and the ZN424P. The value of the capacitor also determines the sampling time necessary. Integrator/Reset circuits can readily be derived from this type of circuit.

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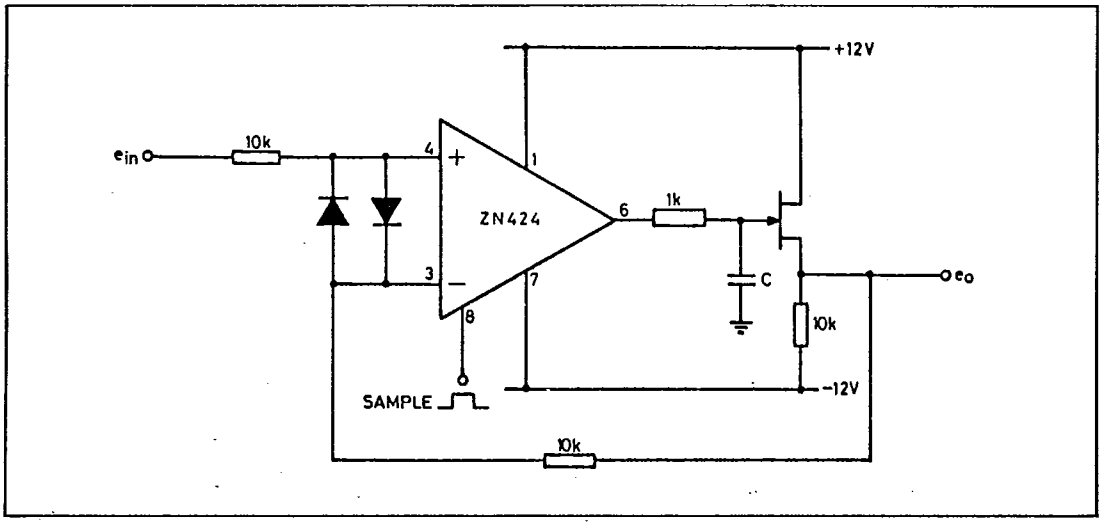
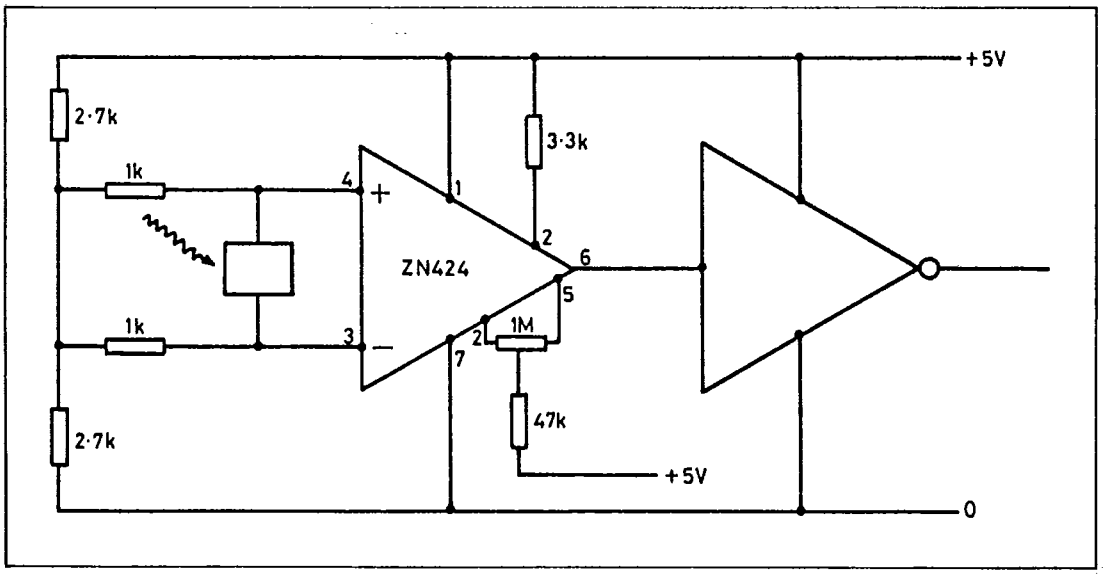


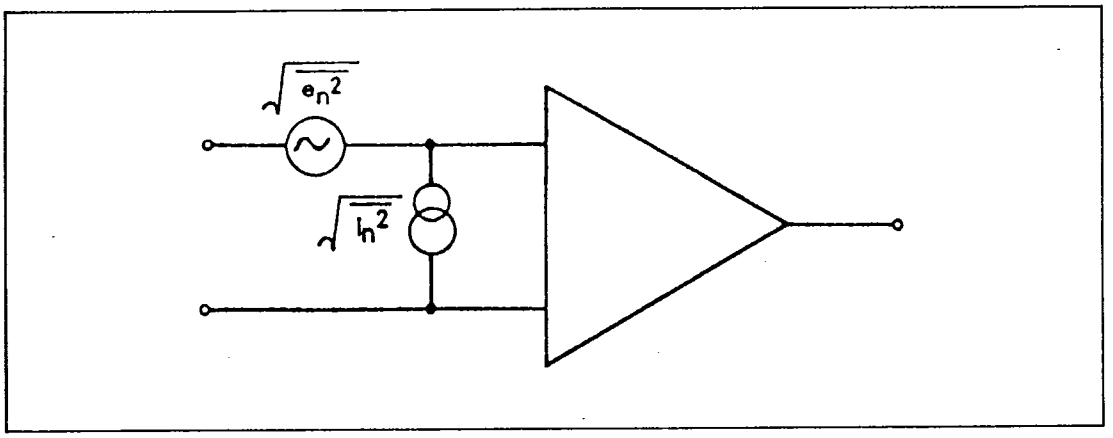
5. Photocell Trigger Circuit Driving TTL Gate(s):

A typical circuit is shown below. The input is biased, so the output is low, when the photocell is irradiated. With no output from the photocell the output is high. The photocell used below gave an output of 60mV, 30μA when irradiated. In this type of circuit the gating facility can be used to switch various combinations of photoelectic, encoder/decoder circuitry.



NOISE PLESSEY SEMICONDUCTORS T-79-07-10

An amplifier always generates noise. At low frequencies flicker noise predominates and increases inversely with the frequency (though presumably not indefinitely). At a sufficiently high frequency this source of noise becomes insignificant compared with shot noise. This is white noise, i.e., has a constant energy/cycle.



Any amplifier may be represented by an ideal amplifier with equivalent noise voltage and current generators at the input as shown above. The mean square noise voltage is shown as $\overline{e_n^2}$ volts^2/cycle and the mean square noise current as $\overline{i_n^2}$ amps^2/cycle. The noise voltage may be measured by short-circuiting the inputs so that no noise current flows into the amplifier. When the input terminals are open-circuited all the noise current flows into the amplifier and the noise voltage generator is open-circuited. The noise that appears at the output of the amplifier will obviously depend upon the shape of the frequency response. If the frequency response is measured the noise measured at the output may be referred back to the input. This is shown below where $\overline{e_n^2}$ and $\overline{i_n^2}$ are plotted against frequency. In an actual case, a source resistance R_S will be connected across the input terminals.

This resistance will itself generate white noise known as Johnson noise of magnitude $\overline{e_r^2} = 4kTR_S$ volts^2/cycle, where k is the Boltzmann constant and T is the absolute temperature. The noise current flowing in this resistance will also produce a mean square noise voltage of $\overline{i_n^2}$ R_S^2volts^2/cycle.

TYPICAL CHARACTERISTICS

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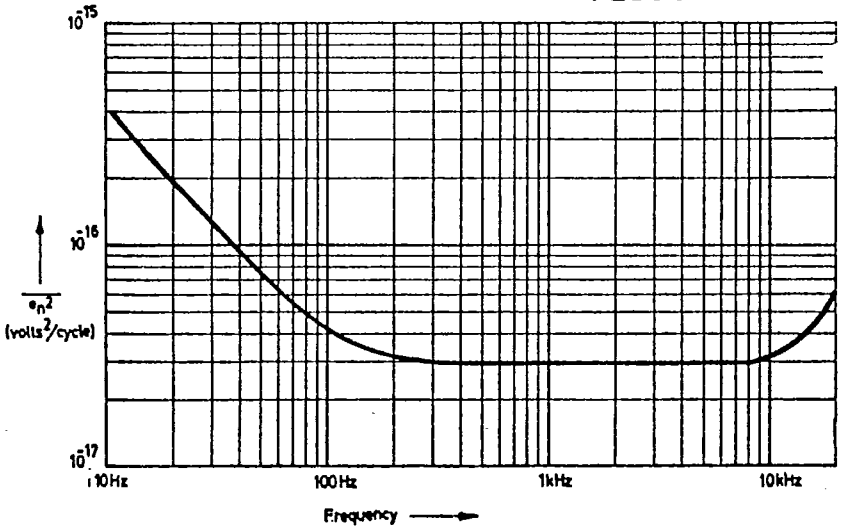

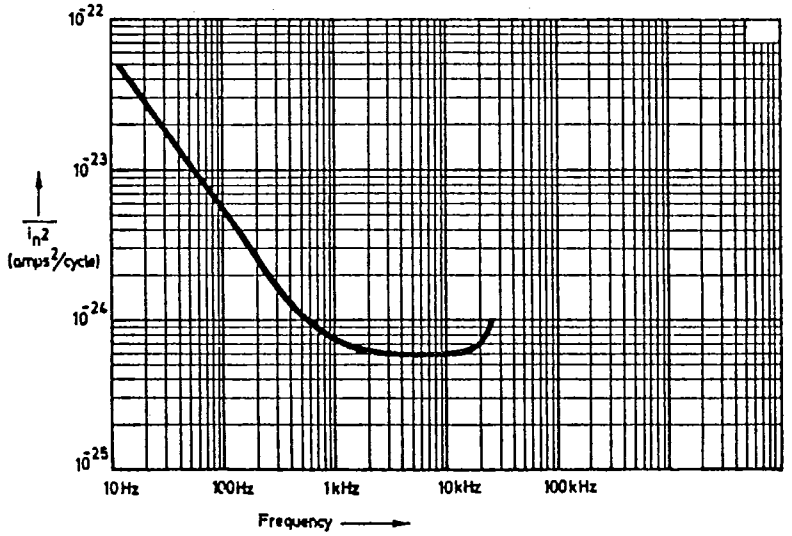

Graph 1. $\overline{e_n^2}$ and $\overline{i_n^2}$ against frequency for ZN424P

Stabilising the ZN424P in Various Gain Configurations

The ZN424P is designed such that any resistive feedback circuit can be stabilised with less than 50 per cent overshoot using $C_1 = 0.1\mu F$. For better than 10 per cent overshoot, the values given in the following table are suitable.

TABLE 1

Closed loop gain	R_F (kΩ)	C_F (pF)	R_1 (Ω)	C_1 (nF)	C_2 (pF)	Rise Time (μs)	Slew Rate (V/μs)
⩾ 250	10	-	-	-	-	0.35	45
100	10	10	68	4.7	-	0.65	12
50	10	10	68	4.7	3.3	0.55	10
20	10	10	68	4.7	7.5	0.4	8
10	10	10	68	4.7	15	0.35	5
5	10	10	68	4.7	33	0.3	3
2	10	10	68	4.7	68	0.22	1.7
1	0	-	15	22	330	0.33	1.5

The rise times and slew rates are given as a guide when the supply current is maintained at about 5mA (see Operating Note 1).
R_1 and C_1 are connected in series between pins 5 and 1; C_2 is connected between pins 5 and 6.
For other values of R_F it may be necessary to change C_F for optimum response.

ZN402 Gated Op Amp (Obsolete)

The ZN402 is electrically similar to the ZN424P and the devices are interchangeable. However, because testing procedures are more rigorous for the ZN424P, its performance is better than that of the ZN402; the ZN424P is therefore recommended for all new designs.