8M x 8 Bit NAND Flash Memory

FEATURES

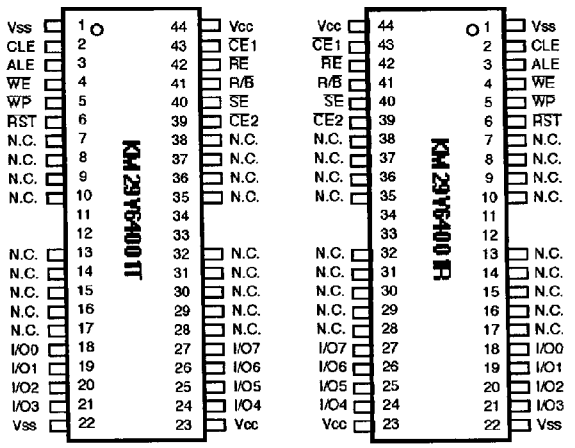
- Single 3.3 - volt Supply
- Organization
  - Memory Cell Array : (8M +128K)bit x 8bit
  - Data Register : (512 + 16)bit x 8bit
- Automatic Program and Erase
  - Page Program : (512 + 16)Byte
  - Block Erase : (8K +256)Byte
  - Status Register
- 528 - Byte Page Read Operation
  - Random Access : 5 μs
  - Serial Page Access : 50 ns
  - Gap-less Sequential read
- Fast Write Cycle Time
  - Program time : 200us
  - Block Erase time : 4ms
- Hardware Reset and Dual $\overline{CE}$ control
- Hardware Data Protection
  - Program/Erase Lockout During Power Transitions
- Reliable CMOS Floating-Gate Technology
  - Endurance :1M Program/Erase Cycles
  - Data Retention : 10 years
- Command Register Operation
- 44(40) - Lead TSOP Type II (400 mil / 0.8 mm pitch)

GENERAL DESCRIPTION

The KM29V64001T/R is a 8M(8,388,608)x8 bit NAND Flash memory with a spare 256K(262,144)x8 bit. Its NAND cell provides the most cost-effective solution for the mass solid state storage market. A program operation programs the 528-byte page in typically 200μs and an erase operation can be performed in typically 4ms on either a 8K-byte block. Data in the page can be read out at 50ns cycle time per byte. The I/O pins serve as the ports for address and data input/output as well as command inputs. The on-chip write controller automates all program and erase system functions, including pulse repetition, where required, and internal verify and margining of data. Even the write-intensive systems can take advantage of the KM29V64001T/R's extended reliability of 1,000,000 program/erase cycles by providing either ECC(Error Checking and Correction) or real time mapping-out algorithm. These algorithms have been implemented in many mass storage applications and also the spare 16 bytes of a page combined with the other 512 bytes can be utilized by system-level ECC.

The KM29V64001T/R is an optimum solution for large nonvolatile storage application such as solid state storage, digital voice recorder, digital still camera and other portable applications requiring nonvolatility.

PIN CONFIGURATION



44(40) TSOP (II) STANDARD TYPE **44(40) TSOP (II) REVERSE TYPE**

Pin Name	Pin Function
I/O0 ~ I/O7	Data Input/Outputs
CLE	Command Latch Enable
ALE	Address Latch Enable
$\overline{CE1}$	Chip Enable 1
$\overline{CE2}$	Chip Enable 2
$\overline{RE}$	Read Enable
$\overline{WE}$	Write Enable
$\overline{WP}$	Write Protect
$\overline{SE}$	Spare area Enable
R/$\overline{B}$	Ready/Busy output
Vcc	Power (+3.3V)
Vss	Ground
N.C.	No Connection

Notes ; Connect all Vcc and Vss pins of each device to power supply outputs.
Do NOT leave Vcc or Vss disconnected.

Figure 1. FUNCTIONAL BLOCK DIAGRAM

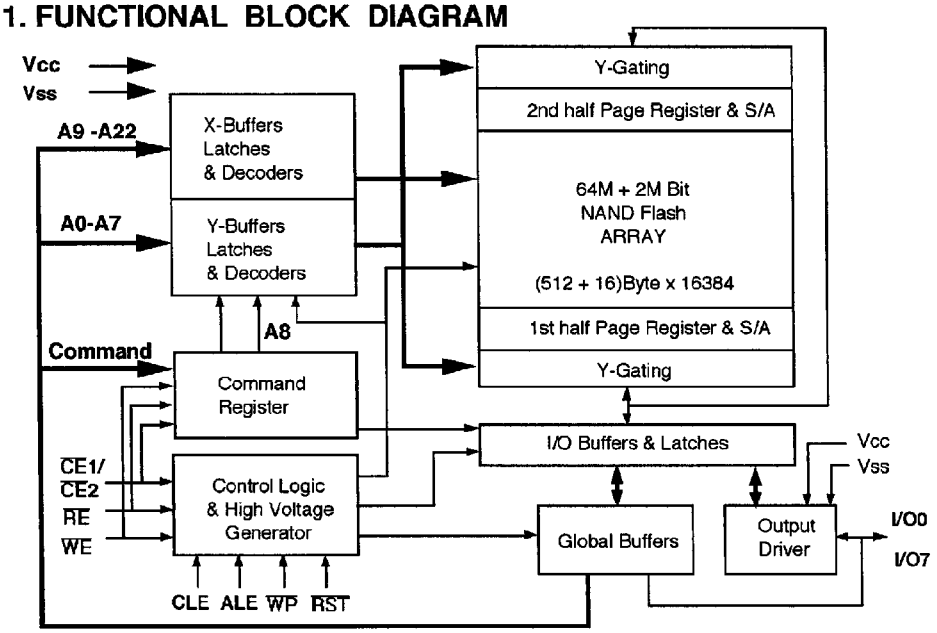
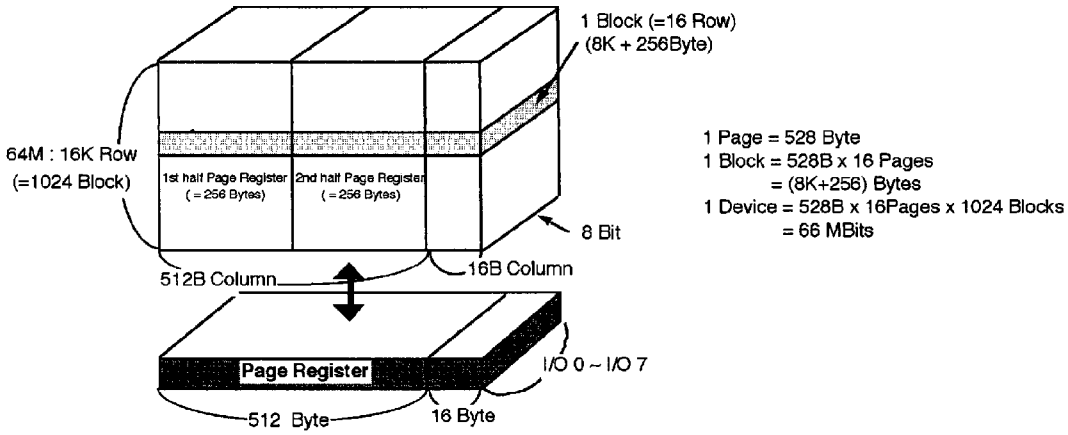


Figure 2. ARRAY ORGANIZATION



	I/O0	I/O1	I/O2	I/O3	I/O4	I/O5	I/O6	I/O7	
1st Cycle	A0	A1	A2	A3	A4	A5	A6	A7	**Column Address**
2nd Cycle	A9	A10	A11	A12	A13	A14	A15	A16	**Row Address**
3rd Cycle	A17	A18	A19	A20	A21	A22	* X	* X	**(Page Address)**

Note : Column Address : Starting Address of the Register.
00H Command (Read) : Defines the starting Address of the 1st half of the Register.
01H Command (Read) : Defines the starting Address of the 2nd half of the Register.

* A8 is initially set to "Low" or "High" by the 00H or 01H Command.
* X can be High or Low.

PRODUCT INTRODUCTION

The KM29V64001 is a 66Mbit(69,206,016 bit) memory organized as 16,384 rows by 528 columns. A spare sixteen columns are located from column address of 512 to 527. A 528-byte data register is connected to memory cell arrays accommodating data transfer between the I/O buffers and memory during page read and page program operations. The memory array is made up of 16 cells that are serially connected to form a NAND structure. Each of the 16 cells reside in a different page. A block consists of the 16 pages formed by one NAND structures, totaling 528 NAND structures of 16 cells. The array organization is shown in Figure 2. The program and read operations are executed on a page basis, while the erase operation is executed on block basis. The memory array consists of 512 separately or grouped erasable 8K-byte blocks. It indicate that the bit by bit erase operation is prohibited on the KM29V64001.

The KM29V64001 has addresses multiplexed into 8 I/O's. This scheme dramatically reduces pin counts and allows system upgrades to future higher densities by maintaining consistency in system board design. Command, address and data are all written through I/O's by bringing $\overline{WE}$ to low while $\overline{CE}$ is low. Data is latched on the rising edge of $\overline{WE}$. Command Latch Enable(CLE) and Address Latch Enable(ALE) are used to multiplex command and address respectively, via the I/O pins. All commands require one bus cycle except for Block Erase command which requires two cycles: a cycle for erase-setup and another for erase-execution after block address loading. The 8M byte physical space requires 23 addresses, thereby requiring three cycles for byte-level addressing: column address, low row address and high row address, in that order. Page Read and Page Program need the same three address cycles following the required command input. In Block Erase operation, however, only the two row address cycles are used. Device operations are selected by writing specific commands into the command register. Table1 defines the specific commands of the KM29V64001.

Table 1. COMMAND SETS

Function	1st. Cycle	2nd. Cycle	Acceptable Command during Busy State
Sequential Data Input	80h	-	
Read 1	00h/01h (1)	-	
Read 2	50h (2)	-	
Gap-less Sequential read	02h	-	
Read ID	90h	-	
Reset	FFh	-	O
Page Program	10h	-	
Block Erase	60h	D0h	
Erase Suspend	B0h	-	O
Erase Resume	D0h	-	
Read Status	70h	-	O

Note : 1) The 00h Command defines starting Address on the 1st half of Registers.
The 01h Command defines starting Address on the 2nd half of Registers.
After data access on the 2nd half of register by the 01H command, the status pointer is automatically moved to the 1st half register (00H) on the next cycle.
2) The 50H command is valid only When the $\overline{SE}$ (pin 40) is low level.

PIN DESCRIPTION

Command Latch Enable(CLE)

The CLE input controls the path activation for commands sent to the command register. When active high, commands are latched into the command register through the I/O ports on the rising edge of the $\overline{WE}$ signal.

Address Latch Enable(ALE)

The ALE input controls the path activation for address and input data to the internal address/data registers. Addresses are latched on the rising edge of $\overline{WE}$ with ALE high, and input data is latched when ALE is low. When the device is in the busy state during program or erase, CE high does not return the device to standby mode.

Chip Enable($\overline{CE}$1, $\overline{CE}$2)

The $\overline{CE}$ input is the device selection control. With either $\overline{CE}$1 or $\overline{CE}$2 high, the device is returned to standby mode. Both $\overline{CE}$1, $\overline{CE}$2 must be low to select the device. When $\overline{CE}$ goes high during a read operation the device is returned to standby mode. However, when the device is in the busy state during program or erase, $\overline{CE}$ high is ignored, and does not return the device to standby mode.

Write Enable($\overline{WE}$)

The $\overline{WE}$ input controls writes to the I/O port. Commands, address and data are latched on the rising edge of the $\overline{WE}$ pulse.

Read Enable($\overline{RE}$)

The $\overline{RE}$ input is the serial data-out control, and when active drives the data onto the I/O bus. Data is valid tREA after the falling edge of $\overline{RE}$ which also increments the internal column address counter by one.

Spear Area Enable($\overline{SE}$)

The $\overline{SE}$ input is the spear area control, and when high deselects the spare area during Read1, Sequential data input and Page program.

I/O Port : I/O 0 - I/O 7

The I/O pins are used to input command, address and data, and to outputs data during read operations. The I/O pins float to high-z when the chip is deselected or the outputs are disabled.

Write Protected($\overline{WP}$)

The $\overline{WP}$ pin provides inadvertent write/erase protection during power transitions. The internal high voltage generator is reset when the $\overline{WP}$ pin is active low.

Ready / $\overline{Busy}$(R/$\overline{B}$)

The R/$\overline{B}$ output indicates the status of the device operation. When low, it indicates that a program, erase or random read operation is in process and return to high state upon completion. It is an open drain output and does not float to high-z condition when the chip is deselected or outputs are disabled.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to Vss	VIN	-0.6 to +5.0	V
Temperature Under Bias	Tbias	-10 to +125	°C
Storage Temperature	Tstg	-65 to +150	°C
Short Circuit Output Current	Ios	5	mA

* Notes

1. Minimum DC voltage is -0.3V an input/output pins. During transitions, this level may undershoot to -2.0V for periods <30ns. Maximum DC voltage on input/output pins is Vcc+0.5V which, during transitions, may overshoot to Vcc+2.0V for periods <20ns.
2. Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded. Functional operation should be restricted to the conditions as detailed in the operational sections of this data sheet. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS (Voltage reference to GND, Ta = 0 to 70 °C)

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	Vcc	3.0	3.3	3.6	V
Supply Voltage	Vss	0	0	0	V

DC AND OPERATING CHARACTERISTICS

(Recommended operating conditions otherwise noted.)

Parameter		Symbol	Test Conditions		Min	Typ	Max	Unit
Operating Current	Sequential Read	Icc1	tcycle=50ns	$\overline{CE}$=VIL, Iout = 0 mA	-	10	30	mA
		Icc2	tcycle= 1 us		-	2	5	mA
	Command, Address Input	Icc3	tcycle=50ns			10	30	mA
	Data Input	Icc4	-		-	10	30	mA
	Register Read	Icc5	tcycle=50ns	Iout = 0mA	-	10	30	mA
	Program	Icc6	-		-	10	30	mA
	Erase	Icc7	-		-	10	40	mA
Stand-by Current (TTL)		ISB1	$\overline{CE}$=VIH, $\overline{WP}$=$\overline{SE}$=0V/Vcc		-	-	1	mA
Stand-by Current (CMOS)		ISB2	$\overline{CE}$=Vcc-0.2, $\overline{WP}$=$\overline{SE}$=0V/Vcc		-	50	100	μA
Input Leakage Current		ILI	VIN =0 to 3.6 V		-	-	±10	μA
Output Leakage Current		ILO	VOUT =0 to 3.6 V		-	-	±10	μA
Input High Voltage , All inputs		VIH	-		2.0	-	Vcc+0.3	V
Input Low Voltage , All inputs		VIL	-		-0.3	-	0.8	V
Output High Voltage Level		VOH	IOH= -400uA		2.4	-	-	V
Output Low Voltage Level		VOL	IOL= 2.1 mA		-	-	0.4	V
Output Low Current (R/$\overline{B}$)		IOL($\overline{R/B}$)	VOL =0.4 V		8	10	-	mA

VALID BLOCK

Symbol	Parameter	Min	Typ	Max	Unit
NVB	Valid Block Number	1004	1014	1024	Blocks

Note : The KM29V64001T/R may include less than 20 unusable blocks. Do not try to access these bad blocks for program and erase. (Refer to technical note)

AC TEST CONDITION

Note : Ta = 0 °C to + 70 °C, Vcc=3.3V± 10 %, unless otherwise noted.

Parameter	Value
Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Times	5 ns
Input and Output Timing Levels	0.8V and 2.0V
Output Load	1 TTL GATE and CL = 100 pF

CAPACITANCE (Ta = 25 °C , Vcc=3.3V, f = 1.0 MHz)

Item	Symbol	Condition	Min	Max	Unit
Input / Output Capacitance	CI/O	VIL = 0V	-	10	pF
Input Capacitance	CIN	VIN = 0V	-	10	pF

Note : Capacitance is periodically sampled and not 100% tested.

MODE SELECTION

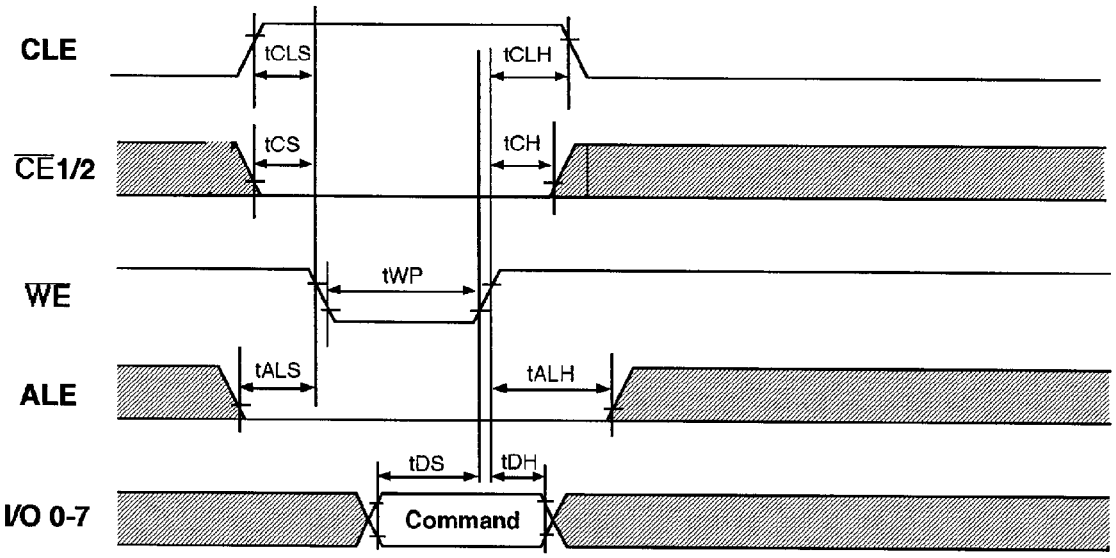
CLE	ALE	CE1	CE2	WE	RE	SE	WP	RST	Mode	I/O	Power
H	L	L	L	↑	H	X	X	H	Command Input	Din	Active
L	H	L	L	↑	H	X	X	H	Address Input(3clock)	Din	Active
L	H	L	L	H	↓	X	X	H	Address Output(3clock)	Dout	Active
L	L	L	L	↑	H	L/H(3)	X	H	Data Input	Din	Active
L	L	L	L	H	↓	L/H(3)	X	H	Sequential Read & Data Output	Dout	Active
X	X	X	X	X	X	L/H(3)	H	H	During Program (Busy)	High-Z	Active
X	X	X	X	X	X	X	H	H	During Erase (Busy)	High-Z	Active
X	X(1)	X	X	X	X	X	L	H	Write Protect	High-Z	Active
X	X	X	X	X	X	X	X	↑	Reset	High-Z	Stand-by
X	X	H	L	X	X	0V/Vcc	0V/Vcc	H	Stand-by	High-Z	Stand-by
X	X	L	H	X	X	0V/Vcc(2)	0V/Vcc(2)	H			
X	X	H	H	X	X	0V/Vcc	0V/Vcc	H			

Notes : 1. X can be VIL or VIH
2. $\overline{WP}$ should be biased to CMOS high or CMOS low for standby.
3. When $\overline{SE}$ is high, spare area is deselected.

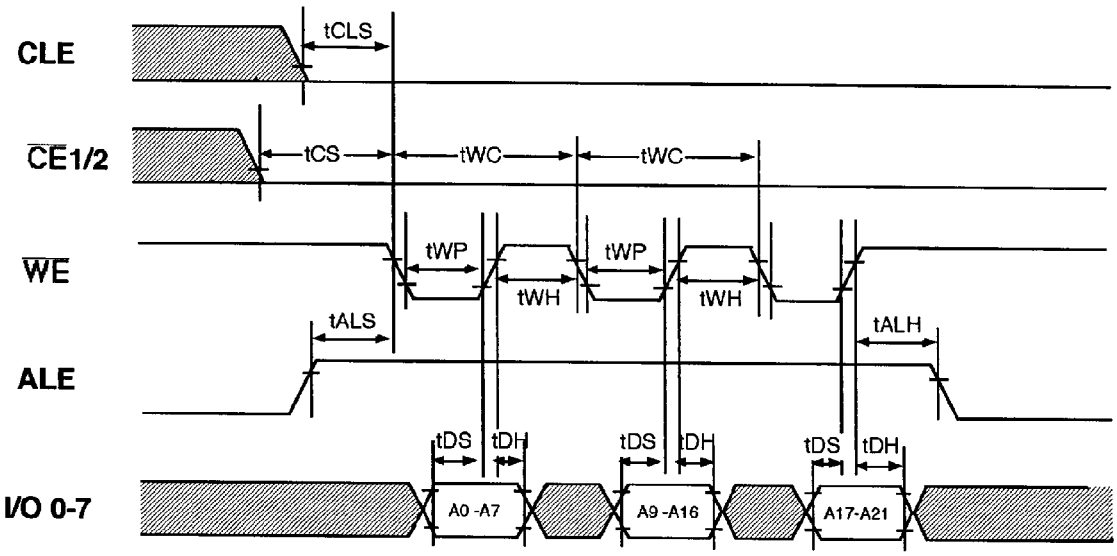
A.C. Characteristics for Command / Address / Data Input

Parameter	Symbol	Min	Max	Unit
CLE Set-up Time	tCLS	0	-	ns
CLE Hold Time	tCLH	10	-	ns
$\overline{CE}$ Setup Time	tCS	0	-	ns
$\overline{CE}$ Hold Time	tCH	10	-	ns
$\overline{WE}$ Pulse Width	tWP	25	-	ns
ALE Set-up Time	tALS	0	-	ns
ALE Hold Time	tALH	10	-	ns
Data Set-up Time	tDS	20	-	ns
Data Hold Time	tDH	10	-	ns
Write Cycle Time	tWC	50	-	ns
$\overline{WE}$ High Hold Time	tWH	10	-	ns

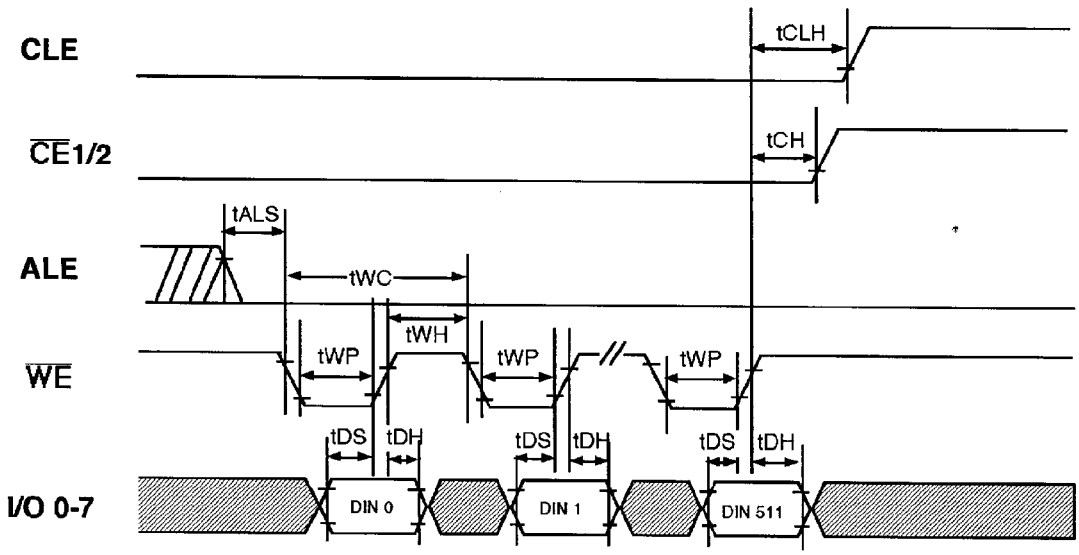
* Command Latch Cycle



* Address Latch Cycle



* Input Data Latch Cycle



A.C. Characteristics for Operation

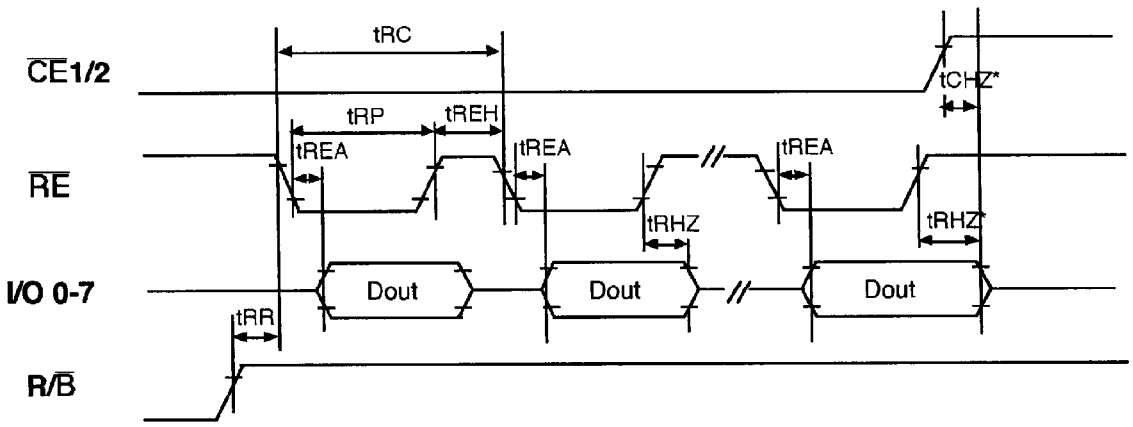
Parameter	Symbol	Min	Max	Unit
Data Transfer from Cell to Register	tR	-	5	μs
ALE to $\overline{RE}$ Delay (Read register, read ID)	tAR1	100	-	ns
ALE to RE Delay (Read cycle)	tAR2	50	-	ns
$\overline{CE}$ to $\overline{RE}$ Delay (Address register read, ID read)	tCR	100	-	ns
Ready to $\overline{RE}$ Low	tRR	20	-	ns
$\overline{RE}$ Pulse Width	tRP	30	-	ns
$\overline{WE}$ High to Busy	tWB	-	100	ns
Read Cycle Time	tRC	50	-	ns
$\overline{RE}$ Access Time	tREA	-	35	ns
$\overline{RE}$ High to Output Hi-Z	tRHZ	15	30	ns
$\overline{CE}$ High to Output Hi-Z	tCHZ	-	20	ns
$\overline{RE}$ High Hold Time	tREH	10	-	ns
Output Hi-Z to $\overline{RE}$ Low	tIR	0	-	ns
Last $\overline{RE}$ High to Busy (at sequential read)	tRB	-	100	ns
$\overline{CE}$ High to Ready (in case of interception by $\overline{CE}$ at read) (1)	tCRY	-	50 + tr(R/$\overline{B}$) (2)	ns
$\overline{CE}$ High Hold Time (at the last serial read) (3)	tCEH	100	-	ns
ALE Setup Time (Register Read)	tALS1	10		ns
$\overline{RE}$ Low to Status Output	tRSTO	-	35	ns
$\overline{CE}$ Low to Status Output	tCSTO	-	45	ns
$\overline{RE}$ High to $\overline{WE}$ Low	tRHW	0	-	ns
$\overline{WE}$ High to $\overline{CE}$ Low	tWHC	30	-	ns
$\overline{WE}$ High to $\overline{RE}$ Low	tWHR	30	-	ns
Erase Suspend Input to Ready	tSR	-	500	us
RE access time (Read ID)	tREADID	-	35	ns
$\overline{RST}$ pin low width (Hardware reset)	tRSTW	300		ns
Device Resetting Time (Read/Program/Erase/after erase suspend)	tRST	-	5/10/500/5	us

Note : 1. If $\overline{CE}$ goes high within 30ns after the rising edge of the last $\overline{RE}$, R/$\overline{B}$ will not transition to V_{OL}.
2. The time to Ready depends on the value of the pull-up resistor tied to R/$\overline{B}$ pin.
3. To break the sequential read cycle, $\overline{CE}$ must be held high for longer than tCEH.

Program/Erase Characteristics

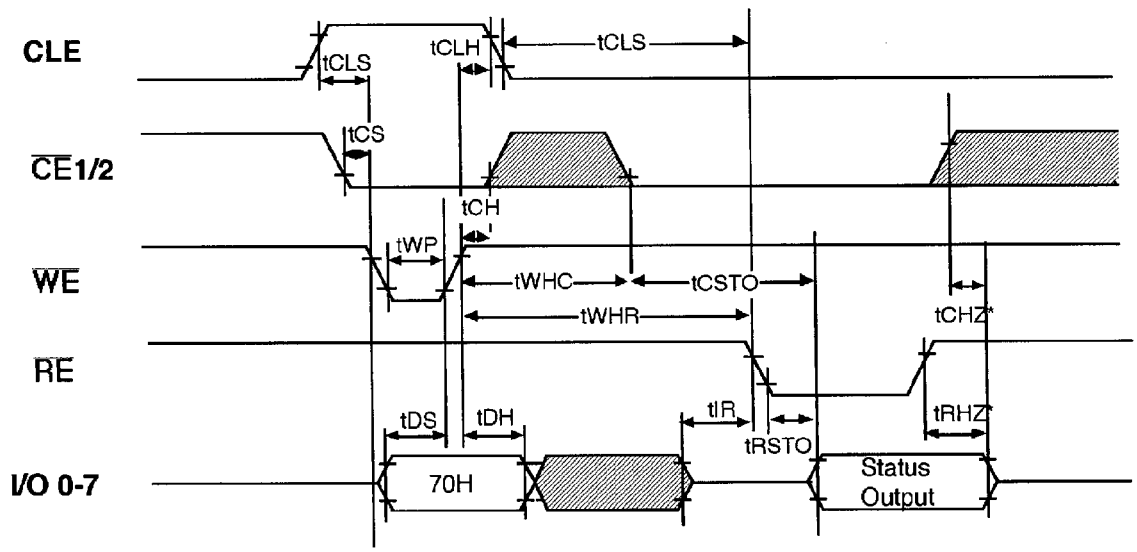
Parameter	Symbol	Min	Typ	Max	Unit
Program Time	tPROG	-	0.2	1.0	ms
Number of Partial Program Cycles in the Same Page	Nop	-	-	10	cycles
Block Erase Time	tBERS	-	4	20	ms

* Sequential Out Cycle after Read (CLE=L, $\overline{WE}$=H, ALE=L)

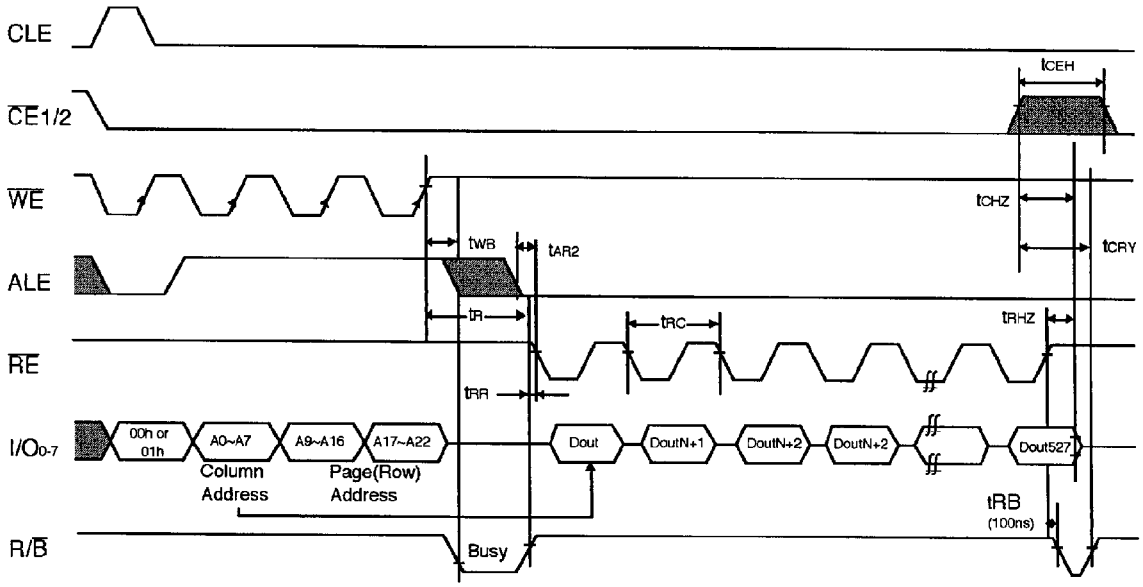


Note : Transition is measured ± 200mV from steady state voltage with load.
This parameter is sampled and not 100% tested.

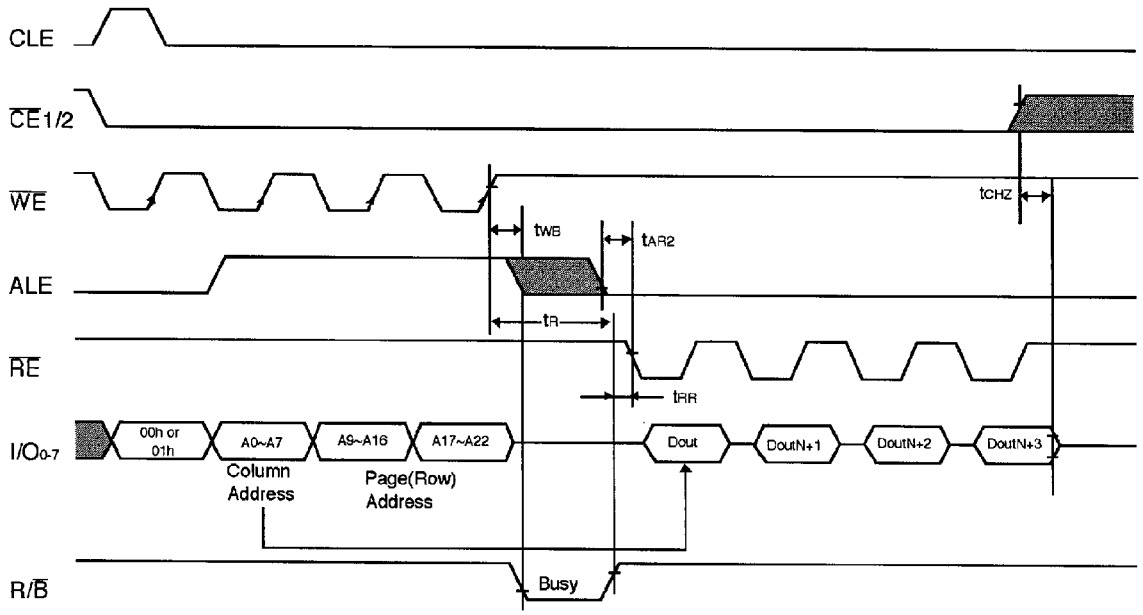
* Status Read Cycle



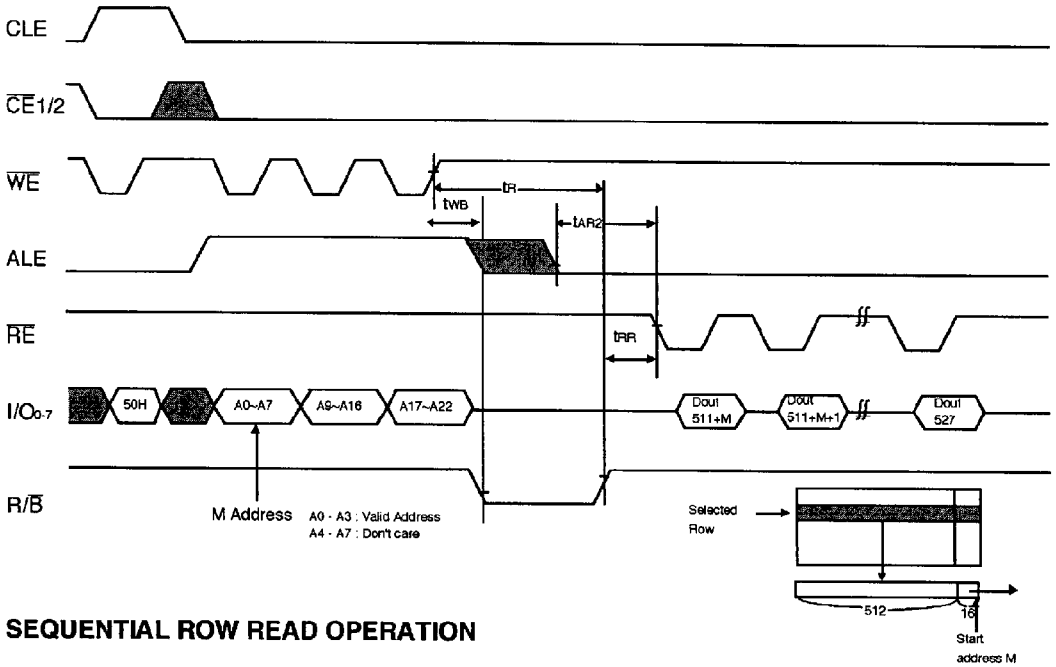
READ1 OPERATION (READ ONE PAGE)



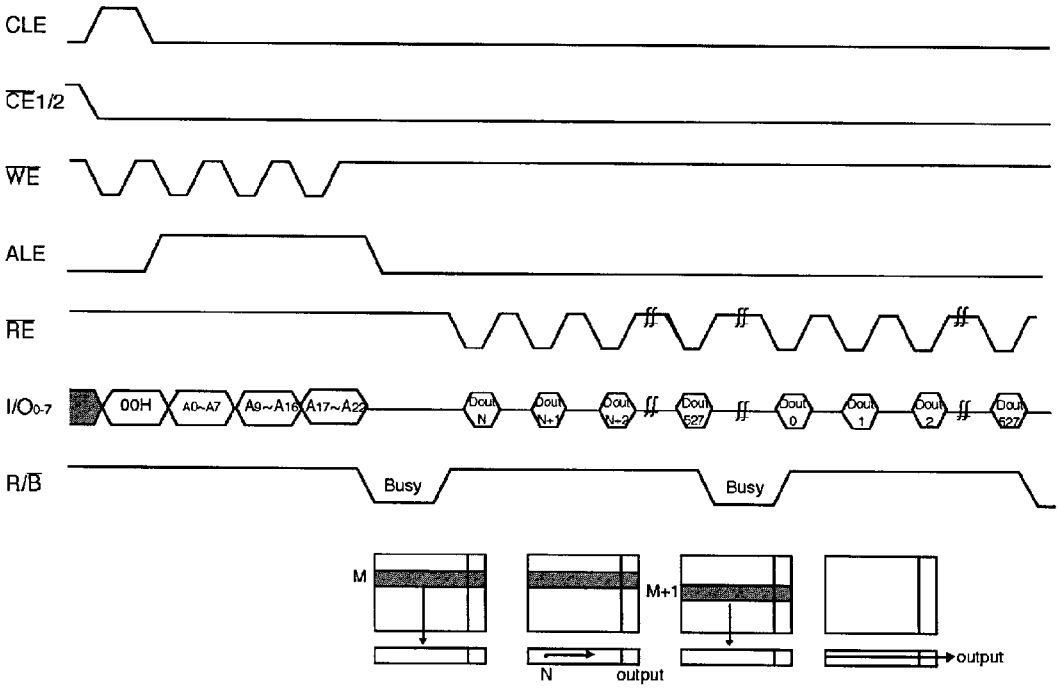
READ1 OPERATION (INTERCEPTED BY CE)



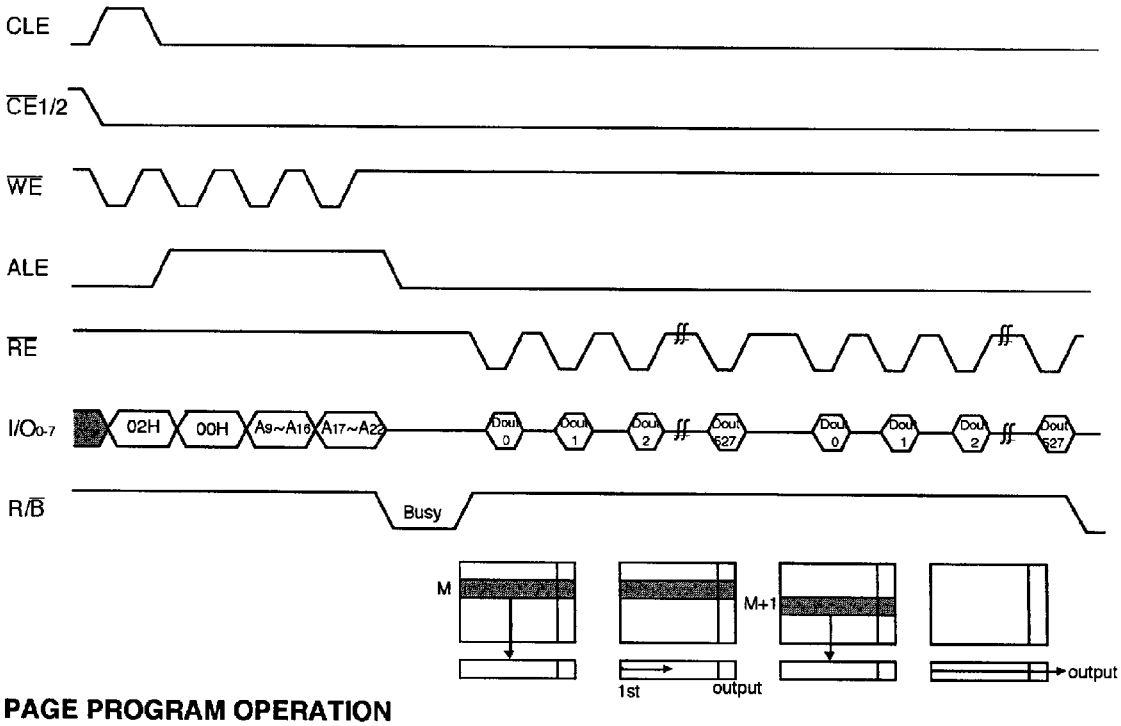
READ2 OPERATION (READ ONE PAGE)



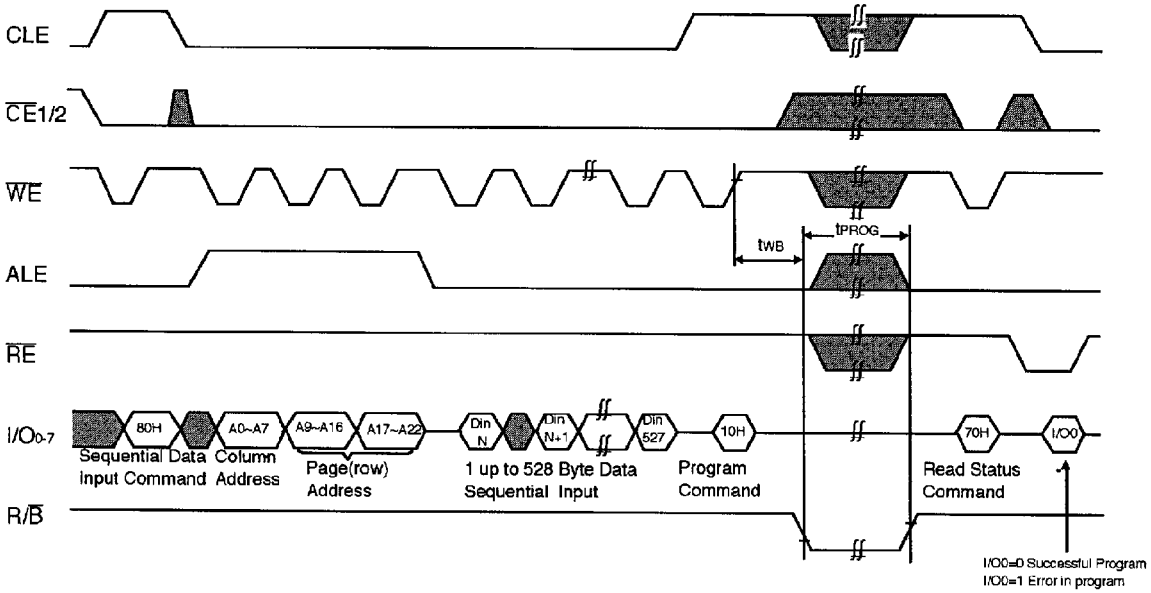
SEQUENTIAL ROW READ OPERATION



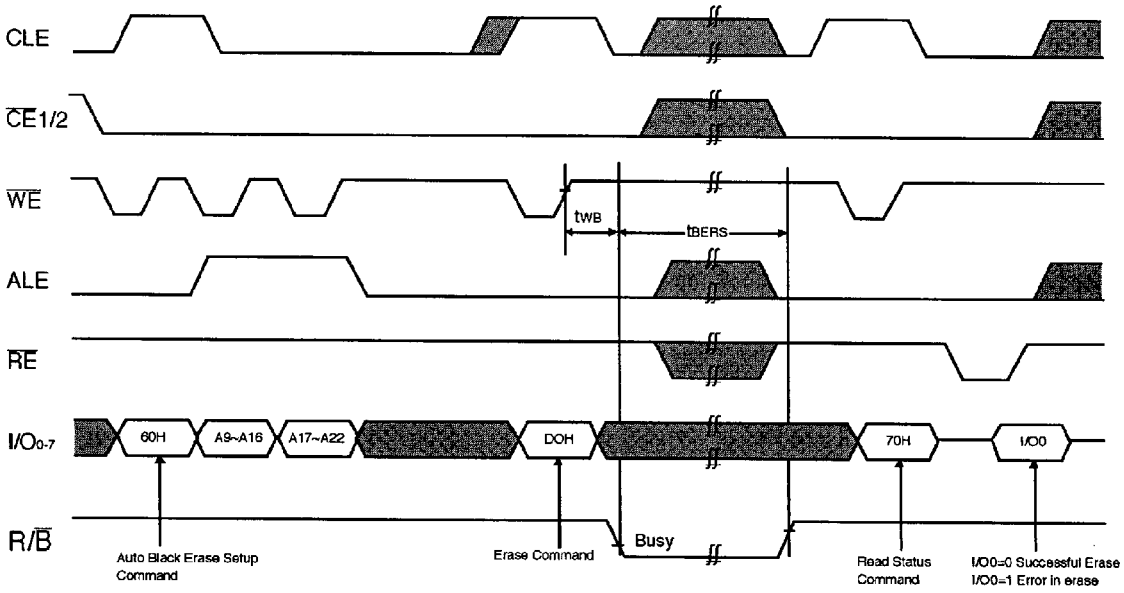
GAP-LESS SEQUENTIAL READ OPERATION



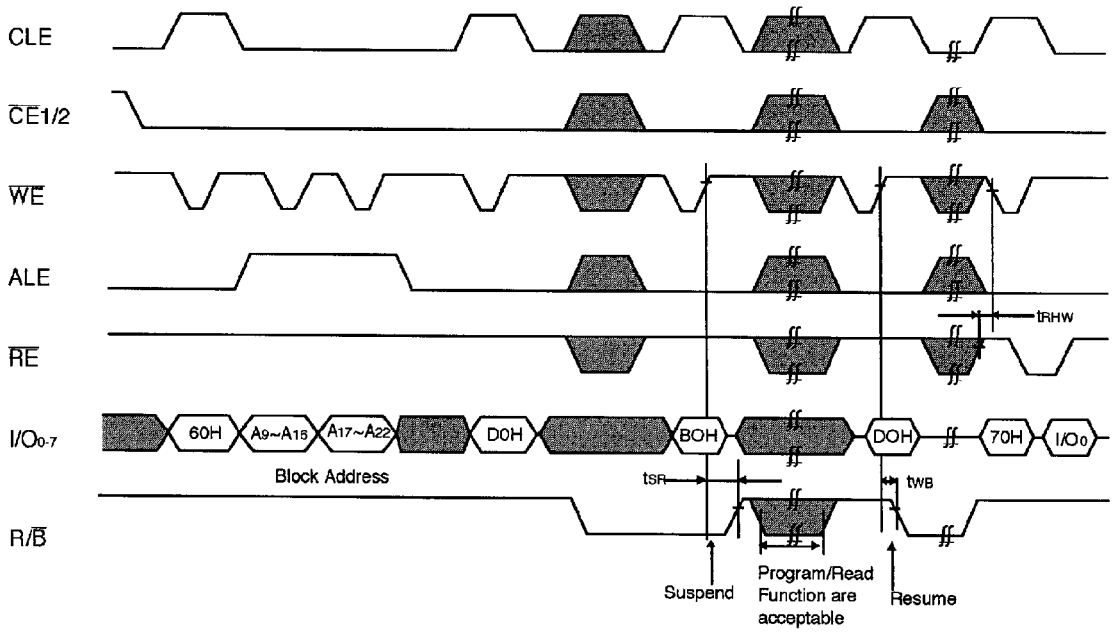
PAGE PROGRAM OPERATION



BLOCK ERASE OPERATION (ERASE ONE BLOCK)



SUSPEND & RESUME OPERATION DURING BLOCK ERASE



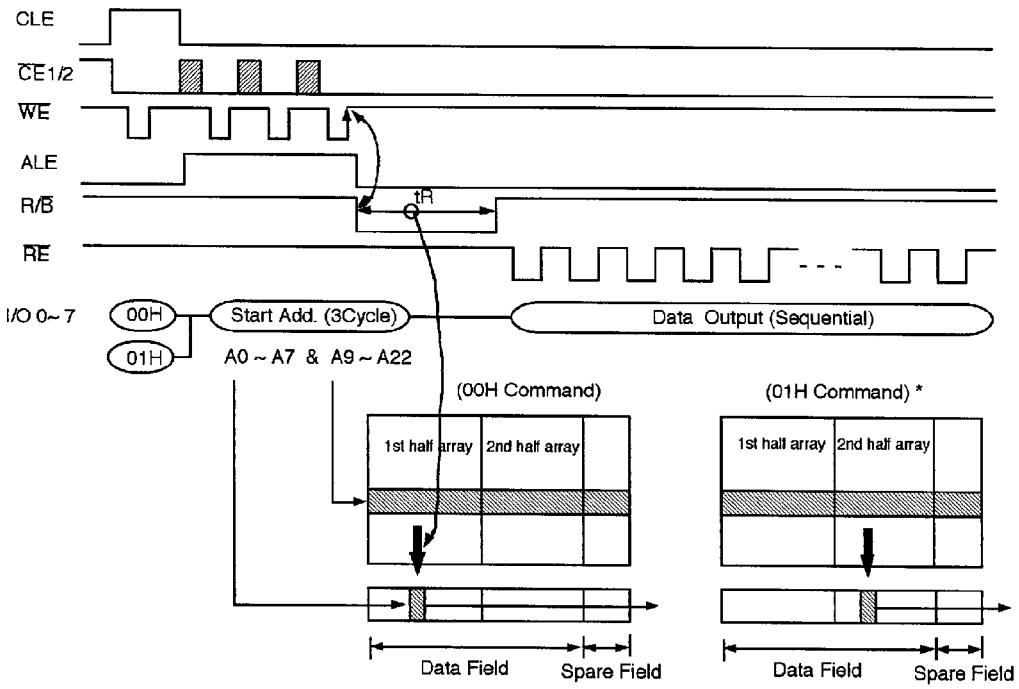
DEVICE OPERATION

PAGE READ

Upon initial device power up , the KM29V64001 defaults to Read1 mode. This operation is also initiated by writing 00H to the command register along with three address cycles. Once the command is latched, it does not need to be written for the following page read operation. Three types of operations are available: random read, serial page read and sequential row read.

The random read mode is enabled when the page address is changed. The 528 bytes of data within the selected page are transferred to the data registers in less than 10us(tR). The CPU can detect the completion of this data transfer (tR) by analyzing the output of Ready/$\overline{Busy}$ pin. Once the data in a page is loaded into the registers, they may be read out in 50ns cycle time by sequentially pulsing $\overline{RE}$ with $\overline{CE}$ staying low. High to low transitions of the $\overline{RE}$ clock output the data starting from the selected column address up to the last column address (column 511 or 527 depending on state of $\overline{SE}$ pin). After the data of last column address is clocked out, the next page is automatically selected for sequential row read. Waiting 5us again allows for reading of the selected page. By 02H command and 00H column address the KM29V64001 also support gab-less sequential read operation that similar operation with normal sequential row read except do not need to wait tR(5us) for reading the next page. The sequential row read operation is terminated by bringing $\overline{CE}$ high. The way the Read1 and Read2 commands work is like a pointer set to either the main area or the spare area. The spare area of bytes 512 to 527 may be selectively accessed by writing the Read 2 command with $\overline{SE}$ pin low level. Address A0 to A3 set the starting address of the spare area while addresses A4 to A7 are ignored. Unless the operation is aborted, the page address is automatically incremented for sequential row read as in Read 1 operation and spare sixteen bytes of each page may be sequentially read. The Read 1 command (00H/01H) is needed to move the pointer back to the main area. Figure 3 thru 6 show typical sequence and timings for each read operation.

Figure 3. Read 1 Operation



* After data access on 2nd half array by 01H command, the start pointer is automatically moved to 1st half array (00H) at next cycle.

Figure 4. Read 2 Operation

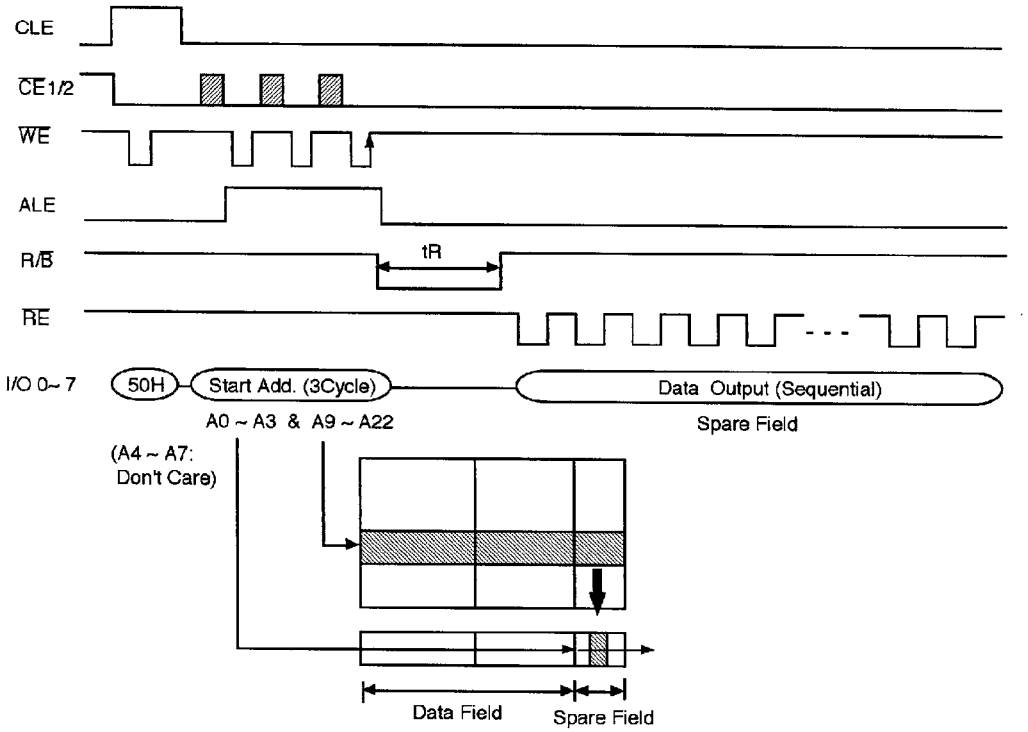


Figure 5. Sequential Row Read 1 Operation

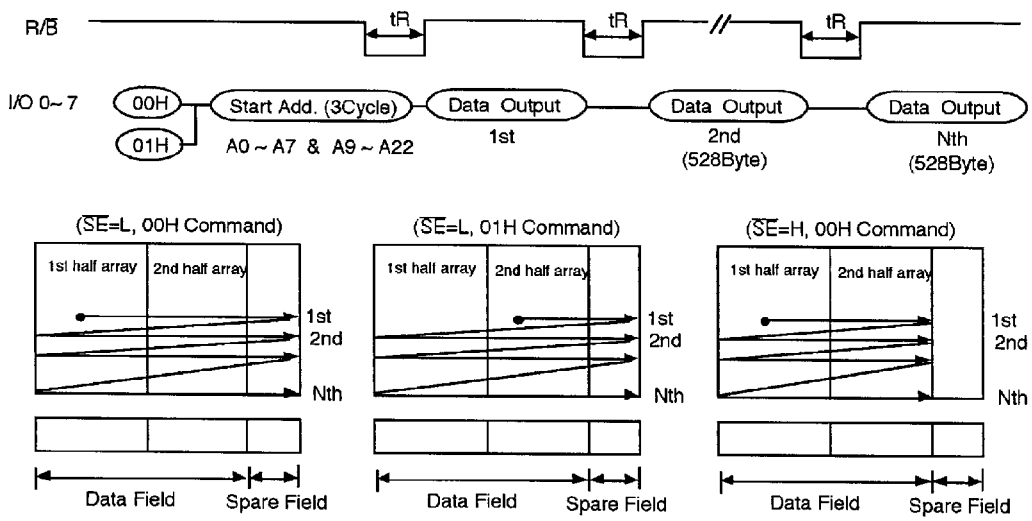


Figure 6. Sequential Row Read 2 Operation ($\overline{SE}$ = fixed low)

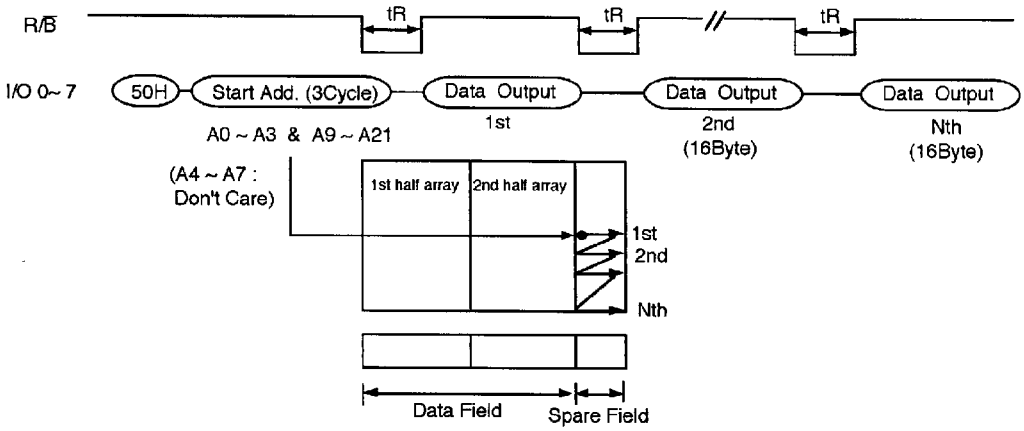
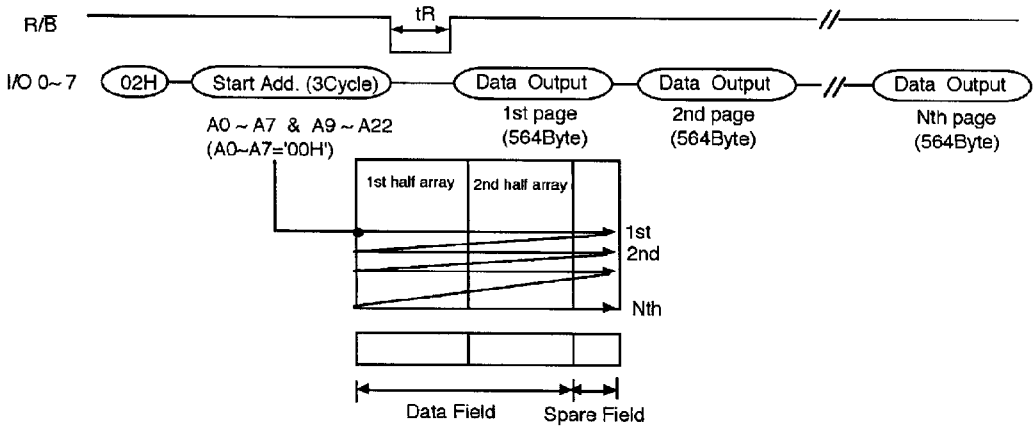


Figure 7. Gap-less Sequential Read Operation ($\overline{SE}$ = fixed low)

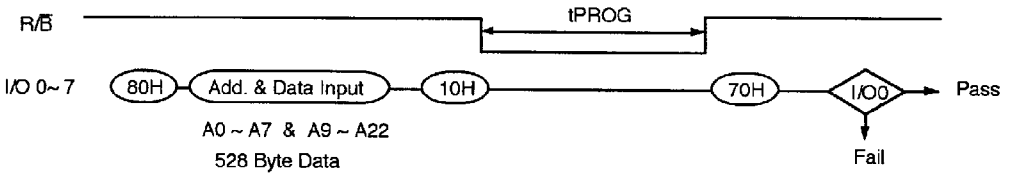


PAGE PROGRAM

The device is programmed basically on a page basis, but it does allow partial page program:a byte or consecutive bytes up to 528, in a single page program cycle. The number of consecutive partial page programming operation within the same page without an intervening erase operation must not exceed ten. The addressing may be done in random order in a block. A page program cycle consists of a serial data loading period in which up to 528 bytes of data may be loaded into the page register, followed by a nonvolatile programming period where the loaded data is programmed into the appropriate cell.

The serial data loading period begins by inputting the Serial Data Input command (80H), followed by the three cycle address input and then serial data loading. The bytes other than those to be programmed do not need to be loaded. The Page Program confirm command (10H) initiates the programming process. Writing 10H alone without previously entering the serial data will not initiate the programming process. The internal write controller automatically executes the algorithms and timings necessary for program and verify, thereby freeing the CPU for other tasks. Once the program process starts, the Read Status Register command may be entered, with $\overline{RE}$ and $\overline{CE}$ low, to read the status register. The CPU can detect the completion of a program cycle by monitoring the Ready/$\overline{Busy}$ output, or the Status bit(I/O 6) of the Status Register. Only the Read Status command and Reset command are valid while programming is in progress. When the Page Program is complete, the Write Status Bit(I/O 0) may be checked (Figure 8). The internal write verify detects only errors for "1"s that are not successfully programmed to "0"s. The command register remains in Read Status command mode until another valid command is written to the command register.

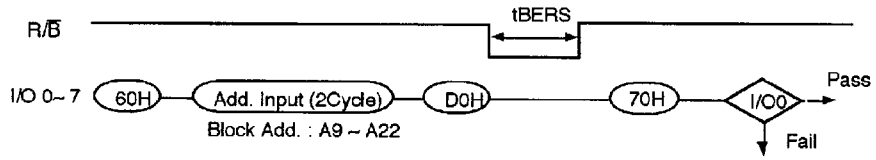
Figure 8. Program & Read Status Operation



BLOCK ERASE

The Erase operation can erase on a block(8KByte) basis. Block address loading is accomplished in two cycles initiated by an Erase Setup command(60H). Only address A13 to A22 is valid while A9 to A12 is ignored. The address of the block to be erased to FFH. The Erase Confirm command(D0H) following the block address loading initiates the internal erasing process. This two-step sequence of setup followed by execution ensures that memory contents are not accidentally erased due to external noises conditions. At the rising edge of $\overline{WE}$ after the erase confirm command input, the internal write controller handles erase, erase-verify and pulse repetition where required. If an erase operation error is detected, the internal verify is halted and erase operation is terminated. When the erase operation is complete, the Write Status Bit(I/O 0) can be checked. Figure 9 detail the sequence.

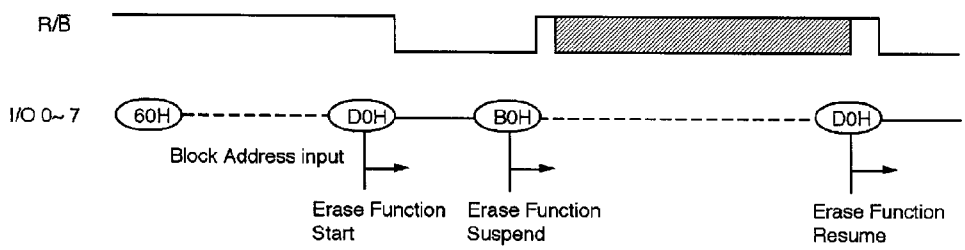
Figure 9. Block Erase Operation



ERASE SUSPEND/ERASE RESUME

The Erase Suspend allows interruption during any erase operation in order to read or program data to or from another block of memory. Once an erase process begins, writing the Erase Suspend command (B0H) to the command register suspends the internal erase process, and the Ready/$\overline{Busy}$ signal return to "1". Erase Suspend Status bit will be also set to "1" when the Status Register is read. At this time, blocks other than the suspended block can be read or programmed. The Status Register and Ready/$\overline{Busy}$ operation will function as usual. After the Erase Resume command is written to it, the erase process is restarted from the beginning of the erasing period. The Erase Suspend Status bit and Ready/$\overline{Busy}$ will return to "0". Refer to Figure 10 for operation sequence.

Figure 10. Erase Suspend & Erase Resume Operation



READ STATUS

The KM29V64001 contains a Status Register which can be read to find out whether program or erase operation is complete, and whether the program or erase operation completed successfully. After writing 70H command to the command register, a read cycle outputs the contents of the Status Register to the I/O pins on the falling edge of $\overline{CE}$ or $\overline{RE}$, whichever occurs last. This two line control allows the system to poll the progress of each device in multiple memory connections even when R/$\overline{B}$ pins are common-wired. $\overline{RE}$ or $\overline{CE}$ does not need to be toggled for updated status. Refer to table 2 for specific Status Register definitions. The command register remains in Status Read mode until further commands are issued to it. Therefore, if the Status Register is read during a random read cycle, the required Read Command (00H or 50H) should be input before serial page read cycle.

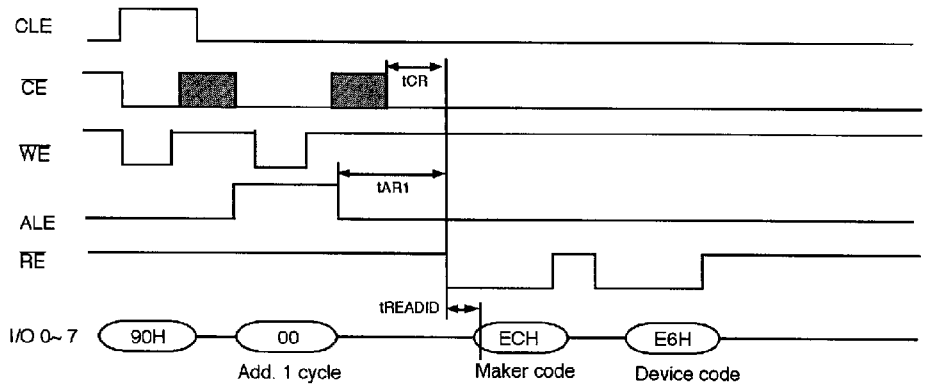
Table 2. STATUS REGISTER DEFINITION

SR	Status	Definition
I/O 0	Program / Erase	"0" : Successful Program/Erase
		"1" : Error in Program/Erase
I/O 1	Reserved for Future Use	"0"
I/O 2		"0"
I/O 3		"0"
I/O 4		"0"
I/O 5	Erase Suspend	"0" : Erase in Progress/Completed
		"1" : Suspended
I/O 6	Device Operation	"0" : Busy "1" : Ready
I/O 7	Write Protect	"0" : Protected "1" : Not Protected

READ ID

The KM29V64001 contains a product identification mode, initiated by writing 90H to the command register, followed by an address input of 00H. Two read cycles sequentially outputs the manufacturer code (ECH), and the device code (E6H) respectively. The command register remains in Read ID mode until further commands are issued to it. Figure 11 shows the operation sequence.

Figure 11. Read ID Operation



RESET

The KM29V64001 offers a hardware and software reset feature, executed by input low level of $\overline{RST}$ pin or writing FFH to the command register. When the device is in Busy state during random read, program or erase modes, the reset operation will abort these operation. The contents of memory cells being altered are no longer valid, as the data will be partially programmed or erased. Internal address registers are cleared to "0"s and data registers to "1"s. The command register is cleared to wait for the next command, and the Status Register is cleared to value C0H when $\overline{WP}$ is high. Refer to table 3 for device status after reset operation. If the device is already in reset state a new reset command will not be accepted to by the command register . The Ready/$\overline{Busy}$ pin transitions to low for tRST after the Reset command is written. Reset command is not necessarily for normal operation. Refer to Figure 12 and 13 below.

Figure 12. S/W RESET Operation

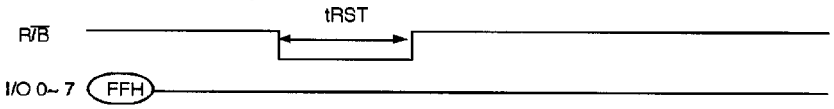


Figure 13. H/W RESET Operation

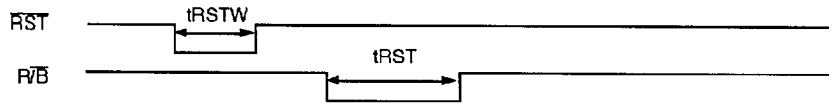
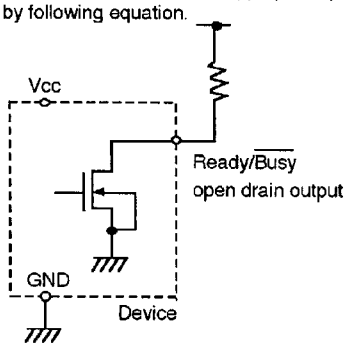


Table 3. DEVICE STATUS

	After Power-up	After Reset
Address Register	All "0"	All "0"
Data Register	All "1"	All "1"
Operation Mode	Read 1	Waiting for next command

READY/$\overline{BUSY}$

The KM29V64001 has a Ready/$\overline{Busy}$ output that provides a hardware method of indicating the completion of a page program, erase and random read completion. The R/$\overline{B}$ pin is normally high but transitions to low after program or erase command is written to the command register or random read is begin after address loading. It returns to high when the internal controller has finished the operation. The pin is an open-drain driver thereby allowing two or more Ready/$\overline{Busy}$ outputs to be Or-tied. An appropriate pull-up resister is required for proper operation and the value may be calculated by following equation.



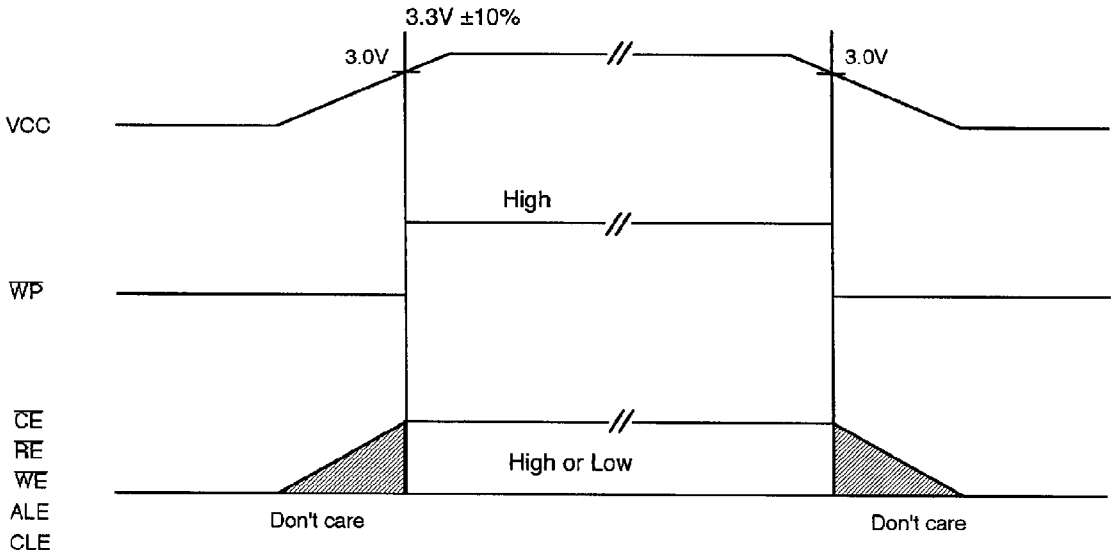
$$Rp = \frac{Vcc(Max.) - V_{OL}(Max.)}{I_{OL} + \Sigma I_L} = \frac{3.2V}{8mA + \Sigma I_L}$$

where I_L is the sum of the input currents of all devices tied to the Ready/$\overline{Busy}$ pin.

DATA PROTECTION

The KM29V64001 has a write protect pin ($\overline{WP}$) to provide protection from any accidental write operation during power transition. During device power up, the $\overline{WP}$ should be at VIL until Vcc reaches approximately 3.0V, during power down should be at VIL when Vcc falls below 3.0V. Refer to Figure 14 below.

Figure 14. AC WAVEFORMS for POWER TRANSITIONS

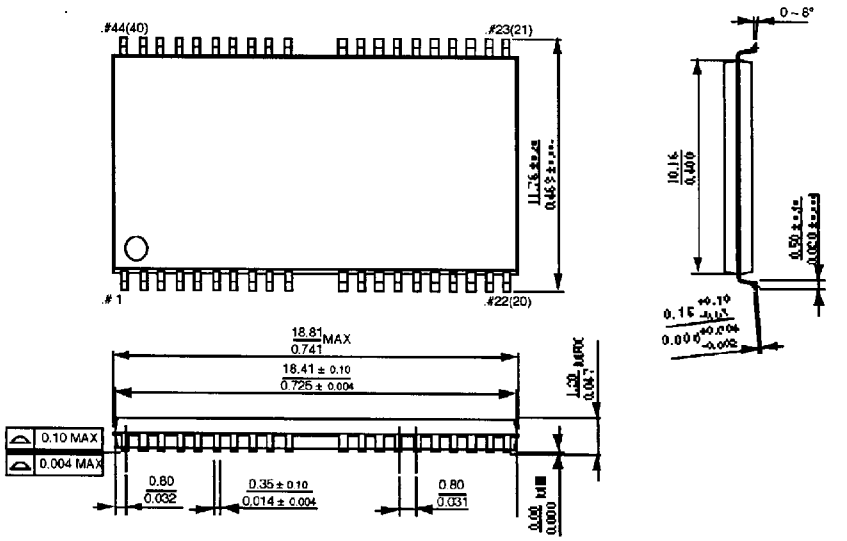


PACKAGE DIMENSION

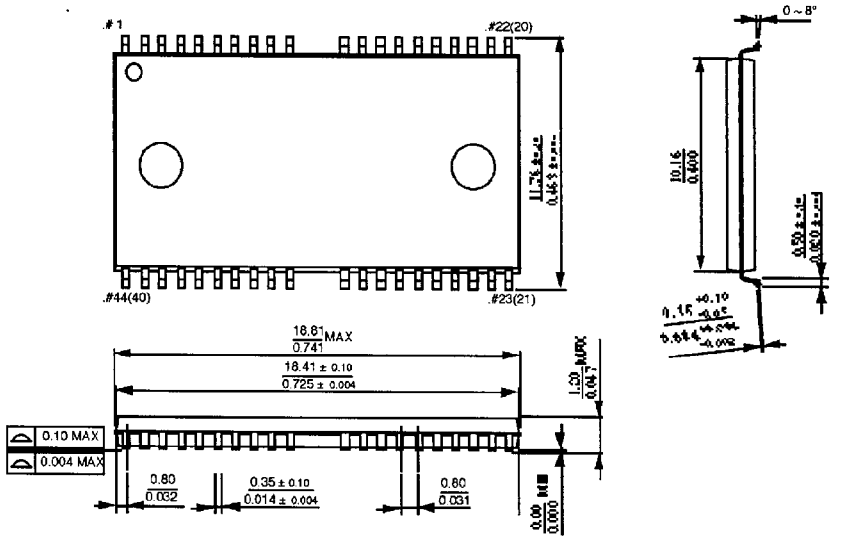
44 (40) LEAD PLASTIC THIN SMALL OUT-LINE PACKAGE TYPE (II)

Unit : mm/inch

44(40)-TSOP2-400F



44(40)-TSOP2-400R



KM29V64001 Technical Notes

INVALID BLOCKS

Typically, the KM29V64001T/R Flash device contains less than 20 unusable blocks. Due to the nature of the device architecture, the device can also be screened and tested for partial invalid blocks for selected systems that can utilize the devices. These devices will have the same quality levels as devices with all valid blocks and will meet all AC and DC characteristics. The system design must be able to mask out the partial block(s) from address mapping. An invalid block(s) do not affect the performance of valid block(s) because it is isolated from the bit line and the common source line by a select transistor.

Identifying Invalid Block(s) in the KM29V64001T / R

All device locations are erased (FFh) prior to shipping. Devices with invalid Block(s) will be randomly written with 00h data within a page in the invalid Block(s). This page may or may not contain the invalid cell(s). The 00h data marks the block(s) that contain the invalid cell(s). A system that can utilize these devices must be able to recognize invalid block(s) via the following suggested flow chart (Figure 1).

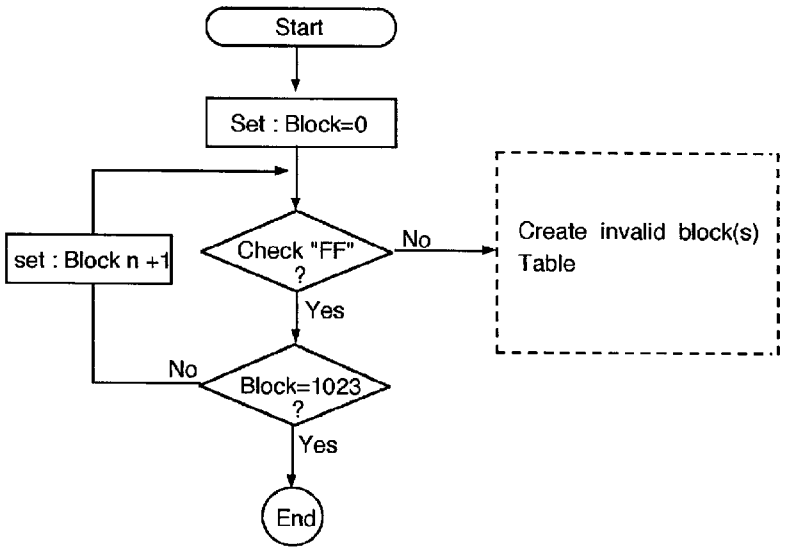


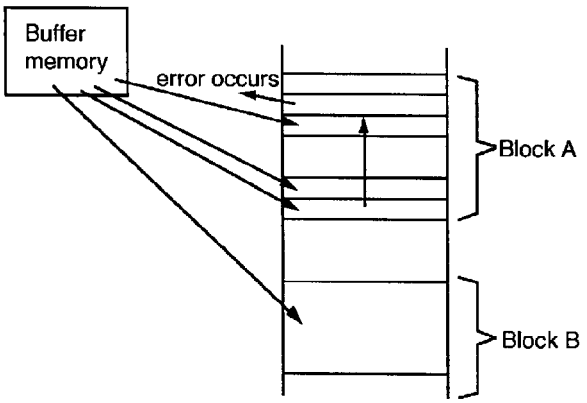
Figure 1 Flow chart to create invalid block table.

KM29V64001 Technical Notes (Continued)

Error in program or erase operation (Fail at status read)

The device may fail during a program or erase operation due to exceeding write/erase cycle limits, for example. The following system architecture will enable high system reliability if a failure occurs :

During Program operation ;



When the error happens in Block 'A', try to reprogram the data into another Block 'B' by loading from an external buffer. Then, prevent further system access to Block 'A' (by creating a 'bad block' table or other appropriate scheme.)

During Erase operation ;

When the error occurs after an erase operation, prevent future accesses to this bad block (again by creating a table within the system or other appropriate scheme.)